
MCUs with High-Precision 16-Bit PWMs Product Brief

Description

PIC12(L)F1571/2 and PIC16(L)F1574/5/8/9 microcontrollers combine the capabilities of 16-bit PWMs with Analog to suit a variety of applications. These devices deliver up to four 16-bit PWMs with independent timers for applications where high resolution is needed, such as LED lighting, stepper motors, power supplies and other general purpose applications. The core independent peripherals (16-bit PWMs, Complementary Waveform Generator), Enhanced Universal Synchronous Asynchronous Receiver Transceiver (EUSART) and Analog (ADCs, Comparator and DAC) enable closed-loop feedback and communication for use in multiple market segments. The Peripheral Pin Select (PPS) functionality allows for I/O pin remapping of the digital peripherals for increased flexibility. The EUSART peripheral enables the communication for applications such as LIN.

Core Features

- C Compiler Optimized RISC Architecture
- Only 49 Instructions
- Operating Speed:
 - DC – 32 MHz clock input
 - 125 ns minimum instruction cycle
- Interrupt Capability
- 16-Level Deep Hardware Stack
- Two 8-Bit Timers
- One 16-Bit Timer
- Up to Four Additional 16-Bit Timers Available Using the 16-Bit PWMs
- Power-on Reset (POR)
- Power-up Timer (PWRT)
- Low-Power Brown-out Reset (LPBOR)
- Programmable Watchdog Timer (WDT) up to 256s
- Programmable Code Protection

Memory

- Up to 14 Kbytes Program Flash Memory (PFM)
- Up to 1 Kbytes Data SRAM Memory
- Direct, Indirect and Relative Addressing modes
- 128 Bytes of Nonvolatile Data Storage, High-Endurance Flash (HEF)

Operating Characteristics

- Operating Voltage Range:
 - 1.8V to 3.6V (PIC12LF1571/2, PIC16LF1574/5/8/9)
 - 2.3V to 5.5V (PIC12F1571/2, PIC16F1574/5/8/9)
- Temperature Range:
 - Industrial: -40°C to 85°C
 - Extended: -40°C to 125°C

Low-Power Features

- Sleep mode: 20 nA @ 1.8V, typical
- Watchdog Timer: 260nA @ 1.8V, typical
- Operating Current:
 - 30 μ A/MHz @ 1.8V, typical

Digital Peripherals

- 16-Bit PWM:
 - Up to four 16-bit PWMs with independent timers
 - Multiple output modes (standard, center aligned, set and toggle on register match)
 - User settings for phase, duty cycle, period, offset and polarity
 - 16-bit timer capability
 - Interrupts generated based on timer matches with offset, duty cycle, period and phase registers.
- Complementary Waveform Generator (CWG):
 - Rising and falling edge dead-band control
 - Multiple signal sources
- Enhanced Universal Synchronous Asynchronous Receiver Transceiver (EUSART):
 - Supports LIN applications
- Peripheral Pin Select (PPS):
 - I/O pin remapping of digital peripherals (PIC16(L)F1574/5/8/9 devices only)

Device I/O Port Features

- Up to 18 I/Os
- Individually Selectable Weak Pull-ups
- Interrupt-on-Change Pins Option with Edge-Selectable Option

PIC12/16(L)F157X

Analog Peripherals

- 10-Bit Analog-to-Digital Converter (ADC):
 - Up to 12 external channels
 - Conversion available during Sleep
- Comparator:
 - Up to two
 - Low-Power/High-Speed modes
 - Fixed Voltage Reference at inverting and non-inverting input(s)
 - Comparator outputs externally accessible
 - Synchronization with Timer1 clock source
 - Software hysteresis enable
- 5-Bit Digital-to-Analog Converter (DAC):
 - 5-bit resolution, rail-to-rail
 - Positive Reference Selection
 - Unbuffered I/O pin output
 - Internal connections to ADCs and comparators
- Voltage Reference:
 - Fixed Voltage Reference with 1.024V, 2.048V and 4.096V output levels

Clocking Structure

- Precision Internal Oscillator:
 - Factory calibrated $\pm 1\%$, typical
 - Software-selectable clock speeds from 31 kHz to 32 MHz
- External Oscillator Block with:
 - Resonator modes up to 20 MHz
 - Two external clock modes up to 32 MHz
- Fail-Safe Clock Monitor
- Two-Speed Oscillator Start-up
- Digital Oscillator Input available

TABLE 1: PIC12(L)F1571/2 AND PIC16(L)F1574/5/8/9 FAMILY TYPES

Device	Data Sheet Index	Program Flash Memory (Kwords)	Program Flash Memory (Kbytes)	Data SRAM (bytes)	I/O Pins	8-Bit/16-Bit Timers	Comparators	16-Bit PWM	10-Bit ADC (ch)	5-Bit DAC	CWG	EUSART	PPS	Debug ⁽¹⁾
PIC12(L)F1571	(A)	1	1.75	128	6	2/4 ⁽²⁾	1	3	4	1	1	0	N	I
PIC12(L)F1572	(A)	2	3.5	256	6	2/4 ⁽²⁾	1	3	4	1	1	1	N	I
PIC16(L)F1574	(B)	4	7	512	12	2/5 ⁽³⁾	2	4	8	1	1	1	Y	I
PIC16(L)F1575	(B)	8	14	1024	18	2/5 ⁽³⁾	2	4	8	1	1	1	Y	I
PIC16(L)F1578	(B)	4	7	512	12	2/5 ⁽³⁾	2	4	12	1	1	1	Y	I
PIC16(L)F1579	(B)	8	14	1024	18	2/5 ⁽³⁾	2	4	12	1	1	1	Y	I

Note 1: I – Debugging integrated on chip.

2: Three additional 16-bit timers available when not using the 16-bit PWM outputs.

3: Four additional 16-bit timers available when not using the 16-bit PWM outputs.

Data Sheet Index:

- A:** DS-40001723 [PIC12\(L\)F1571/2 Data Sheet, 8-Pin Flash, 8-bit MCU with High-Precision 16-bit PWM](#)
B: Future Release [PIC16\(L\)F1574/5/8/9 Data Sheet, 8-Pin Flash, 8-bit MCU with High-Precision 16-bit PWM](#)

Note: For other small form-factor package availability and marking information, please visit <http://www.microchip.com/packaging> or contact your local sales office.

TABLE 2: PACKAGES

Packages	PDIP	SOIC	MSOP	DFN/UDFN	TSSOP	SSOP	QFN/UQFN
PIC12(L)F1571	X	X	X	X			
PIC12(L)F1572	X	X	X	X			
PIC16(L)F1574	X	X			X		X
PIC16(L)F1575	X	X			X		X
PIC16(L)F1578	X	X				X	X
PIC16(L)F1579	X	X				X	X

Note: Pin details are subject to change.

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PIN DIAGRAMS

FIGURE 1: 8-PIN PDIP, SOIC, MSOP, DFN/UDFN

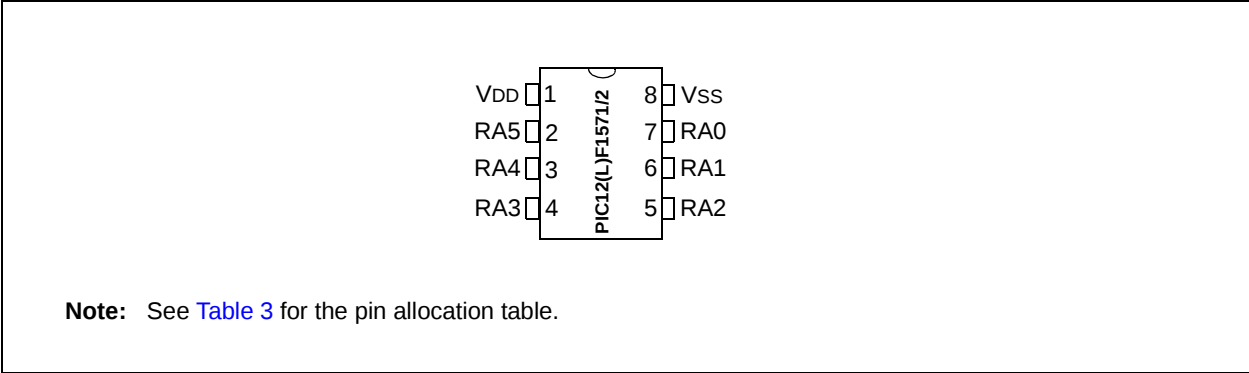


FIGURE 2: 14-PIN PDIP, SOIC, TSSOP

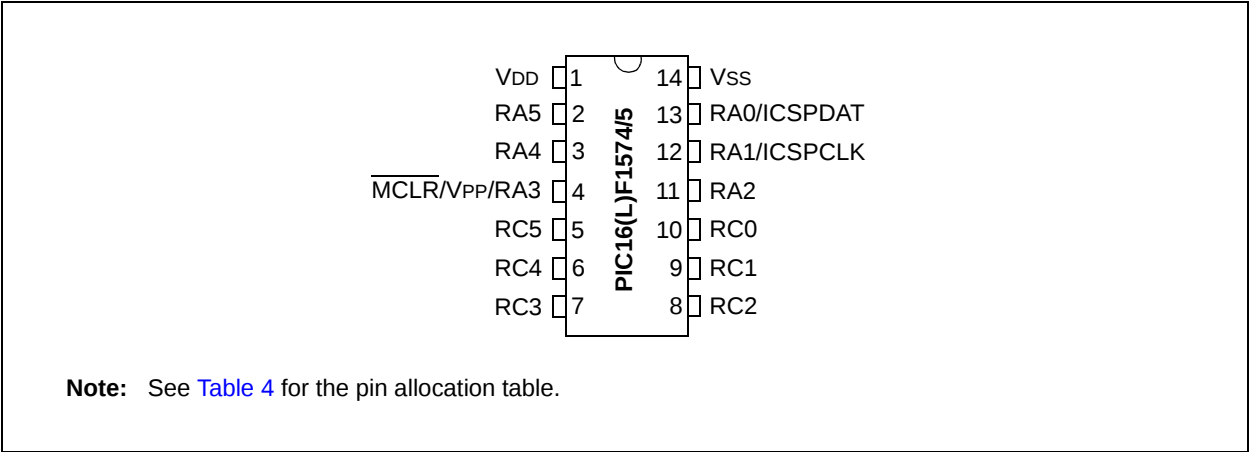


FIGURE 3: 16-PIN QFN/UQFN (4x4)

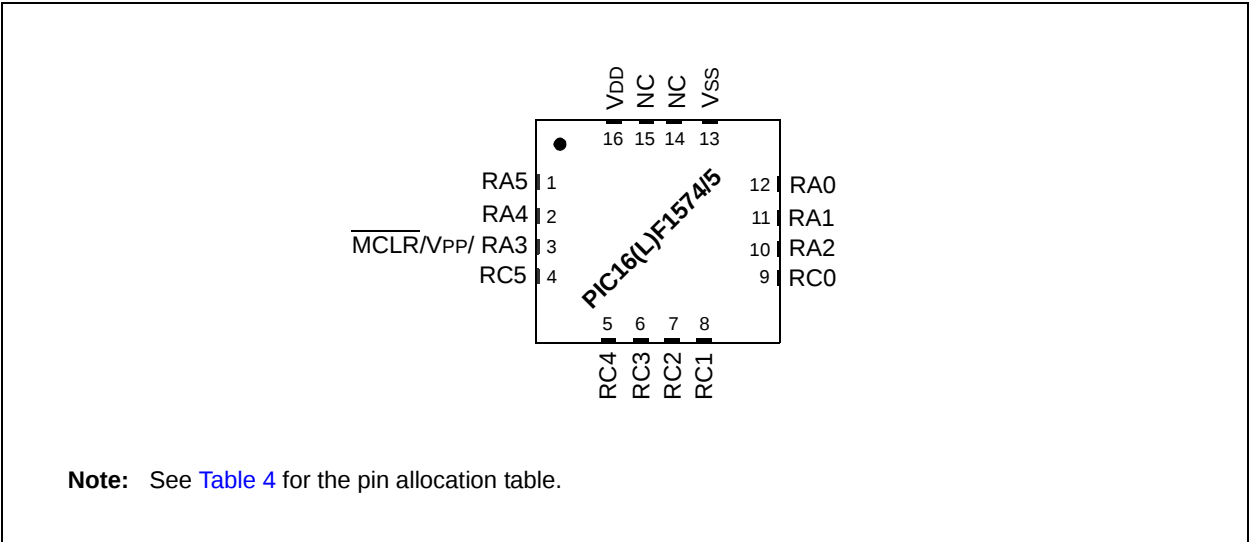
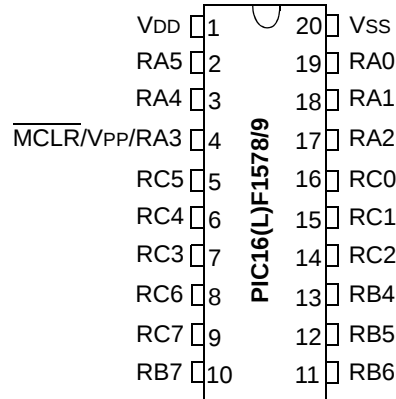
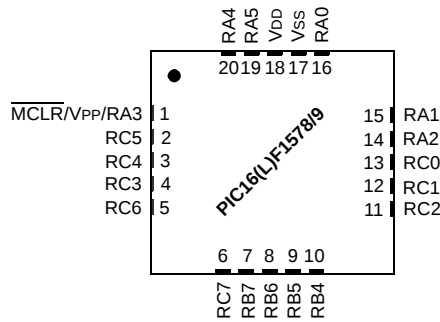


FIGURE 4: 20-PIN PDIP, SOIC, SSOP



Note: See [Table 5](#) for the pin allocation table.

FIGURE 5: 20-PIN QFN/UQFN (4x4)



Note: See [Table 5](#) for the pin allocation table.

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PIN ALLOCATION TABLES

TABLE 3: 8-PIN ALLOCATION TABLE (PIC12(L)F1571/2)

I/O	8-Pin PDIP/SOIC/MSOP/DFN	ADC	Reference	Comparator	Timers	PWM	EUSART ⁽²⁾	CWG	Interrupt	Pull-up	Basic
RA0	7	AN0	DAC1OUT	C1IN+	—	PWM2	TX/CK ⁽²⁾	CWG1B	IOC	Y	ICSPDAT ICDDAT
RA1	6	AN1	VREF+	C1IN0-	—	PWM1	RX/DT ⁽²⁾	—	IOC	Y	ICSPCLK ICDCLK
RA2	5	AN2	—	C1OUT	T0CKI	PWM3	—	$\overline{\text{CWG1FLT}}$ CWG1A	IOC INT	Y	—
RA3	4	—	—	—	T1G ⁽¹⁾	—	—	—	IOC	Y	$\overline{\text{MCLR}}$ V _{PP}
RA4	3	AN3	—	C1IN1-	T1G	PWM2 ⁽¹⁾	TX/CK ^(1,2)	CWG1B ⁽¹⁾	IOC	Y	CLKOUT
RA5	2	—	—	—	T1CKI	PWM1 ⁽¹⁾	RX/DT ^(1,2)	CWG1A ⁽¹⁾	IOC	Y	CLKIN
VDD	1	—	—	—	—	—	—	—	—	—	VDD
VSS	8	—	—	—	—	—	—	—	—	—	VSS

Note 1: Alternate pin function selected with the APFCON register.
2: PIC12(L)F1572 only.

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TABLE 4: 14/16-PIN ALLOCATION TABLE (PIC16(L)F1574/5)

I/O	14-Pin PDIP/SOIC/TSSOP	16-Pin QFN/UQFN	ADC	Reference	Comparator	Timers	PWM	EUSART	CWG	Interrupt	Pull-up	Basic
RA0	13	12	AN0	DAC1OUT1	C1IN+	—	—	—	—	IOC	Y	ICSPDAT ICDDAT
RA1	12	11	AN1	VREF+	C1IN0-/C2IN0-	—	—	—	—	IOC	Y	ICSPCLK ICDCLK
RA2	11	10	AN2	—	—	T0CKI ⁽¹⁾	—	—	CWG1IN ⁽¹⁾	INT ⁽¹⁾ /IOC	Y	—
RA3	4	3	—	—	—	—	—	—	—	IOC	Y	MCLR/VPP
RA4	3	2	AN3	—	C1IN1-	T1G ⁽¹⁾	—	—	—	IOC	Y	CLKOUT
RA5	2	1	—	—	—	T1CKI ⁽¹⁾	—	—	—	IOC	Y	CLKIN
RC0	10	9	AN4	—	C2IN+	—	—	—	—	IOC	Y	—
RC1	9	8	AN5	—	C1IN1-/C2IN1-	—	—	—	—	IOC	Y	—
RC2	8	7	AN6	—	C1IN2-/C2IN2-	—	—	—	—	IOC	Y	—
RC3	7	6	AN7	—	C1IN3-/C2IN3-	—	—	—	—	IOC	Y	—
RC4	6	5	ADCACT ⁽¹⁾	—	—	—	—	CK ⁽¹⁾	—	IOC	Y	—
RC5	5	4	—	—	—	—	—	RX ^(1,3)	—	IOC	Y	—
VDD	1	16	—	—	—	—	—	—	—	—	—	VDD
VSS	14	13	—	—	—	—	—	—	—	—	—	VSS
OUT ⁽²⁾	—	—	—	—	C1OUT	—	PWM1OUT	DT ⁽³⁾	CWG1A	—	—	—
	—	—	—	—	C2OUT	—	PWM2OUT	CK	CWG1B	—	—	—
	—	—	—	—	—	—	PWM3OUT	TX	—	—	—	—
	—	—	—	—	—	—	PWM4OUT	—	—	—	—	—

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS Input Selection registers.
 - 2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS Output Selection registers.
 - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

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TABLE 5: 20-PIN ALLOCATION TABLE (PIC16(L)F1578/9)

I/O	20-Pin PDIP/SSOP	20-Pin QFN/UQFN	ADC	Reference	Comparator	Timers	PWM	EUSART	CWG	Interrupt	Pull-up	Basic
RA0	19	16	AN0	DAC1OUT1	C1IN+	—	—	—	—	IOC	Y	ICSPDAT ICDDAT
RA1	18	15	AN1	VREF+	C1IN0-/C2IN0-	—	—	—	—	IOC	Y	ICSPCLK ICDCLK
RA2	17	14	AN2	—	—	T0CKI ⁽¹⁾	—	—	CWG1IN ⁽¹⁾	INT ⁽¹⁾ /IOC	Y	—
RA3	4	1	—	—	—	—	—	—	—	IOC	Y	MCLR/VPP
RA4	3	20	AN3	—	C1IN1-	T1G ⁽¹⁾	—	—	—	IOC	Y	CLKOUT
RA5	2	19	—	—	—	T1CKI ⁽¹⁾	—	—	—	IOC	Y	CLKIN
RB4	13	10	AN10	—	—	—	—	—	—	IOC	Y	—
RB5	12	9	AN11	—	—	—	—	—	—	IOC	Y	—
RB6	11	8	—	—	—	—	—	—	—	IOC	Y	—
RB7	10	7	—	—	—	—	—	—	—	IOC	Y	—
RC0	16	13	AN4	—	C2IN+	—	—	—	—	IOC	Y	—
RC1	15	12	AN5	—	C1IN1-/C2IN1-	—	—	—	—	IOC	Y	—
RC2	14	11	AN6	—	C1IN2-/C2IN2-	—	—	—	—	IOC	Y	—
RC3	7	4	AN7	—	C1IN3-/C2IN3-	—	—	—	—	IOC	Y	—
RC4	6	3	ADCACT ⁽¹⁾	—	—	—	—	CK ⁽¹⁾	—	IOC	Y	—
RC5	5	2	—	—	—	—	—	RX ^(1,3)	—	IOC	Y	—
RC6	8	5	AN8	—	—	—	—	—	—	IOC	Y	—
RC7	9	6	AN9	—	—	—	—	—	—	IOC	Y	—
VDD	1	18	—	—	—	—	—	—	—	—	—	VDD
VSS	20	17	—	—	—	—	—	—	—	—	—	VSS
OUT ⁽²⁾	—	—	—	—	C1OUT	—	PWM1OUT	DT ⁽³⁾	CWG1A	—	—	—
	—	—	—	—	C2OUT	—	PWM2OUT	CK	CWG1B	—	—	—
	—	—	—	—	—	—	PWM3OUT	TX	—	—	—	—
	—	—	—	—	—	—	PWM4OUT	—	—	—	—	—

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS Input Selection registers.
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 - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

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