18-Bit, 10-Port Crossbar Switch

Product Features

- Full 10-way crossbar
- Independent controls for all ports
- Multiple parts can be used for wider data paths
- Near-zero propagation delay
- 25Ω switches connect input to outputs
- Direct bus connection when switches are ON
- Ultra Low Quiescent Power (1mA Typical)
- Packages available:
  - 256-pin BGA (NA256)

Applications

- Digital network switching:
  - Hubs & Routers
  - ATM Switch Systems
  - Backbone Access Routing
  - Add Drop Multiplexing
- Multiprocessor systems switching
- Large memory bus switching
- Video signal routing & Image processing
- Telecommunications switching
- RAID systems bus switching

Truth Table

Function	Pin	State
Port N - Port M connected*	S_{N-M}	Low
Port N - Port M disconnected*	S_{N-M}	High

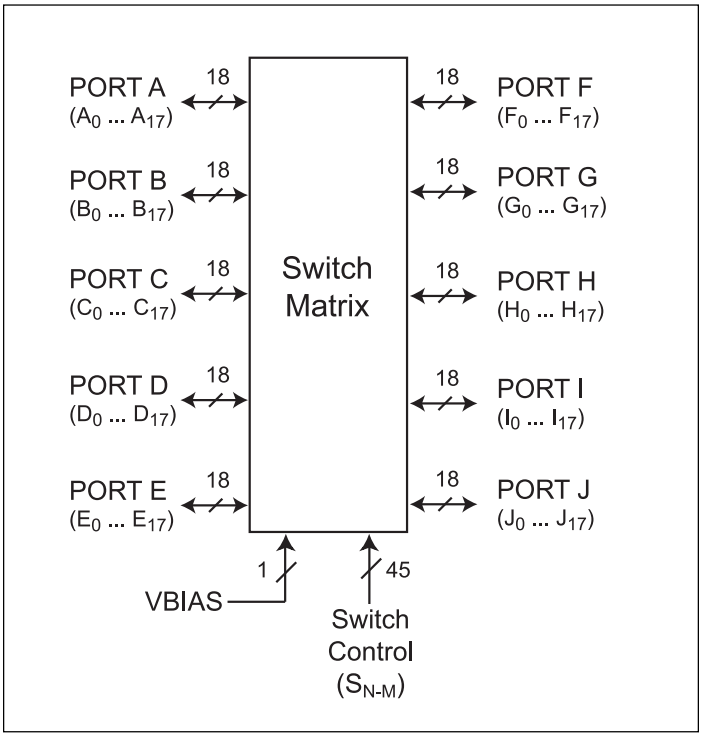
* Specify low numbered port first

Product Description

Pericom's PI5X series of high density logic circuits are produced using the Company's advanced submicron CMOS technology to achieve industry leading performance.

The PI5X1018 is an 18-bit, 10-port crossbar switch designed with a low ON resistance allowing inputs to be connected directly to outputs. The crossbar creates a low propagation delay and adds low additional ground bounce noise. Switches are turned ON in groups of 18 allowing any combination of connected ports. An additional bias voltage pin, VBIAS, permits control of internal pull-up resistors that can be used for pin termination. Several of these devices can be grouped together for wider data and control paths.

Logic Block Diagram



Product Pin Description

Pin Name	Description
A0…A17 through J0…J17	180 Pins total. Dedicated to ten 18-bit ports. Contains internal pull-up resistor controlled by pin V_{BIAS}.
S_{N-M}	45 Pins total. Dedicated to port switching. Where N is from A to I and M is from B to J and N< M. Also, contains internal pull-up resistor controlled by pin V_{BIAS}.
V_{BIAS}	Adjusts internal pull-up resistance value for all pins A-J & S_{N-M}; (default value with internal bias voltage of 2.9V is around 20kΩ). For V_{BIAS} = 0V, pull-up resistor value is less than 5kΩ. For V_{BIAS} = 4.1V, pull-up resistor value is greater than 100kΩ.
V_{DD} & V_{SS}	23 Pins dedicated to Power (VDD) and Ground (VSS)
NC	6 Pins are No Connect

Product Pinout by Name

Name	Ball Pad	Name	Ball Pad	Name	Ball Pad	Name	Ball Pad	Name	Ball Pad	Name	Ball Pad	Name	Ball Pad	Name	Ball Pad
A0	B8	C0	D7	E0	B7	G0	D6	I0	B6	Sa-b	A16	Sf-h	B3	NC	B20
A1	D1	C1	M1	E1	T4	G1	V5	I1	V9	Sa-c	B16	Sf-i	C3	NC	Y1
A2	E1	C2	L2	E2	U1	G2	W5	I2	W9	Sa-d	C16	Sf-j	D3	NC	Y2
A3	E2	C3	M2	E3	U2	G3	Y5	I3	Y9	Sa-e	D16	Sg-h	E3	NC	Y20
A4	F1	C4	N1	E4	U3	G4	U6	I4	Y10	Sa-f	A15	Sg-i	B2		
A5	F2	C5	N2	E5	U4	G5	V6	I5	W10	Sa-g	B15	Sg-j	C2		
A6	F3	C6	P1	E6	V1	G6	W6	I6	V10	Sa-h	C15	Sh-i	D2		
A7	G1	C7	P2	E7	V2	G7	Y6	I7	D10	Sa-i	D15	Sh-j	B1		
A8	G2	C8	P3	E8	V3	G8	U7	I8	C10	Sa-j	A14	Si-j	C1		
A9	C20	C9	C18	E9	B19	G9	A19	I9	A17	Sb-c	B14	V-Bias	N4		
A10	U10	C10	Y14	E10	V17	G10	P17	I10	G17	Sb-d	C14	VDD	F4		
A11	Y11	C11	U15	E11	V18	G11	P18	I11	G18	Sb-e	D14	VDD	G4		
A12	W11	C12	V15	E12	V19	G12	P19	I12	G20	Sb-f	A13	VDD	H17		
A13	V11	C13	W15	E13	V20	G13	P20	I13	G19	Sb-g	B13	VDD	H18		
A14	U11	C14	Y15	E14	U17	G14	N19	I14	F17	Sb-h	C13	VDD	N17		
A15	Y12	C15	U16	E15	U18	G15	N20	I15	F18	Sb-i	D13	VDD	N18		
A16	W12	C16	V16	E16	U19	G16	M19	I16	F19	Sb-j	A12	VDD	N3		
A17	V12	C17	W16	E17	U20	G17	M20	I17	F20	Sc-d	B12	VSS	J17		
B0	A8	D0	C7	F0	A7	H0	C6	J0	A6	Sc-e	C12	VSS	J18		
B1	G3	D1	P4	F1	V4	H1	V7	J1	B10	Sc-f	D12	VSS	J3		
B2	H1	D2	R1	F2	W1	H2	W7	J2	A10	Sc-g	A11	VSS	J4		
B3	H2	D3	R2	F3	W2	H3	Y7	J3	D9	Sc-h	B11	VSS	K17		
B4	J1	D4	R3	F4	W3	H4	U8	J4	C9	Sc-i	C11	VSS	K18		
B5	J2	D5	R4	F5	W4	H5	V8	J5	B9	Sc-j	D11	VSS	K3		
B6	K1	D6	T1	F6	Y3	H6	W8	J6	A9	Sd-e	D5	VSS	K4		
B7	K2	D7	T2	F7	Y4	H7	Y8	J7	D8	Sd-f	C5	VSS	L17		
B8	L1	D8	T3	F8	U5	H8	U9	J8	C8	Sd-g	B5	VSS	L18		
B9	C19	D9	C17	F9	B18	H9	A18	J9	B17	Sd-h	A5	VSS	L3		
B10	U12	D10	Y16	F10	T17	H10	L19	J10	E17	Sd-i	A4	VSS	L4		
B11	U13	D11	Y17	F11	T18	H11	L20	J11	E18	Sd-j	B4	VSS	M17		
B12	V13	D12	W17	F12	T19	H12	K20	J12	E19	Se-f	C4	VSS	M18		
B13	W13	D13	Y18	F13	T20	H13	K19	J13	E20	Se-g	D4	VSS	M3		
B14	Y13	D14	W18	F14	R17	H14	J20	J14	D17	Se-h	E4	VSS	M4		
B15	U14	D15	Y19	F15	R18	H15	J19	J15	D18	Se-i	H4	NC	A1		
B16	V14	D16	W19	F16	R19	H16	H20	J16	D19	Se-j	H3	NC	A2		
B17	W14	D17	W20	F17	R20	H17	H19	J17	D20	Sf-g	A3	NC	A20		

Product Pinout [BGA256 Package]

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	NC	NC	Sf-g	Sd-i	Sd-h	J0	F0	B0	J6	J2	Sc-g	Sb-j	Sb-f	Sa-j	Sa-f	Sa-b	I9	H9	G9	NC
B	Sh-j	Sg-i	Sf-h	Sd-j	Sd-g	I0	E0	A0	J5	J1	Sc-h	Sc-d	Sb-g	Sb-c	Sa-g	Sa-c	J9	F9	E9	NC
C	Si-j	Sg-j	Sf-i	Se-f	Sd-f	H0	D0	J8	J4	I8	Sc-i	Sc-e	Sb-h	Sb-d	Sa-h	Sa-d	D9	C9	B9	A9
D	A1	Sh-i	Sf-j	Se-g	Sd-e	G0	C0	J7	J3	I7	Sc-j	Sc-f	Sb-i	Sb-e	Sa-i	Sa-e	J14	J15	J16	J17
E	A2	A3	Sg-h	Se-h													J10	J11	J12	J13
F	A4	A5	A6	*VDD*													I14	I15	I16	I17
G	A7	A8	B1	*VDD*													I10	I11	I13	I12
H	B2	B3	Se-j	Se-i													*VDD*	*VDD*	H17	H16
J	B4	B5	VSS	VSS													VSS	VSS	H15	H14
K	B6	B7	VSS	VSS													VSS	VSS	H13	H12
L	B8	C2	VSS	VSS													VSS	VSS	H10	H11
M	C1	C3	VSS	VSS													VSS	VSS	G16	G17
N	C4	C5	*VDD*	V-Bias													*VDD*	*VDD*	G14	G15
P	C6	C7	C8	D1													G10	G11	G12	G13
R	D2	D3	D4	D5													F14	F15	F16	F17
T	D6	D7	D8	E1													F10	F11	F12	F13
U	E2	E3	E4	E5	F8	G4	G8	H4	H8	A10	A14	B10	B11	B15	C11	C15	E14	E15	E16	E17
V	E6	E7	E8	F1	G1	G5	H1	H5	I1	I6	A13	A17	B12	B16	C12	C16	E10	E11	E12	E13
W	F2	F3	F4	F5	G2	G6	H2	H6	I2	I5	A12	A16	B13	B17	C13	C17	D12	D14	D16	D17
Y	NC	NC	F6	F7	G3	G7	H3	H7	I3	I4	A11	A15	B14	C10	C14	D10	D11	D13	D15	NC

NA256

PI5X1018 Pin Assignment (Top View)

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120mA
Power Dissipation	0.5W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 4.5V to 5.5V)

Parameters	Description	Test Conditions[1]		Min.	Typ.[2]	Max.	Units
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level		-0.5		0.8	
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}, V_{BIAS} = OPEN				±400	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND, V_{BIAS} = OPEN				±400	
I_{OZH}	High Impedence Output Current	0 ≤ N, M ≤ V_{CC}, V_{BIAS} = OPEN				±1	
I_{OZL}	Low Impedence Output Current	V_{IN} = 0V, V_{BIAS} = OPEN				±400	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA				-1.8	V
I_{OS}	Short Circuit Current[3]	N(M) = 0V, M(N) = V_{CC}		100			mA
V_H	Input Hysteresis at Control Pins				150		mV
R_{ON}	Switch On Resistance[4]	V_{CC} = Min., V_{IN} = 0.0V, I_{ON} = 48mA	Bits 0-9			20	Ω
			All other bits			25	
		V_{CC} = Min., V_{IN} = 2.4V, I_{ON} = 15mA	Bits 0-9			30	
			All other bits			40	

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters[5]	Description	Test Conditions	Typ.	Units
C_{IN}	Control Input Capacitance	V_{IN} = 0V	4	pF
C_{OFF}	Port Pin Capacitance, Port Disconnected	V_{IN} = 0V	27	pF
C_{ON}	Port Pin Capacitance, Port Connected to One Other Port	V_{IN} = 0V	52	pF

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, T_A = 25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. Measured by the voltage drop between N and M pin at indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (N,M) pins.
5. This parameter is guaranteed by design.
6. Where N is a pin of any port and M is a pin of any other port.

Power Supply Characteristics

Parameters	Description	Test Conditions[1]		Min.	Typ.[2]	Max.	Units
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = OPEN or V_{CC}			1.0	mA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = Max.	V_{IN} = 3.4V[3]			2.5	mA

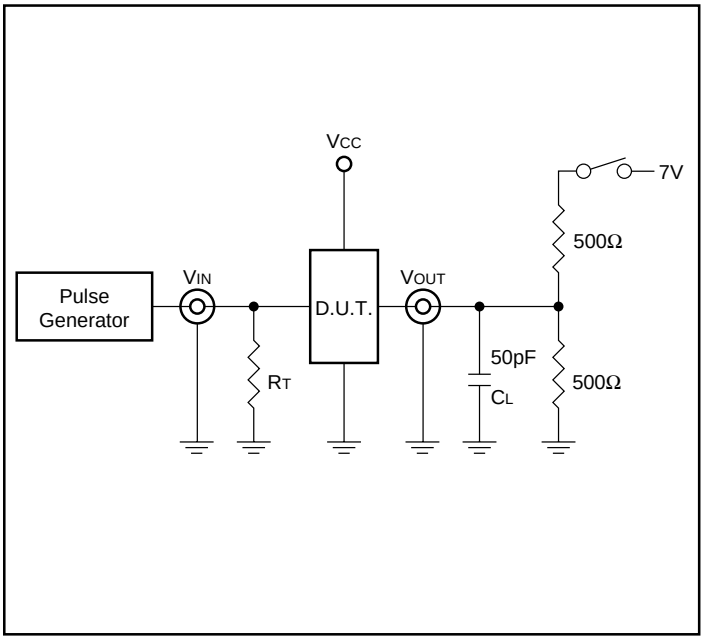
Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V, control inputs only); port A - J pins do not contribute to I_{CC}.
4. This current applies to the control inputs only and represent the current required to switch internal capacitance at the specified frequency. The port A - J inputs generate no significant AC or DC currents as they transition. This parameter is not tested, but is guaranteed by design.

Switching Characteristics over Operating Range

Parameters	Description	Conditions	PI5X1018 (Com)			Units
			Min.	Typ.	Max.	
t_{PLH} t_{PHL}	Propagation Delay[2,3,4] N_0 to M_0, N_0 to M_0 N_9 to M_9, N_9 to M_9	Load = C_L = 20pF	—	1.0	1.25	ns
t_{PLH} t_{PHL}	Propagation Delay[2,3,5] N_X to M_X, N_X to M_X Bits 1 through 8 & 10 thru 17		—	—	2.0	
t_{PZH} t_{PZL}	Bus Enable Time[4,5] S_{N-M} to N_X or M_X	See Note 1	1.5	—	6.0	
t_{PHZ} t_{PLZ}	Bus Enable Time[4,5] S_{N-M} to N_X or M_X		1.5	—	5.0	

Notes:
1. See test circuit and waveforms.
2. This parameter is guaranteed but not tested on Propagation Delays.
3. The bus switch contributes no propagational delay other than the RC delay of the ON resistance of the switch and the load capacitance. Propagational delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
4. Where N_0 is Bit 0 of any port N = A - J and M_0 is Bit 0 of any other port.
5. Where N_X is Bit X (X = 0 - 17) of any port N = A - J and N_X is Bit X (X = 0 - 17) of any other port.

Test Circuits



Switch Position

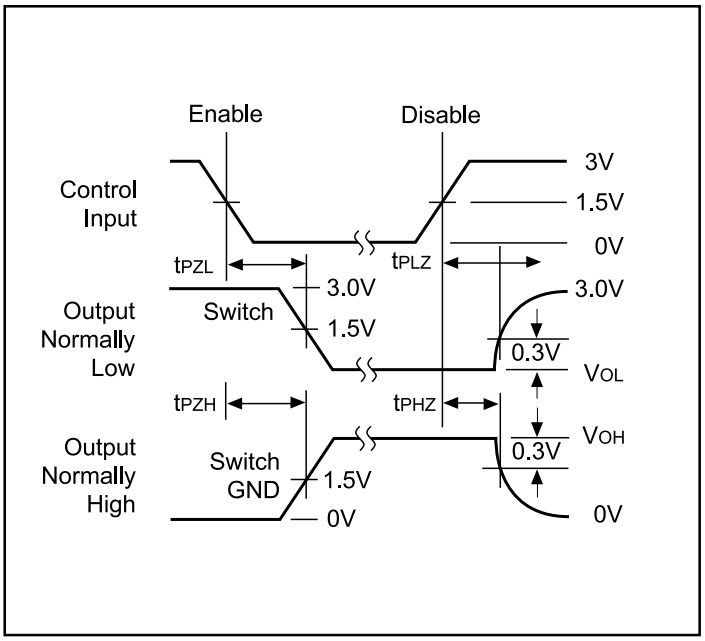
Test	Switch
Disable LOW Enable LOW	Closed
tpd	Open

Definitions:

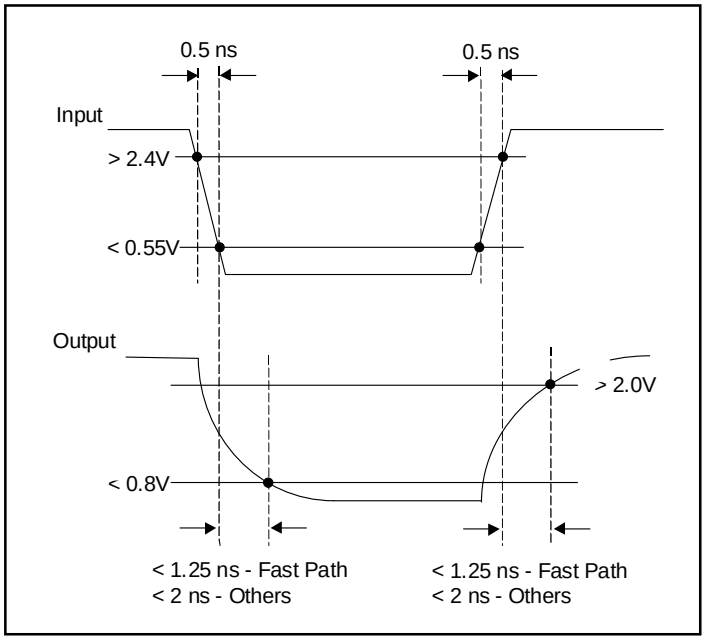
C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

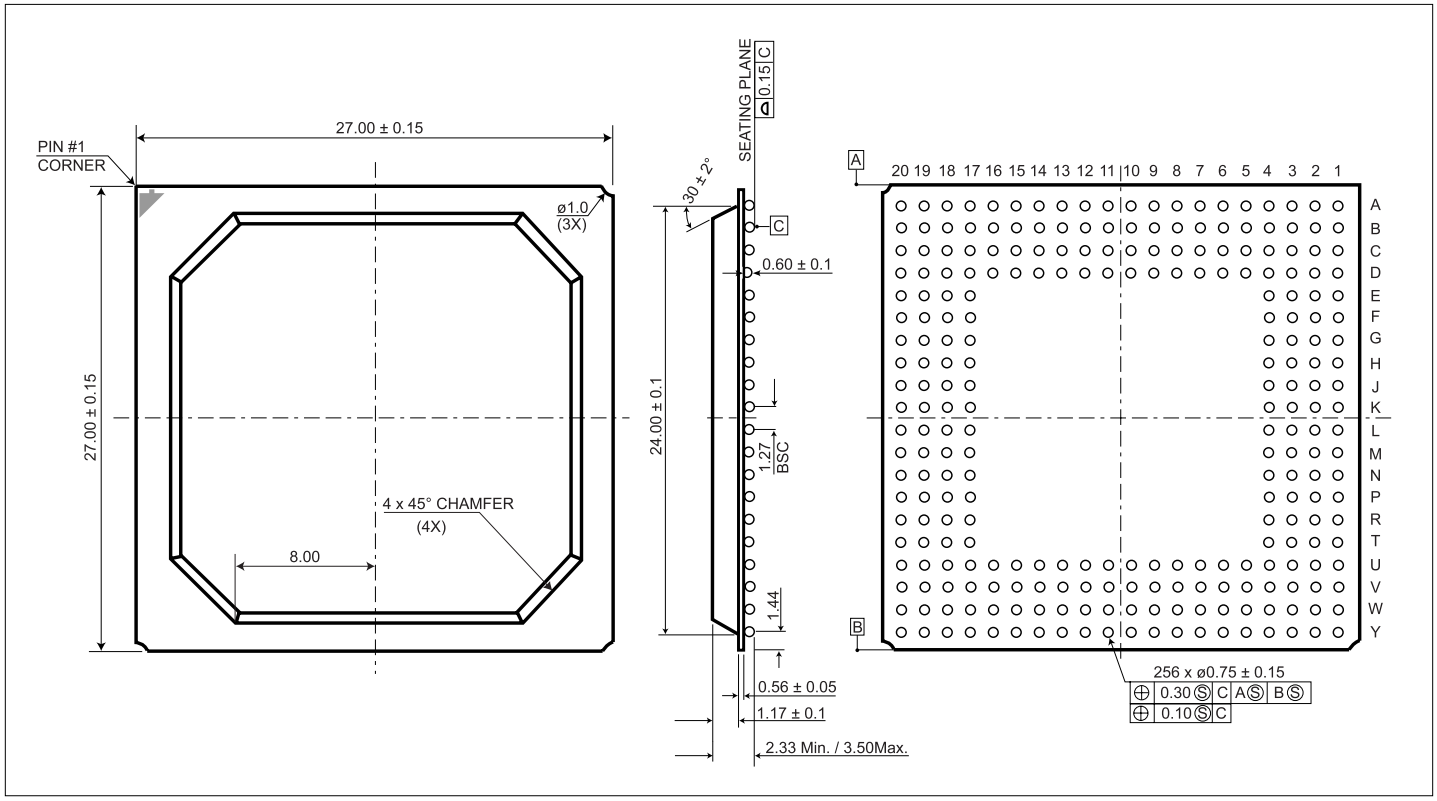
Enable and Disable Timing



Propagation Delay



256-Pin Ball Grid Array Package (27 × 27mm)



Ordering Information

Part	Pin - Package	Dimensions
PI5X1018NA	256 - BGA (NA256)	27mm x 27mm