2-bit bidirectional low voltage translator

Features

- 2-bit bidirectional translator
- Less than 1.5 ns maximum propagation delay to accommodate Standard mode and Fast mode I2C-bus devices and multiple masters
- Allows voltage level translation between 0.8V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V and 5 V buses, which allows direct interface with GTL, GTL+, LVTTL/TTL and 5 V CMOS levels
- Provides bidirectional voltage translation with no direction pin
- Low 3.5 ohm ON-state connection between input and output ports provides less signal distortion
- Supports hot insertion
- 5 V tolerant inputs
- Flow through pin out for ease of printed-circuit board trace routing
- ESD protection exceeds 4KV HBM per JESD22-A114
- Package: UQFN1.6*1.6-8L, MSOP-8L,SOIC-8L

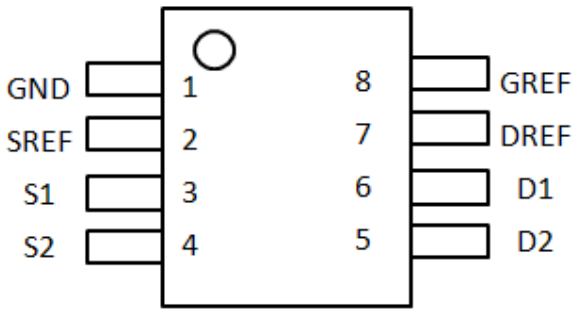
Description

The Gunning Transceiver Logic - Transceiver Voltage Clamps (GTL-TVC) provide high-speed voltage translation with low ON-state resistance and minimal propagation delay. The GTL2002 provides 2 NMOS pass transistors (Sn and Dn) with a common gate (GREF) and a reference transistor (SREF and DREF). The device allows bidirectional voltage translations between 0.8 V and 5.0 V without use of a direction pin.

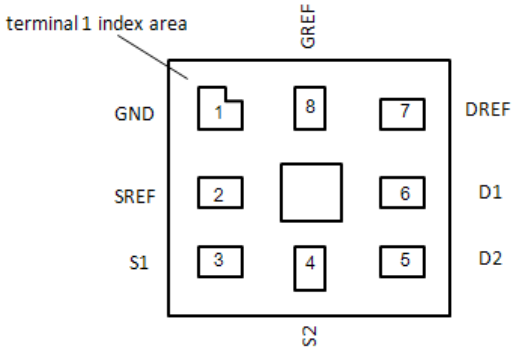
When the Sn or Dn port is LOW the clamp is in the ON-state and a low resistance connection exists between the Sn and Dn ports. Assuming the higher voltage is on the Dn port, when the Dn port is HIGH, the voltage on the Sn port is limited to the voltage set by the reference transistor (SREF). When the Sn port is HIGH, the Dn port is pulled to VCC by the pull-up resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user, without the need for directional control.

All transistors have the same electrical characteristics and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete transistor voltage translation solutions, since the fabrication of the transistors is symmetrical. Because all transistors in the device are identical, SREF and DREF can be located on any of the other two matched Sn/Dn transistors, allowing for easier board layout. The translator's transistors provide excellent ESD protection to lower voltage devices and at the same time protect less ESD-resistant devices.

Pin Configuration



MSOP-8L/SOIC-8L(Top View)



UQFN1.6*1.6-8L(Top View)

Pin Description

Pin No	Name	Description
1	GND	ground (0 V)
2	SREF	low-voltage side reference supply voltage for S1 and D1
3	S1	serial clock, low-voltage side; connect to SREF through a pull-up resistor
4	S2	serial data, low-voltage side; connect to SREF through a pull-up resistor
5	D2	serial data, high-voltage side; connect to DREF through a pull-up resistor
6	D1	serial clock, high-voltage side; connect to DREF through a pull-up resistor
7	DREF	high-voltage side reference supply voltage for S2 and D2
8	GREF	switch enable input; connect to DREF and pull-up through a high resistor

Block Diagram

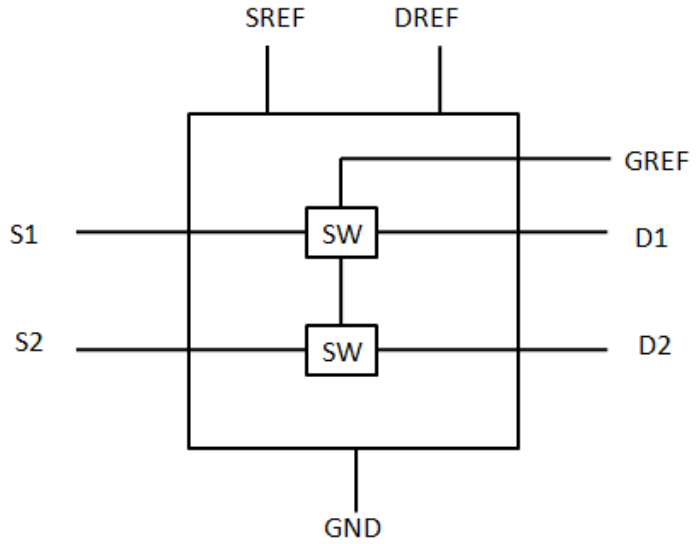


Figure.1Block Diagram

Function selection, HIGH to LOW translation
Assuming Dn is at the higher voltage level.
H = HIGH voltage level; L = LOW voltage level; X = Don't care.

GREF	DREF	SREF	Input Dn	Output Sn	Transistor
H	H	0V	X	X	off
H	H	VTT	H	VTT	on
H	H	VTT	L	L	on
L	L	0V-VTT	X	X	off

[1] GREF should be at least 1.5 V higher than SREF for best translator operation.
[2] Sn is not pulled up or pulled down.
[3] Sn follows the Dn input LOW.
[4] VTT is equal to the SREF voltage.

Function selection, LOW to HIGH translation
Assuming Dn is at the higher voltage level.
H = HIGH voltage level; L = LOW voltage level; X = Don't care.

GREF	DREF	SREF	Input Sn	Output Dn	Transistor
H	H	0V	X	X	off
H	H	VTT	VTT	H	nearly off
H	H	VTT	L	L	on
L	L	0V-VTT	X	X	off

[1] GREF should be at least 1.5 V higher than SREF for best translator operation.
[2] Sn is not pulled up or pulled down.
[3] Sn follows the Dn input LOW.
[4] VTT is equal to the SREF voltage.

Maximum Ratings

Storage Temperature ..... -65°C to +150°C
Reference Voltage[2] ..... -0.5V to +6.0V
Reference bias voltage ..... -0.5V to+6.0V
DC Input Voltage ..... -0.5V to +6.0V
Control Input Votage(EN) ..... -0.5V to+6.0V
channel current (DC)..... 128mA
Input clamping Current..... -50mA
ESD: HBM Mode 4000V

Note:
1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. The input and input/output negative voltage ratings may be exceeded if the input and input/output clamp current ratings are observed.

Recommended operation conditions

V_{CC} = 2.7 V to 5.5 V; GND = 0 V; T_A = -40 °C to +85 °C; unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{I/O}$	Voltage on an input/output pin	S1, D1, S2, D2	0	-	5	V
SREF	Reference voltage (1)	SREF	0	-	5	V
DREF	Reference bias voltage (2)	DREF	0	-	5	V
V_{GREF}	Input voltage on pin GREF	-	0	-	5	V
$I_{(pass)}$	Pass switch current	-	-	-	64	mA
T_A	Ambient temperature	-	-40	-	85	°C

DC Electrical Characteristics

T_A = -40 °C to +85 °C; unless otherwise specified

Parameter	Description	Test Conditions[1]		Min	Typ.[2]	Max	Unit
Input and output DB and SB							
V_{IK}	input clamping voltage	I_I = -18mA; V_{GREF} = 0 V		-	-	-1.2	V
I_{IH}	HIGH-level input current	V_I = 5 V; V_{GREF} = 0 V		-	-	5	µA
C_{GREF}	input capacitance on pin GREF	V_I = 3 V or 0 V		-	11	-	pF
$C_{io(off)}$	off-state input/output capacitance (Sn, Dn)	V_O = 3 V or 0 V; V_{GREF} = 0 V		-	4	-	pF
$C_{io(on)}$	on-state input/output capacitance (Sn, Dn)	V_O = 3 V or 0 V; V_{GREF} = 3 V		-	10.5	-	pF
Ron	ON-state resistance[2] (Sn, Dn)	V_I = 0V; I_O = 64mA	V_{GREF} = 4.5 V	-	3.5	5.5	Ω
			V_{GREF} = 3 V	-	4.7	7.0	Ω
			V_{GREF} = 2.3 V	-	6.3	9.5	Ω
			V_{GREF} = 1.5 V	-	60	140	Ω
		V_I = 2.4V; I_O = 15mA	V_{GREF} = 4.5 V	1	6	15	Ω
			V_{GREF} = 3 V	20	60	140	Ω
		V_I = 1.7V; I_O = 15mA	V_{GREF} = 2.3 V	20	60	140	Ω

Notes:

1) All typical values are at T_A = 25 °C.

2) Measured by the voltage drop between the S1 and S2, or D1 and D2 terminals at the indicated current through the switch. ON-state resistance is determined by the lowest voltage of the two terminals.

Dynamic characteristics

T_A = -40 °C to +85 °C; unless otherwise specified. Values guaranteed by design.

Symbol	Parameter	Conditions	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		Unit
			Min	Max	Min	Max	Min	Max	
V_{GREF} = 3.3 V; V_H = 3.3 V; V_L = 0 V; V_M = 1.15 V									
t_{PLH}	LOW-to-HIGH propagation delay	from (input) S2 or D2 to (output) S1 or D1	0	0.8	0	0.6	0	0.3	ns
t_{PHL}	HIGH-to-LOW propagation delay	from (input) S2 or D2 to (output) S1 or D1	0	1.2	0	1	0	0.5	ns
V_{GREF} = 2.5 V; V_H = 2.5 V; V_L = 0 V; V_M = 0.75 V									
t_{PLH}	LOW-to-HIGH propagation delay	from (input) S2 or D2 to (output) S1 or D1	0	1	0	0.7	0	0.4	ns
t_{PHL}	HIGH-to-LOW propagation delay	from (input) S2 or D2 to (output) S1 or D1	0	1.3	0	1	0	0.6	ns
V_{GREF} = 3.3 V; V_H = 2.3 V; V_L = 0 V; V_T = 3.3 V; V_M = 1.15 V; R_L = 300 Ω									
t_{PLH}	LOW-to-HIGH propagation delay	ffrom (input) S1 orD1 to (output) S2 or D2	0	0.9	0	0.6	0	0.4	ns
t_{PHL}	HIGH-to-LOW propagation delay	from (input) S1 or D1 to (output) S2 or D2	0	1.4	0	1.1	0	0.7	ns
V_{GREF} = 2.5 V; V_H = 1.5 V; V_L = 0 V; V_T = 2.5 V; V_M = 0.75 V; R_L = 300 Ω									
t_{PLH}	LOW-to-HIGH propagation delay	from (input) S1 orD1 to (output) S2 or D2	0	1	0	0.6	0	0.4	ns
t_{PHL}	HIGH-to-LOW propagation delay	from (input) S1 or D1 to (output) S2 or D2	0	1.3	0	1.3	0	0.8	ns

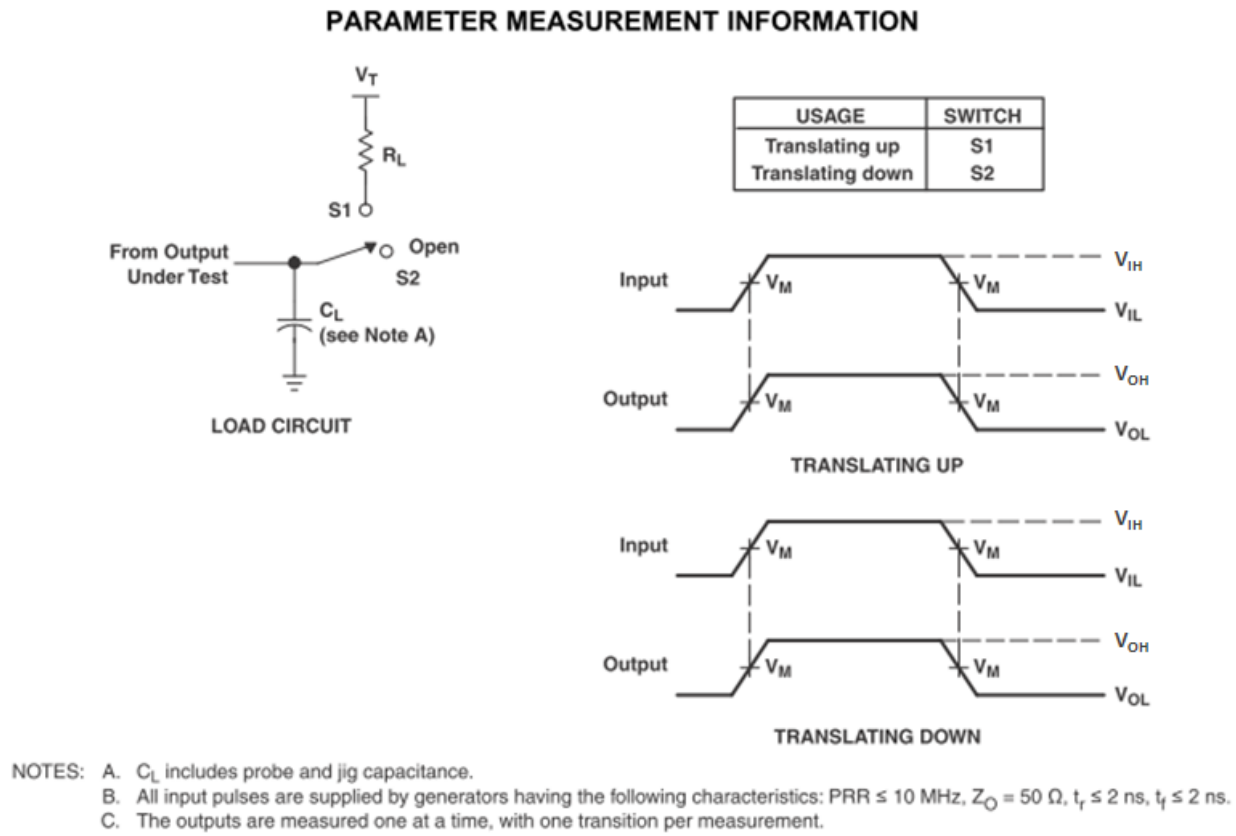


Figure.2 Load Circuit for Outputs

Application Information

For the bidirectional clamping configuration, higher voltage to lower voltage or lower voltage to higher voltage, the GREF input must be connected to DREF and both pins pulled to HIGH side VCC through a pull-up resistor (typically 200 kΩ). A filter capacitor on DREF is recommended. The processor output can be totem pole or open-drain (pull-up resistors may be required) and the chip set output can be totem pole or open-drain (pull-up resistors are required to pull the Dn outputs to VCC). However, if either output is totem pole, data must be unidirectional or the outputs must be 3-stateable and the outputs must be controlled by some direction control mechanism to prevent HIGH-to-LOW contentions in either direction. If both outputs are open-drain, no direction control is needed. The opposite side of the reference transistor (SREF) is connected to the processor core power supply voltage. When DREF is connected through a 200 kΩ resistor to a 3.3 V to 5.5 V VCC supply and SREF is set between 0.8 V to (VCC -1.5 V), the output of each Sn has a maximum output voltage equal to SREF and the output of each Dn has a maximum output voltage equal to VCC.

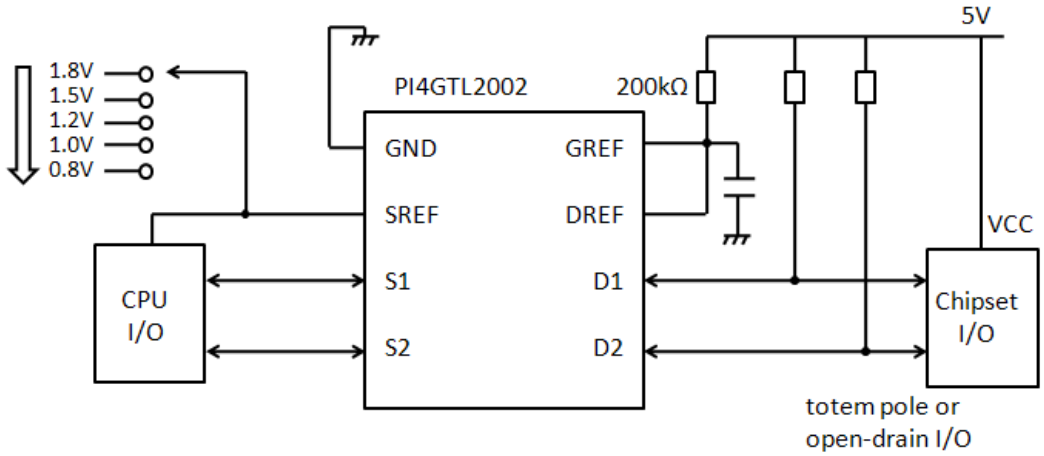


Figure.3 Bidirectional translation to multiple higher voltage levels such as an I2C-bus application

For unidirectional clamping, higher voltage to lower voltage, the GREF input must be connected to DREF and both pins pulled to the higher side VCC through a pull-up resistor (typically 200 kΩ). A filter capacitor on DREF is recommended. Pull-up resistors are required if the chip set I/O are open-drain. The opposite side of the reference transistor (SREF) is connected to the processor core supply voltage. When DREF is connected through a 200 kΩ resistor to a 3.3 V to 5.5 V VCC supply and SREF is set between 0.8 V to (VCC-1.5 V), the output of each Sn has a maximum output voltage equal to SREF.

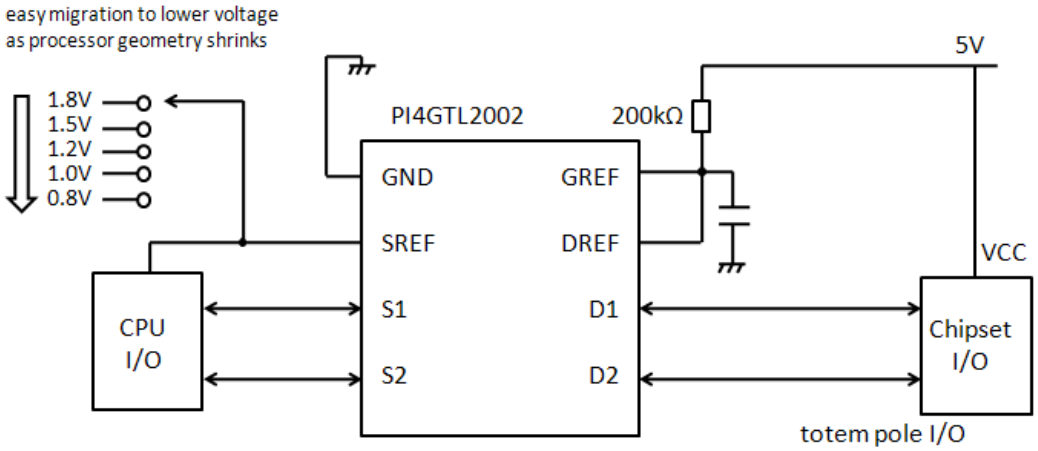


Figure.4 Unidirectional down translation to protect low voltage processor pins

For unidirectional up translation, lower voltage to higher voltage, the reference transistor is connected the same as for a down translation. A pull-up resistor is required on the higher voltage side (Dn or Sn) to get the full HIGH level, since the GTL-TVC device will only pass the reference source (SREF) voltage as a HIGH when doing an up translation. The driver on the lower voltage side only needs pull-up resistors if it is open-drain.

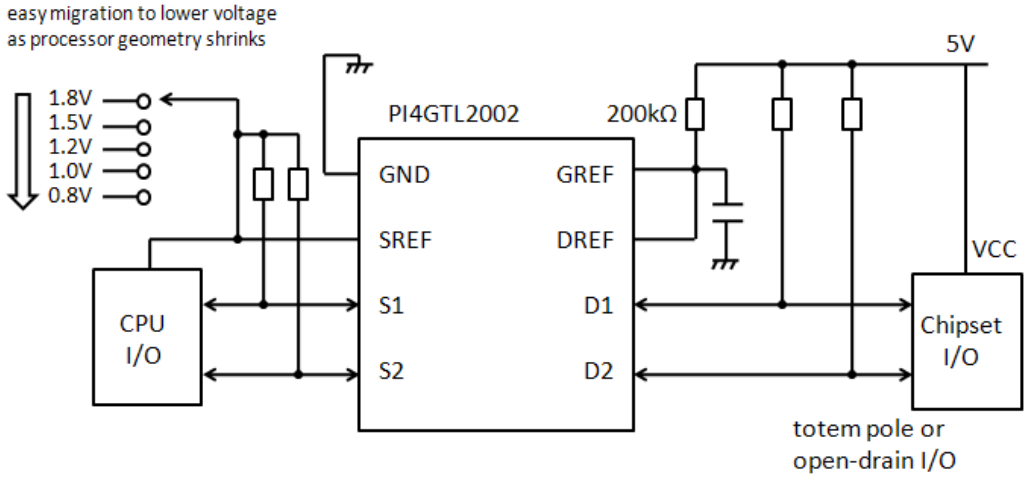


Figure.5 Unidirectional down translation to protect higher voltage processor pins

Pull-up resistors and minimum values

Sizing the pull-up resistor on an open-drain bus is specific to the individual application and is dependent on the following driver characteristics:

- The driver sink current
- The V_{OL} of driver
- The V_{OL} of the PI4GTL2002
- The V_{IL} of the driver
- Frequency of operation

The following tables can be used to estimate the pull-up resistor value in different use cases so that the minimum resistance for the pull-up resistor can be found.

Tables in bellow contain suggested minimum values of pull-up resistors for the PI4GTL2002 with typical voltage translation levels and drive currents.

The calculated values assume that both drive currents are the same.

V_{OL} = V_{IL} = 0.1*VCC and accounts for a 10 % VCC tolerance of the supplies, 1 % resistor values. It should be noted that the resistor chosen in the final application should be equal to or larger than the values shown in the tablew to ensure that the pass voltage is less than 10 % of the VCC voltage, and the external driver should be able to sink the total current from both pull-up resistors.

Pull-up resistor minimum values, 3 mA driver /sink current for PI4GTL2002

SREF Side	DREF side				
	1.5V	1.8V	2.5V	3.3V	5.0V
0.8V	$R_{PU(S)}$ = 825Ω $R_{PU(D)}$ = 825Ω	$R_{PU(S)}$ = 936Ω $R_{PU(D)}$ = 936Ω	$R_{PU(S)}$ = none $R_{PU(D)}$ = 899Ω Or both 1.20kΩ	$R_{PU(S)}$ = none $R_{PU(D)}$ = 1.20kΩ Or both 1.49kΩ	$R_{PU(S)}$ = none $R_{PU(D)}$ = 1.83kΩ Or both 2.12kΩ
1.0V	$R_{PU(S)}$ = 892Ω $R_{PU(D)}$ = 892Ω	$R_{PU(S)}$ = 1kΩ $R_{PU(D)}$ = 1kΩ	$R_{PU(S)}$ = none $R_{PU(D)}$ = 892Ω Or both 1.26kΩ	$R_{PU(S)}$ = none $R_{PU(D)}$ = 1.19kΩ Or both 1.56kΩ	$R_{PU(S)}$ = none $R_{PU(D)}$ = 1.82kΩ Or both 2.19kΩ
1.2V		$R_{PU(S)}$ = 1.07kΩ $R_{PU(D)}$ = 1.07kΩ	$R_{PU(S)}$ = none $R_{PU(D)}$ = 886Ω Or both 1.33kΩ	$R_{PU(S)}$ = none $R_{PU(D)}$ = 1.18kΩ Or both 1.63kΩ	$R_{PU(S)}$ = none $R_{PU(D)}$ = 1.81kΩ Or both 2.26kΩ
1.5V			$R_{PU(S)}$ = none $R_{PU(D)}$ = 875Ω Or both 1.43kΩ	$R_{PU(S)}$ = none $R_{PU(D)}$ = 1.17kΩ Or both 1.73kΩ	$R_{PU(S)}$ = none $R_{PU(D)}$ = 1.8kΩ Or both 2.36kΩ
1.8V			$R_{PU(S)}$ = 1.53kΩ $R_{PU(D)}$ = 1.53kΩ	$R_{PU(S)}$ = none $R_{PU(D)}$ = 1.16kΩ Or both 1.82kΩ	$R_{PU(S)}$ = none $R_{PU(D)}$ = 1.79kΩ Or both 2.46kΩ
2.5V				$R_{PU(S)}$ = 2.06kΩ $R_{PU(D)}$ = 2.06kΩ	$R_{PU(S)}$ = none $R_{PU(D)}$ = 1.77kΩ Or both 2.69kΩ
3.3V					$R_{PU(S)}$ = none $R_{PU(D)}$ = 1.74kΩ Or both 2.96kΩ

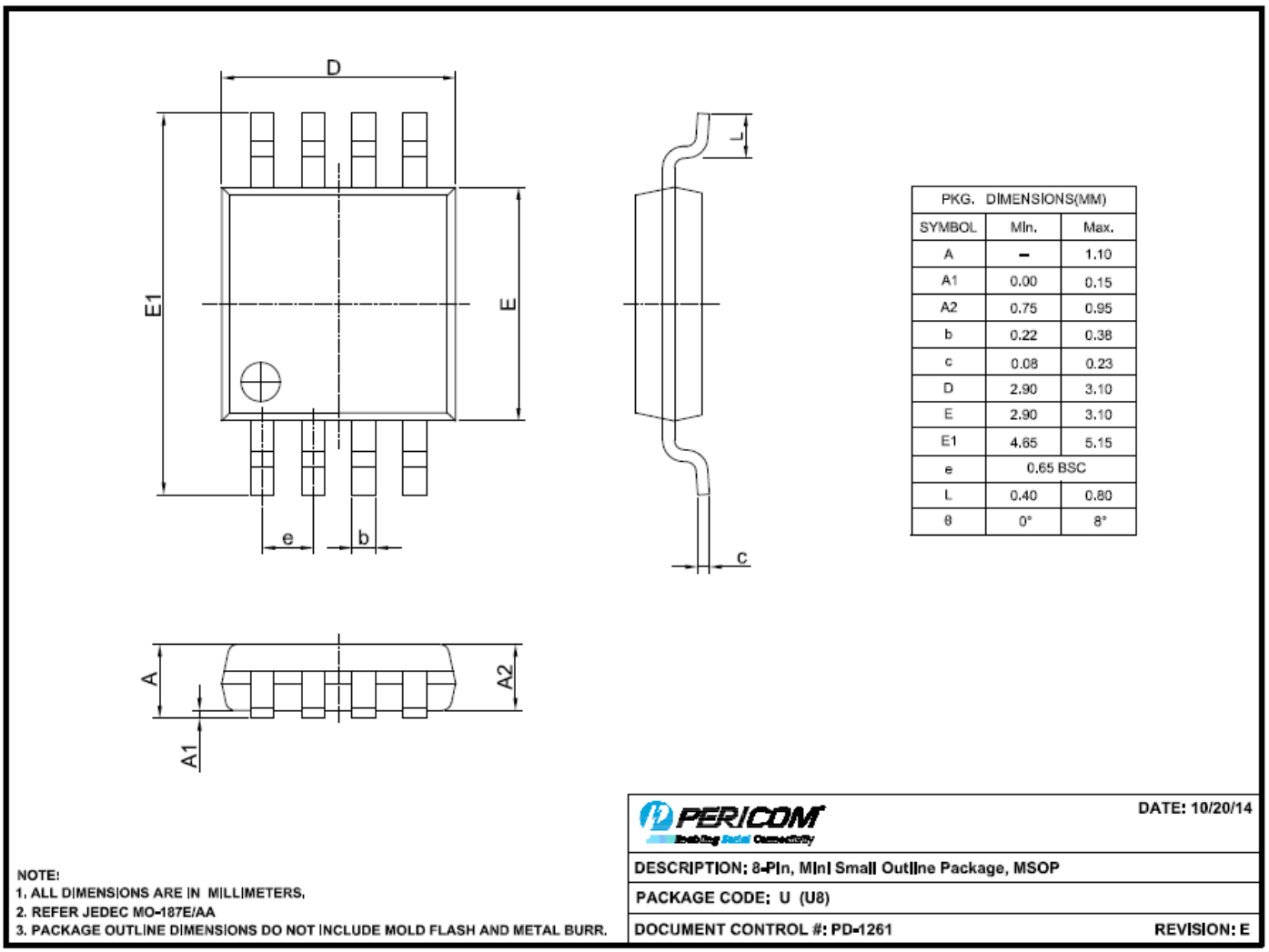
Pull-up resistor minimum values, 10 mA driver/ sink current for PI4GTL2002

SREF Side	DREF side				
	1.5V	1.8V	2.5V	3.3V	5.0V
0.8V	$R_{PU(S)}$ = 247Ω $R_{PU(D)}$ = 247Ω	$R_{PU(S)}$ = 281Ω $R_{PU(D)}$ = 281Ω	$R_{PU(S)}$ = none $R_{PU(D)}$ = 270Ω Or both 359Ω	$R_{PU(S)}$ = none $R_{PU(D)}$ = 359Ω Or both 447Ω	$R_{PU(S)}$ = none $R_{PU(D)}$ = 547Ω Or both 636Ω
1.0V	$R_{PU(S)}$ = 268Ω $R_{PU(D)}$ = 268Ω	$R_{PU(S)}$ =300Ω $R_{PU(D)}$ = 300Ω	$R_{PU(S)}$ = none $R_{PU(D)}$ = 268Ω Or both 379Ω	$R_{PU(S)}$ = none $R_{PU(D)}$ = 357Ω Or both 468Ω	$R_{PU(S)}$ = none $R_{PU(D)}$ = 545Ω Or both 657Ω
1.2V		$R_{PU(S)}$ = 321Ω $R_{PU(D)}$ = 321Ω	$R_{PU(S)}$ = none $R_{PU(D)}$ = 266Ω Or both 399Ω	$R_{PU(S)}$ = none $R_{PU(D)}$ = 355Ω Or both 488Ω	$R_{PU(S)}$ = none $R_{PU(D)}$ = 543Ω Or both 677Ω
1.5V			$R_{PU(S)}$ = none $R_{PU(D)}$ = 263Ω Or both 429Ω	$R_{PU(S)}$ = none $R_{PU(D)}$ = 352Ω Or both 518Ω	$R_{PU(S)}$ = none $R_{PU(D)}$ = 540Ω Or both 707Ω
1.8V			$R_{PU(S)}$ = 460Ω $R_{PU(D)}$ = 460Ω	$R_{PU(S)}$ = none $R_{PU(D)}$ = 348Ω Or both 548Ω	$R_{PU(S)}$ = none $R_{PU(D)}$ = 537Ω Or both 737Ω
2.5V				$R_{PU(S)}$ = 619Ω $R_{PU(D)}$ = 619Ω	$R_{PU(S)}$ = none $R_{PU(D)}$ = 521Ω Or both 808Ω
3.3V					$R_{PU(S)}$ = none $R_{PU(D)}$ = 522Ω Or both 889Ω

Pull-up resistor minimum values, 15 mA driver/ sink current for PI4GTL2002

SREF Side	DREF side				
	1.5V	1.8V	2.5V	3.3V	5.0V
0.8V	$R_{PU(S)}$ = 165Ω $R_{PU(D)}$ = 165Ω	$R_{PU(S)}$ = 187Ω $R_{PU(D)}$ = 187Ω	$R_{PU(S)}$ = none $R_{PU(D)}$ = 180Ω Or both 239Ω	$R_{PU(S)}$ = none $R_{PU(D)}$ = 239Ω Or both 298Ω	$R_{PU(S)}$ = none $R_{PU(D)}$ = 365Ω Or both 424Ω
1.0V	$R_{PU(S)}$ = 178Ω $R_{PU(D)}$ = 178Ω	$R_{PU(S)}$ = 200Ω $R_{PU(D)}$ = 200Ω	$R_{PU(S)}$ = none $R_{PU(D)}$ = 178Ω Or both 253Ω	$R_{PU(S)}$ = none $R_{PU(D)}$ = 237Ω Or both 312Ω	$R_{PU(S)}$ = none $R_{PU(D)}$ = 364Ω Or both 438Ω
1.2V		$R_{PU(S)}$ = 214Ω $R_{PU(D)}$ = 214Ω	$R_{PU(S)}$ = none $R_{PU(D)}$ = 177Ω Or both 266Ω	$R_{PU(S)}$ = none $R_{PU(D)}$ = 236Ω Or both 325Ω	$R_{PU(S)}$ = none $R_{PU(D)}$ = 362Ω Or both 451Ω
1.5V			$R_{PU(S)}$ = none $R_{PU(D)}$ = 175Ω Or both 286Ω	$R_{PU(S)}$ = none $R_{PU(D)}$ = 234Ω Or both 345Ω	$R_{PU(S)}$ = none $R_{PU(D)}$ = 360Ω Or both 471Ω
1.8V			$R_{PU(S)}$ = 306Ω $R_{PU(D)}$ = 306Ω	$R_{PU(S)}$ = none $R_{PU(D)}$ = 232Ω Or both 366Ω	$R_{PU(S)}$ = none $R_{PU(D)}$ =358Ω Or both 492Ω
2.5V				$R_{PU(S)}$ = 413Ω $R_{PU(D)}$ = 413Ω	$R_{PU(S)}$ = none $R_{PU(D)}$ = 354Ω Or both 539Ω
3.3V					$R_{PU(S)}$ = none $R_{PU(D)}$ = 348Ω Or both 593Ω

MSOP-8(U)



PKG. DIMENSIONS(MM)		
SYMBOL	Min.	Max.
A	–	1.10
A1	0.00	0.15
A2	0.75	0.95
b	0.22	0.38
c	0.08	0.23
D	2.90	3.10
E	2.90	3.10
E1	4.65	5.15
e	0.65 BSC	
L	0.40	0.80
θ	0°	8°

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. REFER JEDEC MO-187E/AA
3. PACKAGE OUTLINE DIMENSIONS DO NOT INCLUDE MOLD FLASH AND METAL BURR.

PERICOM Enabling Total Connectivity

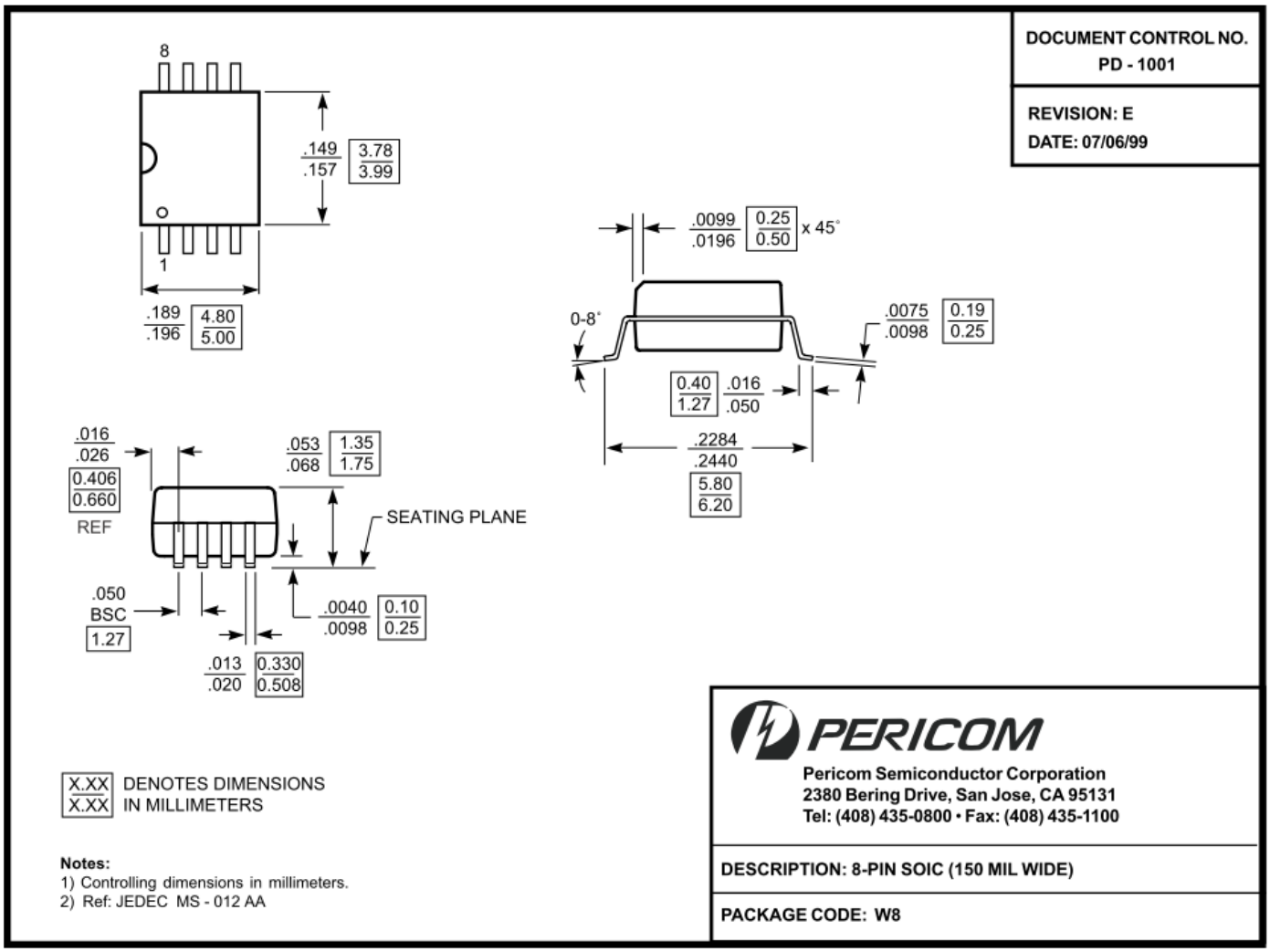
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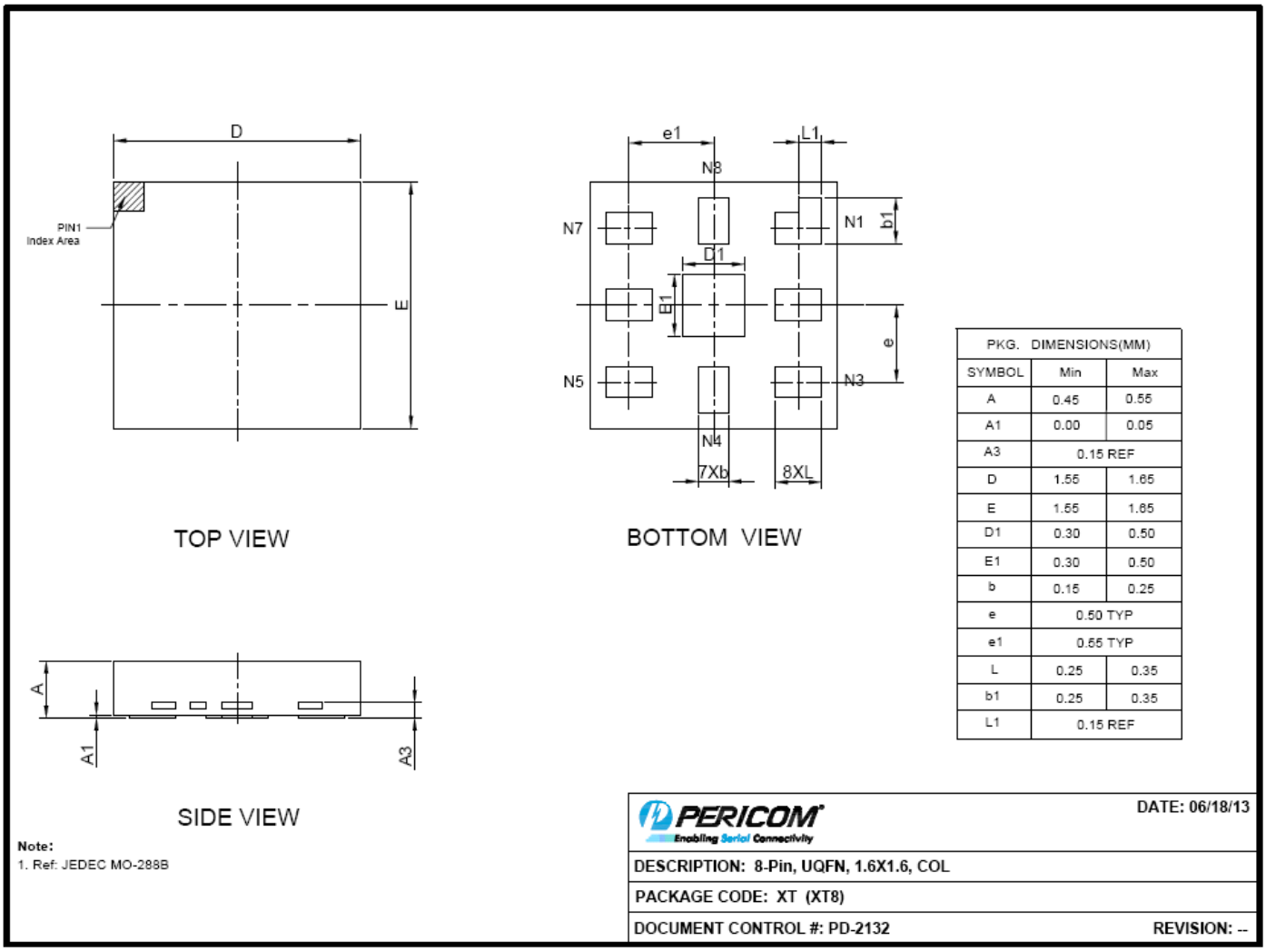
PACKAGE CODE: U (U8)

DOCUMENT CONTROL #: PD-1261 REVISION: E

SOIC-8(W)


DOCUMENT CONTROL NO.
PD - 1001
REVISION: E
DATE: 07/06/99
8
1
.149 / .157 3.78 / 3.99
.189 / .196 4.80 / 5.00
.0099 / .0196 0.25 / 0.50 x 45°
0-8°
.0075 / .0098 0.19 / 0.25
0.40 / 1.27 .016 / .050
.2284 / .2440 5.80 / 6.20
.016 / .026 0.406 / 0.660 REF
.053 / .068 1.35 / 1.75
SEATING PLANE
.050 BSC 1.27
.0040 / .0098 0.10 / 0.25
.013 / .020 0.330 / 0.508
X.XX DENOTES DIMENSIONS
X.XX IN MILLIMETERS
Notes:
1) Controlling dimensions in millimeters.
2) Ref: JEDEC MS - 012 AA
PERICOM
Pericom Semiconductor Corporation
2380 Bering Drive, San Jose, CA 95131
Tel: (408) 435-0800 • Fax: (408) 435-1100
DESCRIPTION: 8-PIN SOIC (150 MIL WIDE)
PACKAGE CODE: W8

UQFN1.6x1.6-8L



PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	0.45	0.55
A1	0.00	0.05
A3	0.15 REF	
D	1.55	1.65
E	1.55	1.65
D1	0.30	0.50
E1	0.30	0.50
b	0.15	0.25
e	0.50 TYP	
e1	0.55 TYP	
L	0.25	0.35
b1	0.25	0.35
L1	0.15 REF	

Ordering Information

Part No.	Package Code	Package
PI4GTL2002XTEX	XT	Lead free and Green UQFN1.6x1.6-8L, Tape & Reel
PI4GTL2002UE	U	Lead free and Green MSOP-8L
PI4GTL2002UEX	U	Lead free and Green MSOP-8L,Tape & Reel
PI4GTL2002WE	W	8-Pin,150 mil Wide SOIC
PI4GTL2002WEX	W	8-Pin,150 mil Wide SOIC, Tape & Reel

Note:
- E = Pb-free and Green
- Adding X Suffix= Tape/Reel

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