PGA900EVM Quick Start Guide

The following quick start guide will help the user to quickly test the front end (GAIN + ADC) and the back end (DAC + GAIN) of the PGA900. It will also show the different memories and software related tools available in the PGA900. Before proceeding, make sure the PGA900EVM is configured in its default configuration and properly connected to the USB2ANY as shown in Figure 1.

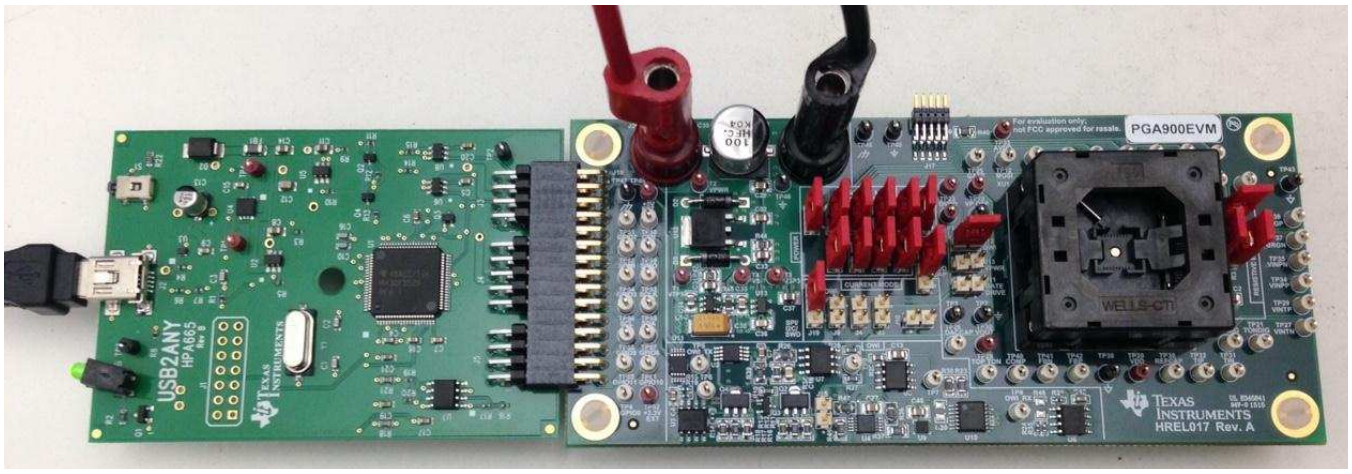

Figure 1. PGA900EVM Default Configuration

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1 Enabling Communication

1. Bring up the PGA900 GUI.
2. The default configuration for PGA900EVM is for voltage mode application. Therefore, configure the PGA900EVM by clicking on the "Interface Settings" tab and setting both the "RLOOP" and the "Additional Voltage" to 0.

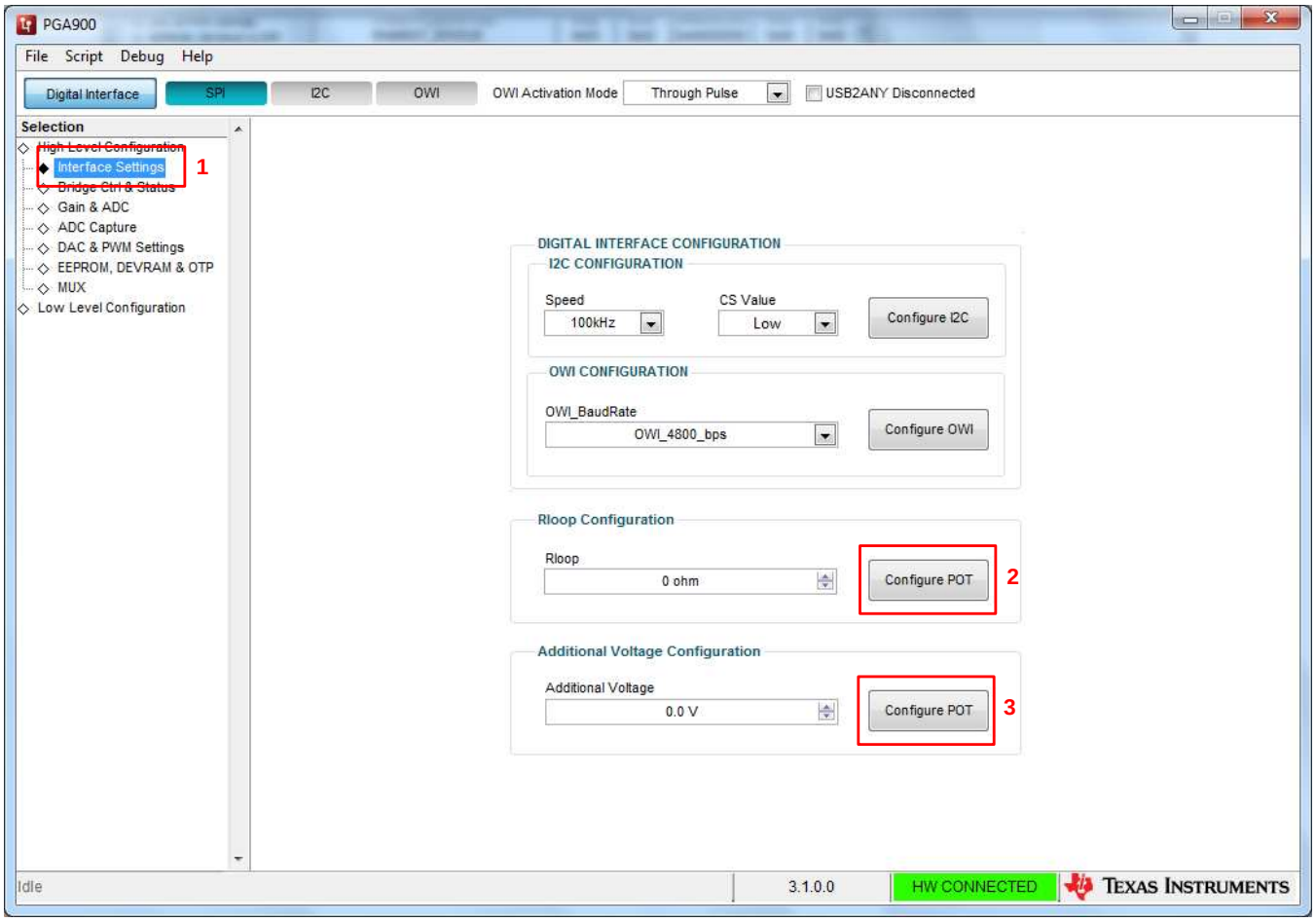

Figure 2. Configuring the Hardware for Voltage Mode

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3. The microcontroller is running at power-up. Set the microcontroller in reset by clicking on the “Microcontoller” button as shown in Figure 3. The button will change to "Digital Interface" to indicate the different digital interfaces are enabled for communication with the device.

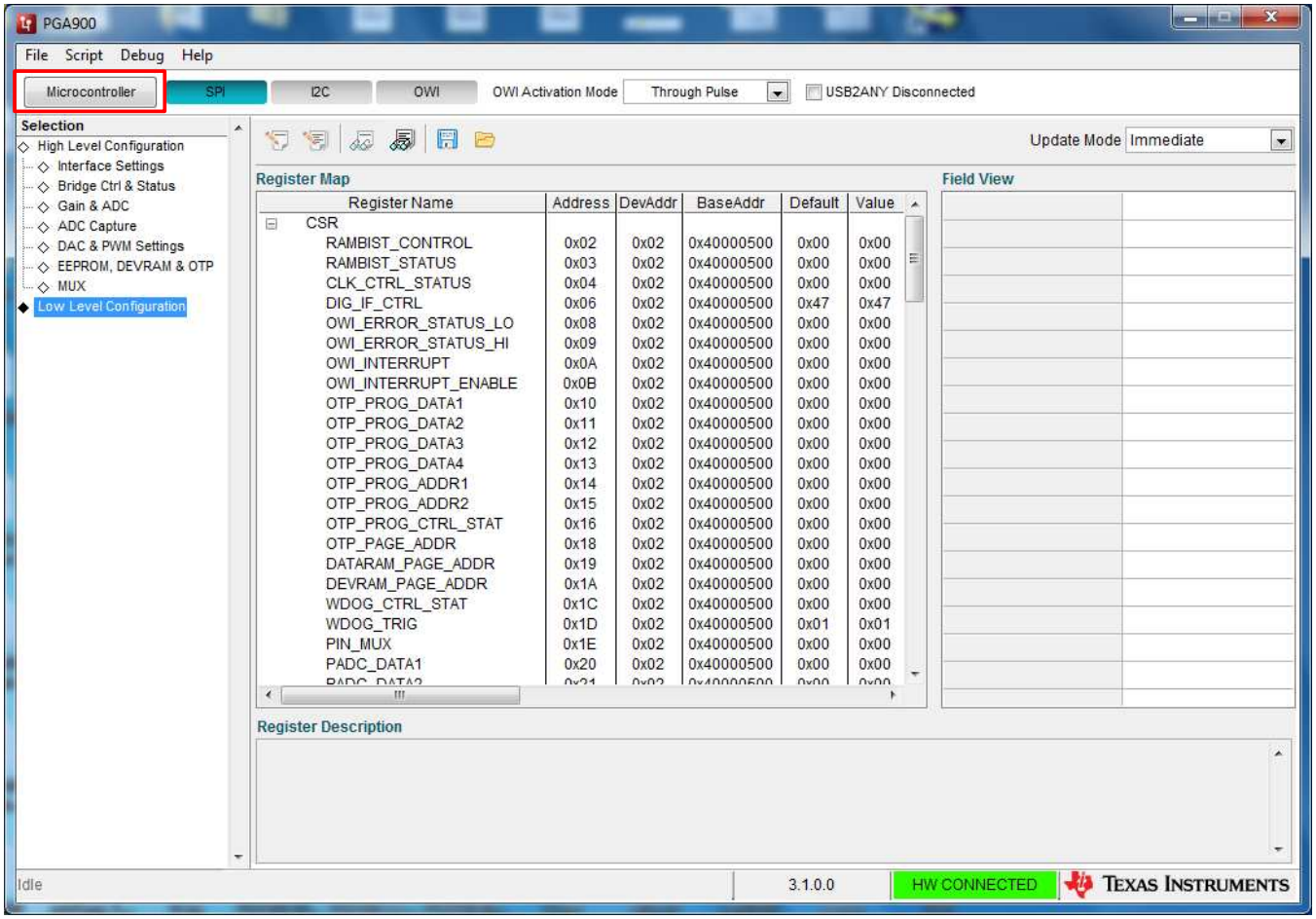

Figure 3. Setting the Microcontroller to Reset

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2 Setting Up PGAIN and Reading PADC Data

Once the digital interfaces are enabled, the device must first be taken out of shutdown mode so that the PGAIN and PADC can be used.

1. Click on the "Gain & ADC" tab.
2. Enable the VREF buffer, disable the analog shutdown and enable the ADCs as shown in Figure 4

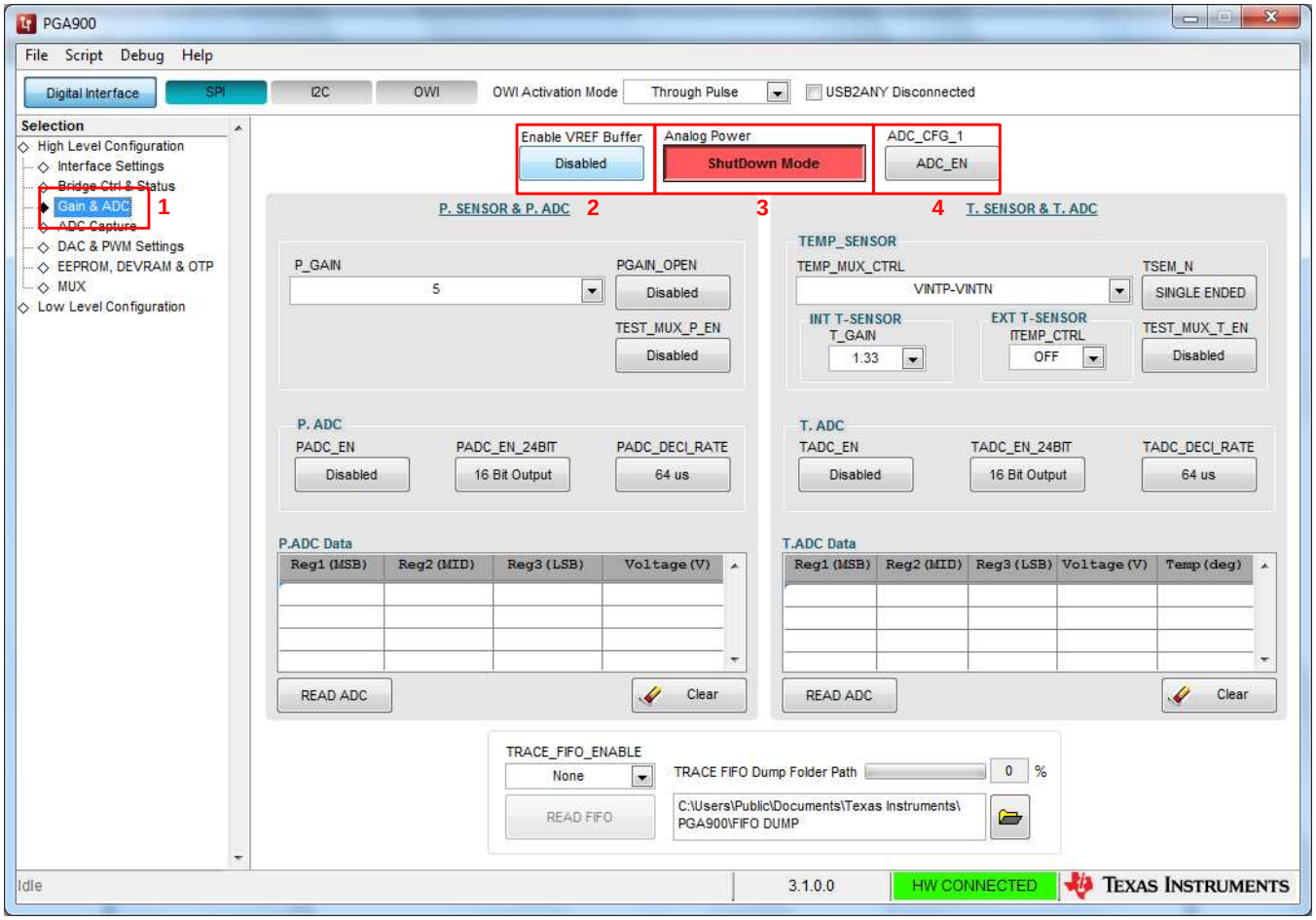

Figure 4. Enabling the Analog Power in PGA900

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3. Click on the “Bridge Ctrl & Status” tab and enable the bridge voltage as shown in Figure 5. The resistive bridge in the PGA900EVM is now being excited by the 2.5 V coming from the PGA900. The bridge in the PGA900EVM has only variable leg (top left). It consists of a 4.7-kΩ resistor in series with a dual digital potentiometer, where the potentiometers are in a parallel configuration. The user has the ability to change one or both or both potentiometers with the Potentiometer Mode menu. For demo purposes, to obtain a 10-mV differential input voltage use Table 1.

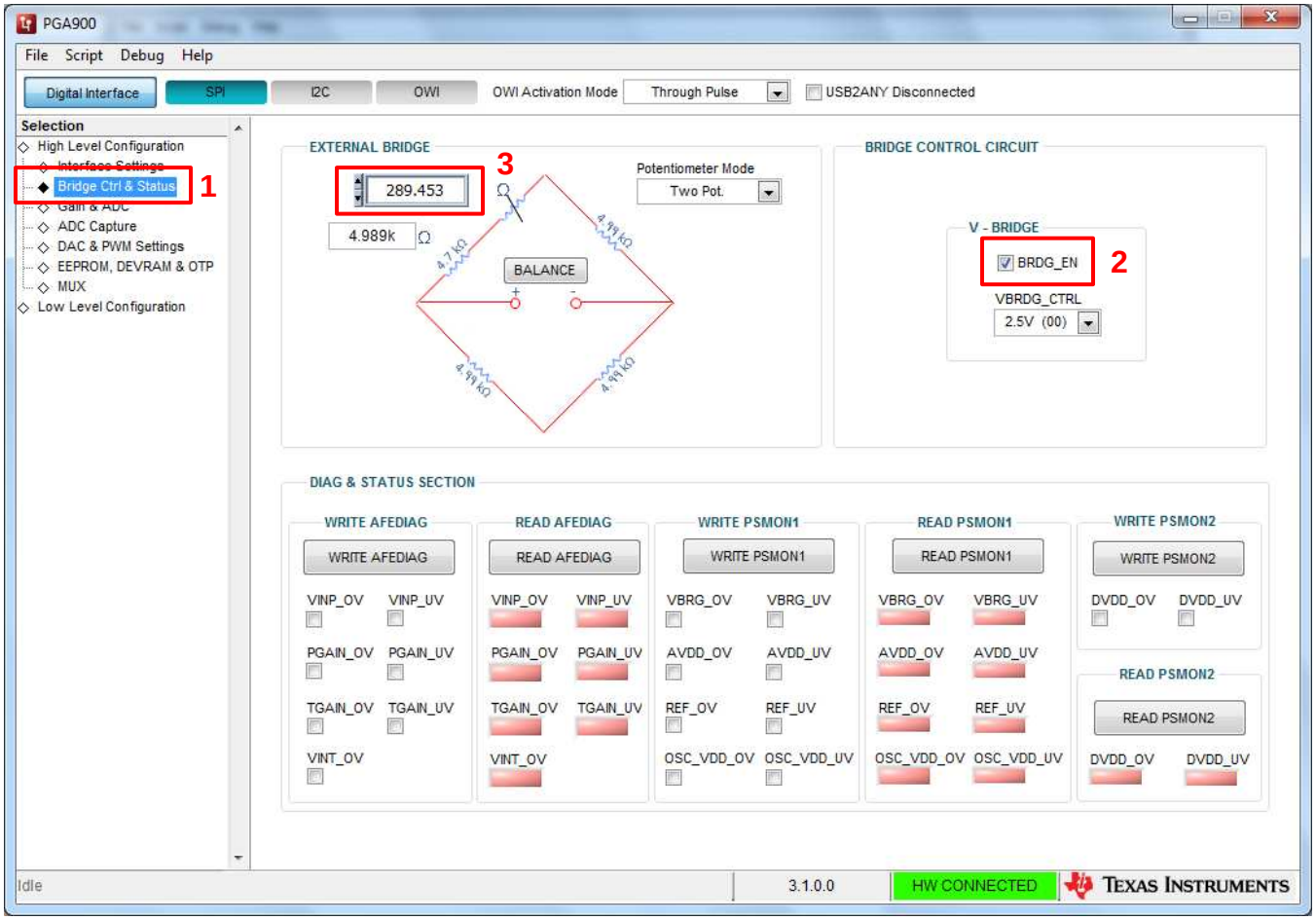

Figure 5. Enabling Bridge Voltage in PGA900 and Configuring Resistive Bridge in PGA900EVM

Table 1. Potentiometer Mode

Approximate differential voltage (mV)	One pot (Ω)	Two pot (Ω)
10	209.7	209.4
15	171.1	170.3
25	92.5	92.2

In the potentiometer box, type the desired resistance from the table above and then click outside the box. You can measure these input voltages by connecting a multimeter between TP34 (VINPP) and TP35 (VINPN) in the PGA900EVM.

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4. Click on the “Gain & ADC” tab. Select a gain for the PGAIN and enable the multiplexers to connect the PGAIN to the PADC as shown in Figure 6. The number of bits and decimation rates can also be chosen. Then click on "Read ADC". For this particular example a gain of 10 V/V was selected for PGAIN and the differential input voltage was set to approximately 10 mV in the previous step. As a result, the ADC input voltage is close to 100 mV.

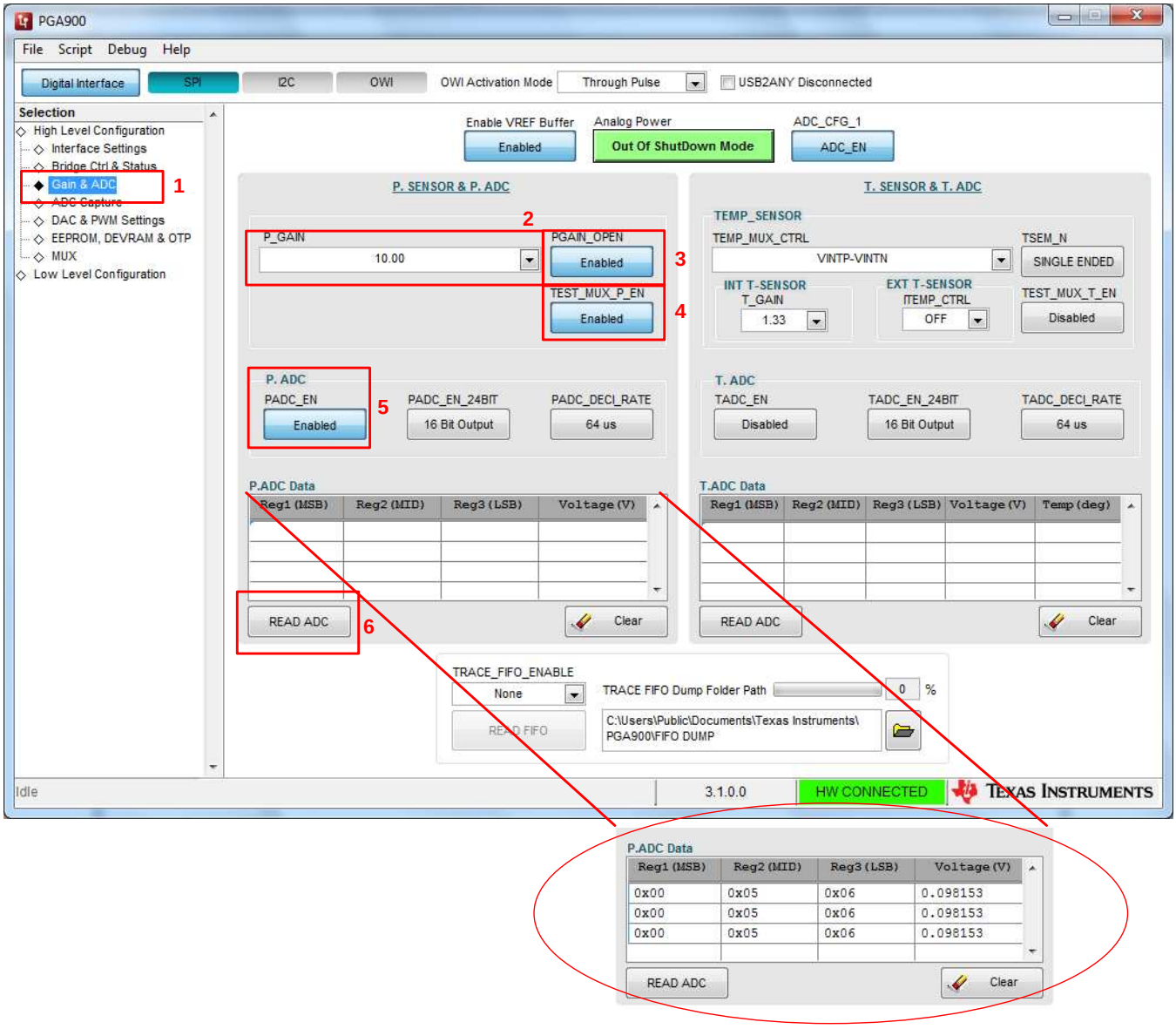

Figure 6. Configuring the PADC

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3 DAC Output Reading

The PGA900GUI can also be used to write directly to the DAC and measure the analog output.

NOTE: For the DAC to output the data from the ADC (either pressure or temperature), the M0 needs to be running the proper software. A reference firmware for the M0 can be found at the product folder for the PGA900.

1. Connect a multimeter between TP1 (VOUT after feedback) and TP39 (ASIC_GND).
2. The microcontroller has to be in reset. Click on the “DAC & PWM Settings” tab.
3. Enable the DAC and the test mux for the DAC.
4. Select the DAC configuration, absolute or ratiometric. Ratiometric is proportional to VDD, therefore for demo purposes, absolute should be chosen.
5. Select the gain from the DAC buffer . The gain is respect to VREF=1.25 V. Therefore, a gain of 4 V/V would imply a maximum output voltage of 5 V.
6. Write to the DAC in hex format. Mid-code is 0x1FFF, full code is 0x3FFF written to the DAC_REG0 register. With the gain set to 4 V/V, mid-code and full code should create a 2.5 and 5V DAC outputs respectively. Please notice that if a 10 V/V gain is selected, the input voltage to the EVM has to be greater than 12.5 V.

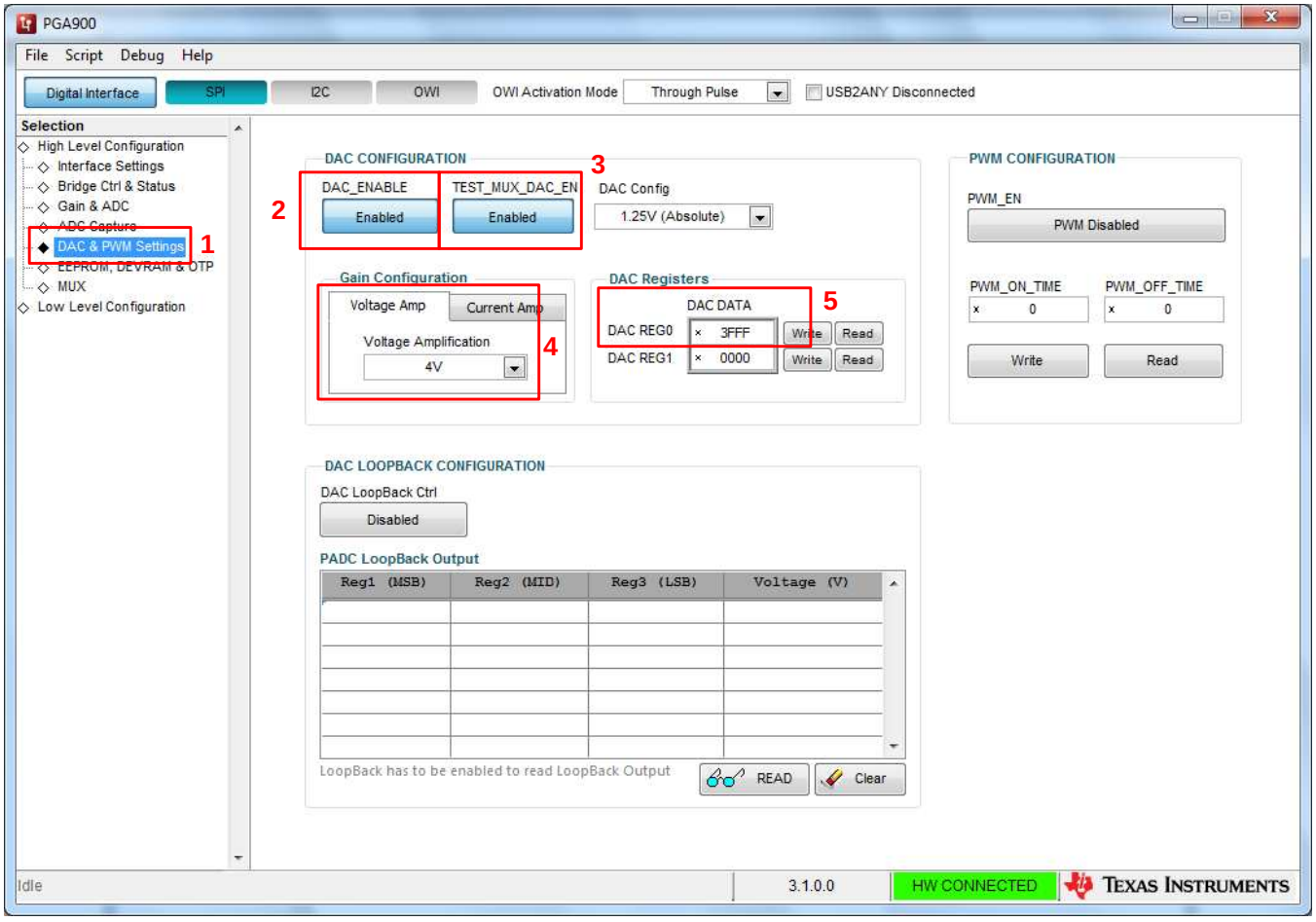

Figure 7. Writing Directly to the DAC in the PGA900

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4 Memory

The PGA900 offers different memory options depending on the customer need. The 128 bytes in the EEPROM can be read as shown in Figure 8. Additionally, DEVRAM provides the option to run code in the microprocessor without using OTP. The .hex files can be downloaded into DEVRAM and once the REMAP bit is enabled, the code overlaps the OTP memory location so that the microcontroller can execute it. Once the device is powered down, the DEVRAM content is erased. OTP is a one-time memory programming option. In order to program the OTP, 7.5 V are needed to be applied to the VP_OTP pin in the PGA900. This can be done by closing J15 in the PGA900EVM.

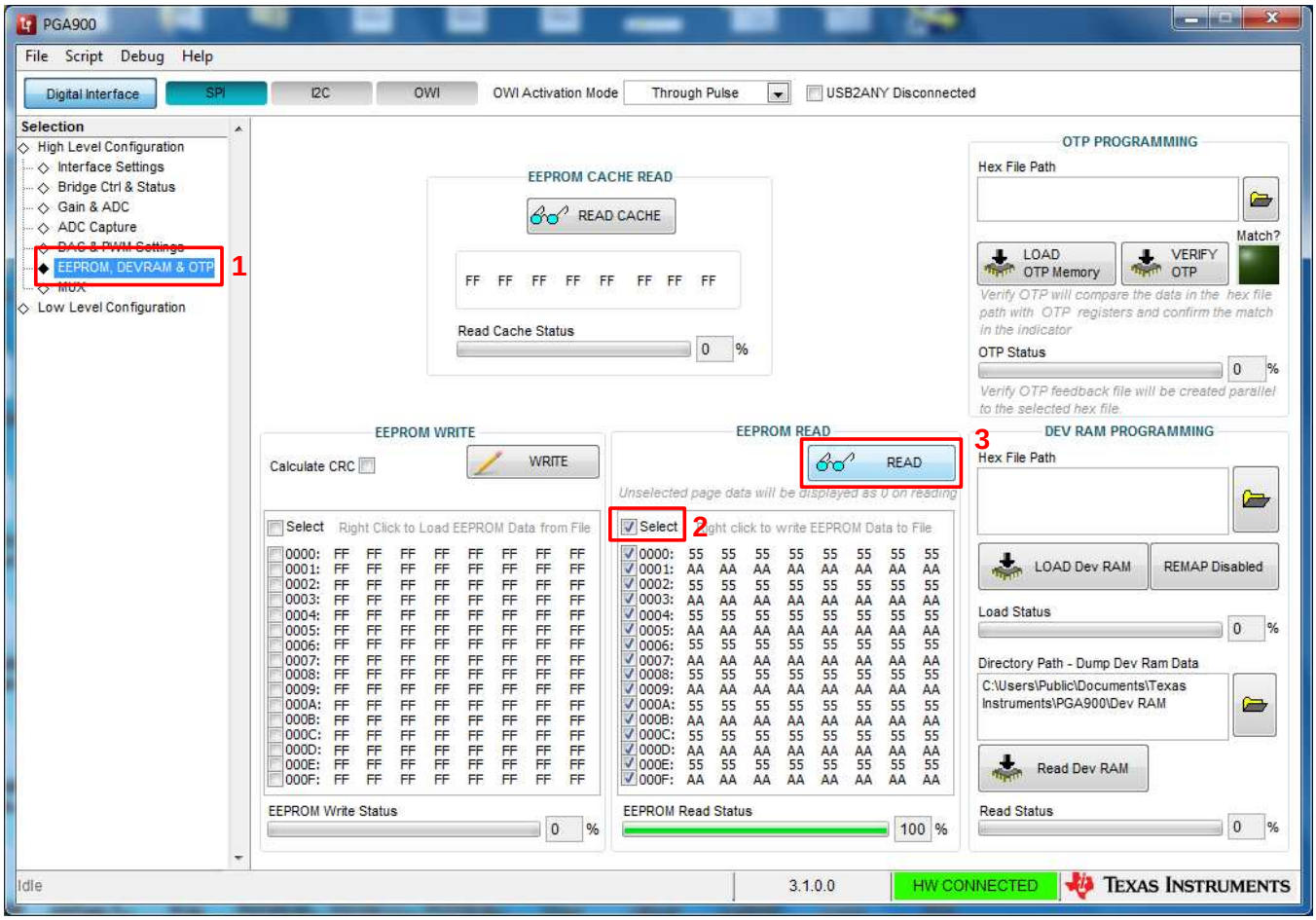

Figure 8. PGA900 Memory Options

5 Resources

For more information, see the following.

- PGA900 product page
- PGA900EVM product page

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