# Product Specification

# PE42452

**UltraCMOS® SP5T RF Switch**
**450–4000 MHz**

### Features

- Five symmetric, absorptive RF ports
- High isolation
  - 61 dB @ 900 MHz
  - 55 dB @ 2100 MHz
  - 52 dB @ 2700 MHz
  - 44 dB @ 4000 MHz
- High linearity
  - IIP2 of 96 dBm
  - IIP3 of 57 dBm
- 1.8V control logic compatible
- 105°C operating temperature
- Fast switching time of 265 ns
- Three pin CMOS logic control
- External negative supply option
- ESD performance
  - 4kV HBM on RF pins to GND
  - 1.5kV HBM on all pins

## Product Description

The PE42452 is a HaRP™ technology-enhanced absorptive SP5T RF switch designed for use in 3G/4G wireless infrastructure and other high performance RF applications.

This switch is a pin-compatible upgraded version of the PE42451 with 1.8V control logic. It is comprised of five symmetric RF ports and has very high isolation. An integrated CMOS decoder facilitates a three-pin low voltage CMOS control interface and an external negative supply option. In addition, no external blocking capacitors are required if 0V DC is present on the RF ports.

The PE42452 is manufactured on Peregrine's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate.

Peregrine's HaRP™ technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS® process, offering the performance of GaAs with the economy and integration of conventional CMOS.

**Figure 1. Functional Diagram**

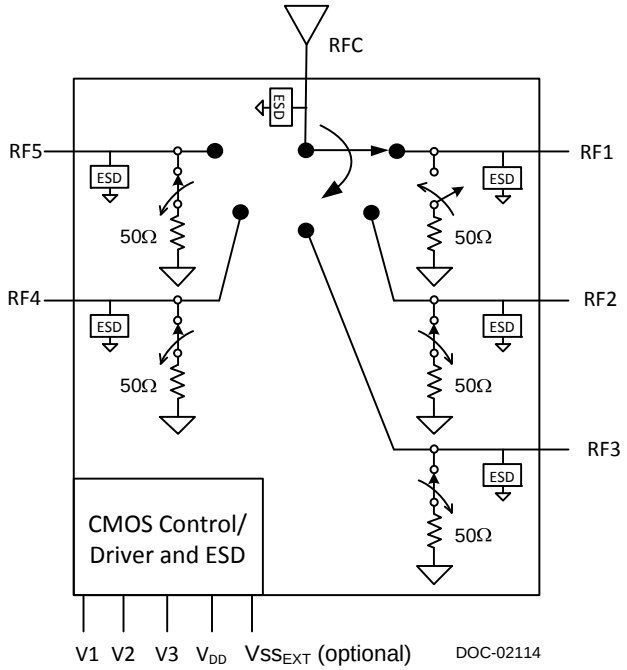



**Figure 2. Package Type**
24-lead 4x4 mm QFN




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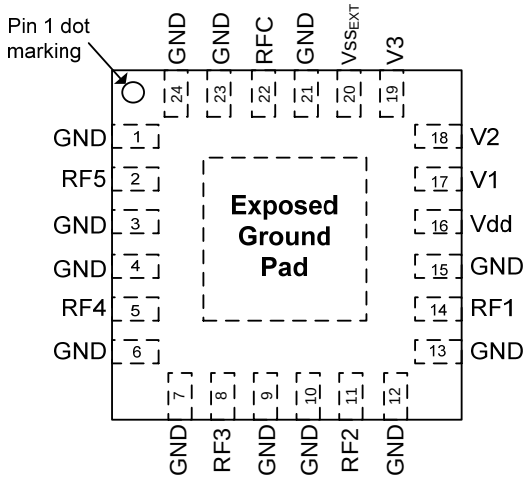
## Table 1. Electrical Specifications @ 25°C ($Z_S = Z_L = 50\Omega$) unless otherwise noted
## Normal mode[1]: $V_{DD}$ = 3.3V, $Vss_{EXT}$ = 0V or Bypass mode[2]: $V_{DD}$ = 3.3V, $Vss_{EXT}$ = -3.3V

| Parameter | Path | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating frequency | | | 450 | | 4000 | MHz |
| Insertion loss | RFC–RFX | 450 MHz–900 MHz<br>900 MHz–2100 MHz<br>2100 MHz–2700 MHz<br>2700 MHz–4000 MHz | | 0.95<br>1.15<br>1.30<br>1.60 | 1.15<br>1.35<br>1.55<br>1.90 | dB<br>dB<br>dB<br>dB |
| Isolation | RFC–RFX | 450 MHz–900 MHz<br>900 MHz–2100 MHz<br>2100 MHz–2700 MHz<br>2700 MHz–4000 MHz | 56<br>52<br>49<br>41 | 61<br>55<br>52<br>44 | | dB<br>dB<br>dB<br>dB |
| Isolation | RFX–RFX | 450 MHz–900 MHz<br>900 MHz–2100 MHz<br>2100 MHz–2700 MHz<br>2700 MHz–4000 MHz | 56<br>51<br>49<br>41 | 60<br>53<br>52<br>42 | | dB<br>dB<br>dB<br>dB |
| Return loss (active port) | RFX | 450–4000 MHz | | 16 | | dB |
| Return loss (terminated port) | RFX | 450–4000 MHz | | 23 | | dB |
| Input 0.1 dB compression point[3] | RFC–RFX | 1950 MHz | | 35 | | dBm |
| Input IP2 | RFC–RFX | 1950 MHz | | 96 | | dBm |
| Input IP3 | RFC–RFX | 1950 MHz | | 57 | | dBm |
| Switching time | | 50% control to 10% or 90% RF | | 265 | 345 | ns |

Notes: 1. Normal mode: single external positive supply used
2. Bypass mode: both external positive supply and external negative supply used
3. The input 0.1 dB compression point is a linearity figure of merit. Refer to *Table 3* for the operating RF input power (50Ω)

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## Figure 3. Pin Configuration (Top View)




## Table 2. Pin Descriptions

| Pin # | Name | Description |
|---|---|---|
| 1, 3, 4, 6, 7, 9, 10, 12, 13, 15, 21, 23, 24 | GND | Ground |
| 2 | RF5[1] | RF port 5 |
| 5 | RF4[1] | RF port 4 |
| 8 | RF3[1] | RF port 3 |
| 11 | RF2[1] | RF port 2 |
| 14 | RF1[1] | RF port 1 |
| 16 | $V_{DD}$ | Supply voltage |
| 17 | V1 | Digital control logic input 1 |
| 18 | V2 | Digital control logic input 2 |
| 19 | V3 | Digital control logic input 3 |
| 20 | $Vss_{EXT}$[2] | External Vss negative voltage control/ ground |
| 22 | RFC[1] | RF common |
| Pad | GND | Exposed pad: Ground for proper operation |

Notes: 1. RF pins 2, 5, 8, 11, 14, and 22 must be at 0V DC. The RF pins do not require DC blocking capacitors for proper operation if the 0V DC requirement is met
2. Use $Vss_{EXT}$ (pin 20, refer to *Table 3*) to bypass and disable internal negative voltage generator. Connect $Vss_{EXT}$ (pin 20, $Vss_{EXT}$ = GND) to enable internal negative voltage generator

## Table 3. Operating Ranges

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Normal mode[1] | | | | | |
| Supply voltage | $V_{DD}$ | 2.3 | | 5.5 | V |
| Supply current | $I_{DD}$ | | 110 | | µA |
| Bypass mode[2] | | | | | |
| Supply voltage | $V_{DD}$ | 2.7 | | 5.5 | V |
| Supply current | $I_{DD}$ | | 50 | | µA |
| Negative supply voltage | $Vss_{EXT}$ | -3.6 | | -3.2 | V |
| Normal or Bypass mode | | | | | |
| Digital input high (V1, V2, V3) | $V_{IH}$ | 1.17 | | 3.6 | V |
| Digital input low (V1, V2, V3) | $V_{IL}$ | -0.3 | | 0.6 | V |
| Digital input current[3] | $I_{CTRL}$ | | | 1 | µA |
| RF input power, CW | $P_{MAX,CW}$ | | | 33 | dBm |
| RF input power into terminated ports, CW | $P_{MAX,TERM}$ | | | 24 | dBm |
| Operating temperature range | $T_{OP}$ | -40 | | +105 | °C |

Notes: 1. Normal mode: connect pin 20 to GND to enable internal negative voltage generator
2. Bypass mode: apply a negative voltage to $Vss_{EXT}$ (pin 20) to bypass and disable internal negative voltage generator
3. The pull-down resistor in the EVK schematic may increase control current

## Table 4. Absolute Maximum Ratings

| Parameter/Condition | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | -0.3 | 5.5 | V |
| Voltage on any DC input | $V_I$ | -0.3 | 3.6 | V |
| Maximum input power | $P_{MAX,ABS}$ | | 34 | dBm |
| Storage temperature range | $T_{ST}$ | -60 | +150 | °C |
| ESD voltage HBM[1]<br>All pins<br>RF pins to ground | $V_{ESD,HBM}$ | | <br>1500<br>4000 | <br>V<br>V |
| ESD voltage MM[2], all pins | $V_{ESD,MM}$ | | 100 | V |
| ESD voltage CDM[3], all pins | $V_{ESD,CDM}$ | | 500 | V |

Notes: 1. Human Body Model (MIL_STD 883 Method 3015)
2. Machine Model (JEDEC JESD22-A115)
3. Charged Device Model ( JEDEC JESD22-C101D)

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.


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## Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS® device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified.

## Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS® devices are immune to latch-up.

## Switching Frequency

The PE42452 has a maximum 25 kHz switching rate in normal mode (pin 20 = GND). A faster switching rate is available in bypass mode (pin 20 = $Vss_{EXT}$). The rate at which the PE42452 can be switched is then limited to the switching time as specified in *Table 1*.

Switching frequency describes the time duration between switching events. Switching time is the time duration between the point the control signal reaches 50% of the final value and the point the output signal reaches within 10% or 90% of its target value.

## Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE42452 in the 24-lead 4x4 QFN package is MSL1.

**Table 5. Truth Table**

| Mode | V3 | V2 | V1 |
|---|---|---|---|
| **All off** | 0 | 0 | 0 |
| **RF1 on** | 0 | 0 | 1 |
| **RF2 on** | 0 | 1 | 0 |
| **RF3 on** | 0 | 1 | 1 |
| **RF4 on** | 1 | 0 | 0 |
| **RF5 on** | 1 | 0 | 1 |
| **All off** | 1 | 1 | 0 |
| **Unsupported** | 1 | 1 | 1 |

Note: Logic State 111 is unsupported and should not be used under any operating conditions

## Optional External Vss Control (VssEXT)

For applications the require a faster switching rate or spur-free performance, this part can be operated in bypass mode. Bypass mode requires an external negative voltage in addition to an external $V_{DD}$ supply voltage.

As specified in *Table 3*, the external negative voltage ($Vss_{EXT}$) when applied to pin 20 will disable and bypass the internal negative voltage generator.

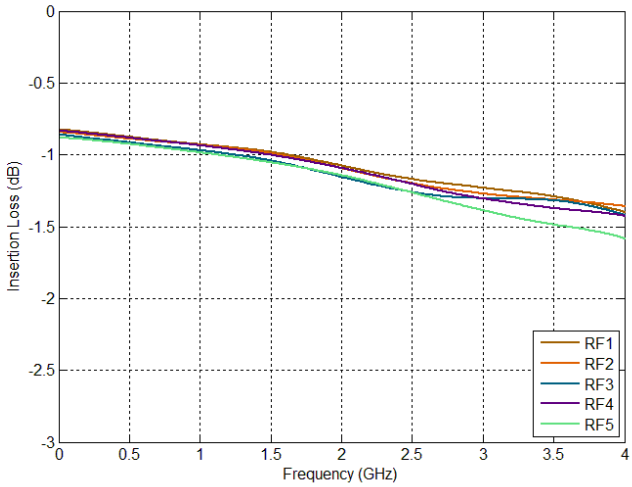
## Spurious Performance

The typical low-frequency spurious performance of the PE42452 in normal mode is –120 dBm (pin 20 = GND). If spur-free performance is desired, the internal negative voltage generator can be disabled by applying a negative voltage to $Vss_{EXT}$ (pin 20).

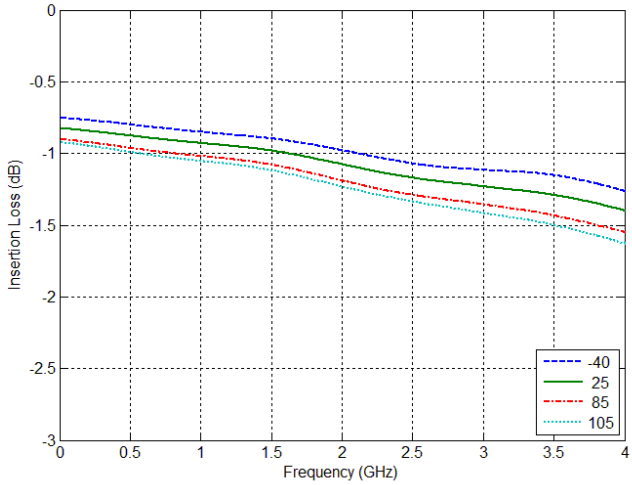
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## Typical Performance Data @ 25°C and $V_{DD}$ = 3.3V unless otherwise noted

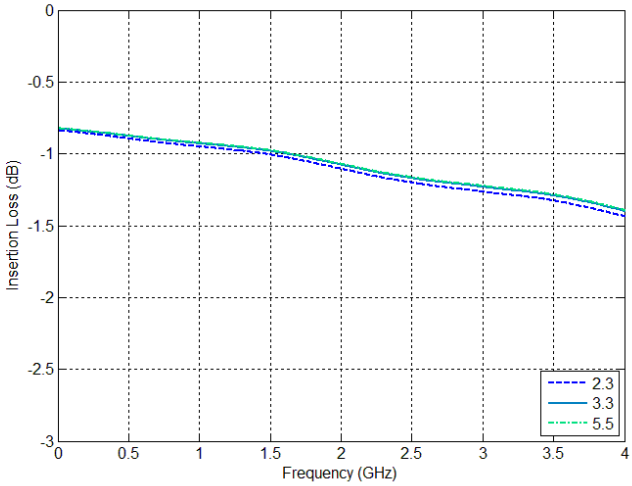
### Figure 4. Insertion Loss (All Paths)




### Figure 5. Insertion Loss vs Temp (RFC–RFX)




### Figure 6. Insertion Loss vs $V_{DD}$ (RFC–RFX)

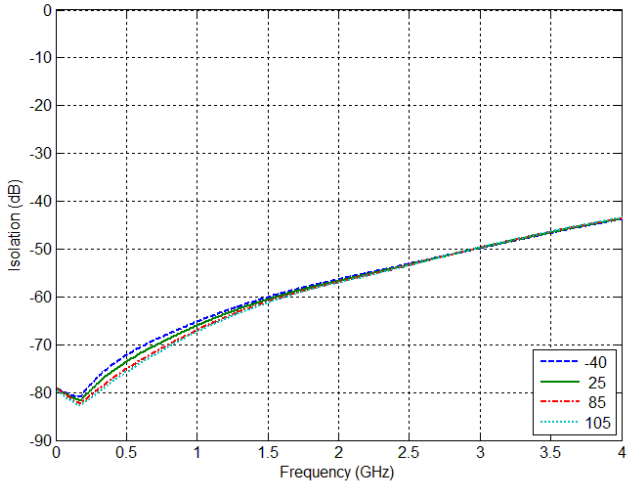




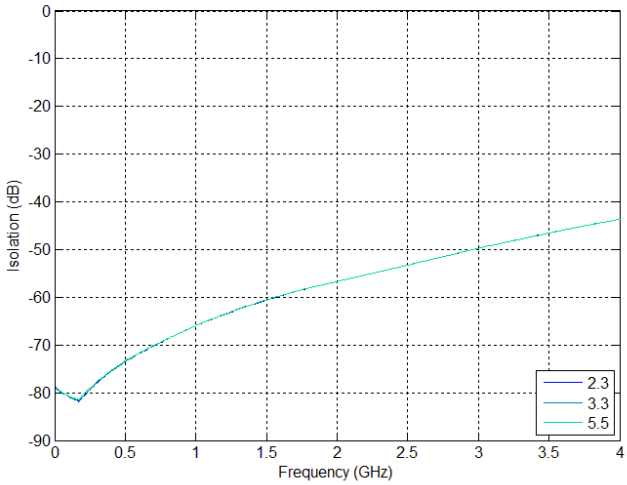
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## Typical Performance Data @ 25°C and $V_{DD}$ = 3.3V unless otherwise noted

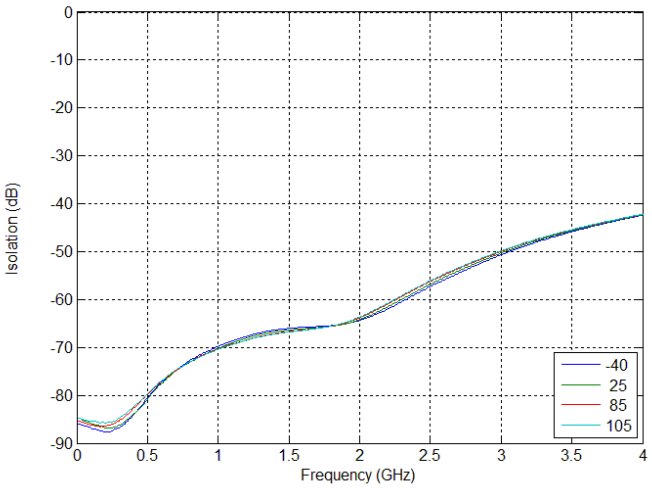
### Figure 7. Isolation vs Temp (RFC–RFX)



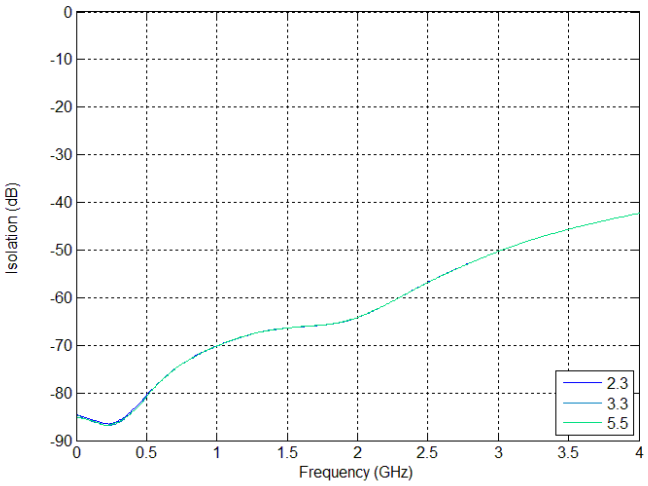

### Figure 8. Isolation vs $V_{DD}$ (RFC–RFX)




### Figure 9. Isolation vs Temp (RFX–RFX)



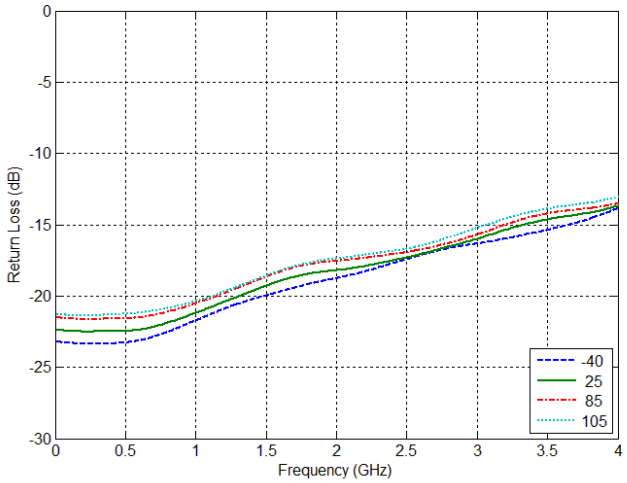

### Figure 10. Isolation vs $V_{DD}$ (RFX–RFX)



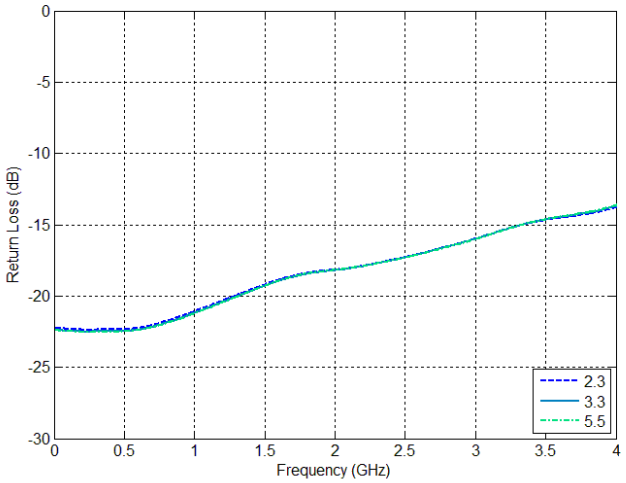

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## Typical Performance Data @ 25°C and $V_{DD}$ = 3.3V unless otherwise noted

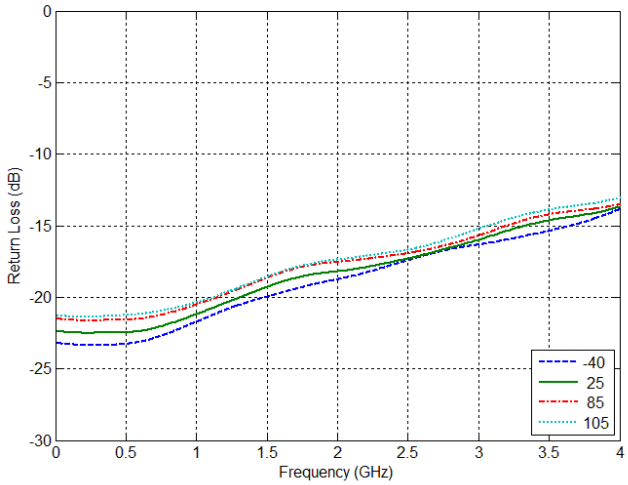
### Figure 11. Active Port Return Loss vs Temp



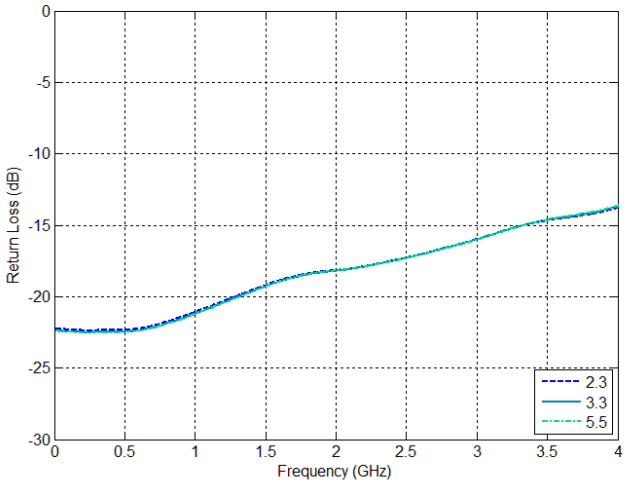

### Figure 12. Active Port Return Loss vs $V_{DD}$



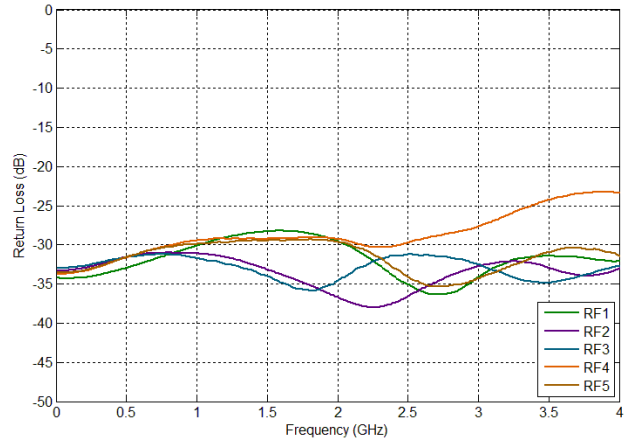

### Figure 13. RFC Port Return Loss vs Temp



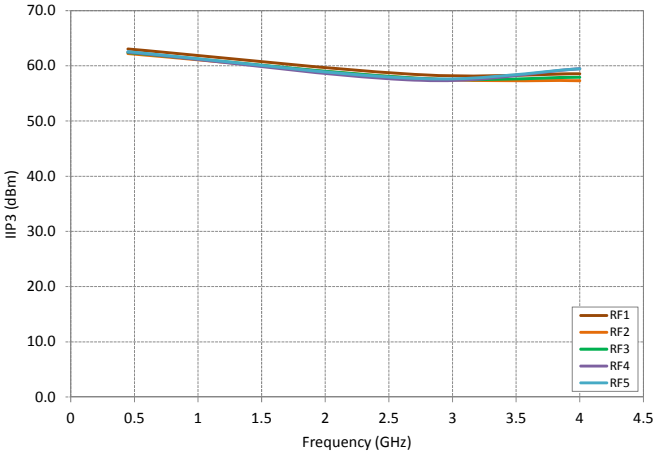

### Figure 14. RFC Port Return Loss vs $V_{DD}$




### Figure 15. Return Loss (All Ports Terminated)




### Figure 16. IIP3 vs Frequency





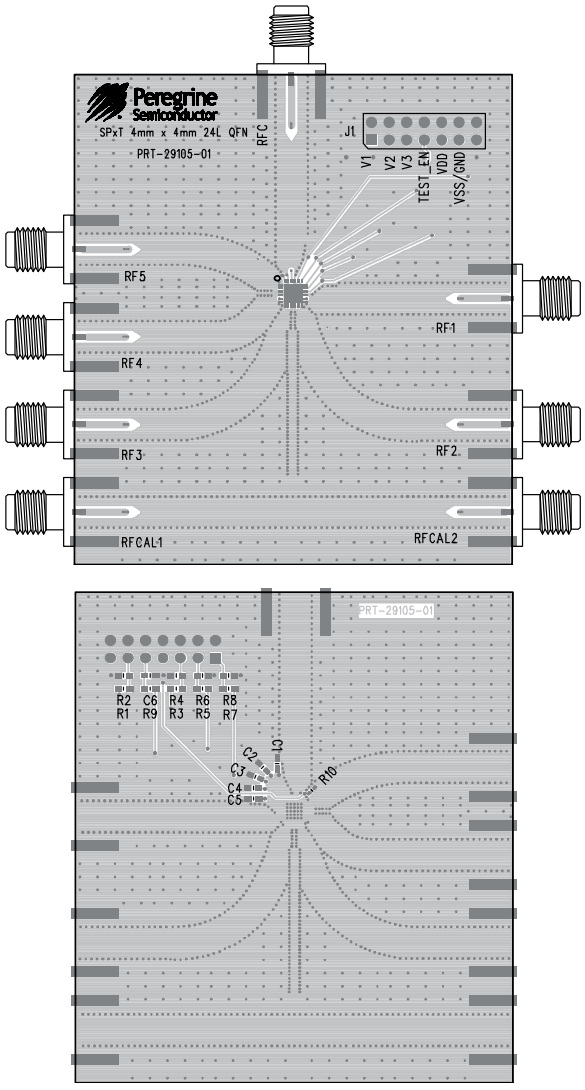
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## Evaluation Kit

The SP5T switch Evaluation Board was designed to ease customer evaluation of Peregrine's PE42452. The RF common port is connected through a 50Ω transmission line via the top SMA connector. RF1, RF2, RF3, RF4 and RF5 are connected through 50Ω transmission lines via side SMA connectors. A through 50Ω transmission is available via SMA connectors RFCAL1 and RFCAL2. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The EVK board is constructed with four metal layers on dielectric materials of Rogers 4003C and 4450 with a total thickness of 32 mils. Layer 1 and layer 3 provide ground for the 50Ω transmission lines. The 50Ω transmission lines are designed in layer 2 for high isolation purpose and use a stripline waveguide design with a trace width of 9.4 mils and trace metal thickness of 1.8 mils. The board stack up for 50 ohm transmission lines has 8 mil thickness of Rogers 4003C between layer 1 and layer 2, and 10 mil thickness of Rogers 4450 between layer 2 and layer 3. Please consult manufacturer's guidelines for proper board material properties in your application. The PCB should be designed in such a way that RF transmission lines and sensitive DC I/O traces such as $Vss_{EXT}$ are heavily isolated from one another, otherwise the true performance of the PE42452 will not be yielded.

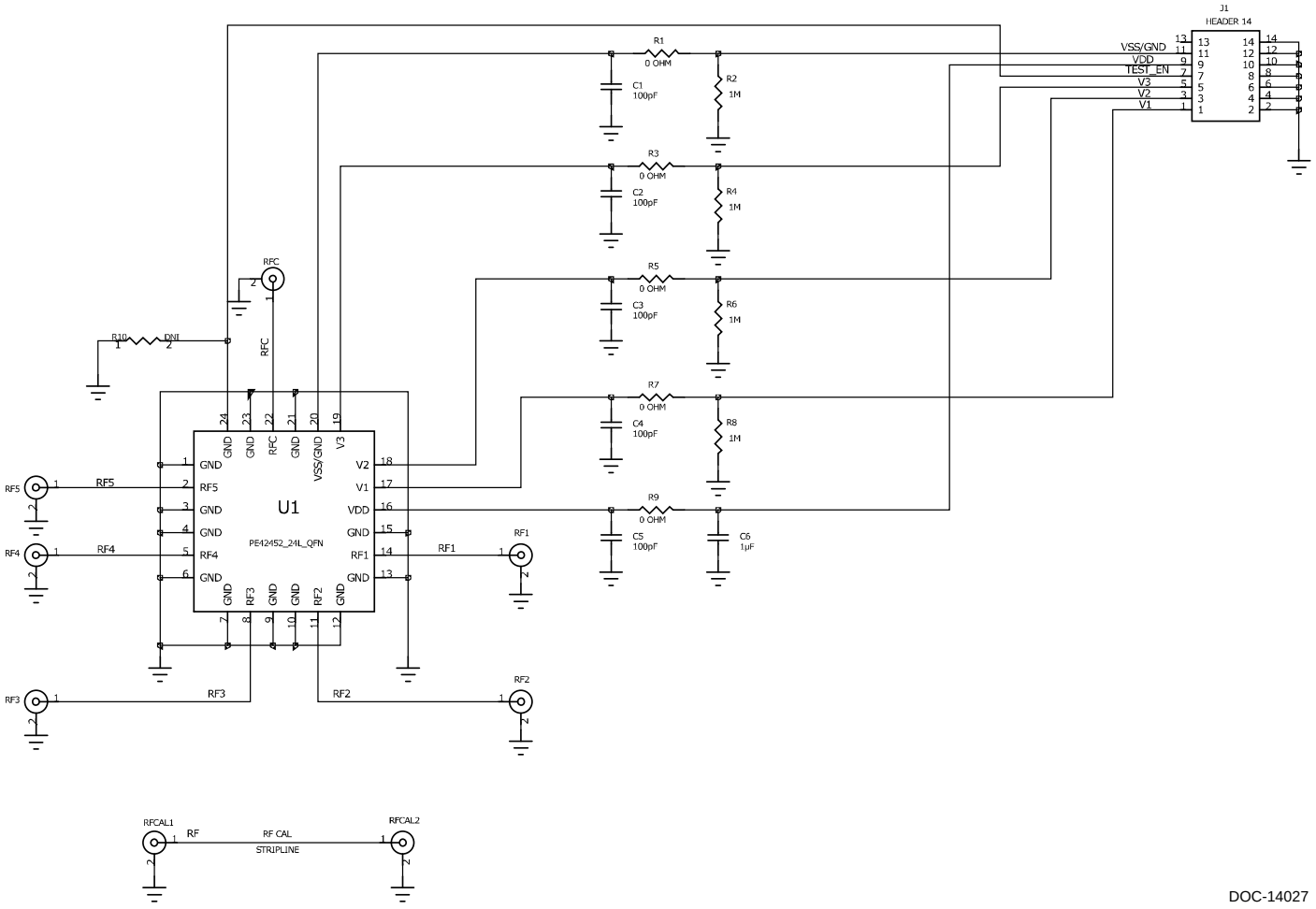
## Figure 17. Evaluation Board Layout




PRT-29105

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## Figure 18. Evaluation Board Schematic




DOC-14027


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**Figure 19. Package Drawing**
24-lead 4x4 mm QFN

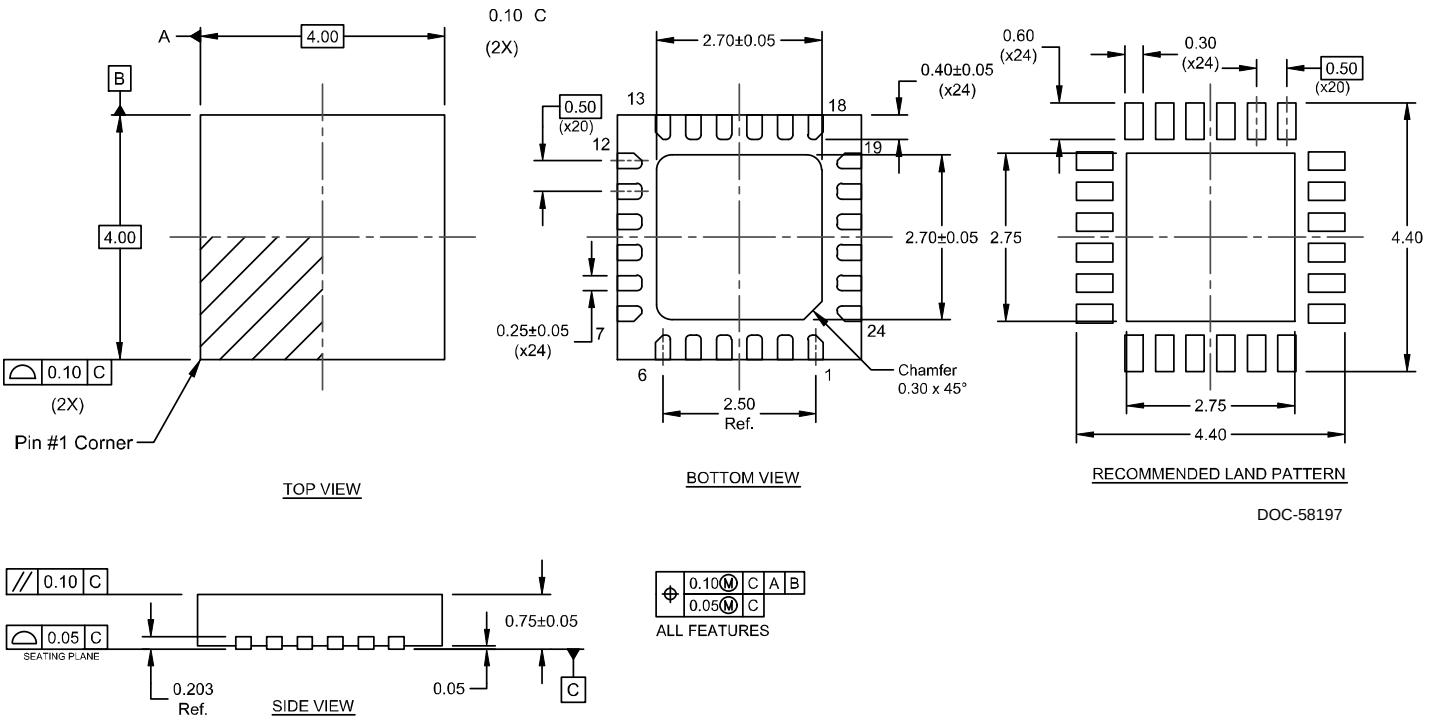
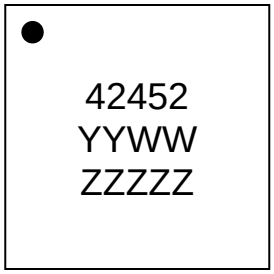



**Figure 20. Marking Specifications**

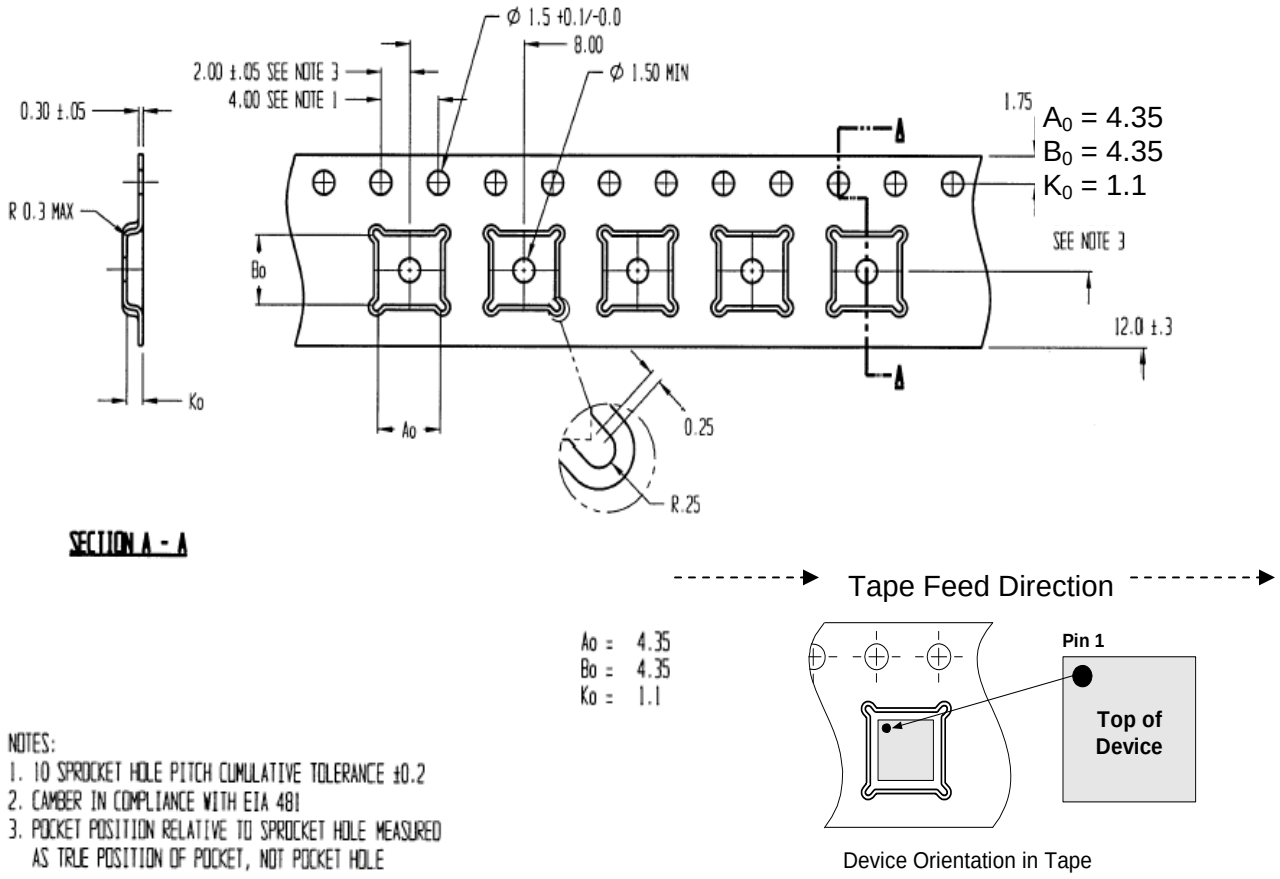



DOC-51207

● = Pin 1 designator
YYWW = Date code
ZZZZZ = Las five digits of the lot number

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## Figure 21. Tape and Reel Drawing




## Table 6. Ordering Information

| Ordering Code | Description | Package | Shipping Method |
|---|---|---|---|
| PE42452A-Z | PE42452 SP5T RF switch | Green 24-lead 4x4 mm QFN | 3000 units/T&R |
| EK42452-01 | PE42452 Evaluation kit | Evaluation kit | 1/Box |

## Sales Contact and Information

For sales and contact information please visit www.psemi.com.

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