Product Specification

PE4237

SPDT UltraCMOS™ RF Switch
DC - 4000 MHz

Product Description

The PE4237 RF Switch is designed to cover a broad range of applications from near DC to 4000 MHz. This reflective switch integrates on-board CMOS control logic driven by a single-pin, low voltage CMOS or TTL control input. Using a nominal +3-volt power supply, a 1 dB compression point of +32 dBm can be achieved. The PE4237 also exhibits outstanding isolation of better than 43 dB at 1000 MHz and is offered in a small 3x3 mm DFN package.

The PE4237 is manufactured on Peregrine's UltraCMOS™ process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Features

- Single 3.0-volt power supply
- Low insertion loss: 0.35 dB at 1000 MHz, 0.45 dB at 2000 MHz
- High isolation of 43 dB at 1000 MHz, 35 dB at 2000 MHz
- Typical 1 dB compression point of +32 dBm
- Single-pin CMOS or TTL logic control
- Available in a 6-lead DFN package

Figure 1. Functional Diagram

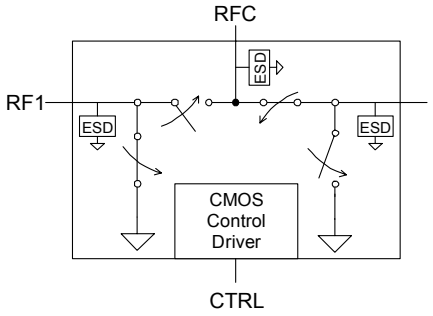


Figure 2. Package Type

6-lead DFN



Table 1. Electrical Specifications @ +25 °C, V_{DD} = 3 V (ZS = ZL = 50 Ω)

Parameter	Conditions	Minimum	Typical	Maximum	Units
Operation Frequency[1]		DC		4000	MHz
Insertion Loss	1000 MHz 2000 MHz		0.35 0.45	0.50 0.60	dB dB
Isolation – RFC to RF1/RF2	1000 MHz 2000 MHz	41 33	43 35		dB dB
Isolation – RF1 to RF2	1000 MHz 2000 MHz	33.5 26.5	35 28		dB dB
Return Loss	1000 MHz 2000 MHz	19 10.5	24 14		dB dB
'ON' Switching Time	50% CTRL to 0.1 dB final value, 2 GHz		200		ns
'OFF' Switching Time	50% CTRL to 25 dB isolation, 2 GHz		90		ns
Video Feedthrough[2]			15		mV_{pp}
Input 1 dB Compression	2000 MHz	30	32		dBm
Input IP3	2000 MHz, 17 dBm	50			dBm

Notes: 1. Device linearity will begin to degrade below 10 MHz.

2. The DC transient at the output of any port of the switch when the control voltage is switched from Low to High or High to Low in a 50 Ω test set-up, measured with 1ns risetime pulses and 500 MHz bandwidth.

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Figure 3. Pin Configuration

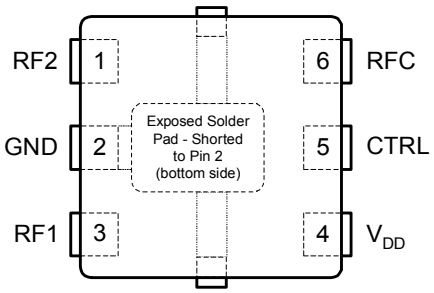


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	RF2	RF2 port.[1]
2	GND	Ground Connection. Traces should be physically short and connected to the ground plane. This pin is connected to the exposed solder pad that also must be soldered to the ground plane for best performance.
3	RF1	RF1 port.[1]
4	V_{DD}	Nominal 3 V supply connection.
5	CTRL	CMOS or TTL logic level: High = RFC to RF1 signal path Low = RFC to RF2 signal path
6	RFC	Common RF port for switch.[1]

Notes: 1. All RF pins must be DC blocked with an external series capacitor or held at 0 V_{DC}.

Table 3. Operating Ranges

Parameter	Min	Typ	Max	Units
V_{DD} Power Supply Voltage	2.7	3.0	3.3	V
I_{DD} Power Supply Current (V_{DD} = 3V, V_{CNTL} = 3V)		29	35	µA
T_{OP} Operating temperature range	-40		85	°C
Control Voltage High	0.7xV_{DD}			V
Control Voltage Low			0.3xV_{DD}	V

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE4237 in the 6-lead 3x3 DFN package is MSL1.

Table 4. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Power supply voltage	-0.3	4.0	V
V_I	Voltage on any input except for the CTRL input	-0.3	V_{DD}+ 0.3	V
V_{CTRL}	Voltage on CTRL input		5.0	V
T_{ST}	Storage temperature range	-65	150	°C
P_{IN}	Input power (50 Ω)		35	dBm
V_{ESD}	ESD voltage (Human Body Model)		250	V

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Control Logic Input

The control logic input pin (CTRL) is typically driven by a 3-volt CMOS logic level signal. For flexibility to support systems that have 5-volt control logic drivers, the control logic input has been designed to handle a standard 5-volt TTL control signal. This TTL control signal input must not exceed 5-volts or damage to the switch could result.

Table 5. Control Logic Truth Table

Control Voltage	Signal Path
CTRL = CMOS or TTL High	RFC to RF1
CTRL = CMOS or TTL Low	RFC to RF2

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 4.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

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Typical Performance Data @ -40 °C to 85 °C (Unless Otherwise Noted)

Figure 4. Insertion Loss - RFC to RF1

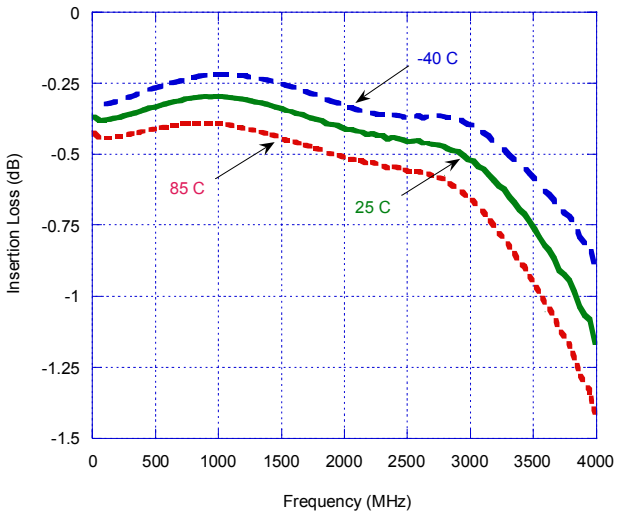


Figure 5. Input 1dB Compression Point

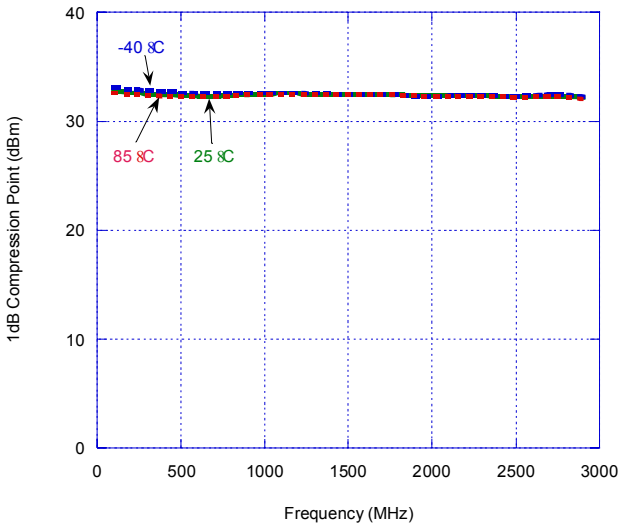


Figure 6. Insertion Loss - RFC to RF2

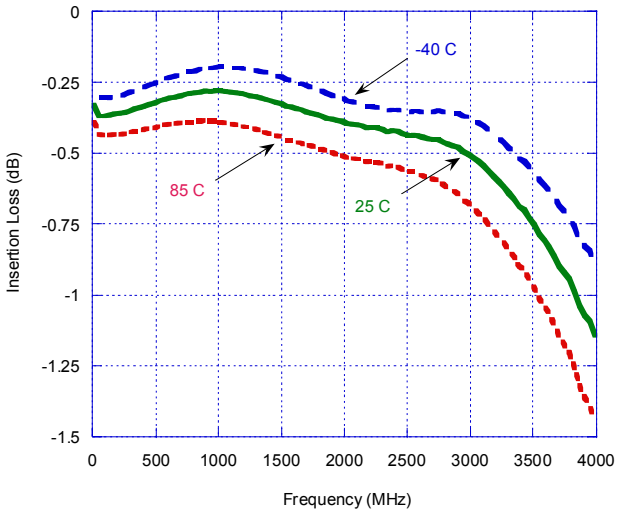
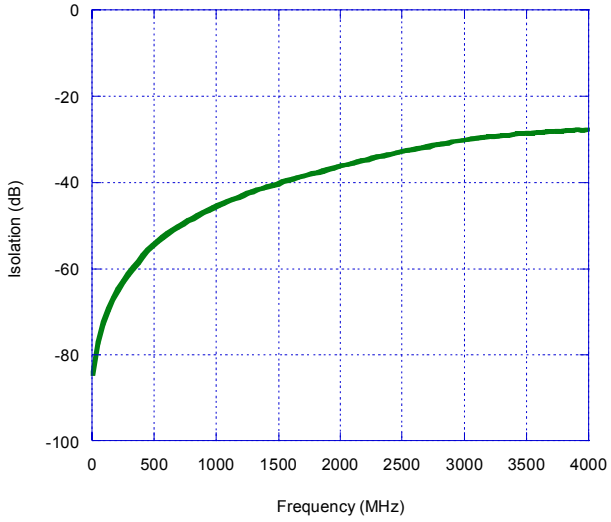


Figure 7. Isolation - RFC to RF1
T = 25 °C



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Typical Performance Data @ 25 °C

Figure 8. Isolation – RFC to RF2

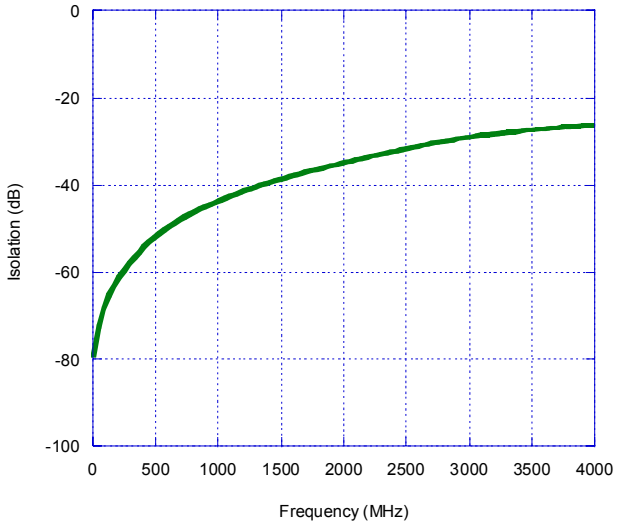


Figure 9. Isolation – RF1 to RF2, RF2 to RF1

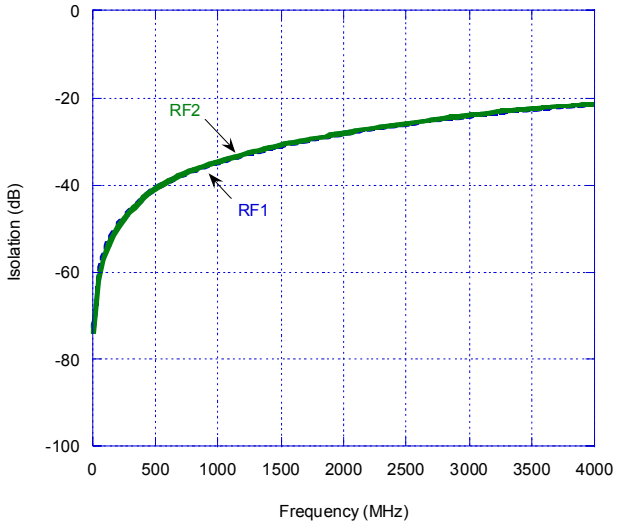


Figure 10. Return Loss – RFC to RF1, RF2

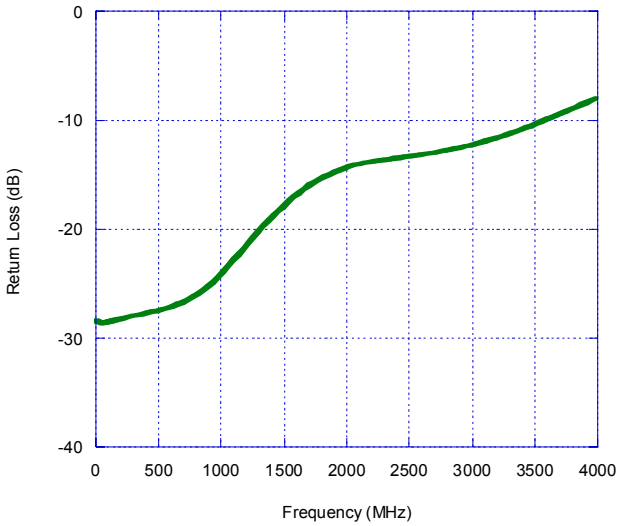
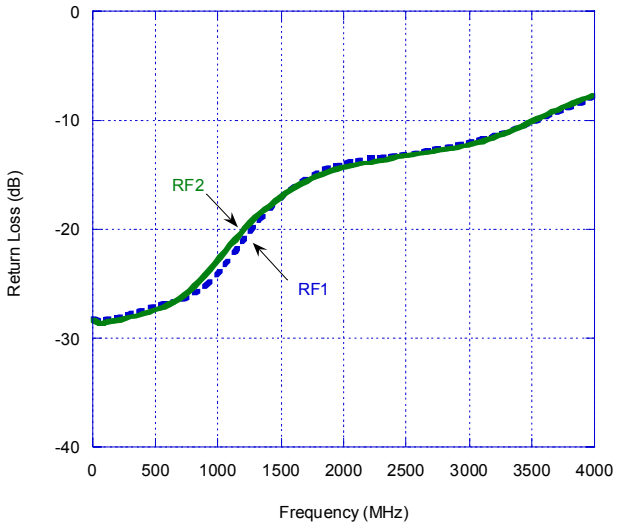


Figure 11. Return Loss – RF1, RF2



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Evaluation Kit

The SPDT Switch Evaluation Kit board was designed to ease customer evaluation of the PE4237 SPDT switch. The RF common port is connected through a 50 Ω transmission line to the top left SMA connector, J1. Port 1 and Port 2 are connected through 50 Ω transmission lines to the top two SMA connectors on the right side of the board, J2 and J3. A through transmission line connects SMA connectors J4 and J5. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a two metal layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 0.0476", trace gaps of 0.030", dielectric thickness of 0.028", metal thickness of 0.0021" and ε_r of 4.4.

J6 provides a means for controlling DC and digital inputs to the device. Starting from the lower left pin, the second pin to the right (J6-3) is connected to the device CNTL input. The fourth pin to the right (J6-7) is connected to the device V_{DD} input. A decoupling capacitor (100 pF) is provided on both CTRL and V_{DD} traces. It is the responsibility of the customer to determine proper supply decoupling for their design application. Removing these components from the evaluation board has not been shown to degrade RF performance.

Figure 12. Evaluation Board Layouts
Peregrine Specification 101/0085

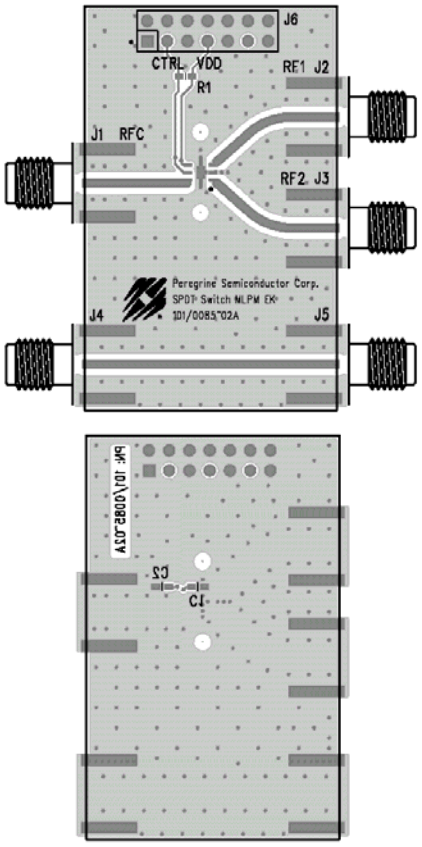
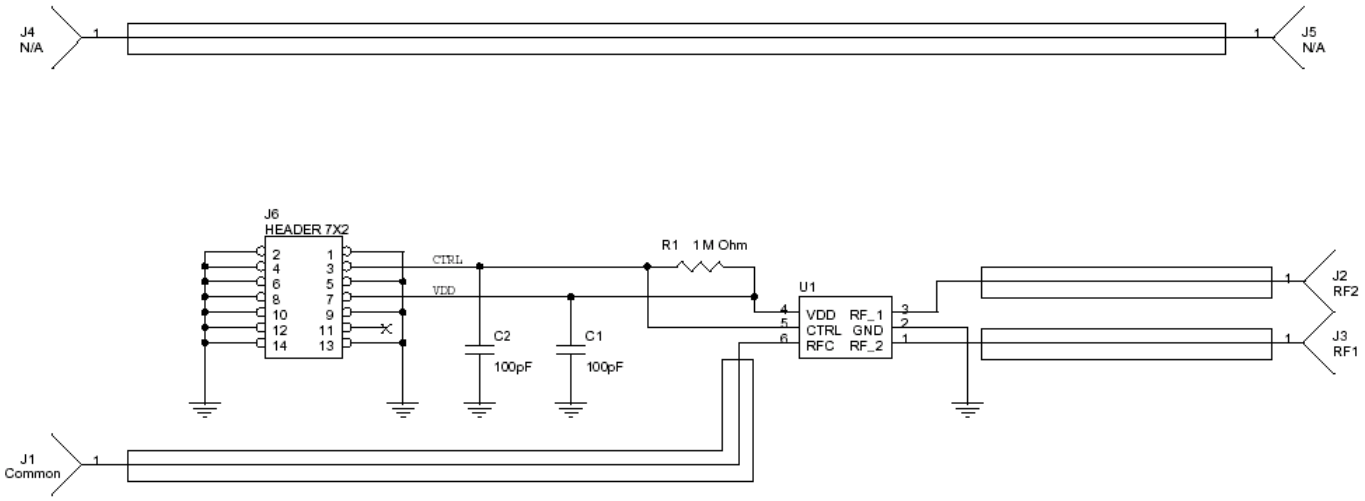


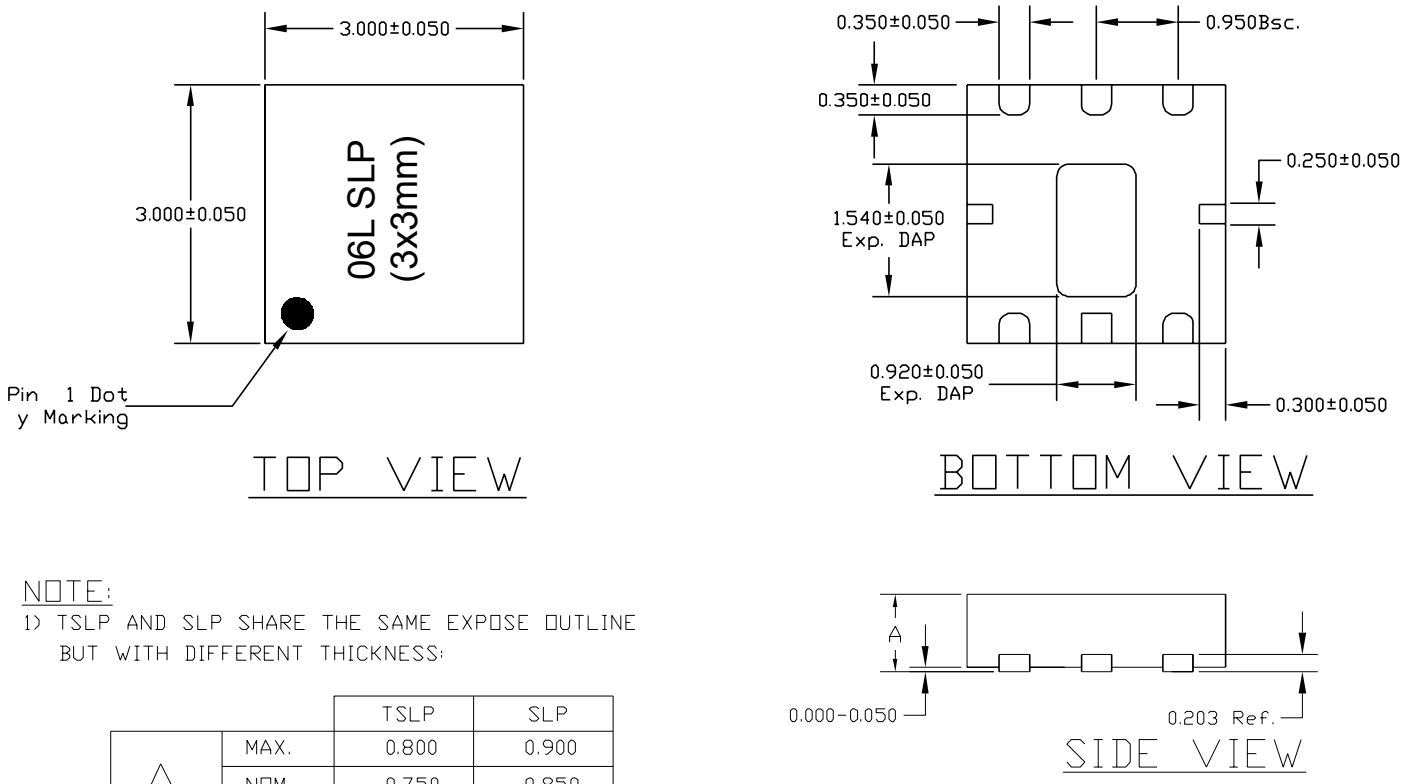
Figure 13. Evaluation Board Schematic
Peregrine Specification 102/0110



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Figure 14. Package Drawing

6-lead DFN



		TSLP	SLP
A	MAX.	0.800	0.900
	NOM.	0.750	0.850
	MIN.	0.700	0.800

NOTE: The exposed solder pad (on the bottom of the package) is electrically connected to pin 2 (fused.)

Figure 15. Marking Specifications

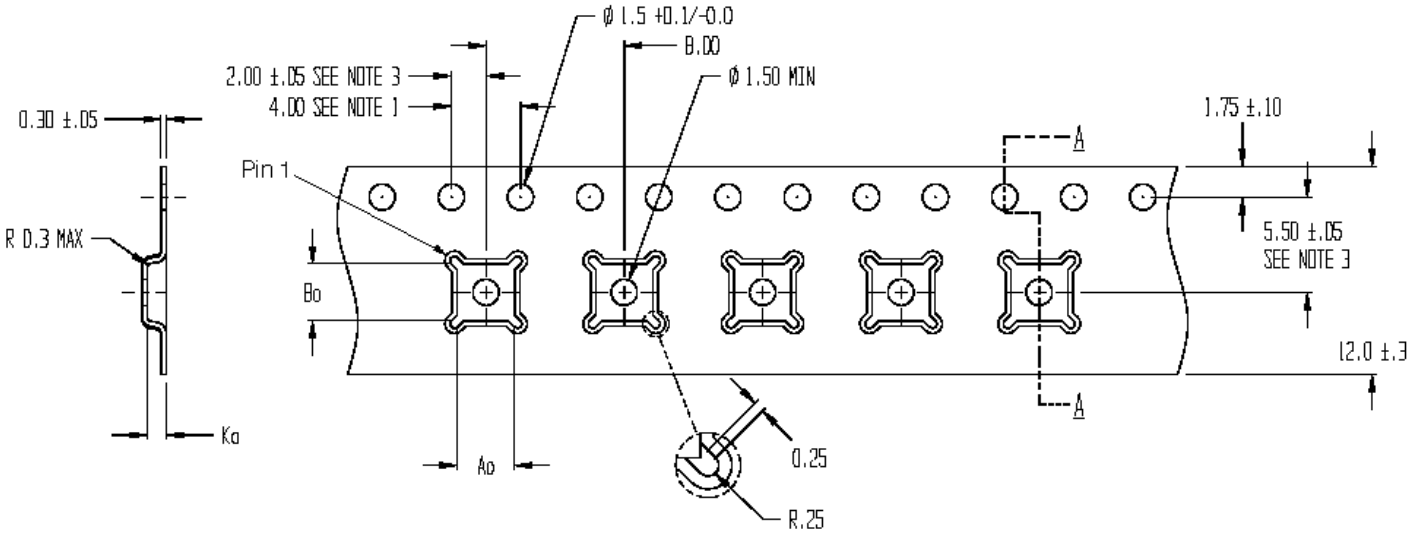


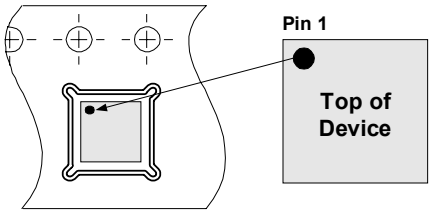
YYWW = Date Code (last two digits of year and work week)
ZZZZZ = Last five digits of Lot Number

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Figure 16. Tape and Reel Specifications

6-lead DFN





Device Orientation in Tape

NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. CAMBER IN COMPLIANCE WITH EIA 481
3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

Table 6. Dimensions

Dimension	DFN 3x3 mm
Ao	3.23 ± 0.1
Bo	3.17 ± 0.1
Ko	1.37 ± 0.1
P	4 ± 0.1
W	8 +0.3, -0.1
T	0.254 ± 0.02
R7 Quantity	3000
R13 Quantity	N.A.

Note: R7 = 7 inch Lock Reel, R13 = 13 inch Lock Reel

Table 7. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
4237-51	4237	PE4237G-06DFN 3x3mm-12800F	Green 6-lead 3x3 mm DFN	Tape or loose
4237-52	4237	PE4237G-06DFN 3x3mm-3000C	Green 6-lead 3x3 mm DFN	3000 units / T&R
4237-00	PE4237-EK	PE4237-06DFN 3x3mm-EK	Evaluation Kit	1 / Box

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