APD-128G064D

Vishay Dale

Plasma Panel Display Modules

128 x 64 Graphics Display with Video Interface, DC Converter and Drive Circuitry



The APD-128G064D is a dot matrix graphic display with an array of 128 x 64 pixels available. The module is composed of a highly reliable DC plasma display, Video Interface, DC converter and drive circuitry which are assembled to form a rugged, slim profile display sub-system.

Interface to the APD-128G064D is through a video interface. Patented open construction display technology assures a stable, flicker free screen.

STANDARD ELECTRICAL SPECIFICATIONS

DESCRIPTION	SYMBOL	MIN.	TYP.	MAX.	UNITS
Panel Supply Voltage	VDC	8.0	12.0	28.0	V
Panel Supply Current	IDC	0.15	0.4	1.5	A

ENVIRONMENTAL SPECIFICATIONS

Operating Temperature: 20°C to + 70°C.

Storage Temperature: - 40°C to + 85°C.

Operating Humidity: 95% RH non-condensing.

Mechanical Shock: 30 G.

Vibration: 0.018" [0.457mm] displacement amplitude from 10-50Hz, 2 G acceleration from 50 to 2000Hz logarithmic sweep rate.

Mean Time Between Failure: 60,000 hours.

FEATURES

- 128 x 64 pixel array for bright and vivid graphics.
- Video interface.
- Powerful software commands make display integration simple and efficient.
- + 8 to + 24 VDC display voltage.

OPTICAL SPECIFICATIONS

Pixel Pitch: 0.040.

Pixel Size: 0.020" [0.610] square.

Pixel Array: 128 x 64.

Luminance: 50 foot lamberts typical.

Color: Neon orange.

Refresh Cycle: 120 Hz typical.

Viewing Angle: 150° cone.

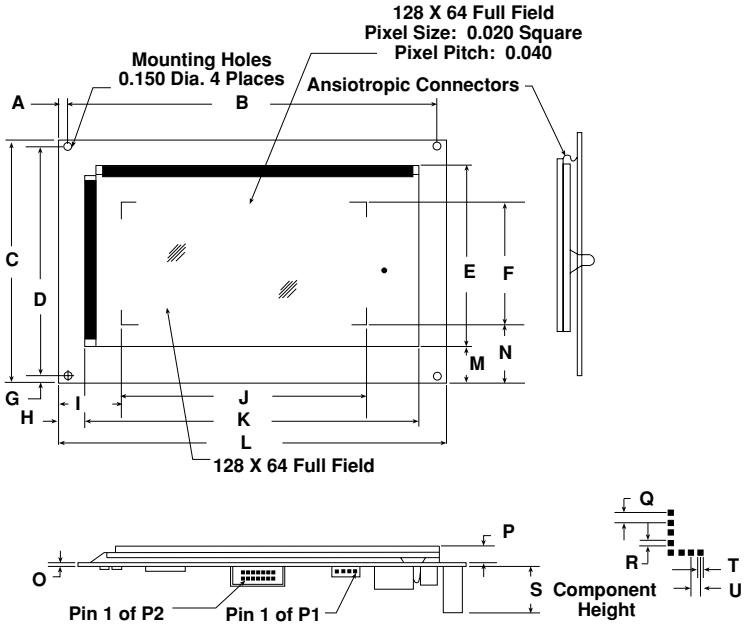
Contrast Ratio: 30:1

ELECTROSTATIC CAUTION

Vishay Dale display panels use electrostatic sensitive components. These assemblies should be unpacked and handled in an ESD controlled area only. When shipping use packing materials designed for protection of electrostatic sensitive components.

Vishay Dale believes that the information described in this publication is accurate and reliable, and much care has been taken in its preparation. However, no responsibility, financial or otherwise, is accepted for any consequences arising out of the use of this information.

DIMENSIONS in inches [millimeters]



A	0.150 [3.81]
B	7.70 [195.58]
C	5.00 [127.00]
D	4.70 [119.38]
E	3.55 [90.17]
F	2.548 [64.72]
G	0.150 [3.81]
H	0.650 [16.51]
I	1.45 [36.83]
J	5.10 [129.54]
K	6.80 [172.72]
L	8.00 [203.20]
M	0.925 [23.50]
N	1.226 [31.14]
O	0.062 [1.57]
P	0.395 [10.03]
Q	0.040 [1.02]
R	0.020 [0.508]
S	0.970 [24.64]
T	0.020 [0.508]
U	0.040 [1.02]

DESCRIPTION OF INPUT SIGNALS

DOT CLOCK: This signal enters the SERIAL DATA on each low to high transition. A total of 128 DOT CLOCK transitions must be present for each line of column/anode data.

SERIAL DATA: This signal presents the pixel data in positive logic format. A logic one represents a lit pixel and a logic zero represents an extinguished pixel. Data is entered from right to left. The first pixel data entered will represent the leftmost pixel in the row.

COLUMN LATCH: This signal latches the pixel data into the driver outputs. When the COLUMN LATCH signal goes to logic one the data entered previously will fall through to the driver outputs. When the signal returns to a logic zero, the data is latched and the shift register is now ready to accept the next row of data. Must be held low while entering new SERIAL DATA.

DISPLAY ENABLE: This signal enables the output drivers. Using a duty cycle control, this signal may also be used for intensity control. The DISPLAY ENABLE must be at logic zero before the COLUMN LATCH signal transitions. To avoid display blurring, the ROW CLOCK signal should also transition while DISPLAY ENABLE is a logic zero. It is recommended that this signal remain low for 10µS minutes.

ROW DATA: This signal is the first line marker for the scan. This input should be held high to correspond to the first row of pixel data.

ROW CLOCK: This signal clocks ROW DATA on the falling edge. The ROW CLOCK signal is repetitive and must be present for proper scanning of the display module.

The APD-128G064D has a unique input protection circuit that assures the column drivers stay blanked on power up. The protection circuit unblanks the column drivers when the ROW CLOCK signal begins (i.e. the display begins scanning).

POWER SUPPLY: (Recommended)		
VDC	+ 12 V ± 0.6 V	1.5 A Max.*, 0.4 A Typ.

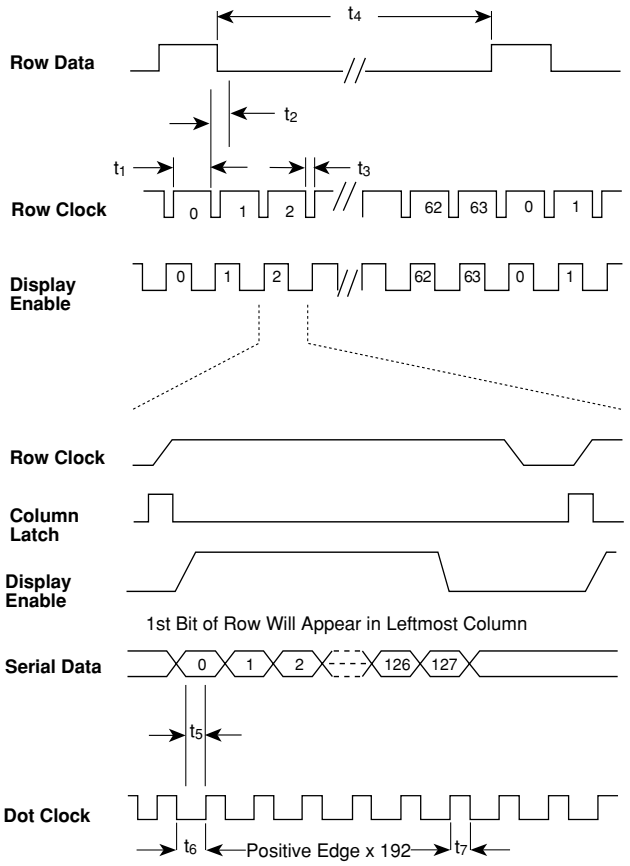
***NOTE:** The maximum VDC draw denotes a power up condition when the DC converter starts. Typical duration is 15-30 mS.

POWER SUPPLY CONNECTION		
CONNECTOR	**PIN**	**SIGNAL**
J1	1	+ 12 VDC
	2	GROUND
	3	GROUND
	4	N/C

SIGNAL DESCRIPTION		
PIN	**FUNCTION**	**DESCRIPTION**
1	DEm	Display enable signal
3	Rdata	Row driver data input
5	Rclk	Row clock
7	latch	Column latch
9	Dot CLK	Dot clock
11	Sdata	Serial column data
*	GND	Common Ground

This information is subject to change without notice.

LOGIC AND DATA TIMING



PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS
t_1	130	112	—	nS
t_2	75	1000	—	uS
t_3	16.6	14.3	—	uS
t_4	5	20	200	Hz
t_5	25	—	—	nS
t_6	75	—	—	nS
t_7	75	—	—	nS

ORDERING INFORMATION

DESCRIPTION	PART NUMBER
Display Unit	APD-128G064D
Non-Glare Filter (Amber CP)	280109-19
Video Controller (+ 5V)	PDS-500
Video Controller (+ 12V)	PDS-500-1

APPLICABLE MATING CONNECTORS	MANUFACTURER	PART NUMBER
TO POWER INPUT (P1)	MOLEX	09-50-3081
	MOLEX	09-06-5087
Vishay Dale Power Connector Kit 280108-05	AMP	640428-8
	METHODE	3300-108
TO LOGIC INPUT (P2)	MOLEX	39-27-1146
	ROBINSON NUGENT	IDS-C14PK-TC
Vishay Dale Data Connector Kit 280108-05	AMP	746195-2, 746582-2
	3M	3314-5002, 3314-5202

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