To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

MOS INTEGRATED CIRCUIT

μPD16707A

263/256-OUTPUT TFT-LCD GATE DRIVER

DESCRIPTION

The μPD16707A is a TFT-LCD gate driver equipped with 263/256-output lines. It can output a high-gate scanning voltage in response to CMOS level input because it provided with a level-shift circuit inside the IC circuit. It can also drive the XGA /SXGA/ SXGA+, and since the input signal is placed symmetrically, this product can wire easily between gate drivers.

FEATURES

- CMOS level input (2.3 to 3.6 V)
- 263/256 outputs
- High-output voltage (V_{DD2} to V_{EE}: 40 V MAX.)
- Capable of All-ON outputting (/AOR, /AOL)
- Input terminal symmetrical placement
- ★ • Adapted to TCP/COF

★ **Remark** /xxx indicates active low signal.

★ ORDERING INFORMATION

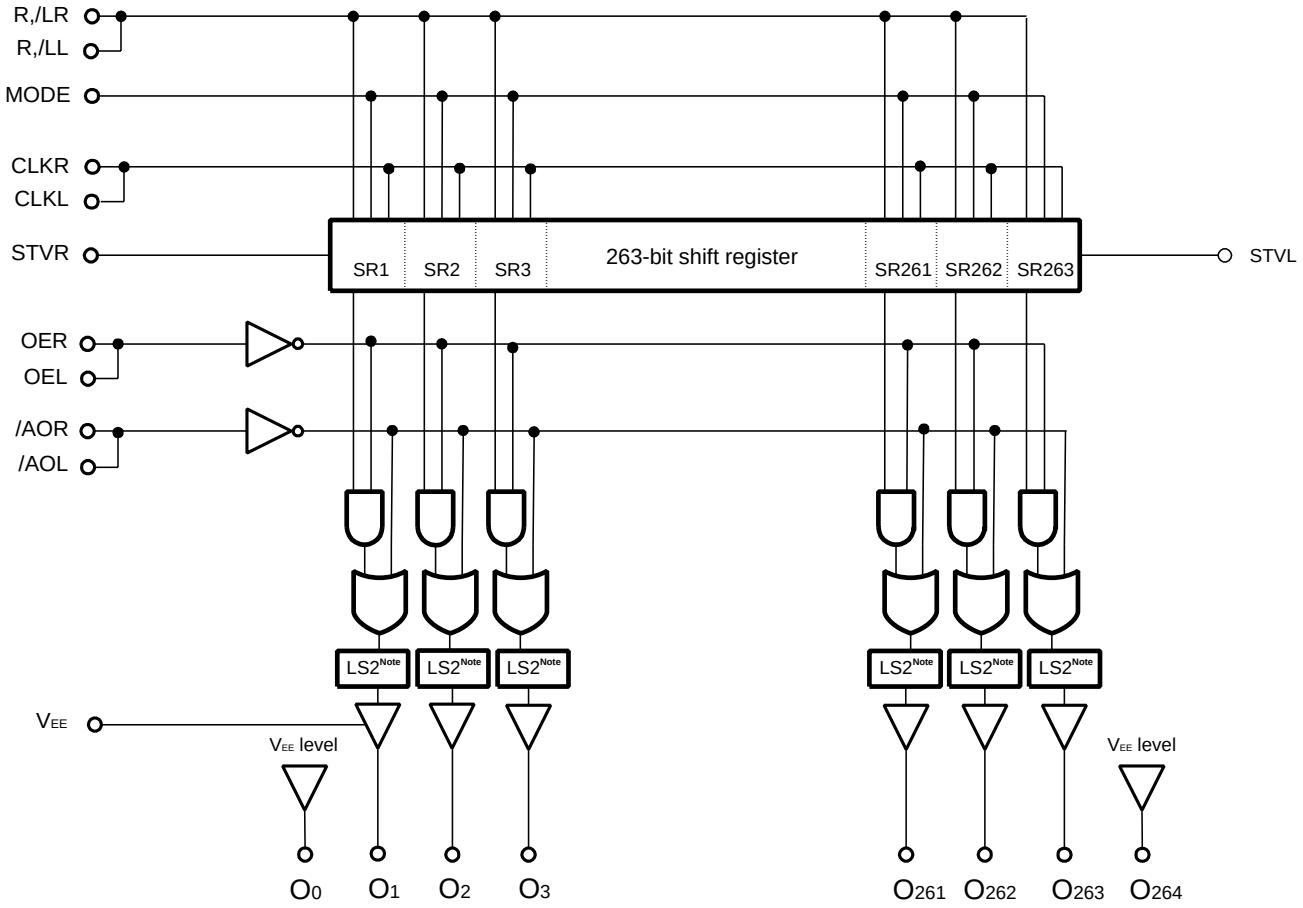
Part Number	Package
μPD16707AN-xxx	TCP (TAB package)
μPD16707ANL-xxx	COF

Remark Purchasing the above chip entail the exchange of documents such as a separate memorandum or product quality, and the TCP's external shape is customized. To order the required shape, so please contact one of our sales representatives.

Document No. S16563EJ1V0DS00 (1st edition)
Date Published January 2004 NS CP (K)
Printed in Japan

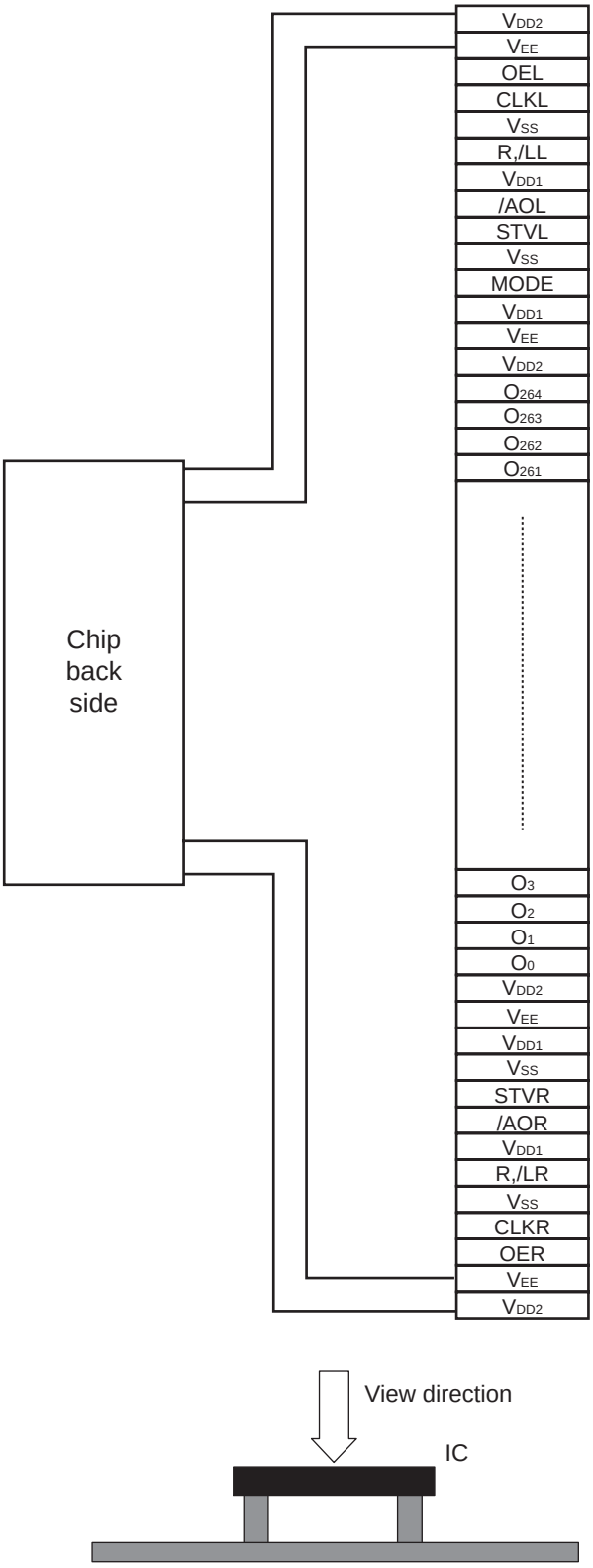
The mark ★ shows major revised points.

1. BLOCK DIAGRAM



Note LS2: Shifts CMOS level and output level (V_{DD2} to V_{EE}).

2. PIN CONFIGURATION (μPD16707AN-xxx: TCP) (Copper Foil Surface, Face-up)



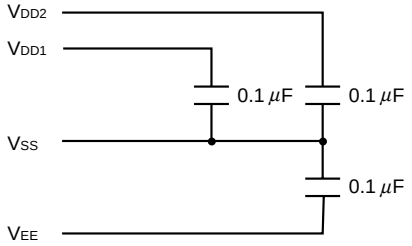
Remark This figure does not specify the TCP package.

3. PIN FUNCTIONS

Pin Symbol	Pin Name	I/O	Description
O_1 to O_{263}	Driver	Output	These pins output scan signals that drive the vertical direction (gate lines) of a TFT-LCD. The output signals change in synchronization with the rising edge of shift clock CLK. The driver output amplitude is V_{DD2}-V_{EE}.
O_0, O_{264}	Driver	Output	The signal of V_{EE} level is outputted by fixation.
R,/LR, R,/LL	Shift direction control	Input	The shift direction control pin of shift register. R,/LR, R,/LL = H (right shift): STVR → O_1 → O_{263} → STVL R,/LR, R,/LL = L (left shift): STVL → O_{263} → O_1 → STVR R,/LR and R,/LL are connected inside IC.
★ STVR, STVL	Start pulse	I/O	This is the I/O of the internal shift register. The start pulse is read at the rising edge of shift clock CLK (CLKR, CLKL), and scan signals are output from the driver output pins. The input level is a V_{DD1}-V_{SS} (logic level). When in MODE = H, the start pulse is output at the falling edge of the 263rd clock of shift clock CLK, and is cleared at the falling edge of the 264th clock. The output level is V_{DD1}-V_{SS} (logic level).
CLKR, CLKL	Shift clock	Input	This pin inputs a shift clock to the internal shift register. The shift operation is performed in synchronization with the rising edge of this input. CLKR and CLKL are connected inside IC.
OER, OEL	Output enable	Input	When this pin goes high level, the driver output is fixed to V_{EE} level. The shift register is not cleared. CLK is asynchronous in the clock. OER and OEL are connected inside IC.
/AOR, /AOL	All-on control	Input	When this pin goes low level, all driver output = V_{DD2} level. The shift register is not cleared. This pin has priority over OER and OEL. This pin is pulled up to V_{DD1} power supply inside IC. CLK is asynchronous in the clock. /AOR and /AOL are connected inside IC.
MODE	Selection of number of outputs	Input	MODE = V_{DD1} or open: 263 outputs MODE = V_{SS}: 256 outputs (Driver pins O_{129} to O_{135} are invalid.) Input level is V_{DD1}-V_{SS} (logic level) This pin is pulled up to V_{DD1} power supply inside IC.
V_{DD1}	Logic power supply	–	2.3 to 3.6 V
V_{DD2}	Driver positive power supply	–	5 to 30 V. The driver output: High level
V_{SS}	Logic ground	–	Connect this pin to the ground of the system.
V_{EE}	Negative Power supply for internal operation	–	−15 to −3 V. The driver output: Low level

Cautions 1. To prevent latch-up, turn on power to V_{DD1}→V_{EE}→V_{DD2}→logic input in this order. Turn off power in the reverse order. These power up/down sequence must be observed also during transition period.

2. Insert a capacitor of about 0.1 μF between each power line, as shown below, to secure noise margin such as V_{IH} and V_{IL}.

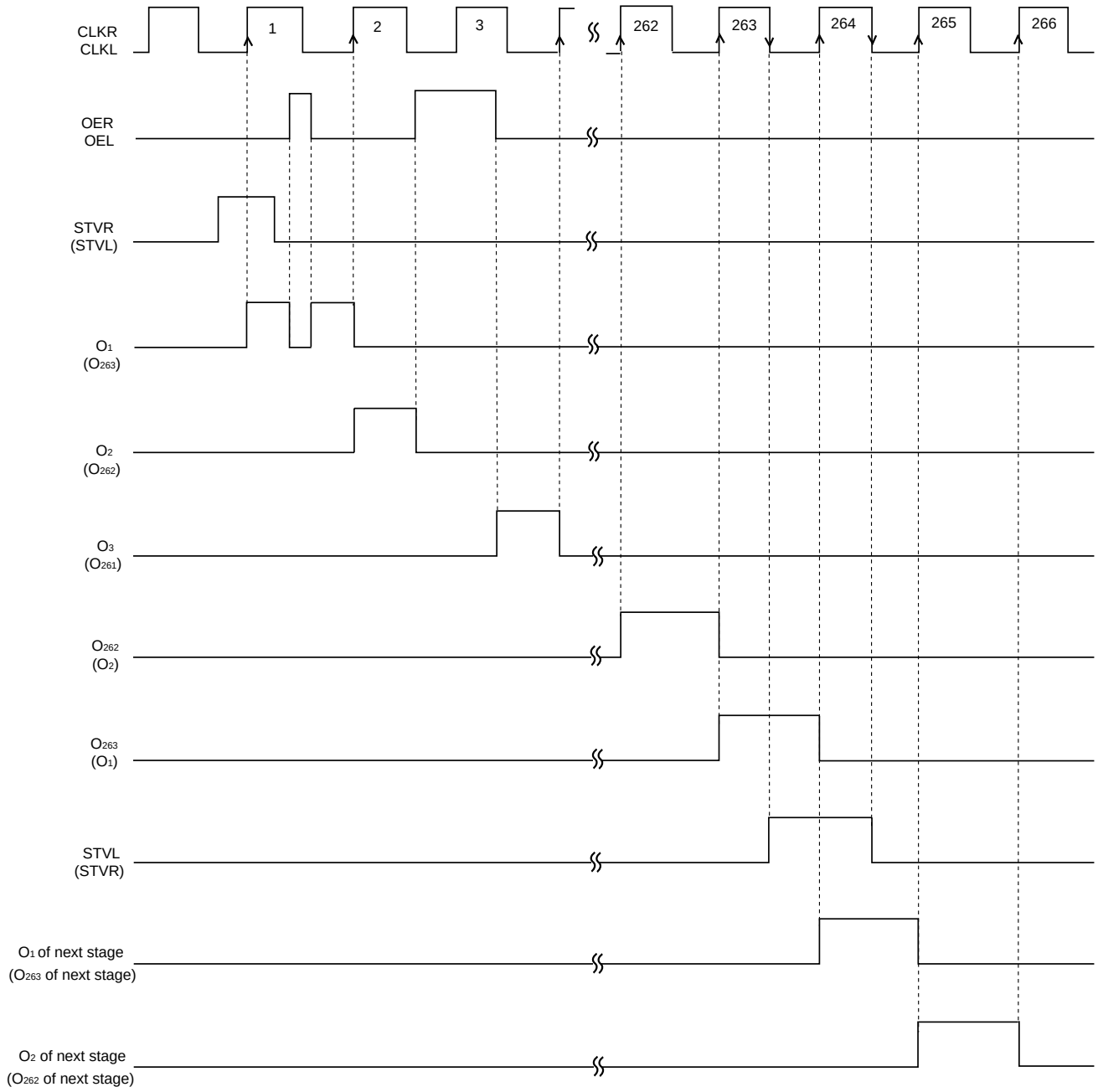


4. RELATIONS OF ENABLE OUTPUT PIN NUMBER SELECTION AND OUTPUT PIN

Switching is possible for 263/256 with μPD16707A by the MODE pin.

MODE = H or open	MODE = L
263-output Mode	256-output Mode
O_1	O_1
O_2	O_2
O_3	O_3
O_4	O_4
O_5	O_5
O_6	O_6
↓	↓
O_{127}	O_{127}
O_{128}	O_{128}
O_{129}	$V_{OUT} = V_{EE}$
O_{130}	$V_{OUT} = V_{EE}$
O_{131}	$V_{OUT} = V_{EE}$
O_{132}	$V_{OUT} = V_{EE}$
O_{133}	$V_{OUT} = V_{EE}$
O_{134}	$V_{OUT} = V_{EE}$
O_{135}	$V_{OUT} = V_{EE}$
O_{136}	O_{136}
O_{137}	O_{137}
↓	↓
O_{259}	O_{259}
O_{260}	O_{260}
O_{261}	O_{261}
O_{262}	O_{262}
O_{263}	O_{263}

5. TIMING CHART (R,/LR = R,/LL = H, MODE = H, /AOR = /AOL = H)



Remark The signal name in parenthesis is it at the time of R,/LR = R,/LL = L.

6. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Rating	Unit
Logic Supply Voltage	V_{DD1}	−0.5 to +7.0	V
Driver Positive Supply Voltage	V_{DD2}	−0.5 to +32	V
Power Supply Voltage	V_{DD2}-V_{EE}	−0.5 to +42	V
Internal Operation Negative Supply Voltage	V_{EE}	−16 to + 0.5	V
Input Voltage	V_I	−0.5 to V_{DD1} + 0.5	V
Operating Ambient Temperature	T_A	−20 to +75	°C
Storage Temperature	T_{stg}	−55 to +125	°C

Caution Product qualify may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range (T_A = –20 to +75°C, V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Logic Supply Voltage	V_{DD1}		2.3	3.3	3.6	V
Driver Positive Supply Voltage	V_{DD2}		5	20	30	V
Internal Operation Negative Supply Voltage	V_{EE}		−15	−5	−3	V
Power Supply Voltage	V_{DD2}-V_{EE}		8	25	40	V
Clock Frequency	f_{CLK}				500	kHz

Electrical Characteristics (T_A = –20 to +75°C, V_{DD1} = 2.3 to 3.6 V, V_{DD2} = 20 V, V_{EE} = –5 V, V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
High level Input Voltage	V_{IH}	CLKR, CLKL, STVR, STVL, R,/LR, R,/LL, OER, OEL, MODE	0.8 V_{DD1}		V_{DD1}	V
Low level Input Voltage	V_{IL}		V_{SS}		0.2 V_{DD1}	V
High level Output Voltage	V_{OH}	STVR (STVL), I_{OH} = –40 μA	V_{DD1} – 0.4		V_{DD1}	V
Low level Output Voltage	V_{OL}	STVR (STVL), I_{OL} = +40 μA	V_{SS}		V_{SS} + 0.4	V
LCD Driver Output ON Resistance	R_{ON}	V_{OUT} = V_{EE} + 1.0 V or V_{DD2} – 1.0 V		0.4	1.0	kΩ
Pull-up Resistance	R_{PU}	V_{DD1} = 3.0 V (/AOR, /AOL, MODE)	10	50	100	kΩ
Input Leak Current	I_{IL}	V_I = 0 V or 3.6 V (except for /AOR, /AOL, MODE)			±1.0	μA
Static Current Dissipation	I_{DD1}	V_{DD1}, f_{CLK} = 50 kHz, OER = OEL = L, f_{STV} = 60 Hz, no load		20	200	μA
	I_{DD2}	V_{DD2}, f_{CLK} = 50 kHz, OER = OEL = L, f_{STV} = 60 Hz, no load		10	100	μA
	I_{EE}	V_{EE}, f_{CLK} = 50 kHz, OER = OEL = L, f_{STV} = 60 Hz, no load	–300	–30		μA

Remark STV: STVR (STVL)

★ **Note** The TYP. value are reference values at V_{DD1} = 3.0 V, T_A = 25°C.

Switching Characteristics (T_A = –20 to +75°C, V_{DD1} = 2.3 to 3.6 V, V_{DD2} = 20 V, V_{EE} = –5 V, V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
★ Cascade Output Delay Time	t_{PHL1}	C_L = 20 pF,			500	ns
	t_{PLH1}	CLKR (CLKL) → STVL (STVR)			500	ns
Driver Output Delay Time	t_{PHL2}	C_L = 300 pF, CLKR (CLKL) → O_n			500	ns
	t_{PLH2}				500	ns
	t_{PHL3}	C_L = 300 pF, OER (OEL) → O_n			500	ns
	t_{PLH3}				500	ns
Output Rise Time	t_{TLH}	C_L = 300 pF			800	ns
Output Fall Time	t_{THL}				800	ns
Input Capacitance	C_I	T_A = 25°C			15	pF

Timing Requirements (T_A = –20 to +75°C, V_{DD1} = 2.3 to 3.6 V, V_{DD2} = 20 V, V_{EE} = –5 V, V_{SS} = 0 V)

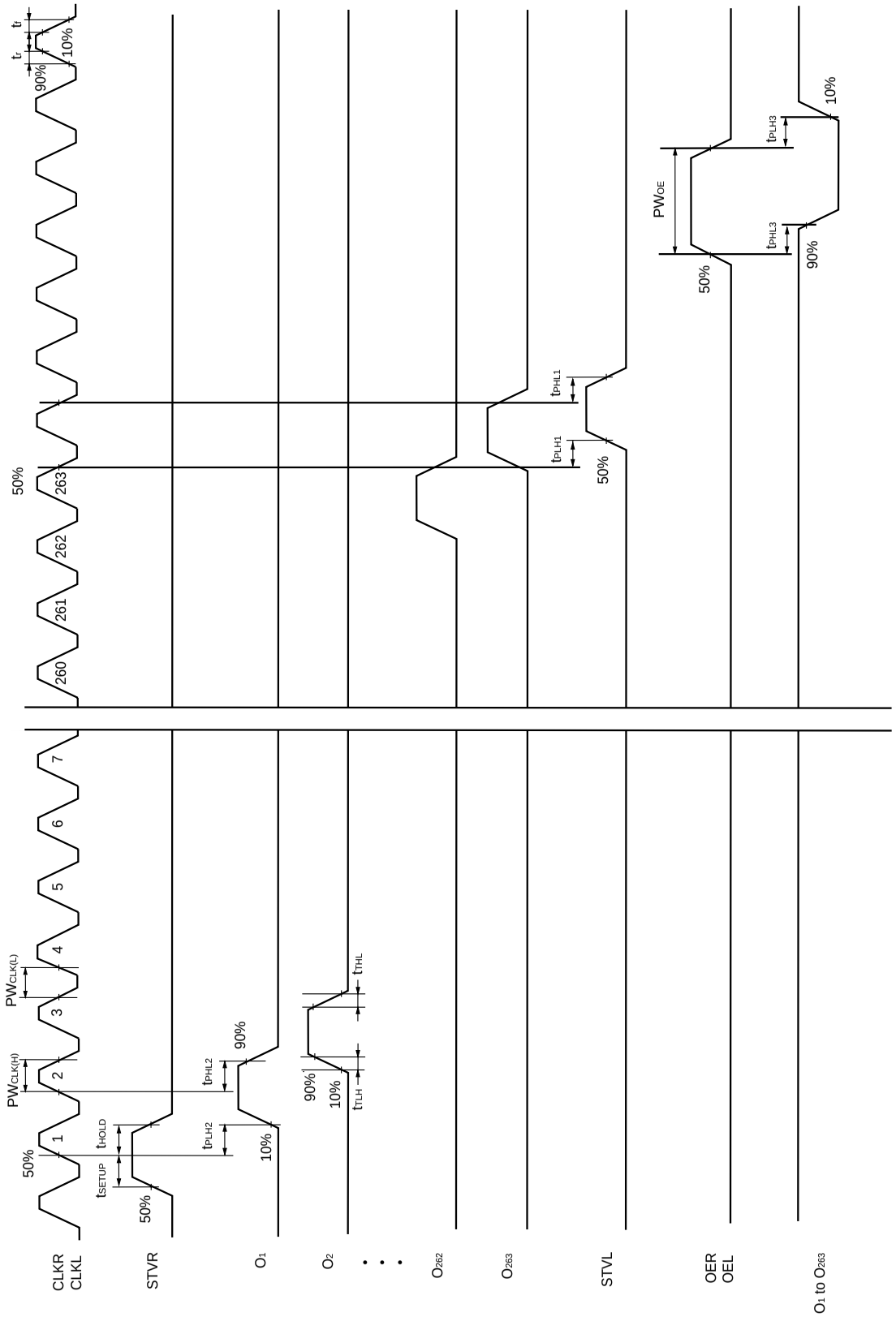
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse High Width	$PW_{CLK(H)}$		500			ns
Clock Pulse Low Width	$PW_{CLK(L)}$		500			ns
Enable Pulse Width	PW_{OE}		1000			ns
Data Setup Time	t_{SETUP}	STVR (STVL) ↑→ CLKR, CLKL↑	200			ns
Data Hold Time	t_{HOLD}	CLKR, CLKL ↑→ STVR (STVL) ↓	200			ns

Remark Unless otherwise specified, the input level is defined to be V_{IH} = 0.8 V_{DD1}, V_{IL} = 0.2 V_{DD1}.

Caution Keep the time and fall time of the logic input to $t_r = t_f$ = 20 ns (10 to 90% of the rated values).

Switching Characteristics Waveform (R,/LR = R,/LL = H, MODE = H)

Unless otherwise specified, the input level is defined to be V_{IH} = 0.8 V_{DD1}, V_{IL} = 0.2 V_{DD1}.



7. RECOMMENDED MOUNTING CONDITIONS

The following conditions must be met of mounting conditions of the μPD16707A.

For more details, refer to the

★ **[Semiconductor Device Mounting Manual] (http://www.necel.com/pkg/en/mount/index.html)**

Please consult with our sales offices in case other mounting process is used, or in case the mounting is done under different conditions.

μPD16707AN-xxx: TCP (TAB Package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C, heating for 2 to 3 seconds : pressure 100g (per solder)
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100°C: pressure 3 to 8 kg/cm^2: time 3 to 5 sec. Real bonding 165 to 180°C: pressure 25 to 45 kg/cm^2: time 30 to 40 sec. (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite,Ltd).

Caution To find out the detailed conditions for mounting the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more mounting methods at a time.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades On NEC Semiconductor Devices (C11531E)

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