PCT2202

Ultra low power, 1.8 V, 1 deg. C accuracy, digital temperature sensor with I²C-bus interface

Rev. 1.1 — 14 August 2015 Product data sheet

1. General description

The PCT2202 is an I²C-bus, serial output temperature sensor available in a tiny WLCSP6 package. Requiring no external components, the PCT2202 is capable of reading temperatures at 12-bit resolution or 0.0625 °C with an accuracy of ±0.5 °C from 0 °C to 85 °C.

The PCT2202 features SMBus and I²C-bus interface compatibility including HSM (High-Speed Mode: 3.4 MHz), and allows up to four devices on one bus. It also features an SMB alert function.

The PCT2202 is ideal for extended temperature measurement in a variety of communication, computer, consumer, environmental, industrial, and instrumentation applications. The device is specified for operation over a temperature range of −40 °C to +125 °C and a voltage range of 1.65 V to 1.95 V.

2. Features and benefits

- Tiny WLCSP6 package
- Accuracy: 0.5 °C from 0 °C to +85 °C
- Low quiescent current:
  - 30 μA Active
  - 1 μA Shut-down
- Supply range: 1.8 V ± 0.15 V
- Resolution: 12 bits
- Two-wire I²C-bus serial interface including HS Mode 3.4 MHz
- Firmware identical to TMP102
- ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM[1] per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA

3. Applications

- Portable and battery-powered applications
- Power supply temperature monitoring
- Computer peripheral thermal protection
- Notebook computers

1. WLCSP6 was too small so CDM was tested with die in package.

- Battery management
- Thermostat controls
- Electromechanical device temperatures
- General temperature measurements:
  - Industrial controls
  - Test equipment
  - Medical instrumentation

4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PCT2202UK	22x[1]	WLCSP6	wafer level chip-size package; 6 bumps; 0.69 × 1.09 × 0.382 mm (backside coating included)	PCT2202UK

[1] x = work week of assembly operation.

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature range
PCT2202UK	PCT2202UKZ	WLCSP6	Reel 7” Q1/T1 *special mark chips dry pack	3000	T_{oper} = –55 °C to +125 °C

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5. Block diagram

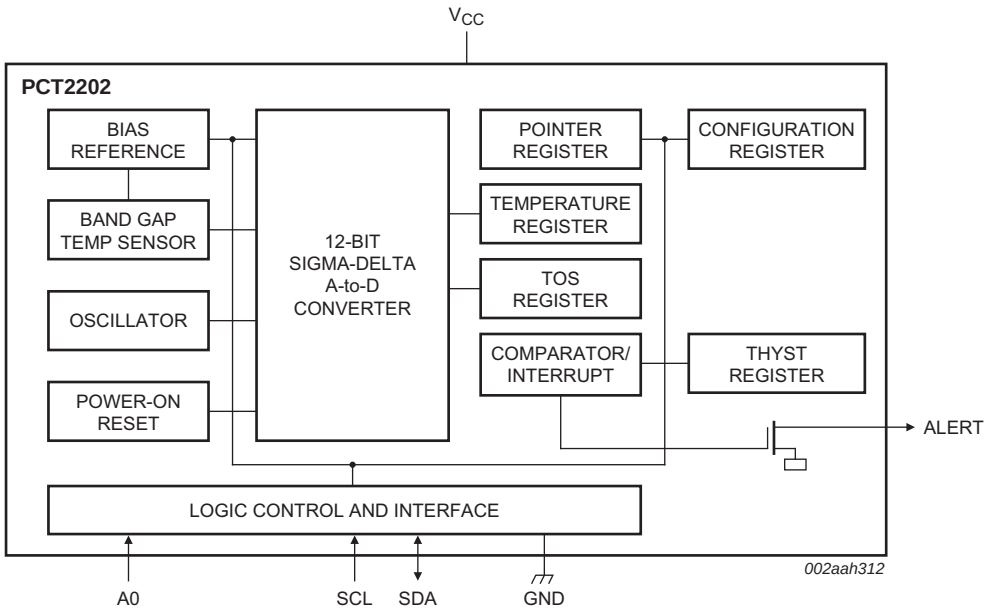


Fig 1. Block diagram of PCT2202

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6. Pinning information

6.1 Pinning

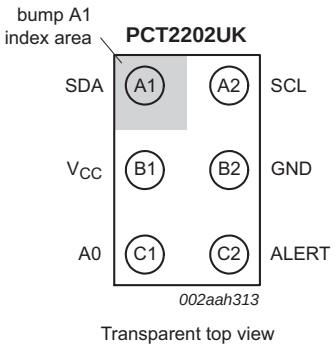


Fig 2. Pin configuration for WLCSP6

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
SCL	A2	Digital input. I²C-bus serial clock input.
GND	B2	Ground. To be connected to the system ground.
ALERT	C2	Overtemperature Shutdown output; open-drain.
A0	C1	Digital input. User-defined I²C-bus address (connect to V_{DD}, GND SDA or SCL).
V_{CC}	B1	Power supply.
SDA	A1	Digital I/O. I²C-bus serial bidirectional data line; open-drain.

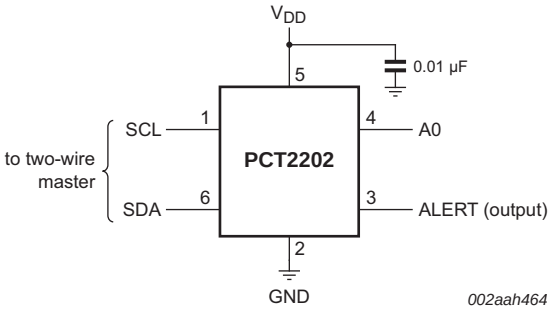
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7. Functional description

The PCT2202 is a digital temperature sensor that is optimal for thermal management and thermal protection applications. The PCT2202 is two-wire and SMBus interface compatible, and is specified over a temperature range of −40 °C to +125 °C.

Pull-up resistors are required on SCL, SDA and ALERT. A 0.01 μF bypass capacitor is recommended on the power supply pin, as shown in Figure 3.



Remark: SCL, SDA and ALERT pins require pull-up resistors.

Fig 3. Typical connections

The temperature sensor in the PCT2202 is the chip itself. Thermal paths run through the package leads, as well as the plastic package. The lower thermal resistance of metal causes the leads to provide the primary thermal path.

To maintain accuracy in applications requiring air or surface temperature measurement, care should be taken to isolate the package and leads from ambient air temperature. A thermally-conductive adhesive is helpful in achieving accurate surface temperature measurement.

7.1 Pointer register

Figure 4 shows the internal register structure of the PCT2202. The 8-bit Pointer register of the device is used to address a given data register. The Pointer register uses the two LSBs (see Table 4) to identify which of the data registers should respond to a read or write command. Table 4 identifies the bits of the Pointer register byte. During a write command, P2 through P7 must always be 0. Table 5 describes the pointer address of the registers available in the PCT2202. Power-up reset value of P1/P0 is ‘00’. By default, the PCT2202 reads the temperature on power-up.

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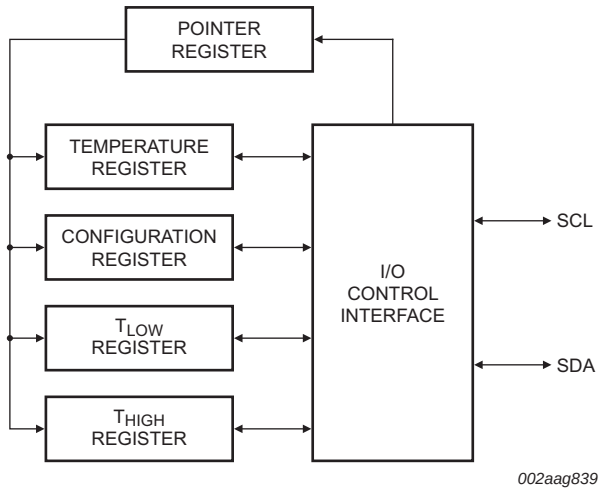


Fig 4. Internal register structure

Table 4. Pointer register byte

P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	0	0	register bits	

Table 5. Pointer addresses

P1	P0	Register
0	0	Temperature register (read only)
0	1	Configuration register (read/write)
1	0	T_{LOW} register (read/write)
1	1	T_{HIGH} register (read/write)

7.2 Temperature register

The Temperature register of the PCT2202 is configured as a 12-bit read-only register (Configuration register EM bit = 0, see Section 7.3.1 “EM - Extended mode bit”), or as a 13-bit, read-only register (Configuration register EM bit = 1) that stores the output of the most recent conversion. Two bytes must be read to obtain data, and are described in Table 6 and Table 7. Note that byte 1 is the most significant byte, followed by byte 2, the least significant byte. The first 12 bits (13 bits in Extended mode) are used to indicate temperature. The least significant byte does not have to be read if that information is not needed. The data format for temperature is summarized in Table 8 and Table 9. One LSB equals 0.0625 °C. Negative numbers are represented in binary two’s complement format. Following power-up or reset, the Temperature register will read 0 °C until the first conversion is complete. Bit D0 of byte 2 indicates Normal mode (EM bit = 0) or Extended mode (EM bit = 1) and can be used to distinguish between the two temperature register data formats. The unused bits in the Temperature register always read ‘0’.

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Table 6. Byte 1 of Temperature register

Extended mode 13-bit configuration shown in parentheses.

D7	D6	D5	D4	D3	D2	D1	D0
T11 (T12)	T10 (T11)	T9 (T10)	T8 (T9)	T7 (T8)	T6 (T7)	T5 (T6)	T4 (T5)

Table 7. Byte 2 of Temperature register

Extended mode 13-bit configuration shown in parentheses.

D7	D6	D5	D4	D3	D2	D1	D0
T3 (T4)	T2 (T3)	T1 (T2)	T0 (T1)	0 (T0)	0 (0)	0 (0)	0 (1)

Table 8. 12-bit temperature data format

The resolution for the Temp ADC in Internal temperature mode is 0.0625 °C/count.

Temperature (°C)	Digital output (binary)	Hex
128	0111 1111 1111	7FFh
127.9375	0111 1111 1111	7FFh
100	0110 0100 0000	640h
80	0101 0000 0000	500h
75	0100 1011 0000	4B0h
50	0011 0010 0000	320h
25	0001 1001 0000	190h
0.25	0000 0000 0100	004h
0	0000 0000 0000	000h
−0.25	1111 1111 1100	FFCh
−25	1110 0111 0000	E70h
−55	1100 1001 0000	C90h

For positive temperatures (for example, +50 °C): Two's complement is not performed on positive numbers, therefore, simply convert the number to binary code with the 12-bit, left-justified format, and MSB = 0 to denote a positive sign.
Example: (+50 °C) / (0.0625 °C/count) = 800 (decimal) = 320h = 0011 0010 0000.

For negative temperatures (for example, −25 °C): Generate the two's complement of a negative number by complementing the absolute value binary number and adding 1. Denote a negative number with MSB = 1.
Example: (|−25 °C|) / (0.0625 °C/count) = 400 (decimal) = 190h = 001 1001 0000.
Two's complement format: 1110 0110 1111 + 1 = 1110 0111 0000.

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Table 9. 13-bit temperature data format

Temperature (°C)	Digital output (binary)	Hex
150	0 1001 0110 0000	0960h
128	0 1000 0000 0000	0800h
127.9375	0 0111 1111 1111	07FFh
100	0 0110 0100 0000	0640h
80	0 0101 0000 0000	0500h
75	0 0100 1011 0000	04B0h
50	0 0011 0010 0000	0320h
25	0 0001 1001 0000	0190h
0.25	0 0000 0000 0100	0004h
0	0 0000 0000 0000	0000h
−0.25	1 1111 1111 1100	1FFCh
−25	1 1110 0111 0000	1E70h
−55	1 1100 1001 0000	1C90h

7.3 Configuration register

The Configuration register is a 16-bit read/write register used to store bits that control the operational modes of the temperature sensor. Read/write operations are performed MSByte first. The format and power-up/reset value of the Configuration register is shown in Table 10. For compatibility, the first byte corresponds to the Configuration register in the LM75 and PCT2075. All registers are updated byte-by-byte.

Table 10. Configuration and power-up/reset format

Byte	D7	D6	D5	D4	D3	D2	D1	D0
1	OS	R1	R0	F1	F0	POL	TM	SD
	0	1	1	0	0	0	0	0
2	CR1	CR0	AL	EM	0	0	0	0
	1	0	1	0	0	0	0	0

7.3.1 EM - Extended mode bit

The Extended mode bit configures the device for Normal mode operation (EM = 0) or Extended mode operation (EM = 1). In Normal mode, the Temperature register and High-limit and Low-limit registers use a 12-bit data format. Normal mode is used to make the PCT2202 compatible with the LM75 and PCT2075.

Extended mode (EM = 1) allows measurement of temperatures above +128 °C by configuring the Temperature register and High-limit and Low-limit registers for 13-bit data format.

7.3.2 AL - ALERT bit

The AL bit is a read-only function. Reading the AL bit will provide information about the comparator mode status. The state of the POL bit inverts the polarity of data returned from the AL bit. For POL = 0, the AL bit will read as ‘1’ until the temperature equals or exceeds T_{HIGH} for the programmed number of consecutive faults, causing the AL bit to read as ‘0’.

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The AL bit will continue to read as '0' until the temperature falls below T_{LOW} for the programmed number of consecutive faults, when it will again read as '1'. The status of the TM bit does not affect the status of the AL bit.

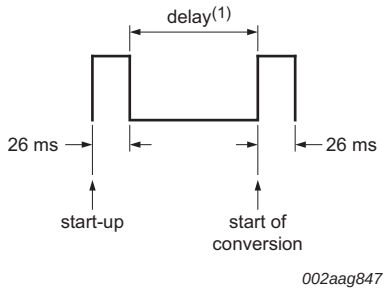
7.3.3 CR1, CR0 - Conversion rate bits

The conversion rate bits, CR1 and CR0, configure the PCT2202 for conversion rates of 8 Hz, 4 Hz, 1 Hz or 0.25 Hz. The default rate is 4 Hz. The PCT2202 has a typical conversion time of 26 ms. To achieve different conversion rates, the PCT2202 makes a conversion and after that powers down and waits for the appropriate delay set by CR1 and CR0. Table 11 shows the settings for CR1 and CR0.

Table 11. Conversion rate settings

CR1	CR0	Conversion rate
0	0	0.25 Hz
0	1	1 Hz
1	0	4 Hz (default)
1	1	8 Hz

After power-up or general-call reset, the PCT2202 immediately starts a conversion, as shown in Figure 5. The first result is available after 26 ms (typical). The active quiescent current during conversion is 40 μA (typical at +27 °C). The quiescent current during delay is 2.2 μA (typical at +27 °C).



(1) Delay is set by CR1 and CR0.

Fig 5. Conversion start

7.3.4 SD - Shut-down mode bit

The Shut-down mode bit saves maximum power by shutting down all device circuitry other than the serial interface, reducing current consumption to typically less than 0.5 μA. Shut-down mode is enabled when the SD bit is '1'. The device shuts down when current conversion is completed. When SD is equal to '0', the device maintains a continuous conversion state.

7.3.5 TM - Thermostat mode bit

The Thermostat mode bit indicates to the device whether to operate in Comparator mode (TM = 0) or Interrupt mode (TM = 1). For more information on comparator and interrupt modes, see Section 7.4 "High-limit and low-limit registers".

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7.3.6 POL - Polarity bit

The Polarity bit allows the user to adjust the polarity of the ALERT pin output. If POL = 0, the ALERT pin will be active LOW, as shown in Figure 6. For POL = 1, the ALERT pin will be active HIGH and the state of the ALERT pin is inverted.

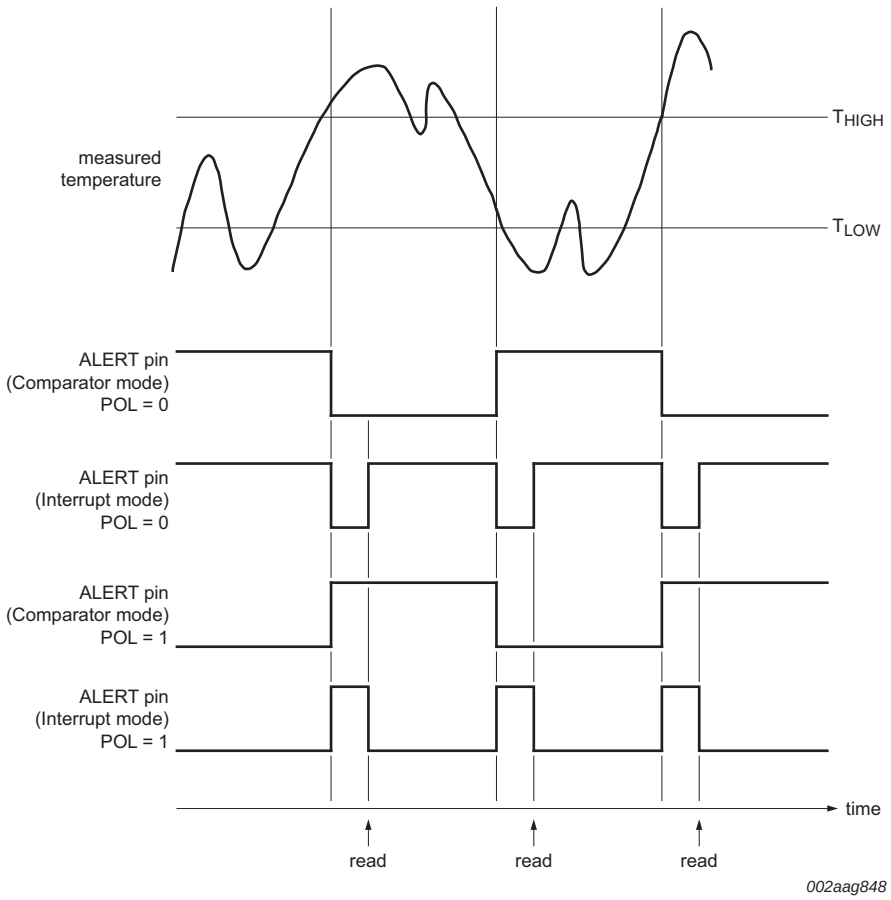


Fig 6. Output transfer function

7.3.7 F1, F0 - Fault queue bits

A fault condition exists when the measured temperature exceeds the user-defined limits set in the T_{HIGH} and T_{LOW} registers. Additionally, the number of fault conditions required to generate and alert may be programmed using the fault queue. The fault queue is provided to prevent a false alert as a result of environmental noise. The fault queue requires consecutive fault measurements in order to trigger the alert function. Table 12 defines the number of measured faults that may be programmed to trigger an alert condition in the device. For T_{HIGH} and T_{LOW} register format and byte order, see Section 7.4 “High-limit and low-limit registers”.

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Table 12. PCT2202 fault settings

F1	F0	Consecutive faults
0	0	1
0	1	2
1	0	4
1	1	6

7.3.8 R1, R0 - Converter resolution bits

R1 and R0 are read-only bits. The PCT2202 converter resolution is set on start-up to '11'. This sets the Temperature register to a 12-bit resolution.

7.3.9 OS - One-shot/conversion ready

The PCT2202 features a One-shot temperature measurement mode. When the device is in Shut-down mode, writing a '1' to the OS bit starts a single temperature conversion. During the conversion, the OS bit reads '0'. The device returns to the shut-down state at the completion of the single conversion. After the conversion, the OS bit reads '1'. This feature is useful for reducing power consumption in the PCT2202 when continuous temperature monitoring is not required.

As a result of the short conversion time, the PCT2202 can achieve a higher conversion rate. A single conversion typically takes 26 ms and a read can take place in less than 20 μs. When using One-shot mode, 30 or more conversions per second are possible.

7.4 High-limit and low-limit registers

In Comparator mode (TM = 0), the ALERT pin becomes active when the temperature equals or exceeds the value in T_{HIGH} and generates a consecutive number of faults according to fault bits F1 and F0. The ALERT pin remains active until the temperature falls below the indicated T_{LOW} value for the same number of faults.

In Interrupt mode (TM = 1), the ALERT pin becomes active when the temperature equals or exceeds the value in T_{HIGH} for a consecutive number of fault conditions (as shown in Table 12). The ALERT pin remains active until a read operation of any register occurs, or the device successfully responds to the SMBus Alert Response address. The ALERT pin will also be cleared if the device is placed in Shut-down mode. Once the ALERT pin is cleared, it becomes active again only when temperature falls below T_{LOW}, and remains active until cleared by a read operation of any register or a successful response to the SMBus Alert Response address. Once the ALERT pin is cleared, the above cycle repeats, with the ALERT pin becoming active when the temperature equals or exceeds T_{HIGH}. The ALERT pin can also be cleared by resetting the device with the General Call Reset command. This action also clears the state of the internal registers in the device, returning the device to Comparator mode (TM = 0).

Both operational modes are represented in Figure 6. Table 13 and Table 14 describe the format for the T_{HIGH} and T_{LOW} registers. Note that the most significant byte is sent first, followed by the least significant byte. Power-up reset values for T_{HIGH} and T_{LOW} are: T_{HIGH} = +80 °C and T_{LOW} = +75 °C. The format of the data for T_{HIGH} and T_{LOW} is exactly the same as the Temperature register — binary two's complement format.

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Table 13. Byte 1 and Byte 2 of T_{HIGH} register

Extended mode 13-bit configuration shown in parentheses.

Byte	D7	D6	D5	D4	D3	D2	D1	D0
1	H11 (H12)	H10 (H11)	H9 (H10)	H8 (H9)	H7 (H8)	H6 (H7)	H5 (H6)	H4 (H5)
2	H3 (H4)	H2 (H3)	H1 (H2)	H0 (H1)	0 (H0)	0 (0)	0 (0)	0 (0)

Table 14. Byte 1 and Byte 2 of T_{LOW} register

Extended mode 13-bit configuration shown in parentheses.

Byte	D7	D6	D5	D4	D3	D2	D1	D0
1	L11 (L12)	L10 (L11)	L9 (L10)	L8 (L9)	L7 (L8)	L6 (L7)	L5 (L6)	L4 (L5)
2	L3 (L4)	L2 (L3)	L1 (L2)	L0 (L1)	0 (L0)	0 (0)	0 (0)	0 (0)

8. Bus overview

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

The device that initiates the transfer is called a ‘master’, and the devices controlled by the master are ‘slaves’. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, a START condition is initiated, indicated by pulling the data line (SDA) from a HIGH to LOW logic level while SCL is HIGH. All slaves on the bus shift in the slave address byte on the rising edge of the clock, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA LOW.

Data transfer is then initiated and sent over eight clock pulses followed by an Acknowledge bit. During data transfer SDA must remain stable while SCL is HIGH, because any change in SDA while SCL is HIGH will be interpreted as a START or STOP signal.

Once all data have been transferred, the master generates a STOP condition indicated by pulling SDA from LOW to HIGH, while SCL is HIGH.

8.1 Serial interface

The PCT2202 operates as a slave device only on the I²C-bus and SMBus. Connections to the bus are made via the open-drain I/O lines SDA and SCL. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The PCT2202 supports the transmission protocol for Standard mode, Fast mode, Fast-mode Plus (1 kHz to 1 MHz) and High-speed mode (1 kHz to 3.4 MHz). All data bytes are transmitted MSByte first.

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8.2 Serial bus address

To communicate with the PCT2202, the master must first address slave devices via a slave address byte. The slave address byte consists of seven address bits, and a direction bit indicating the intent of executing a read or write operation.

The PCT2202 features an address pin to allow up to four devices to be addressed on a single bus. Table 15 describes the pin logic levels used to properly connect up to four devices.

Table 15. Address pin (ADD0) and slave addresses

Device two-wire address	A0 pin connection
1001 000	GND
1001 001	V_{DD}
1001 010	SDA
1001 011	SCL

8.3 Write/read operation

Accessing a particular register on the PCT2202 is accomplished by writing the appropriate value to the Pointer register. The value for the Pointer Register is the first byte transferred after the slave address byte with the R/$\overline{W}$ bit LOW. Every write operation to the PCT2202 requires a value for the Pointer register (see Figure 15).

When reading from the PCT2202, the last value stored in the Pointer register by a write operation is used to determine which register is read by a read operation. To change the register pointer for a read operation, a new value must be written to the Pointer register.

This action is accomplished by issuing a slave address byte with the R/$\overline{W}$ bit LOW, followed by the Pointer register byte. No additional data are required. The master can then generate a START condition and send the slave address byte with the R/$\overline{W}$ bit HIGH to initiate the read command. See Figure 16 for details of this sequence. If repeated reads from the same register are desired, it is not necessary to continually send the Pointer register bytes, because the PCT2202 remembers the Pointer register value until it is changed by the next write operation.

Note that register bytes are sent with the most significant byte first, followed by the least significant byte.

8.4 Slave mode operations

The PCT2202 can operate as a slave receiver or slave transmitter. As a slave device, the PCT2202 never drives the SCL line — it is an input only.

8.4.1 Slave receiver mode

The first byte transmitted by the master is the slave address, with the R/$\overline{W}$ bit LOW. The PCT2202 then acknowledges reception of a valid address. The next byte transmitted by the master is the Pointer register. The PCT2202 then acknowledges reception of the Pointer register byte. The next byte or bytes are written to the register addressed by the Pointer register. The PCT2202 acknowledges reception of each data byte. The master can terminate data transfer by generating a START or STOP condition.

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8.4.2 Slave transmitter mode

The first byte transmitted by the master is the slave address, with the R/$\overline{W}$ bit HIGH. The slave acknowledges reception of a valid slave address. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the Pointer register. The master acknowledges reception of the data byte. The next byte transmitted by the slave is the least significant byte. The master acknowledges reception of the data byte. The master can terminate data transfer by generating a Not-Acknowledge on reception of any data byte, or generating a START or STOP condition.

8.5 SMBus Alert function

The PCT2202 supports the SMBus Alert function. When the PCT2202 operates in Interrupt mode (TM = 1), the ALERT pin may be connected as an SMBus Alert signal. When a master senses that an ALERT condition is present on the ALERT line, the master sends an SMBus Alert command (0001 1001) to the bus. If the ALERT pin is active, the device acknowledges the SMBus Alert command and responds by returning its slave address on the SDA line. The eighth bit (LSB) of the slave address byte indicates if the ALERT condition was caused by the temperature exceeding T_{HIGH} or falling below T_{LOW}. For POL = 0, this bit is LOW if the temperature is greater than or equal to T_{HIGH}; this bit is HIGH if the temperature is less than T_{LOW}. The polarity of this bit is inverted if POL = 1. Refer to Figure 17 for details of this sequence.

If multiple devices on the bus respond to the SMBus Alert command, arbitration during the slave address portion of the SMBus Alert command determines which device will clear its ALERT status. The device with the lowest two-wire address wins the arbitration. If the PCT2202 wins the arbitration, its ALERT pin becomes inactive at the completion of the SMBus Alert command. If the PCT2202 loses the arbitration, its ALERT pin remains active.

8.6 General Call - Software Reset

The PCT2202 responds to a two-wire General Call address (0000 000) if the eighth bit is ‘0’. The device acknowledges the General Call address and responds to commands in the second byte. If the second byte is 0000 0110, the PCT2202 internal registers are reset to power-up values. The PCT2202 does not support the General Address acquire command.

8.7 High-speed (Hs) mode

In order for the two-wire bus to operate faster than the Fm+ speed (1 MHz), the master device must issue an Hs-mode master code (0000 1xxx) as the first byte after a START condition to switch the bus to high-speed operation. The PCT2202 does not acknowledge this byte, but switches its input filters on SDA and SCL and its output filters on SDA to operate in Hs-mode, allowing transfers at up to 3.4 MHz. After the Hs-mode master code has been issued, the master transmits a two-wire slave address to initiate a data transfer operation. The bus continues to operate in Hs-mode until a STOP condition occurs on the bus. Upon receiving the STOP condition, the PCT2202 switches the input and output filters back to Fast-mode operation.

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8.8 Time-out function

The PCT2202 resets the serial interface if SCL is held LOW for 30 ms (typical). The PCT2202 releases the bus if it is pulled LOW and waits for a START condition. To avoid activating the time-out function, it is necessary to maintain a communication speed of at least 10 kHz for SCL operating frequency to conform to the SMBus specification.

8.9 Noise

The PCT2202 is a very low-power device and generates very low noise on the supply bus. Applying an RC filter to the V_{DD} pin of the PCT2202 can further reduce any noise the PCT2202 might propagate to other components. R_F in Figure 7 should be less than 5 kΩ and C_F should be greater than 10 nF.

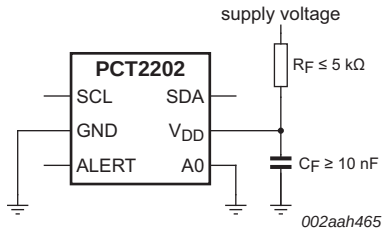


Fig 7. Noise reduction

9. Limiting values

Table 16. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-	2.5	V
V_I	input voltage	[1]	–0.5	+2.5	V
I_I	input current		–5.0	+5.0	mA
T_{oper}	operating temperature		–55	+125	°C
T_{stg}	storage temperature		–60	+150	°C
T_j	junction temperature		-	+125	°C

[1] Input voltage rating applies to all PCT2202 input voltages.

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10. Characteristics

Table 17. Characteristics

T_{amb} = +25 °C and V_{DD} = 1.65 V to 1.95 V, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Temperature input						
	temperature range		–40	-	+125	°C
T_{acc}	temperature accuracy	0 °C to +85 °C	-	0.5	1	°C
		–40 °C to +125 °C	-	1	2	°C
	temperature vs. supply voltage		-	0.2	0.5	°C/V
T_{res}	temperature resolution		-	0.0625	-	°C
Digital input/output						
V_{IH}	HIGH-level input voltage		0.7 × V_{DD}	-	1.95	V
V_{IL}	LOW-level input voltage		–0.5	-	0.3 × V_{DD}	V
I_I	input current	V_I = 0 V to 1.95 V	-	-	1	µA
V_{OL}	LOW-level output voltage	SDA pin; I_{OL} = 3 mA	0	-	0.2 × V_{DD}	V
		ALERT pin; I_{OL} = 3 mA	0	-	0.2 × V_{DD}	V
	resolution		-	12	-	bit
t_{conv}	conversion time		-	26	35	ms
	conversion modes	CR1 = 0; CR0 = 0	-	0.25	-	conv/s
		CR1 = 0; CR0 = 1	-	1	-	conv/s
		CR1 = 1; CR0 = 0 (default)	-	4	-	conv/s
		CR1 = 1; CR0 = 1	-	8	-	conv/s
t_{to}	time-out time		-	30	40	ms
Power supply						
	operating supply voltage		+1.65	-	+1.95	V
I_q	quiescent current	serial bus inactive; CR1 = 1, CR0 = 0 (default)	-	30	45	µA
		serial bus active; f_{SCL} = 400 kHz	-	40	-	µA
		serial bus active; f_{SCL} = 3.4 MHz	-	45	-	µA
I_{sd}	shutdown current	serial bus inactive	-	0.5	1	µA
		serial bus active; f_{SCL} = 400 kHz	-	7	-	µA
		serial bus active; f_{SCL} = 3.4 MHz	-	12	-	µA

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11. Typical characteristics

At T_{amb} = +25 °C and V_{DD} = 1.8 V, unless noted otherwise.

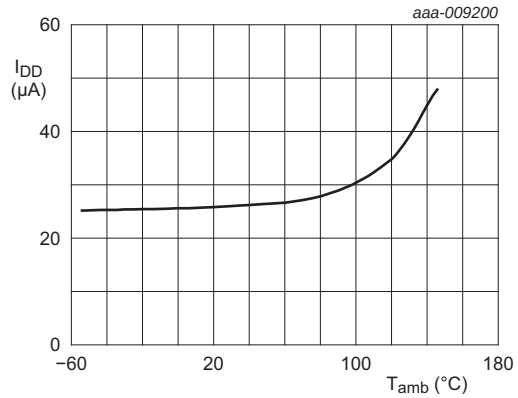


Fig 8. Supply current versus temperature (bus inactive; 4 conversions per second)

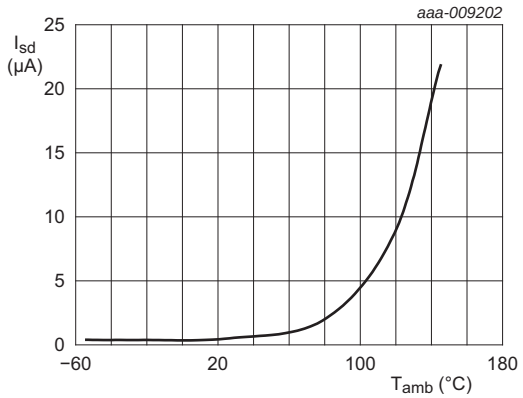


Fig 9. Shutdown current versus temperature (bus inactive)

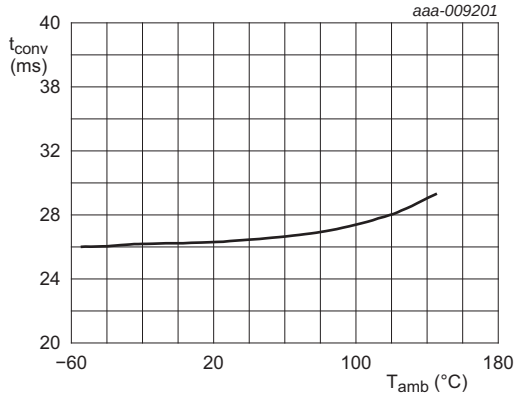


Fig 10. Conversion time versus temperature

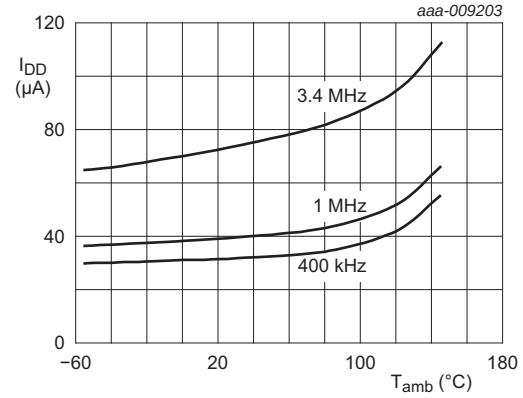


Fig 11. Supply current versus temperature (per bus frequency; 4 conversions per second)

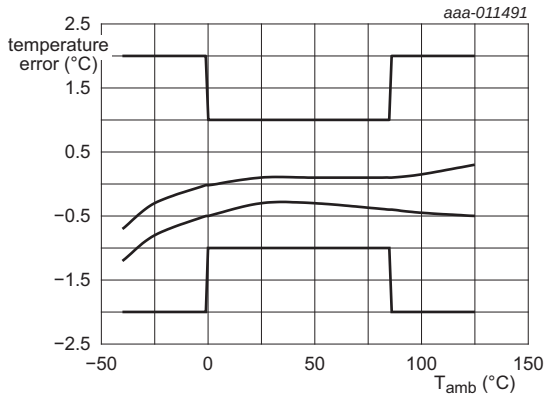


Fig 12. Temperature error versus ambient temperature

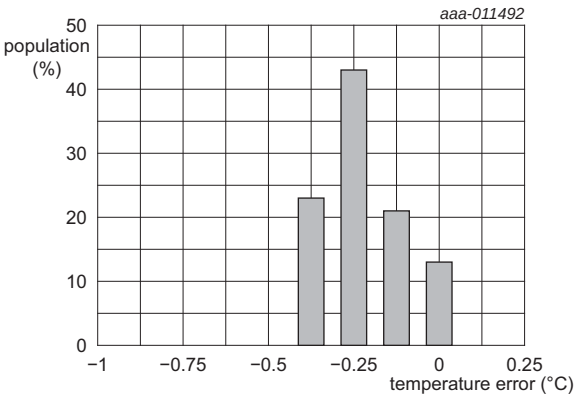


Fig 13. Temperature error at 25 °C

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12. Timing diagrams

The PCT2202 is two-wire and SMBus compatible. Figure 14 to Figure 17 describe the various operations on the PCT2202. Parameters for Figure 14 are defined in Table 18.

Bus definitions are:

Bus idle — Both SDA and SCL lines remain HIGH.

Start data transfer — A change in the state of the SDA line from HIGH to LOW while the SCL line is HIGH defines a START condition. Each data transfer is initiated with a START condition.

Stop data transfer — A change in the state of the SDA line from LOW to HIGH while the SCL line is HIGH defines a STOP condition. Each data transfer is terminated with a repeated START or STOP condition.

Data transfer — The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. It is also possible to use the PCT2202 for single byte updates. To update only the most significant byte, terminate the communication by issuing a START or STOP communication on the bus.

Acknowledge — Each receiving device, when addressed, is obliged to generate an Acknowledge bit. A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the Acknowledge clock pulse. Set-up and hold times must be taken into account. On a master receive, the termination of the data transfer can be signaled by the master generating a **Not-Acknowledge** (‘1’) on the last byte that has been transmitted by the slave.

Table 18. Timing characteristics

Symbol	Parameter	Conditions	Fast mode		High-speed mode		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	V_{DD} = 1.8 V	0.001	0.4	0.001	3.4	MHz
t_{BUF}	bus free time between a STOP and START condition		600	-	160	-	ns
$t_{HD;STA}$	hold time (repeated) START condition		100	-	100	-	ns
$t_{SU;STA}$	set-up time for a repeated START condition		100	-	100	-	ns
$t_{SU;STO}$	set-up time for STOP condition		100	-	100	-	ns
$t_{HD;DAT}$	data hold time		0	-	0	-	ns
$t_{SU;DAT}$	data set-up time		100	-	10	-	ns
t_{LOW}	LOW period of the SCL clock	V_{DD} = 1.8 V	1300	-	160	-	ns
t_{HIGH}	HIGH period of the SCL clock		600	-	60	-	ns
t_f	fall time of both SDA and SCL signals		-	300	-	-	ns
t_r	rise time of both SDA and SCL signals		-	300	-	160	ns
		for SCL ≤ 100 kHz	-	1000	-	-	ns

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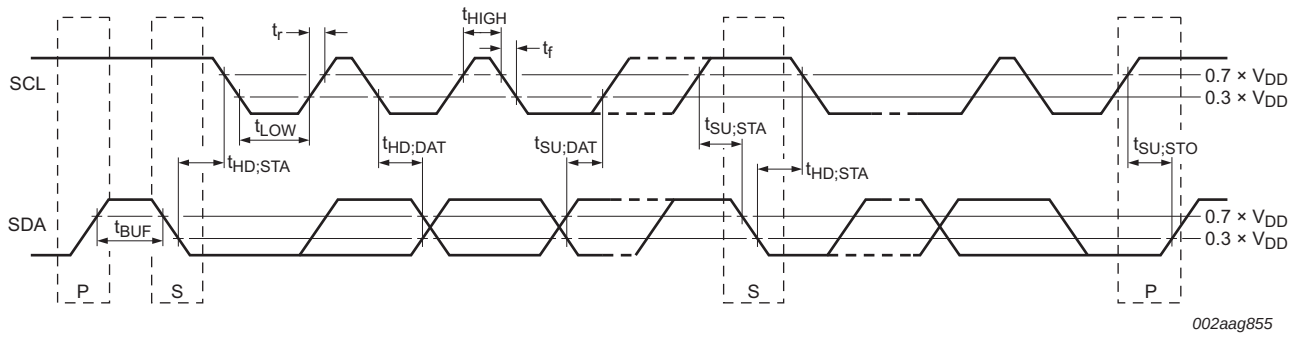
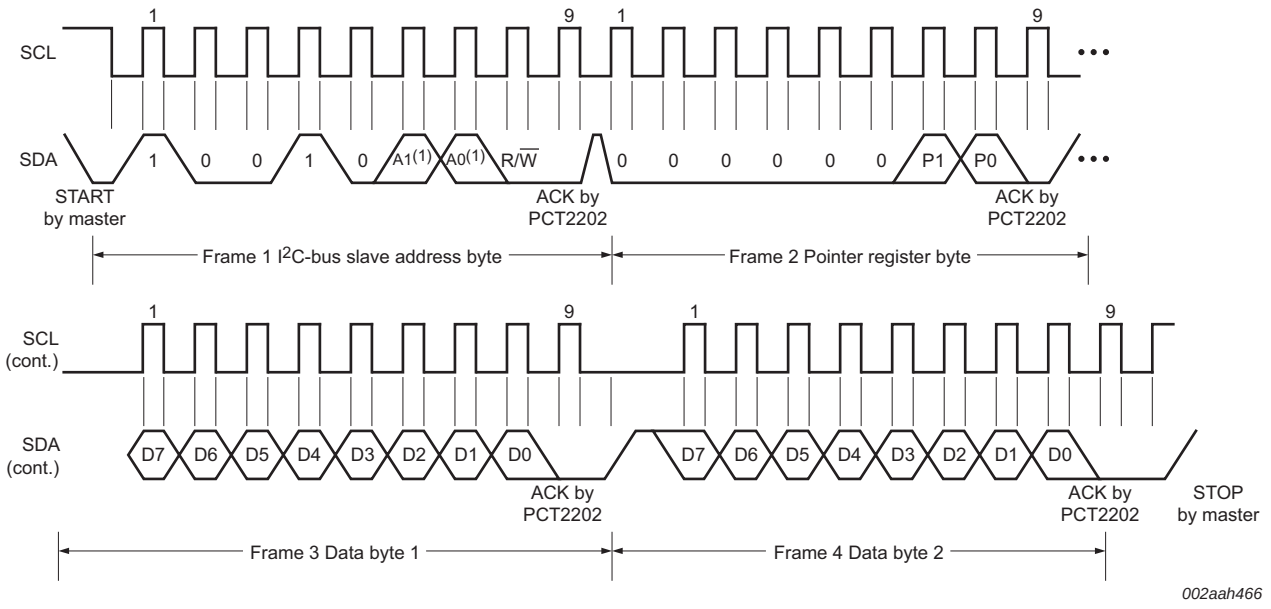


Fig 14. I²C-bus timing diagram

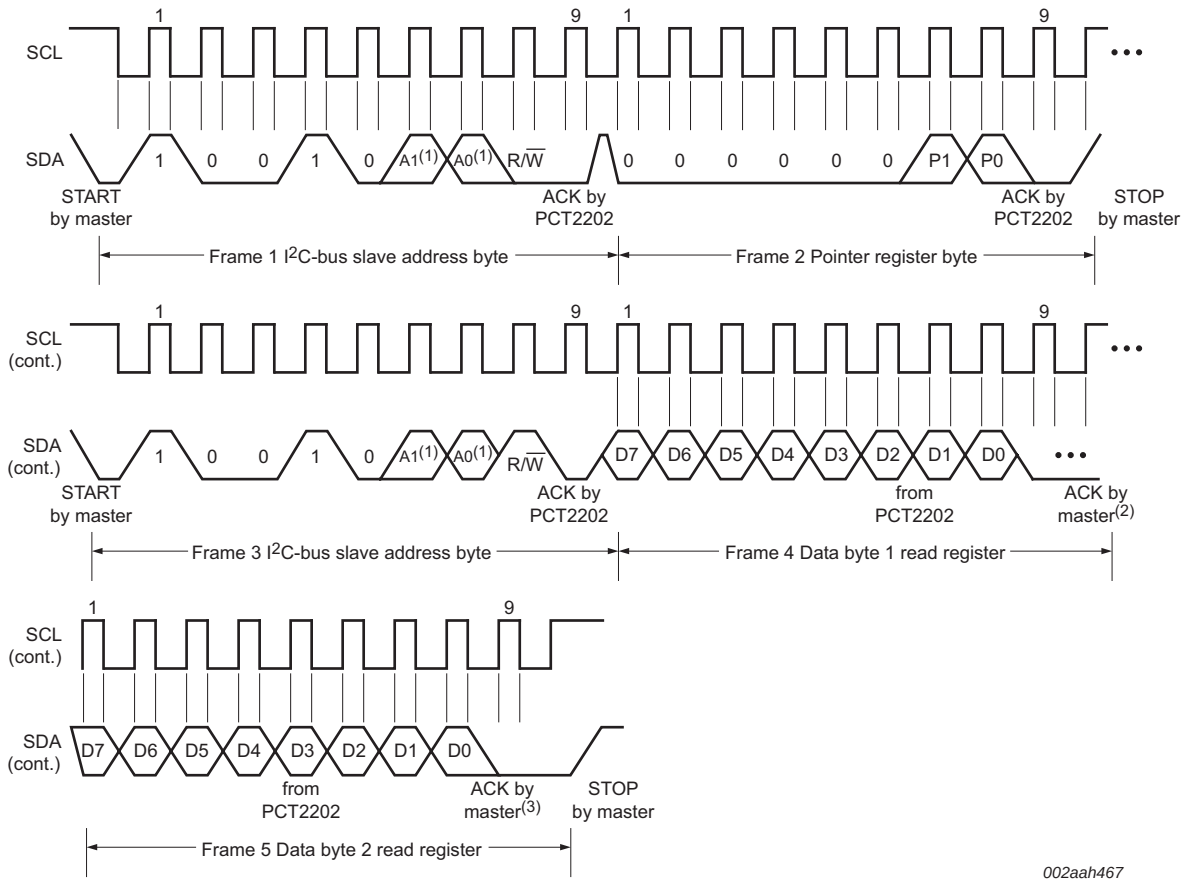


(1) The value of A0 and A1 bits are determined by the A0 pin.

Fig 15. I²C-bus timing diagram for 'write word' format

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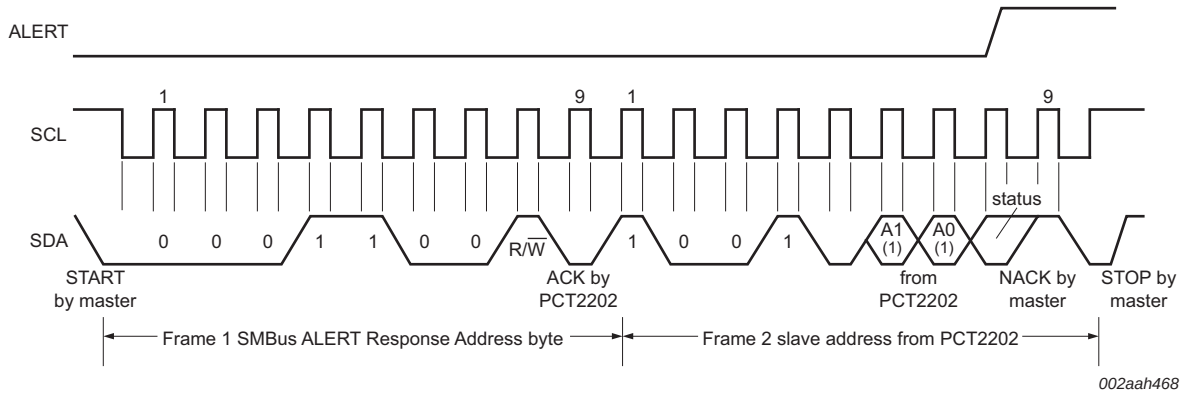


(1) The value of A0 and A1 bits are determined by the A0 pin.

(2) Master should leave SDA HIGH to terminate a single-byte read operation.

(3) Master should leave SDA HIGH to terminate a two-byte read operation.

Fig 16. I²C-bus timing diagram for 'read word' format



(1) The value of A0 and A1 bits are determined by the A0 pin.

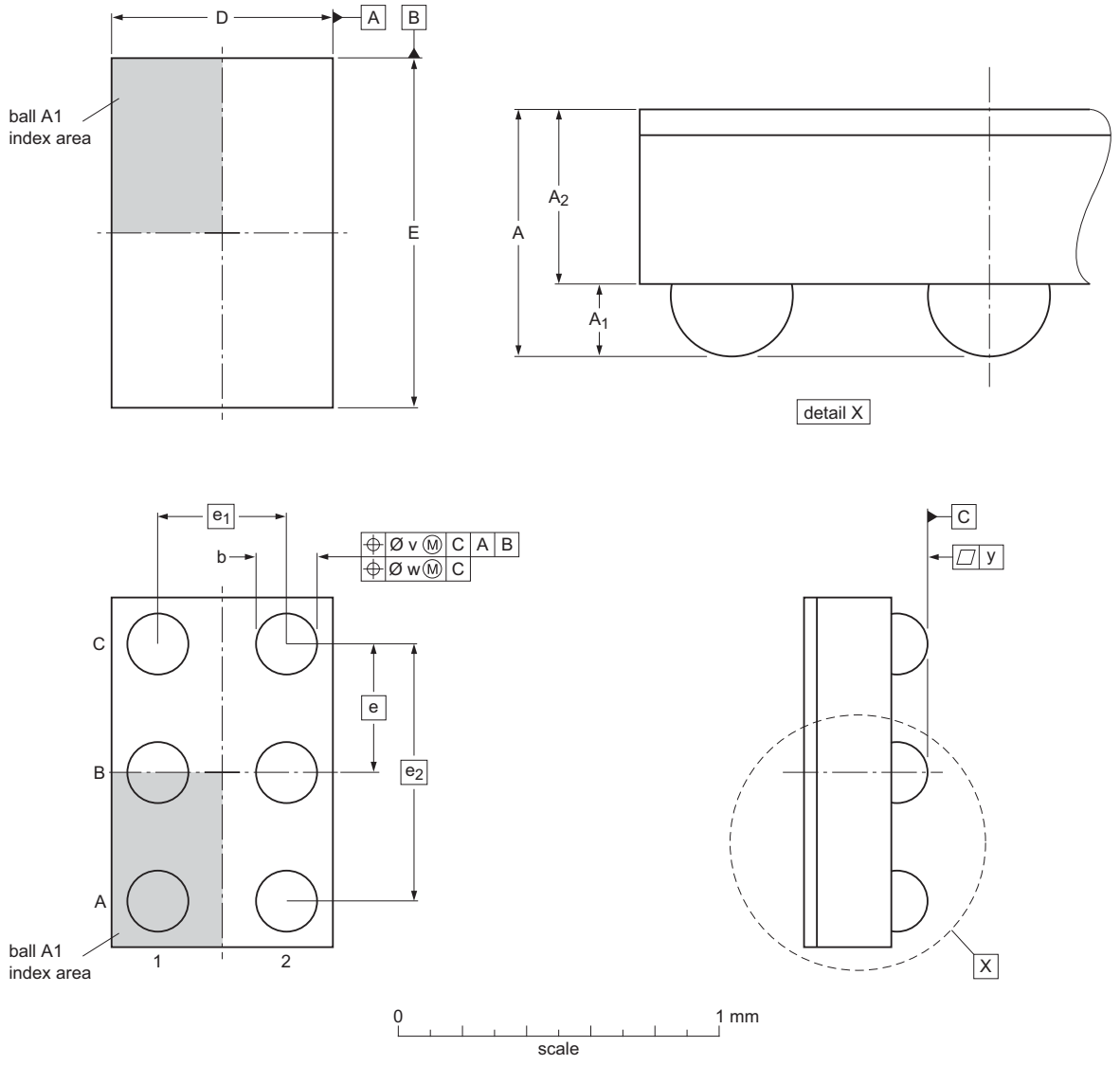
Fig 17. Timing diagram for SMBus ALERT

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13. Package outline

WLCSP6: wafer level chip-scale package; 6 bumps; 0.69 x 1.09 x 0.38 mm (Backside coating included) **PCT2202**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
	max	0.41	0.125	0.287	0.22	0.72	1.12						
mm	nom	0.38	0.110	0.272	0.19	0.69	1.09	0.4	0.4	0.8	0.15	0.05	0.05
	min	0.35	0.095	0.257	0.16	0.66	1.06						

wlcsp6_pct2202_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
PCT2202	- - -	- - -	- - -			~~13-10-07~~ 14-11-19

Fig 18. Package outline PCT2202UK (WLCSP6)

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14. Soldering of WLCSP packages

14.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note *AN10439 "Wafer Level Chip Scale Package"* and in application note *AN10365 "Surface mount reflow soldering description"*.

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

14.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

14.3 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 19) than a SnPb process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 19.

Table 19. Lead-free process (from J-STD-020D)

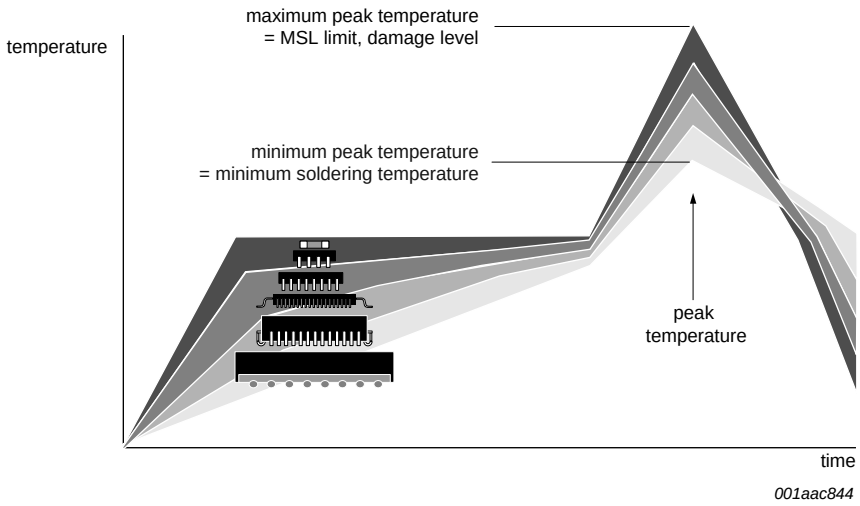
Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 19.

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MSL: Moisture Sensitivity Level

Fig 19. Temperature profiles for large and small components

For further information on temperature profiles, refer to application note *AN10365 "Surface mount reflow soldering description"*.

14.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

14.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

14.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

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Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note *AN10365 "Surface mount reflow soldering description"*.

14.3.4 Cleaning

Cleaning can be done after reflow soldering.

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15. Soldering: PCB footprints

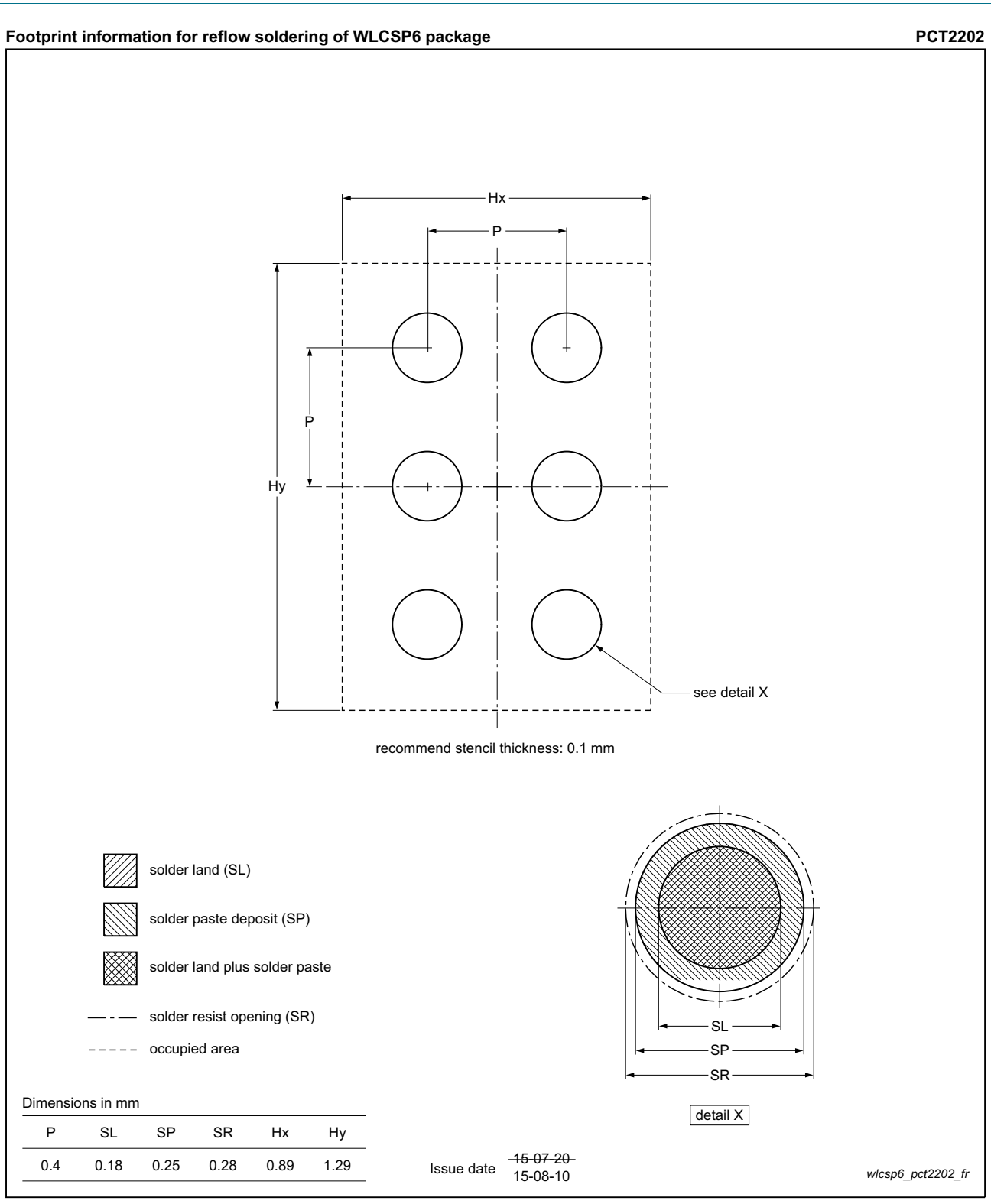


Fig 20. PCB footprint for PCT2202 (WLCSP6); reflow soldering

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16. Abbreviations

Table 20. Abbreviations

Acronym	Description
CDM	Charged-Device Model
DP	Dry Pack
ESD	ElectroStatic Discharge
HBM	Human Body Model
I²C-bus	Inter-Integrated Circuit bus
LSB	Least Significant Bit
LSByte	Least Significant Byte
MSB	Most Significant Bit
MSByte	Most Significant Byte
SMBus	System Management Bus

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17. Revision history

Table 21. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCT2202 v.1.1	20150814	Product data sheet	-	PCT2202 v.1
Modifications:	• Added Section 15 “Soldering: PCB footprints”.			
PCT2202 v.1	20141205	Product data sheet	-	-

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Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[2] The term 'short data sheet' is explained in section "Definitions".

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