PCM4201EVM User's Guide

This document provides the information needed to set up and operate the PCM4201EVM evaluation module (EVM). For a more detailed description of the PCM4201, please refer to the product datasheet available from the Texas Instruments web site at www.ti.com. Additional support documents are listed in the section of this guide entitled ***Related Documentation from Texas Instruments*** and ***Additional Documentation***. Throughout this document, the acronym **EVM** and the phrase **evaluation module** are synonymous with the PCM4201EVM. This user s guide includes setup and configuration instructions, information regarding absolute operating conditions, an electrical schematic, PCB layout drawings, and a bill of materials (BOM) for the EVM.

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1 Introduction

The PCM4201 is a low power, high-performance, single channel audio analog-to-digital (A/D) converter designed for use in battery-operated or portable professional audio applications, including digital wireless microphones and digital audio recorders/processors. The PCM4201 features a 24-bit linear PCM data output, with a data format compatible with digital signal processors and digital audio interface transmitters (including the DIT4096 and DIT4192 from Texas Instruments).

The PCM4201 includes three sampling modes, supporting sampling rates up to 108kHz. The Normal Speed Low Power mode supports sampling rates up to 54kHz, and employs 64x oversampling to reduce overall converter power. The Normal Speed High Performance mode supports sampling rates up to 54kHz with 128x oversampling, resulting in higher dynamic range than the Low Power mode, at the expense of increased power dissipation. The Double Speed mode supports sampling frequencies up to 108kHz, and is provided for those cases where higher sampling rates may be required.

A digital high-pass filter is included for DC removal. Dedicated control pins are included for sampling mode selection, Slave/Master mode port operation, digital high-pass filter enable/disable, and reset/power-down functions.

A +5V power supply is required for the analog section of the device, while a +3.3V power supply is typically utilized for the digital circuitry. The digital supply may operate at voltages as low as +1.8V, with a corresponding 10mW to 20mW reduction in power dissipation, depending upon the sampling mode selection. Figure 1 illustrates the functional block diagram for the PCM4201.

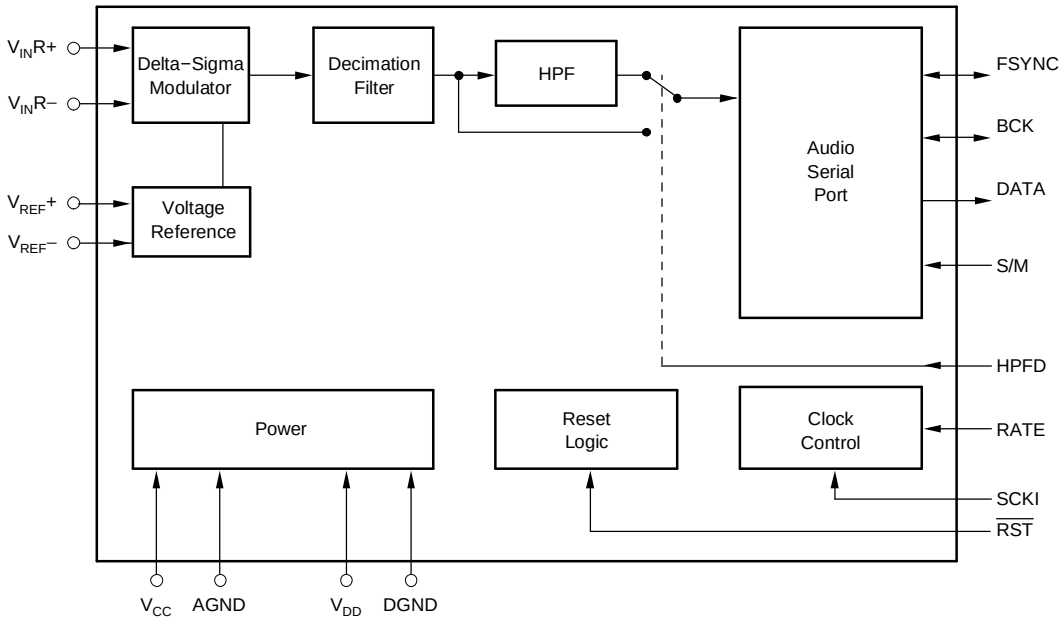


Figure 1. PCM4201 Functional Block Diagram

1.1 PCM4201EVM Features

The PCM4201EVM provides a convenient platform for evaluating the performance and functions of the PCM4201 device. The primary EVM features include:

- Simple configuration using an onboard DIP switch
- Differential voltage input supporting 3-pin XLR or balanced TRS connections
- Differential input buffer and filter circuit utilizing the Texas Instruments OPA2134 dual op amp
- Flexible input buffer power supply connection (dual or single supply options) and resistor/capacitor configuration allow for circuit experimentation and op amp substitution

- Buffered audio serial port output supports connection to external DSP hardware or audio test equipment
- An onboard Texas Instruments DIT4096 provides an AES3-encoded digital output suitable for use with audio test systems or commercial audio equipment, supporting output sampling rates up to 108kHz
- Onboard crystal oscillators, operating at 22.5792MHz and 24.576MHz, support 44.1kHz, 48kHz, 88.2kHz, and 96kHz sampling rates and all three sampling modes of the PCM4201
- An external clock input allows operation at alternative sampling frequencies

As shipped, the PCM4201EVM requires +15V, –15V, and +5V analog power supplies. Options are provided to operate the analog section from a single power supply by utilizing alternative op amps for the input buffer circuit. A +5V digital supply is required, with a +3.3V digital supply being derived onboard using a Texas Instruments REG1117 voltage regulator IC. Connections are provided for an external digital supply for the PCM4201, allowing digital operation down to +1.8V.

1.2 PCM4201EVM General Description and Functional Block Diagram

The PCM4201EVM provides a complete platform for evaluating the performance and features of the PCM4201 single channel audio A/D converter. Figure 2 illustrates the functional block diagram for the evaluation module.

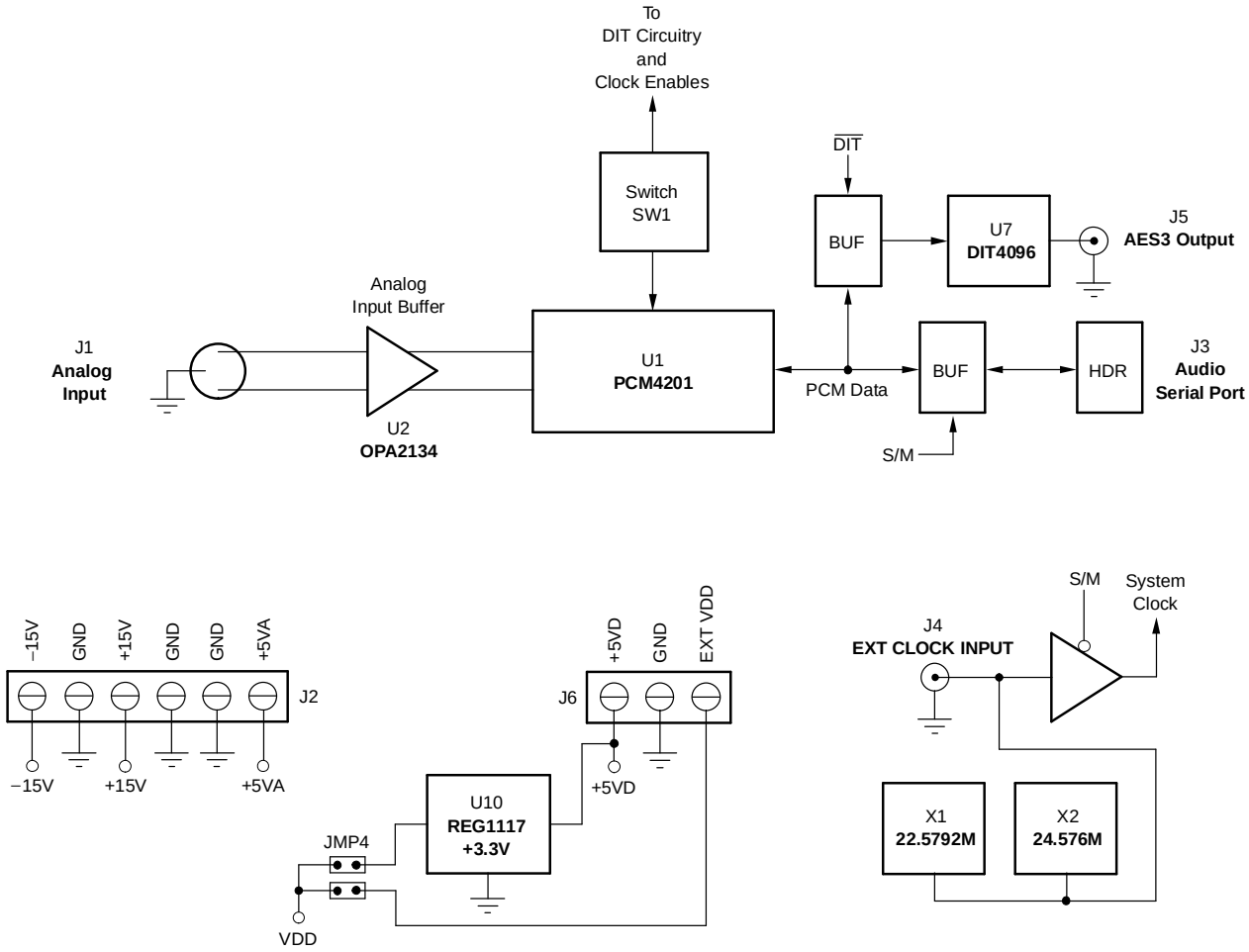


Figure 2. PCM4201EVM Functional Block Diagram

A differential analog input is supported at connector J1. The analog input supports either a 3-pin male XLR or balanced TRS input plug. The analog input is buffered and filtered using a low noise input circuit, utilizing a Texas Instruments' OPA2134 dual audio op amp IC. The output of the buffer circuit is connected to the differential input of the PCM4201, which is then used to convert the analog signal to a 24-bit linear PCM representation in the digital domain.

The 24-bit PCM output data is made available at header J3. The audio data can also be routed to the DIT4096 digital interface transmitter, supporting an AES3-encoded output, which is provided at BNC connector J5. The buffered header is convenient for interfacing to external development hardware or digital signal processors, while the AES3-encoded outputs may be connected to audio test systems or commercial audio equipment.

Power is connected to the board at either terminal block J2 for the analog supplies, or at terminal block J6 for the digital supplies.

Manual reset circuits are provided for both the PCM4201 (U1) and the DIT4096 (U7). The ADC RESET switch (SW2) is utilized for resetting the A/D converter, while the DIT RESET switch (SW3) is utilized for resetting the AES3 transmitter.

The system or master clock for the evaluation module may be generated onboard or by an external clock source. Oscillators X1 and X2 operate at fixed clock frequencies of 22.5792MHz and 24.576MHz, respectively. The oscillators provide low jitter clock sources for measuring the performance of the PCM4201 in Master mode operation. Alternatively, an external clock source may be connected at J4 for Master mode operation, supporting alternative sampling rates. For Slave mode operation, the system clock is provided from an external source through header J3. Switch SW1 provides configuration control for the PCM4201, the DIT4096, the onboard oscillators, and the external clock input at connector J4.

1.3 Related Documentation from Texas Instruments

The following documents provide information regarding Texas Instruments integrated circuits used in the assembly of the PCM4201EVM. The latest revisions of these documents are available from the TI web site at www.ti.com.

Data Sheet	Literature Number
PCM4201 Datasheet	SBAS342
DIT4096 Datasheet	SBOS225
OPA2134 Datasheet	SBOS058
REG1117 Datasheet	SBVS001
SN74ALVC245 Datasheet	SCES271
SN74LVC1G04 Datasheet	SCES214
SN74LVC1G08 Datasheet	SCES217
SN74LVC1G125 Datasheet	SCES223

1.4 Additional Documentation

The following documents or references provide information regarding selected non-TI components used in the assembly of the PCM4201EVM. These documents are available from the corresponding manufacturer.

Document/Reference	Manufacturer
SM7745H Series CMOS Oscillators	Pletronics (http://www.pletronics.com)

2 Getting Started

This section provides information regarding handling, package contents, and absolute operating conditions for the PCM4201EVM.

2.1 Electrostatic Discharge Warning

CAUTION
Failure to observe proper ESD handling precautions may result in damage to EVM components.

Many of the components used in the assembly of the PCM4201EVM are susceptible to damage by electrostatic discharge (ESD). Customers are advised to observe proper ESD handling procedure when unpacking and handling the PCM4201EVM. All handling should be performed at an approved ESD workstation or test bench, using a grounded wrist strap. Failure to observe proper handling procedure may result in damage to the EVM and/or the module components.

2.2 EVM Package Contents

Upon opening the PCM4201EVM package, please check to make sure that these items are included:

- One PCM4201EVM evaluation module
- One printed copy of the PCM4201 product datasheet
- One printed copy of this PCM4201EVM User's Guide

If any of these items are missing, please contact the TI Product Information Center in your region.

2.3 Absolute Operating Conditions

CAUTION
Exceeding the absolute operating conditions may result in damage to the evaluation module and/or the equipment connected to it.

The user should be aware of the absolute operating conditions for the PCM4201EVM. Table 1 summarizes the critical data points.

Table 1. Absolute Operating Conditions

	Min	Max	Units
Power Supplies			
+15V	+5.0	+18.0	V
-15V	-5.0	-18.0	V
+5VA	+4.5	+5.5	V
+5VD	+4.5	+5.5	V
EXT VDD	+1.8	+3.6	V
Audio Serial Port (J3)			
V_{IH}, Input High Voltage	0.7 x V_{DD}	+3.6	V
V_{IL}, Input Low Voltage	-0.3	0.3 x V_{DD}	V
External Clock Input (J4)			
V_{IH}, Input High Voltage	0.7 x V_{DD}	+3.6	V
V_{IL}, Input Low Voltage	-0.3	0.3 x V_{DD}	V
Analog Inputs (J1)			
Input Voltage, Differential	0	18.5	V_{PP}

3 Hardware Description and Configuration

This section provides hardware description and configuration information for the PCM4201EVM.

3.1 Power Supply Configuration

The PCM4201EVM requires three analog power supplies and one digital power supply for operation. The analog supplies are connected at terminal block J2, while the digital supply is connected at terminal block J6.

Analog supplies include +15V and –15V DC for powering the input buffer circuit, as well as +5.0V DC for powering the analog section of the PCM4201. All supplies should be rated for at least 500mA of output current.

The digital supply requires +5.0V DC and should be rated for at least 500mA of output current. The +5.0V supply is regulated to +3.3V DC by an onboard Texas Instruments REG1117 linear voltage regulator (U10), which is used to power the digital section of the PCM4201 and the majority of the support logic circuitry. The core logic and line driver sections of the AES3 transmitter (U7) utilize the +5.0V digital supply directly.

An optional external VDD power supply is supported at terminal block J6. Jumper JMP4 is utilized to select either the onboard +3.3V voltage regulator (U10) or an external power source. Shorting pins 1 and 2 together using the supplied jumper block selects the onboard +3.3V voltage regulator. Shorting pins 3 and 4 together will select the external supply (EXT VDD) on terminal block J6. Only one source may be selected at any time.

The External VDD may be operated as low as +1.8V. However, the DIT4096 transmitter will only operate at voltages down to +2.0V. Use the audio serial port interface at header J3 when operating VDD at voltages lower than +2.0V.

3.2 Analog Input

The PCM4201EVM includes a Neutrik combo XLR connector (J1), which accepts either a 3-pin male XLR or a 1/4-inch TRS phono plug. The analog input can accept up to a $18.5V_{PP}$ differential input signal. This signal is then attenuated by a factor of 3.7 by the input buffer circuit, which corresponds to the $5.0V_{PP}$ full scale differential input voltage for the PCM4201 analog input.

The input buffer circuit is comprised of an OPA2134 dual audio operational amplifier and associated passive components. The input buffer provides active attenuation and low-pass filtering for the analog input signal. The OPA2134 is biased to approximately +2.5V, with the bias voltage being derived from the +5V analog supply using a voltage divider.

The input buffer circuit may be configured to accept either dual or single supply op amps. Jumper JMP2 allows the –15V supply to be shorted to ground. The +15V may then be adjusted to the appropriate single supply voltage for the op amp. When using a single supply op amp, it may be necessary to change the values of the buffer feedback and input resistors in order to adjust the gain or attenuation to match the maximum input/output voltage swing allowed by the single supply configuration.

3.3 System Clock Configuration

The OSC1 and OSC2 elements of switch SW1 are utilized to select the system clock source for the PCM4201EVM. Table 2 summarizes the available options. The onboard oscillators support 44.1kHz, 48kHz, 88.2kHz, and 96kHz sampling rates for Master mode audio serial port operation. Alternatively, the external clock input (J4) may be used to supply the system clock from an external source, supporting additional sampling rates.

For Slave mode operation, the system clock is input at the SCKI pin of the audio serial port header (J3).

Table 2. System Clock Source Selection

OSC2	OSC1	SYSTEM CLOCK SOURCE
LO	HI	X1, 22.5792MHz
HI	LO	X2, 24.576MHz
LO	LO	External Clock from connector J3 or J4

3.4 Sampling Mode Selection

The PCM4201 supports three sampling modes, allowing the user to select the best power/performance combination for a given application.

The Normal Speed Low Power mode provides the lowest overall power dissipation while supporting sampling rates up to 54kHz. The modulator oversampling rate is $64f_S$ for this mode.

The Normal Speed High Performance mode provides the best dynamic performance at the expense of increased power dissipation. Sampling rates up to 54kHz are supported. The modulator oversampling rate is $128f_S$ for this mode, improving the overall dynamic range and THD+N when compared to the Low Power mode.

The Double Speed mode supports sampling frequencies up to 108kHz with power dissipation just slightly higher than the Normal Speed High Performance mode. The modulator oversampling rate is $64f_S$ for this mode.

The sampling mode is selected using the RATE VDD and RATE GND elements of switch SW1. Table 3 shows the settings required for each sampling mode.

Table 3. Sampling Mode Selection

RATE VDD	RATE GND	SAMPLING MODE
OFF	ON	Double Speed
ON	OFF	Normal Speed Low Power
OFF	OFF	Normal Speed High Performance

3.5 Digital High-Pass Filter

The PCM201 includes a digital high-pass filter, which is utilized to remove the DC component from the digitized signal. The high-pass filter is located at the output of the digital decimation filter in the overall A/D signal chain. The –3dB corner frequency of the high-pass filter is set by the following relationship:

$$F_{-3dB} = \frac{f_S}{48,000}, \text{ where } f_S = \text{ output sampling rate}$$

The digital high-pass filter may be enabled or disabled using the HPFD element of switch SW1. Table 4 summarizes the HPFD switch settings. There may be a small increase distortion for low frequency inputs (less than 100Hz) when the high-pass filter is enabled.

Table 4. Digital High-Pass Filter Configuration

HPFD	HIGH-PASS FILTER FUNCTION
LO	Enabled
HI	Disabled

3.6 Audio Serial Port Interface

The PCM4201EVM audio serial port is accessed at header J3. The port includes the audio bit clock (BCK), the audio frame synchronization clock (FSYNC), and the serial audio data (DATA). The system clock (SCKI) is also available at the audio serial port. The audio serial port may be operated in Slave or Master Mode.

In Slave Mode, the BCK, FSYNC, and SCKI clocks are inputs to the PCM4201EVM, and may be provided from an external source (DSP, FPGA, etc.) via header J3. The BCK and FSYNC clocks must be synchronous with one another and the audio data.

In Master Mode, the BCK, FSYNC, and SCKI clocks are outputs, being derived by the PCM4201 using the on-board crystal oscillators or external clock source applied at connector J4.

The Slave or Master Mode port configuration is programmed using the S/M element of switch SW1. Table 5 summarizes the available settings.

Table 5. Slave/Master Mode Configuration

S/M	AUDIO SERIAL PORT SLAVE/MASTER MODE
LO	Master
HI	Slave

Slave or Master Mode audio serial port operation also dictates the required rate of the system clock (SCKI) supported for various sampling modes. A summary of the supported rates is shown in Table 6 and Table 7.

Table 6. System Clock Rates for Master Mode Operation

SCKI RATE	SAMPLING MODE WITH MASTER MODE AUDIO SERIAL PORT
$512f_S$	Normal Speed Low Power
$512f_S$	Normal Speed High Performance
$256f_S$	Double Speed

Table 7. System Clock Rates for Slave Mode Operation

SCKI RATE	SAMPLING MODE WITH SLAVE MODE AUDIO SERIAL PORT
$256f_S$ or $512f_S$	Normal Speed Low Power
$256f_S$ or $512f_S$	Normal Speed High Performance
$256f_S$	Double Speed

3.7 Digital Interface Transmitter

A Texas Instruments DIT4096 digital interface transmitter provides an AES3-encoded output for the PCM4201EVM. The $\overline{\text{DIT}}$ and DITCLK elements of switch SW1 are utilized to configure the transmitter. The output of the transmitter is available at connector J5. This output is designed for use with 75Ω coaxial cable connections.

The transmitter is enabled using the $\overline{\text{DIT}}$ element of switch SW1. The $\overline{\text{DIT}}$ switch operation is summarized in Table 8.

Table 8. Digital Interface Transmitter Configuration

$\overline{DIT}$	DIGITAL INTERFACE TRANSMITTER
LO	Enabled
HI	Disabled

The audio data format for the transmitters is hardwired for 24-bit Left Justified data format. Only one channel (Channel A of the AES3 stream) will carry 24-bit linear PCM audio data.

Like the PCM4201, the DIT4096 transmitters must be configured for the proper Master (or System) clock frequency. The transmitter master clock is driven by the same source as the PCM4201 system clock, as described in Section 3.3 of this document. The transmitter master clock rate selection must match the system clock rate selection for the PCM4201. Table 9 summarizes the master clock rate options for the DIT4096 transmitter using the DITCLK element of switch SW1.

Table 9. Transmitter Master Clock Configuration

DITCLK	TRANSMITTER MASTER CLOCK RATE
LO	$256f_S$
HI	$512f_S$

3.8 Reset Operations

The PCM4201EVM includes two reset switches, SW2 and SW3. Both are momentary contact, normally open pushbutton switches. Switch SW2 provides the manual reset for the PCM4201, while switch SW3 provides the manual reset the DIT4096 digital interface transmitter.

The PCM4201 may be reset at any time by momentarily pressing and then releasing switch SW2. This generates a reset pulse and initiates a reset sequence for the device.

For the transmitter reset function, the output of the reset circuit is connected to the $\overline{RST}$ pin of the DIT4096 transmitter. The DIT4096 may be reset only when the $\overline{DIT}$ switch of SW1 is set LO by momentarily pressing and then releasing switch SW3. If the $\overline{DIT}$ switch is set HI, the output of the AND gate in the reset circuit is forced low, which will force the transmitter into power down mode. The transmitter reset circuit is shown in Figure 3.

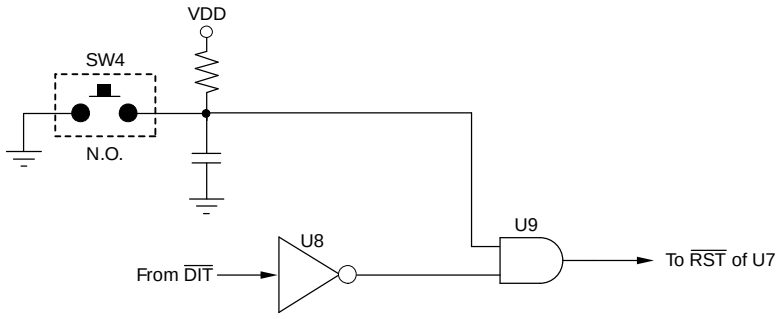


Figure 3. Transmitter Reset Circuitry

4 Schematic, PCB Layout, and Bill of Materials

This section provides the electrical schematic and physical layout information for the PCM4201EVM. The bill of materials (BOM) is included as a component reference.

Note:
Board layouts are not to scale. These figures are intended to show how the board is laid out; they are not intended to be used for manufacturing PCM4201EVM PCBs.

4.1 Schematic

The electrical schematic for the PCM4201EVM is shown in Figure 4. The components shown in the schematic are listed in Table 10 for reference.

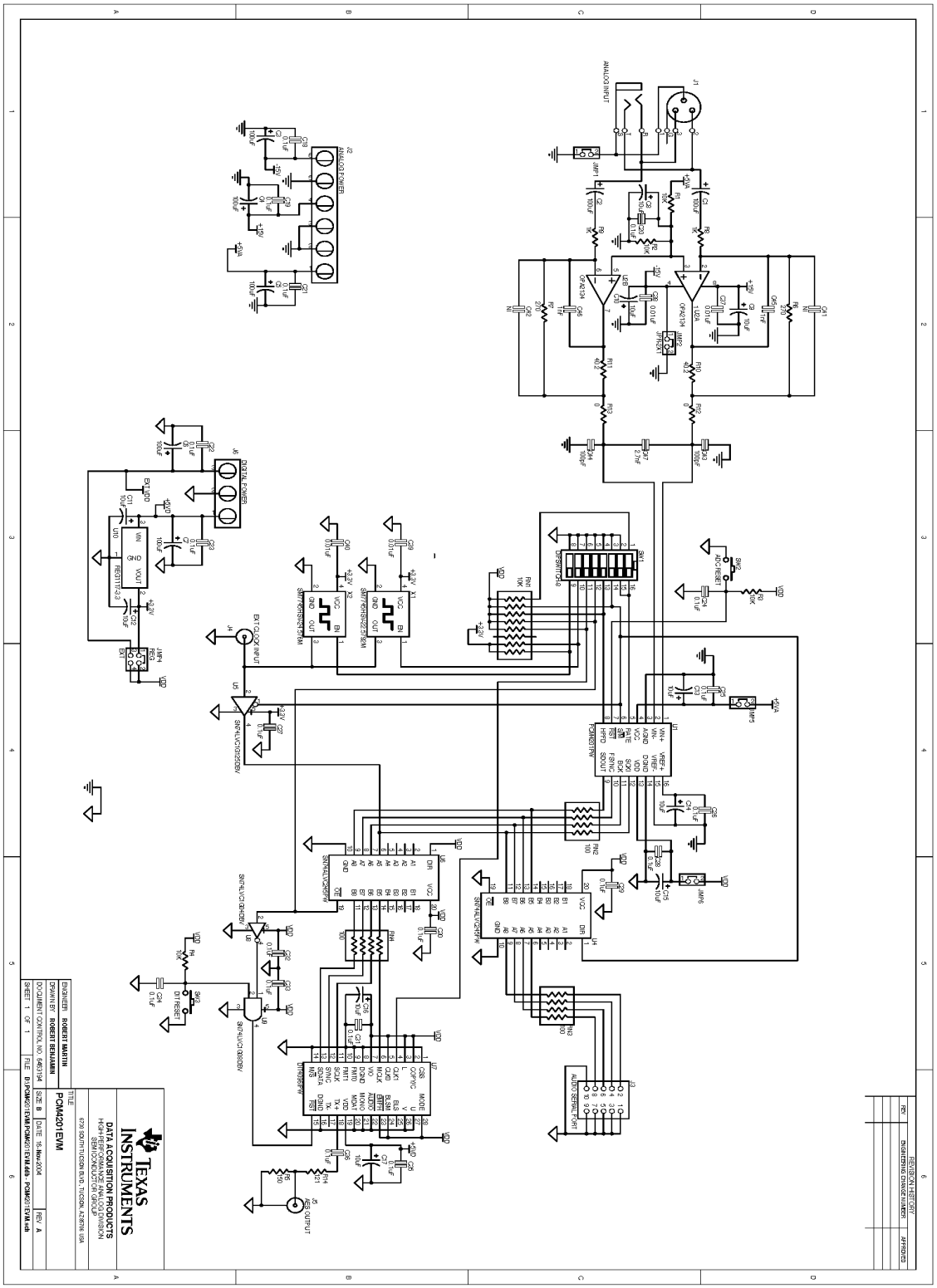


Figure 4. PCM4201EVM Schematic

4.2 PCB Layout

The PCB layout is a 4-layer printed circuit board (PCB) with the following layer structure:

- Layer 1: Top (component side)
- Layer 2: Ground plane
- Layer 3: Power
- Layer 4: Bottom (solder side)

Figure 5 through Figure 10 show the top and bottom side silkscreen images, along with top, ground plane, power, and bottom layers of the PCB.

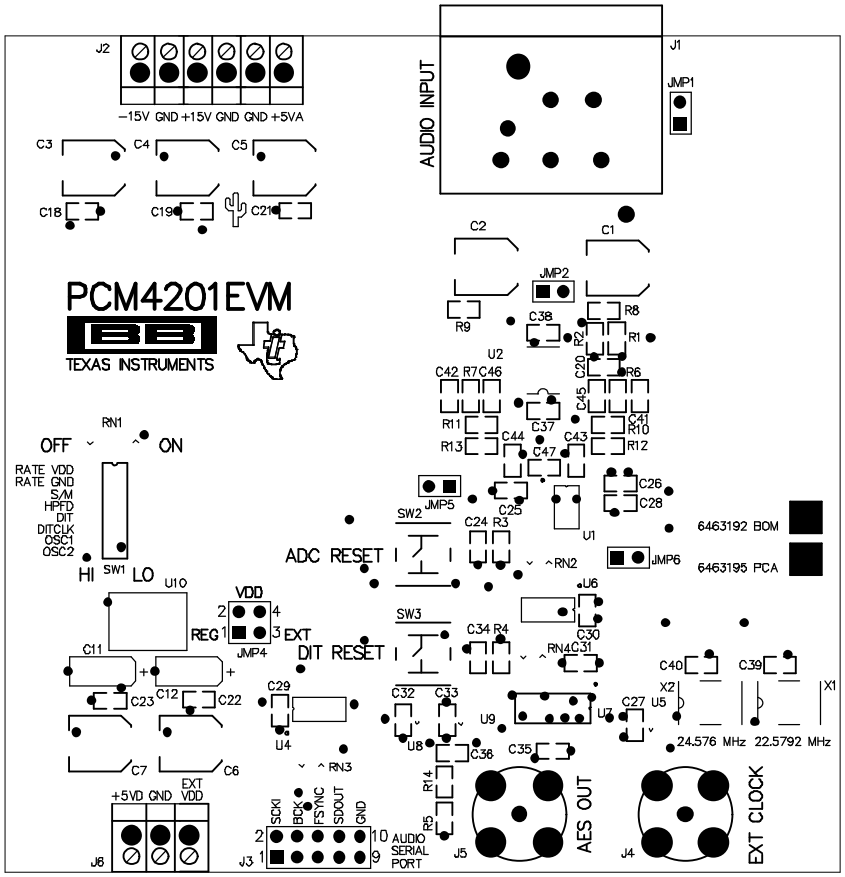


Figure 5. Top Side Silkscreen

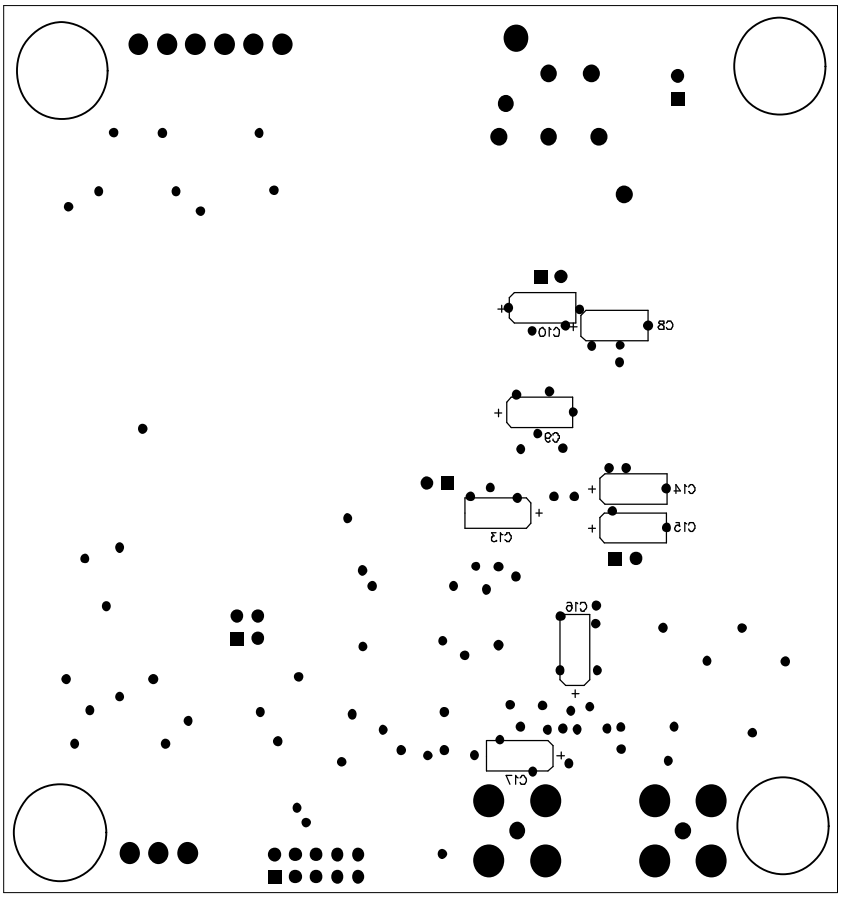


Figure 6. Bottom Side Silkscreen

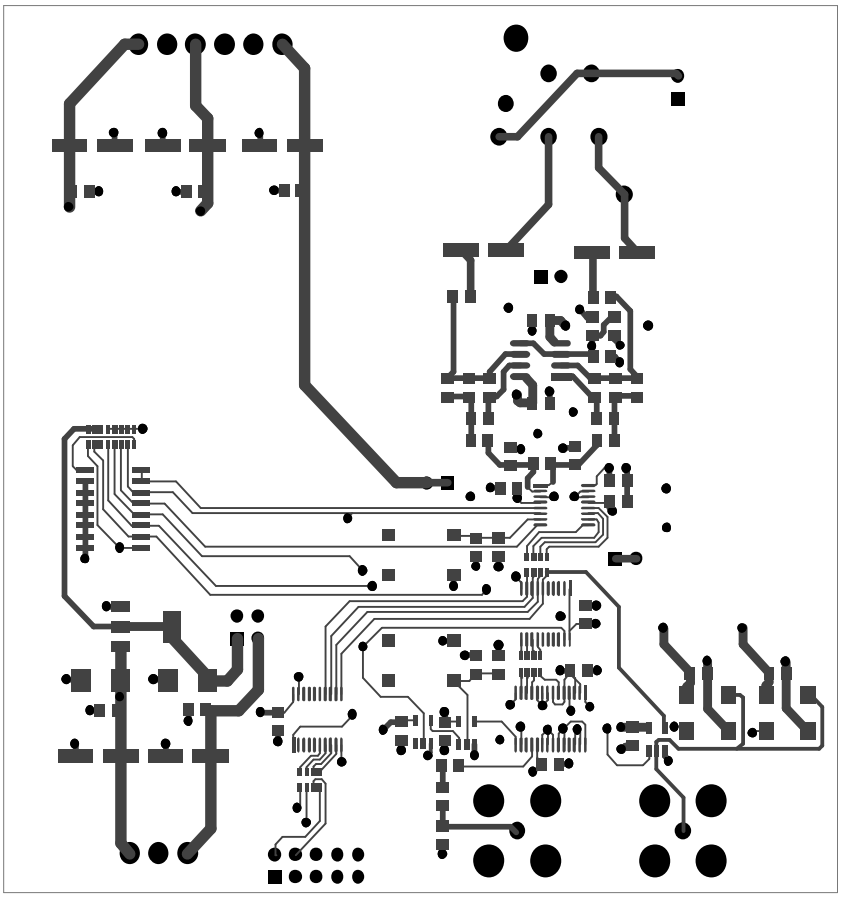


Figure 7. Top Layer (Component Side)

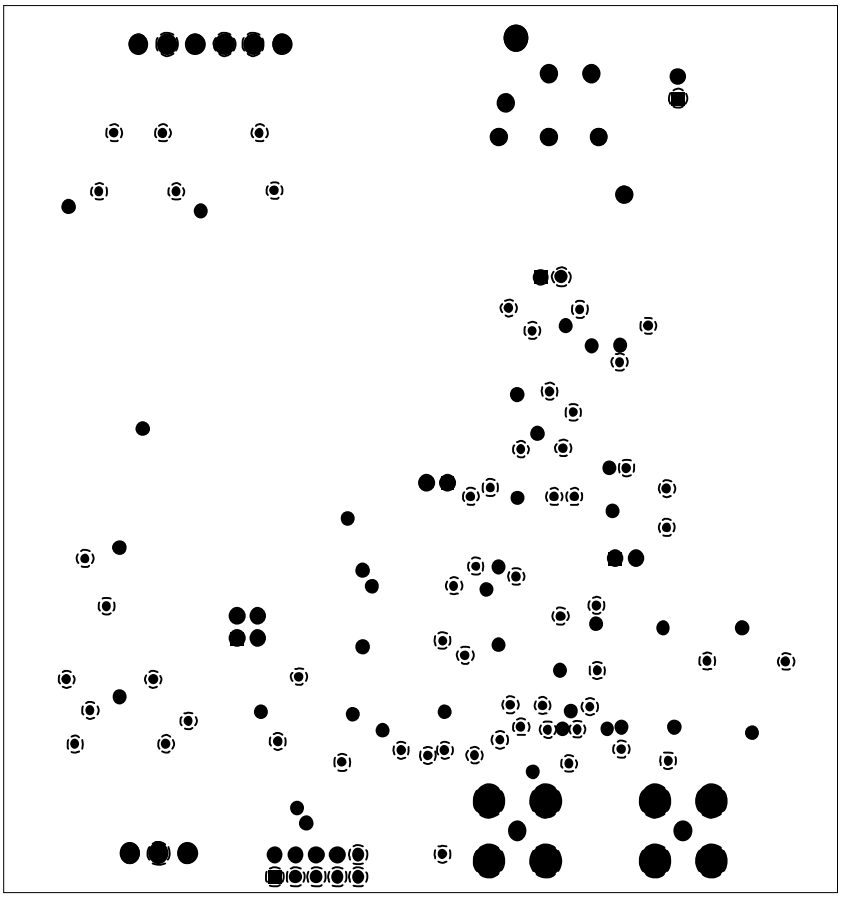


Figure 8. Ground Layer

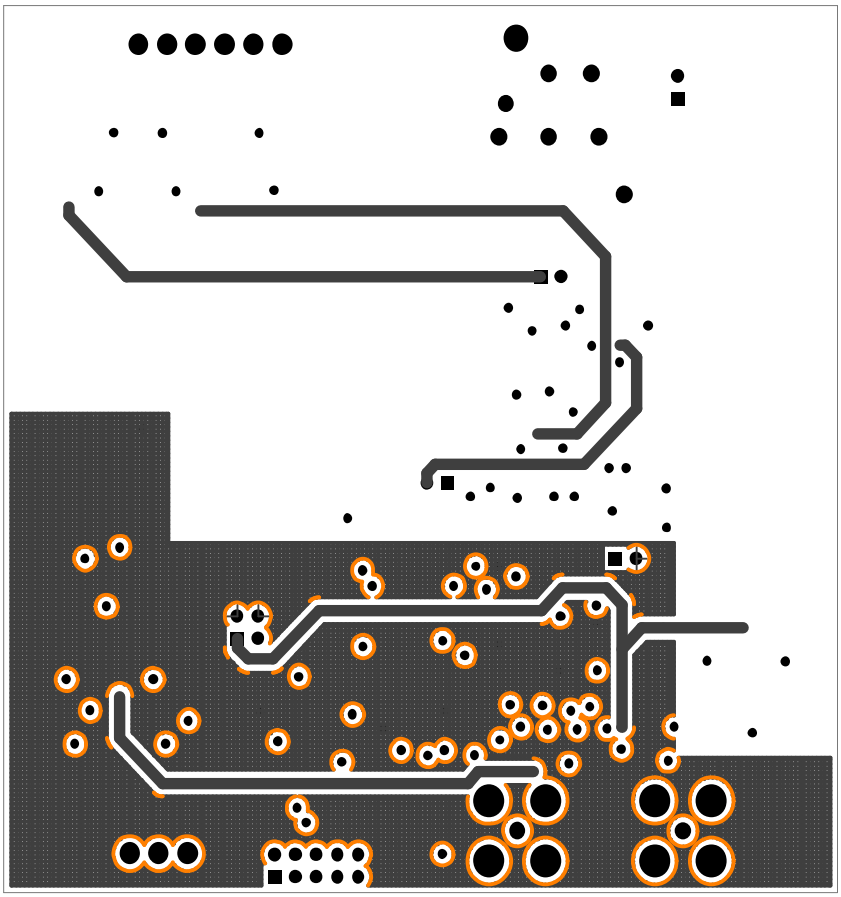


Figure 9. Power Plane Layer

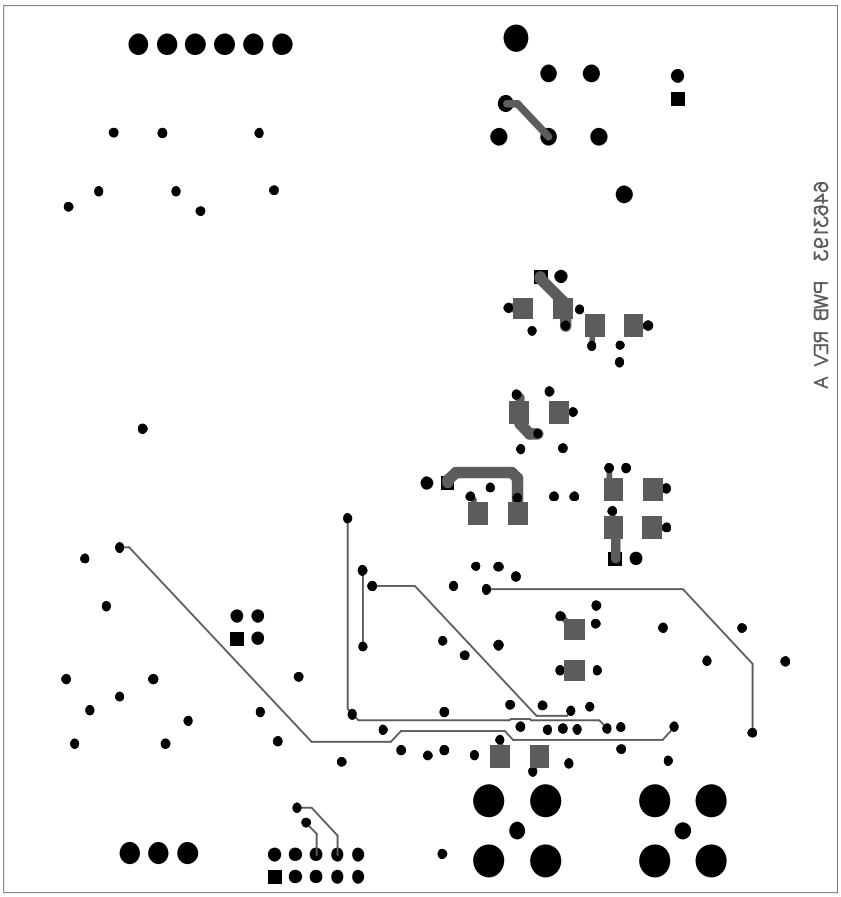


Figure 10. Bottom Layer (Solder Side)

4.3 Bill of Materials

The Bill of Materials, listing the components use in the assembly of the PCM4201EVM, is shown in Table 10.

Table 10. PCM4201EVM Bill of Materials

ITEM	VALUE	Ref Des	QTY PER BOARD	MFR	MFR PART NUMBER	DESCRIPTION
1	100pF	C43, C44	2	TDK	C2012C0G1H101J	Chip Capacitor, C0G Ceramic, 100pF ±5%, 50WV, Size = 0805
2	1000pF	C45, C46	2	TDK	C2012C0G1H102J	Chip Capacitor, C0G Ceramic, 1000pF ±5%, 50WV, Size = 0805
3	2700pF	C47	1	TDK	C2012C0G1H272J	Chip Capacitor, C0G Ceramic, 2700pF ±5%, 50WV, Size = 0805
4	N/A	C41, C42	N/A	N/A	N/A	Optional Component; Not Installed, Size = 0805
5	0.01μF	C37-C40	4	TDK	C2012X7R1H103K	Chip Capacitor, X7R Ceramic, 0.01μF ±10%, 50WV, Size = 0805
6	0.1μF	C18-C36	19	TDK	C2012X7R1H104K	Chip Capacitor, X7R Ceramic, 0.1μF ±10%, 50WV, Size = 0805
7	10μF	C8-C17	10	Kemet	T494C106K025AS	Chip Capacitor, Low ESR Tantalum, 10μF ±10%, 25WV, Size = C
8	100μF	C1-C7	7	Panasonic	EEV-FK1E101XP	Capacitor, SMT Aluminum Electrolytic, 100μF ±20%, 25WV
9		J1	1	Neutrik	NCJ6FI-H	Combo Connector, Female XLR and TRS, Vertical PC Mount
10		J2	1	Weidmuller	996772	3.5mm PCB Terminal Block, 6 poles
11		J3	1	Samtec	TSW-105-07-G-D	Terminal Strip, 10-pin (5x2)
12		J4, J5	2	Amp	414305-1	RCA Phono Jack, Black Shell
13		J6	1	Weidmuller	1699680000	3.5mm PCB Terminal Block, 3 poles
14		JMP1, JMP2	2	Samtec	TSW-102-07-G-S	Terminal Strip, 2-pin (2x1)
15		JMP4	1	Samtec	TSW-102-07-G-D	Terminal Strip, 4-pin (2x2)
16	0	R12, R13	2	Panasonic	ERJ-6GEY0R00V	Chip Resistor, 0Ω, Shunt, Size = 0805
17	40.2	R10, R11	2	Panasonic	ERJ-6ENF40R2V	Chip Resistor, Thick Film, 1% Tolerance, 40.2Ω, 1/10W, Size = 0805
18	121	R14	1	Panasonic	ERJ-6ENF1210V	Chip Resistor, Thick Film, 1% Tolerance, 121Ω, 1/10W, Size = 0805
19	150	R5	1	Panasonic	ERJ-6ENF1500V	Chip Resistor, Thick Film, 1% Tolerance, 150Ω, 1/10W, Size = 0805
20	270	R6, R7	2	Panasonic	ERA-6YEB271V	Chip Resistor, Metal Film, 0.1% Tolerance, 270Ω, 1/10W, Size = 0805
21	1K	R8, R9	2	Panasonic	ERA-6YEB102V	Chip Resistor, Metal Film, 0.1% Tolerance, 1kΩ, 1/10W, Size = 0805
22	10K	R1-R4	4	Panasonic	ERJ-6ENF1002V	Chip Resistor, Thick Film, 1% Tolerance, 10kΩ, 1/10W, Size = 0805
23	10K	RN1	1	CTS	742C163103J	Thick Film Chip Resistor Array, 10kΩ, 16-Terminal, 8 Resistors, Isolated
24	100	RN2, RN2, RN4	3	CTS	742C083101J	Thick Film Chip Resistor Array, 100Ω, 16-Terminal, 8 Resistors, Isolated
25		SW1	1	ITT Industries/ C&K	TDA08H0SK1	DIP Switch, 8 Element, Half-Pitch, Surface-Mount, Tape Sealed
26		SW2, SW3	2	Omron	B3S-1000	Momentary Tact Switch, SMT without Ground Terminal
27		U1	1	Texas Instruments	PCM4201PW	Single Channel 24-Bit Audio A/D Converter

Table 10. PCM4201EVM Bill of Materials (continued)

28		U2	1	Texas Instruments	OPA2134UA	Dual Audio Op Amp
29		U3	N/A	N/A	N/A	Component Removed, Reference Maintained
30		U4, U6	2	Texas Instruments	SN74ALVC245PW	Octal Bus Transceiver w/ Tri-State Outputs
31		U5	1	Texas Instruments	SN74LVC1G125DBV	Single Non-Inverting Buffer w/ Tri-State Output
32		U7	1	Texas Instruments	DIT4096IPW	96kHz Digital Audio Transmitter
33		U8	1	Texas Instruments	SN74LVC1G04PW	Single Inverter
34		U9	1	Texas Instruments	SN74LVC1G08DBV	Single 2-Input Positive AND Gate
35		U10	1	Texas Instruments	REG1117-3.3	Linear Voltage Regulator, +3.3V
36		X1	1	Pletronics	SM7745HSV-22.5792M	+3.3V Surface Mount Clock Oscillator CMOS Output with Active High Enable 22.5792MHz ±50ppm
37		X2	1	Pletronics	SM7745HSV-24.576M	+3.3V Surface Mount Clock Oscillator CMOS Output with Active High Enable 24.576MHz ±50ppm
38			2	Samtec	SNT-100-BK-G-H	Shorting Blocks
39			4	3M Bumpon	SJ-5003	Self-Adhesive Rubber Feet

FCC Warnings

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

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EVM WARNINGS AND RESTRICTIONS

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Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 37°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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