24-BIT, 96-kHz STEREO AUDIO CODEC WITH MICROPHONE AMPLIFIER, BIAS, MUXTIPLEXER, AND PGA

FEATURES

- **Microphone Amplifier and Bias**
  - **Monaural Microphone Amplifier: 34-dB Gain at Differential Input**
  - **Microphone Bias: 1 mA at 3.75 V**
- **Multiplexer and PGA**
  - **Multiplex of Stereo Single-Ended Line Inputs and Monaural Microphone Amplifier**
  - **0.1 Vrms to 1.5 Vrms Full-Scale Input Range**
  - **22-kΩ Input Resistance at 0.1-Vrms Input**
  - **20 dB to –4 dB/range, 1 dB/step PGA**
- **Reference Output: ±10 mA at 2.5 V**
- **24-Bit Delta-Sigma ADC and DAC**
- **Stereo ADC:**
  - **Full-Scale Input: 3 Vp-p**
  - **Antialiasing Filter Included**
  - **1/64 Decimation Filter:**
    - **Pass-Band Ripple: ±0.05 dB**
    - **Stop-Band Attenuation: –65 dB**
  - **On-Chip High-Pass Filter: 0.91 Hz at f_S = 48 kHz**
  - **High Performance:**
    - **THD+N: –94 dB (Typical)**
    - **SNR: 101 dB (Typical)**
    - **Dynamic Range: 101 dB (Typical)**
- **Stereo DAC:**
  - **Single-Ended Voltage Output: 4 Vp-p**
  - **Analog Low-Pass Filter Included**
  - **×8 Oversampling Digital Filter:**
    - **Pass-Band Ripple: ±0.03 dB**
    - **Stop-Band Attenuation: –50 dB**
  - **High Performance:**
    - **THD+N: –97 dB (Typical)**
    - **SNR: 105 dB (Typical)**
    - **Dynamic Range: 104 dB (Typical)**
- **S/PDIF Output for DAC Digital Input**
- **Multiple Functions With I^2C Interface:**
  - **Digital De-Emphasis: 32-, 44.1-, 48-kHz**
  - **Zipper-Noise-Free Digital Attenuation and Soft Mute for DAC**
  - **HPF Bypass Control for ADC**
  - **S/PDIF Output Control**
  - **Power Down: ADC/DAC Independently**
- **External Power-Down Pin:**
  - **ADC/DAC Simultaneously**
- **Audio Data Format: 24-Bit I^2S Only**
- **Sampling Rate:**
  - **16–96 kHz for Both ADC and DAC**
- **System Clock: 256 f_S Only**
- **Dual Power Supplies:**
  - **5 V for Analog and 3.3 V for Digital**
- **Package: VQFN-32**

DESCRIPTION

The PCM3052A is a low-cost, single-chip, 24-bit stereo audio codec (ADC and DAC) with single-ended analog voltage input and output. It also has an analog front end consisting of a 34-dB microphone amplifier, microphone bias generator, 2 stereo multiplexers, and a wide-range PGA. Analog-to-digital converters (ADCs) employ delta-sigma modulation with 64-times oversampling. On the other hand, digital-to-analog converters (DACs) employ modulation with 64- and 128-times oversampling. ADCs include a digital decimation filter with a high-pass filter, and DACs include an 8-times oversampling digital interpolation filter. The PCM3052A has many functions which are controlled using the I^2C interface: DAC digital de-emphasis, digital attenuation, soft mute etc. The PCM3052A also has an S/PDIF output pin for the DAC digital input. The power-down mode, which works on ADCs and DACs simultaneously, is provided by an external pin. The PCM3052A is suitable for a wide variety of cost-sensitive PC audio (recorder and player) applications where good performance is required. The PCM3052A is fabricated using a highly advanced CMOS process and is available in a small 32-pin VQFN package.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		PCM3052A
Supply voltage	$V_{CC}1$, $V_{CC}2$, $V_{CC}3$	–0.3 V to 6.5 V
	V_{DD}	–0.3 V to 4 V
Supply voltage differences	$V_{CC}1$, $V_{CC}2$, $V_{CC}3$	±0.1 V
Ground voltage differences	AGND1, AGND2, AGND3, DGND	±0.1 V
Digital input voltage	$\overline{PDWN}$, DIN, SCKI, SDA, SCL, ADR, I2CEN	–0.3 V to 6.5 V
	DOUT, LRCK, BCK, DOUTS	– 0.3 V to (V_{DD} + 0.3 V) < 4 V
Analog input voltage	$V_{IN}L$, $V_{IN}R$, $V_{REF}1$, $V_{REF}2$, REFO, ATEST, L/$\overline{M}$, $V_{OUT}R$, $V_{OUT}L$, V_{COM}, MINP, MINM, MBIAS	–0.3 V to (V_{CC} + 0.3 V) < 6.5 V
Input current (any pins except supplies)		±10 mA
Ambient temperature under bias		–40°C to 125°C
Storage temperature		–55°C to 150°C
Junction temperature		150°C
Lead temperature (soldering)		260°C, 5 s
Package temperature (reflow, peak)		260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Digital supply voltage		3	3.3	3.6	V
V_{CC}	Analog supply voltage		4.5	5	5.5	V
	Digital input logic family			TTL compatible		
	Digital input clock frequency	System clock	4		25	MHz
		Sampling clock	16		96	kHz
	Analog input voltage	Line input, full scale, PGA = 0 dB		3		Vp-p
		Microphone input, full scale, PGA = 0 dB		30		mVp-p
	Digital output load capacitance				20	pF
	Line output load resistance		5			kΩ
	Line output load capacitance				50	pF
	Microphone bias output load resistance		3.75			kΩ
	Reference output load resistance		250			Ω
T_A	Operating free-air temperature		–40		85	°C

ELECTRICAL CHARACTERISTICS

All specifications at T_A = 25°C, $V_{CC}1 = V_{CC}2 = V_{CC}3$ = 5 V, V_{DD} = 3.3 V, f_S = 48 kHz, SCKI = 256 f_S, 24-bit data, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT/OUTPUT – DATA FORMAT						
	Audio data interface format			I^2S		
	Audio data bit length			24		Bits
	Audio data format			MSB-first, 2s complement		
f_S	Sampling frequency, ADC		16	48	96	kHz
	Sampling frequency, DAC		16	48	96	kHz
	System clock frequency	256 f_S	4		25	MHz
INPUT LOGIC						
V_{IH} (1)	Input logic level		2		V_{DD}	VDC
V_{IL} (1)					0.8	
V_{IH} (2) (3)	Input logic level		2		5.5	VDC
V_{IL} (2) (3)					0.8	
I_{IH} (2)	Input logic current	$V_{IN} = V_{DD}$			±10	µA
I_{IL} (2)		V_{IN} = 0 V			±10	
I_{IH} (1)(3)	Input logic current	$V_{IN} = V_{DD}$		65	100	µA
I_{IL} (1) (3)		V_{IN} = 0 V			±10	
OUTPUT LOGIC						
V_{OH} (4)	Output logic level	I_{OUT} = –4 mA	2.8			VDC
V_{OL} (4) (5)		I_{OUT} = 4 mA			0.5	
V_{OH} (6)		I_{OUT} = –0.3 mA	4.5			VDC
V_{OL} (6)		I_{OUT} = 0.3 mA			0.5	
MICROPHONE AMPLIFIER						
	Input level	Single-ended		1	15	mVrms
	Gain	Single-ended		40		dB
	Input resistance	Single-ended	5	6		kΩ
	Frequency response	–3 dB		20		kHz
	SNR	1-kHz, 100-mVrms output		59		dB
	THD+N	1-kHz, 1-Vrms output		–77		dB
MICROPHONE BIAS GENERATOR						
	Output voltage	I_{OUT} = –1 mA	0.75 $V_{CC}1$ – 0.15	0.75 $V_{CC}1$	0.75 $V_{CC}1$ + 0.15	V
	Output source current				1	mA
	Output impedance			48		Ω
	Output noise voltage	100 Hz–20 kHz, with 10-µF decoupling		1.8		µVrms
REFERENCE OUTPUT						
	Output voltage	I_{OUT} = ±10 mA	0.5 $V_{CC}1$ – 0.15	0.5 $V_{CC}1$	0.5 $V_{CC}1$ + 0.15	V
	Output source/sink current				10	mA
	Output impedance			6		Ω
	Output noise voltage	100 Hz–20 kHz, with 10-µF decoupling		1.8		µVrms

(1) Pins 10, 11: LRCK, BCK (Schmitt-trigger input with 50-kΩ typical internal pulldown resistor)
(2) Pins 12, 17, 18, 19, 21: DIN, SCKI, SDA, SCL, I2CEN (Schmitt-trigger input, 5-V tolerant)
(3) Pins 9, 20 : $\overline{\text{PDWN}}$, ADR (Schmitt-trigger input with 50-kΩ typical internal pulldown resistor, 5-V tolerant).
(4) Pins 13, 14: DOUT, DOUTS
(5) Pin 18: SDA (Open-drain LOW output)
(6) Pin 3: L/$\overline{\text{M}}$

ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, $V_{CC}1 = V_{CC}2 = V_{CC}3$ = 5 V, V_{DD} = 3.3 V, f_S = 48 kHz, SCKI = 256 f_S, 24-bit data, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AFE MULTIPLEXER						
	Input channel			2		CH
	Input range for full scale	$V_{IN}L$, $V_{IN}R$	0.1	1	1.5	Vrms
	Input Impedance	$V_{IN}L$, $V_{IN}R$	22	143		kΩ
	Antialiasing filter frequency response	–3 dB, PGA gain = 0 dB		300		kHz
	Input center voltage (VREF1)			0.5 $V_{CC}1$		V
AFE PGA						
	Gain range		–4	0	20	dB
	Gain step			1		dB
	Monotonicity			Ensured		
ADC CHARACTERISTICS						
	Resolution			24		Bits
	Full-scale input voltage	$V_{IN}L$, $V_{IN}R$ at PGA gain = 0 dB		0.6 $V_{CC}1$		Vp-p
DC Accuracy						
	Gain mismatch, channe-to-channel	Full scale input, $V_{IN}L$, $V_{IN}R$		±1	±2	% of FSR
	Gain error	Full scale input, $V_{IN}L$, $V_{IN}R$		±2	±4	% of FSR
	Bipolar-zero error	HPF bypass, $V_{IN}L$, $V_{IN}R$		±2		% of FSR
Dynamic Performance (7)						
THD+N	Total harmonic distortion + noise	f_S = 48 kHz, V_{IN} = –0.5 dB		–94	–88	dB
		f_S = 96 kHz, V_{IN} = –0.5 dB		–89		
		f_S = 48 kHz, V_{IN} = –60 dB		–38		
		f_S = 96 kHz, V_{IN} = –60 dB		–38		
	Dynamic range	f_S = 48 kHz, A-weighted	95	101		dB
		f_S = 96 kHz, A-weighted		101		
S/N	Signal-to-noise ratio	f_S = 48 kHz, A-weighted	95	101		dB
		f_S = 96 kHz, A-weighted		101		
	Channel separation (between L-ch and R-ch of line-in)	f_S = 48 kHz	92	98		dB
		f_S = 96 kHz		99		
	Channel separation (between microphone and line-in)	f_S = 48 kHz	92	98		dB
		f_S = 96 kHz		99		
Digital Filter Performance						
	Pass band	±0.05 dB			0.454 f_S	Hz
	Stop band		0.583 f_S			Hz
	Pass-band ripple				±0.05	dB
	Stop-band attenuation	0.583 f_S	–65			dB
	Delay time			17.4/f_S		s
	HPF frequency response	–3 dB		0.019 f_S		MHz
DAC CHARACTERISTICS						
	Resolution			24		Bits
DC Accuracy						
	Gain mismatch, channel-to-channel			±1	±2	% of FSR
	Gain error			±2	±6	% of FSR
	Bipolar zero error			±1		% of FSR

(7) f_{IN} = 1 kHz, using System Two™ audio measurement system by Audio Precision™ in the RMS mode with 20-kHz LPF and 400-Hz HPF in the calculation, at PGA gain = 0 dB, for $V_{IN}L$ and $V_{IN}R$.

ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, $V_{CC}1 = V_{CC}2 = V_{CC}3$ = 5 V, V_{DD} = 3.3 V, f_S = 48 kHz, SCKI = 256 f_S, 24-bit data, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dynamic Performance (8)						
THD+N	Total harmonic distortion + noise	f_S = 48 kHz, V_{OUT} = 0 dB		–97	–90	dB
		f_S = 96 kHz, V_{OUT} = 0 dB		–99		
		f_S = 48 kHz, V_{OUT} = –60 dB		–42		
		f_S = 96 kHz, V_{OUT} = –60 dB		–43		
	Dynamic range	f_S = 48 kHz, EIAJ, A-weighted	98	104		dB
		f_S = 96 kHz, EIAJ, A-weighted		106		
S/N	Signal-to-noise ratio	f_S = 48 kHz, EIAJ, A-weighted	99	105		dB
		f_S = 96 kHz, EIAJ, A-weighted		106		
	Channel separation	f_S = 48 kHz	97	103		dB
		f_S = 96 kHz		104		
Analog Output						
	Output voltage			0.8 $V_{CC}2$		Vp-p
	Center voltage			0.5 $V_{CC}2$		V
	Load impedance	AC coupling	5			kΩ
	LPF frequency response	f = 20 kHz		–0.03		dB
		f = 40 kHz		–0.20		
Digital Filter Performance						
	Pass band	±0.03 dB			0.454 f_S	Hz
	Stop band		0.546 f_S			Hz
	Pass-band ripple				±0.03	dB
	Stop-band attenuation	0.546 f_S	–50			dB
	Delay time			20/f_S		s
	De-emphasis error			±0.1		dB
POWER SUPPLY REQUIREMENTS						
$V_{CC}1$ $V_{CC}2$ $V_{CC}3$	Voltage range		4.25	5	5.5	VDC
V_{DD}			3	3.3	3.6	
I_{CC} (9)	Supply current	f_S = 48 kHz		39	50	mA
		f_S = 96 kHz		41		
		Full power down (10)		300		µA
I_{DD}		f_S = 48 kHz		10	15	mA
		f_S = 96 kHz		19		
		Full power down (10)		90		µA
	Power dissipation	Operation, f_S = 48 kHz		228	300	mW
		Operation, f_S = 96 kHz		268		
		ADC operation at f_S = 48 kHz/DAC power down		180		
		ADC power down/DAC operation at f_S = 48 kHz		63		
		Full power down (10)		1.8		

(8) f_{OUT} = 1 kHz, using System Two audio measurement system by Audio Precision in the RMS mode with 20-kHz LPF and 400-Hz HPF.
(9) $I_{CC} = I_{CC}1 + I_{CC}2 + I_{CC}3$
(10) Halt SCKI, BCK, LRCK.

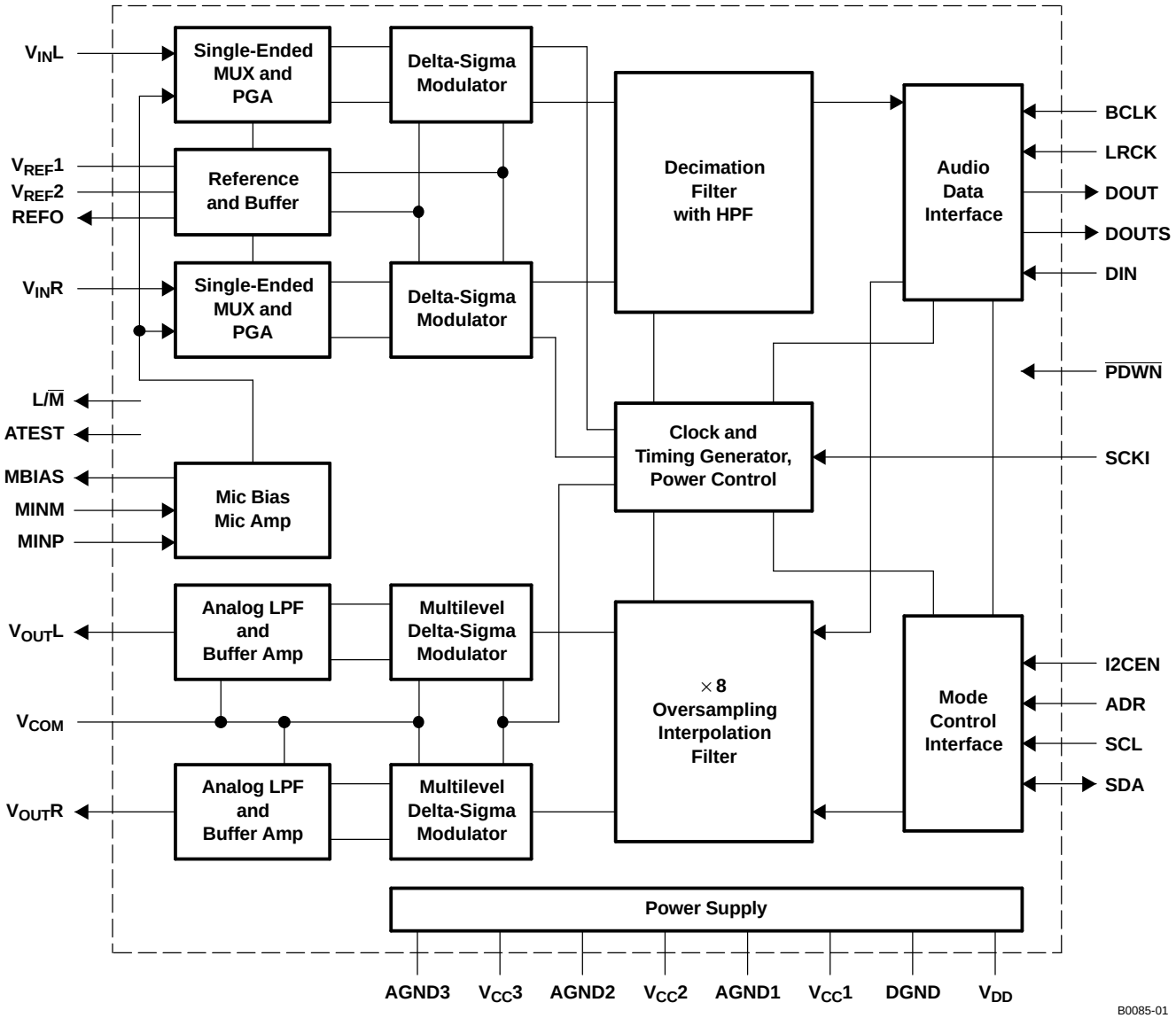
ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, $V_{CC}1 = V_{CC}2 = V_{CC}3$ = 5 V, V_{DD} = 3.3 V, f_S = 48 kHz, SCKI = 256 f_S, 24-bit data, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE RANGE						
	Operation temperature		–40		85	°C
θ_{JA}	Thermal resistance			100		°C/W

DEVICE INFORMATION

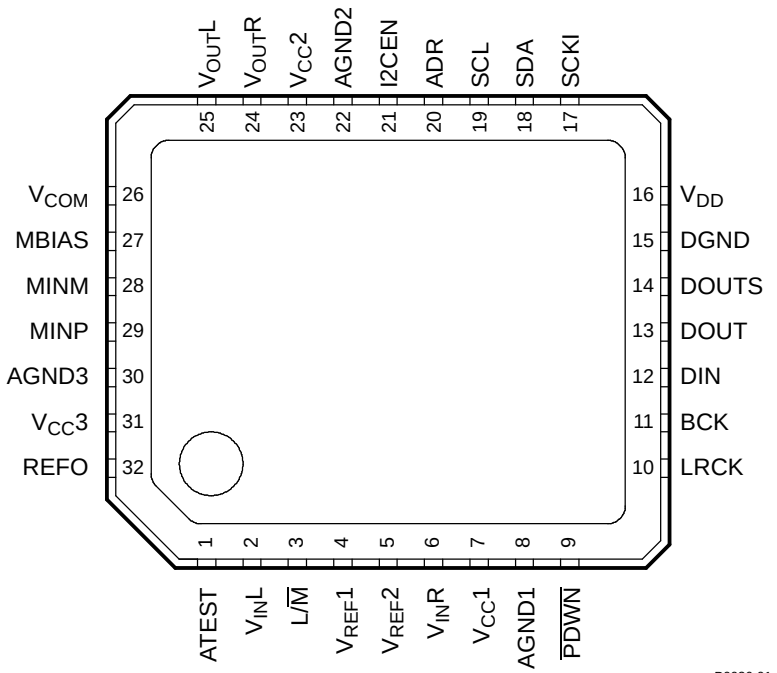
BLOCK DIAGRAM



DEVICE INFORMATION (continued)

PIN ASSIGNMENTS

RTF PACKAGE
(TOP VIEW)



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TERMINAL FUNCTIONS

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ADR	20	I	Mode control address select input (1)
AGND1	8		ADC analog ground
AGND2	22		DAC analog ground
AGND3	30		Microphone amplifier and bias analog ground
ATEST	1	O	Analog test, must be open
DGND	15		Digital ground
BCK	11	I	Audio data bit clock input (2)
DIN	12	I	Audio data digital input (3)
DOUT	13	O	Audio data digital output
DOUTS	14	O	S/PDIF data digital output
I2CEN	21	I	Mode control enable/disable input, active HIGH (3)
L/$\overline{M}$	3	O	ADC line/microphone select indicator
LRCK	10	I	Audio data latch enable input (2)
MBIAS	27	O	Microphone bias output/decoupling, 0.75 $V_{CC}1$
MINM	28	I	Microphone amplifier input to ADC, inverting
MINP	29	I	Microphone amplifier input to ADC, non-inverting
$\overline{PDWN}$	9	I	ADC and DAC power down control input, active LOW(1)
REFO	32	O	Reference output / decoupling, 0.5 $V_{CC}1$

(1) Schimtt-trigger input with 50-kΩ typical internal pulldown resistor, 5-V tolerant
(2) Schimtt-trigger input with 50-kΩ typical internal pulldown resistor
(3) Schimtt-trigger input, 5-V tolerant

DEVICE INFORMATION (continued)

TERMINAL FUNCTIONS (continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
SCKI	17	I	System clock input, 256 f_S (3)
SCL	19	I	Mode control clock input (3)
SDA	18	I/O	Mode control data input/output (4)
$V_{CC}1$	7		ADC analog power supply, 5 V
$V_{CC}2$	23		DAC analog power supply, 5 V
$V_{CC}3$	31		Microphone amplifier and bias analog power supply, 5 V
V_{COM}	26		DAC common voltage decoupling, 0.5 $V_{CC}2$
V_{DD}	16		Digital power supply, 3.3 V
$V_{IN}L$	2	I	Line input to ADC, L-channel
$V_{IN}R$	6	I	Line input to ADC, R-channel
$V_{OUT}L$	25	O	Analog output from DAC, L-channel
$V_{OUT}R$	24	O	Analog output from DAC, R-channel
$V_{REF}1$	4		ADC reference 1 voltage output, 0.5 $V_{CC}1$
$V_{REF}2$	5		ADC reference 2 voltage decoupling, $V_{CC}1$

(4) Schimtt-trigger input/open-drain LOW output, 5-V tolerant

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTER (ADC SECTION)

All specifications at T_A = 25°C, $V_{CC}1 = V_{CC}2 = V_{CC}3$ = 5 V, V_{DD} = 3.3 V, f_S = 48 kHz, SCKI = 256f_S, 24-bit data, unless otherwise noted.

DIGITAL FILTER

OVERALL CHARACTERISTICS

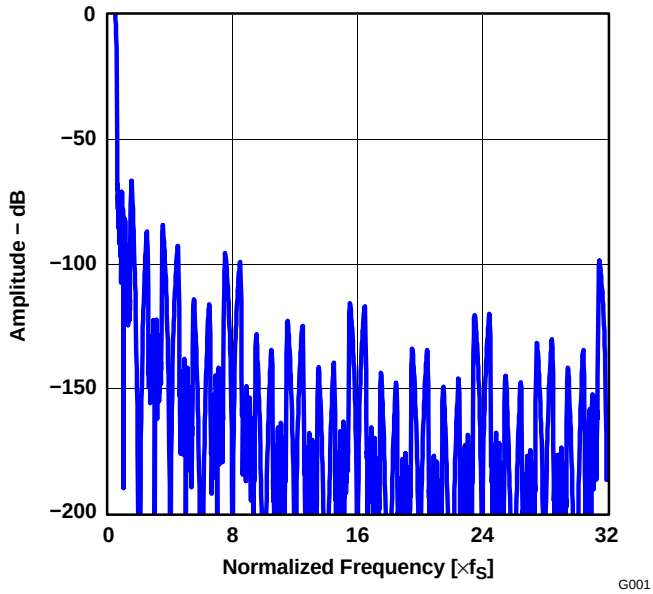


Figure 1.

STOP-BAND ATTENUATION CHARACTERISTICS

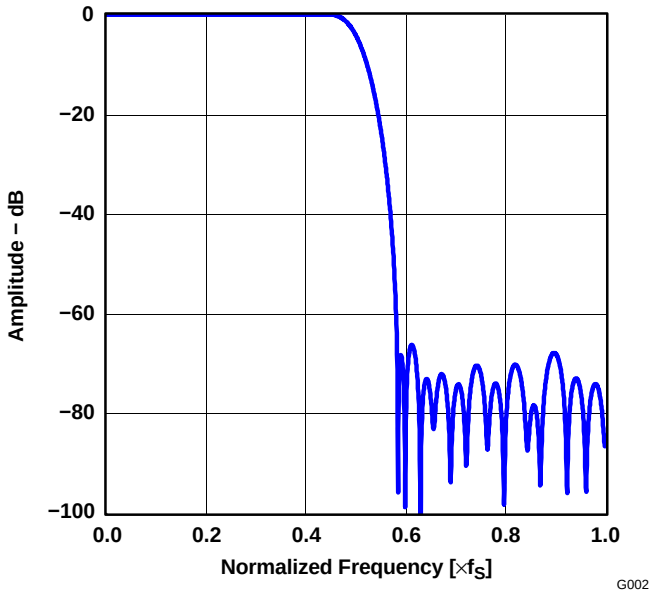


Figure 2.

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTER (ADC SECTION) (continued)

All specifications at T_A = 25°C, $V_{CC}1 = V_{CC}2 = V_{CC}3$ = 5 V, V_{DD} = 3.3 V, f_S = 48 kHz, SCKI = 256f_S, 24-bit data, unless otherwise noted.

PASS-BAND RIPPLE CHARACTERISTICS

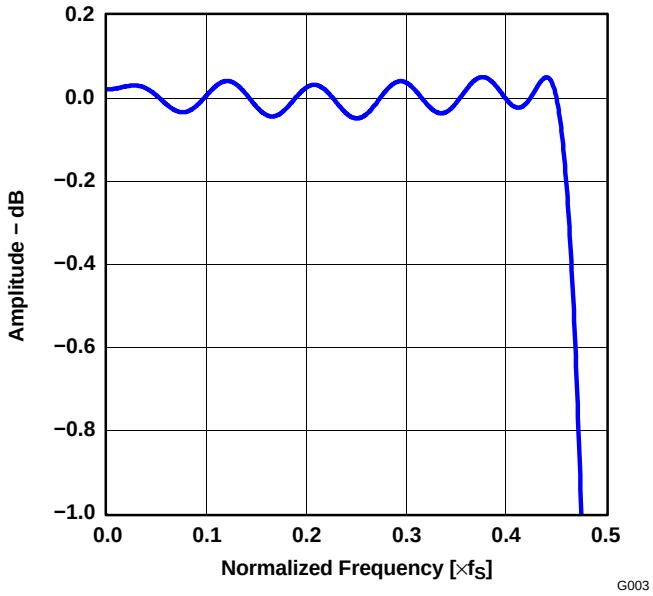


Figure 3.

TRANSITION BAND CHARACTERISTICS

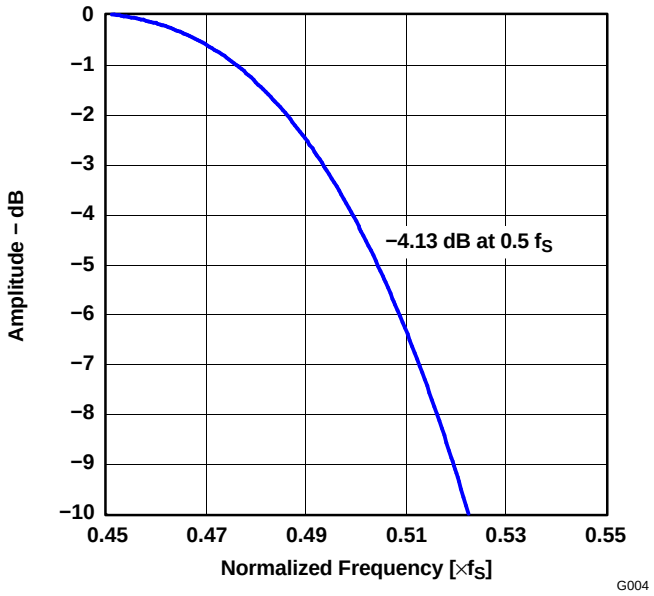


Figure 4.

HIGH-PASS FILTER STOP-BAND CHARACTERISTICS

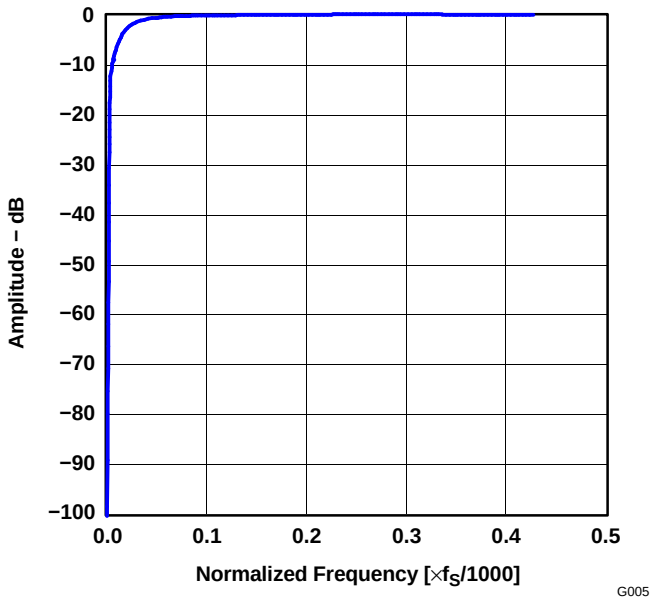


Figure 5.

HIGH-PASS FILTER PASS-BAND CHARACTERISTICS

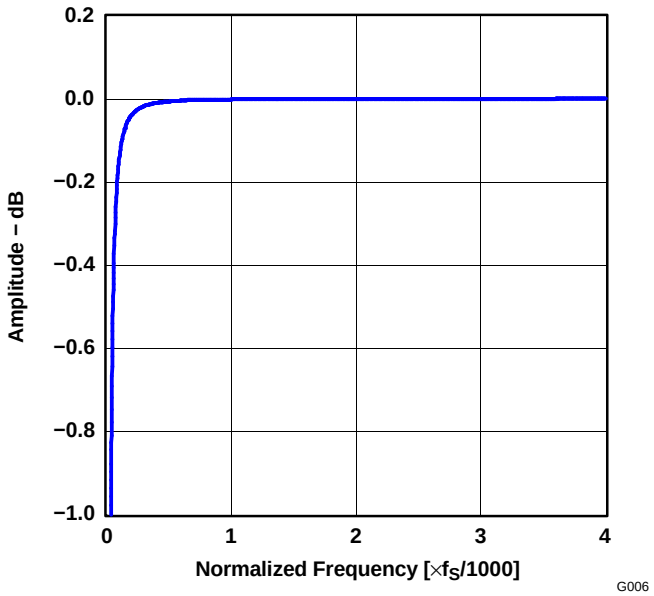


Figure 6.

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTER (ADC SECTION) (continued)

All specifications at T_A = 25°C, $V_{CC}1 = V_{CC}2 = V_{CC}3$ = 5 V, V_{DD} = 3.3 V, f_S = 48 kHz, SCKI = 256f_S, 24-bit data, unless otherwise noted.

ANALOG FILTER (Line Input, PGA Gain = 0 dB)

ANTIALIASING FILTER STOP-BAND CHARACTERISTICS

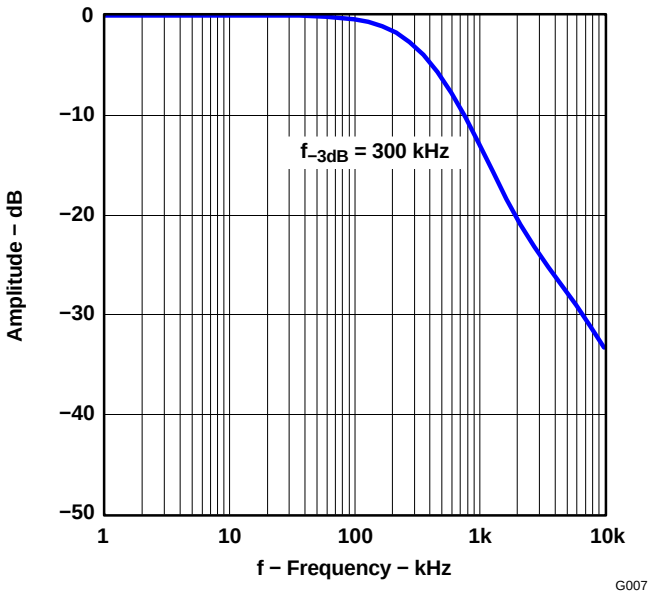


Figure 7.

ANTIALIASING FILTER PASS-BAND CHARACTERISTICS

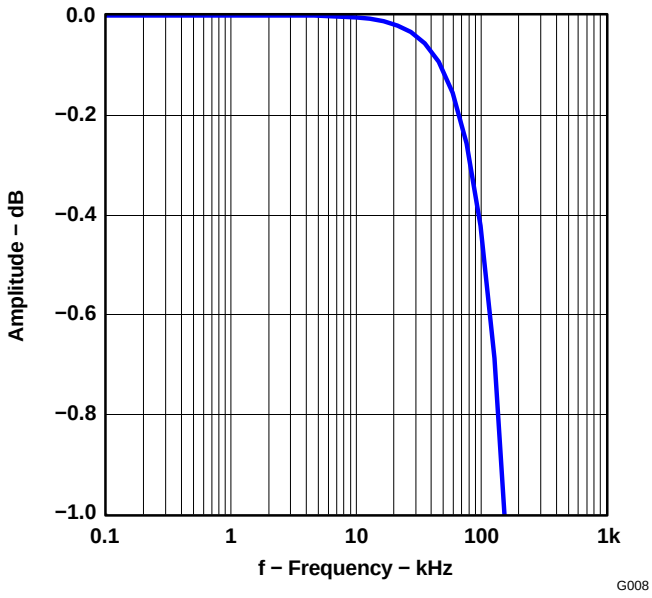


Figure 8.

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTER (DAC SECTION)

All specifications at T_A = 25°C, $V_{CC}1 = V_{CC}2 = V_{CC}3$ = 5 V, V_{DD} = 3.3 V, f_S = 48 kHz, SCKI = 256f_S, 24-bit data, unless otherwise noted.

DIGITAL FILTER

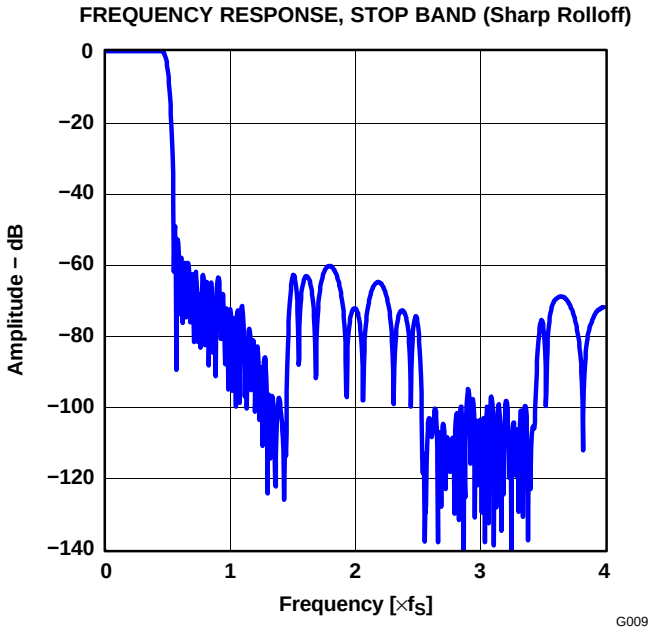


Figure 9.

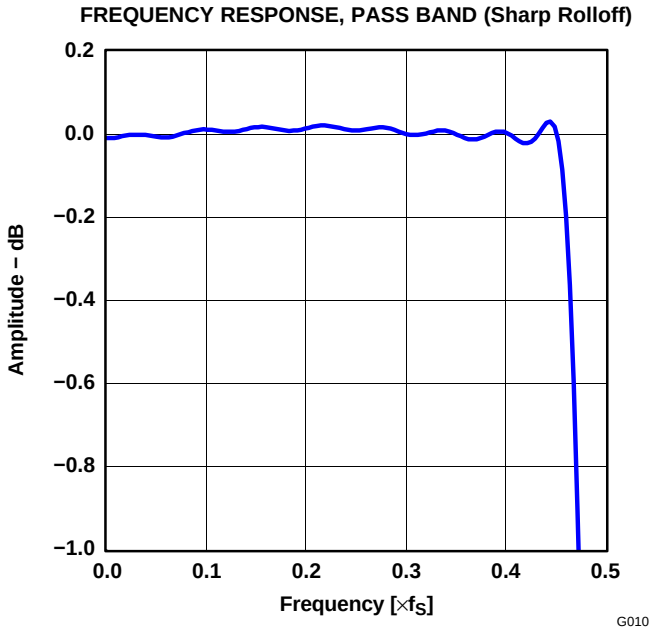
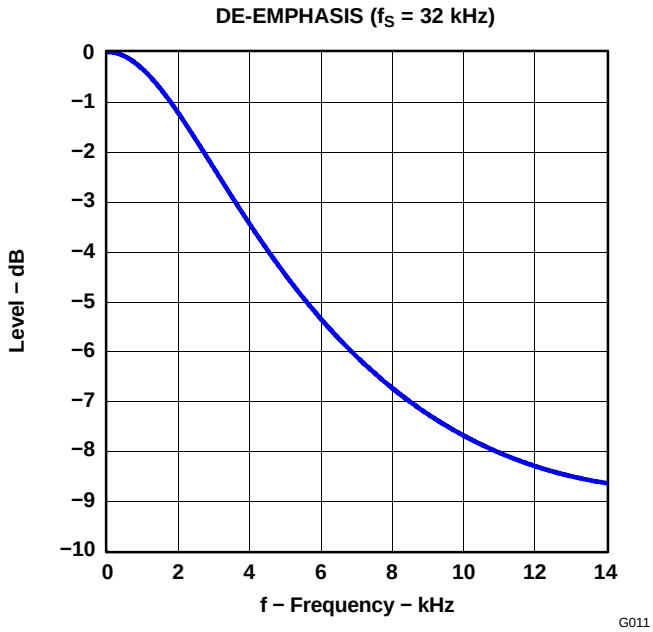


Figure 10.



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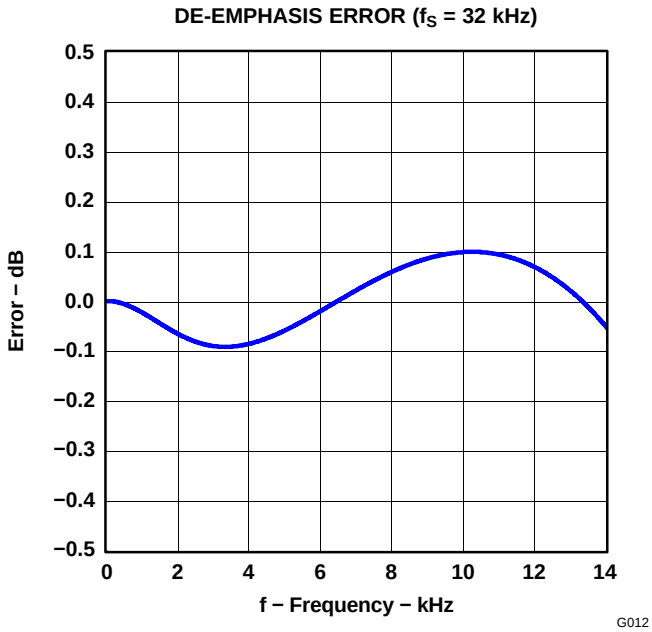


Figure 12.

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTER (DAC SECTION) (continued)

All specifications at T_A = 25°C, $V_{CC}1 = V_{CC}2 = V_{CC}3$ = 5 V, V_{DD} = 3.3 V, f_S = 48 kHz, SCKI = 256f_S, 24-bit data, unless otherwise noted.

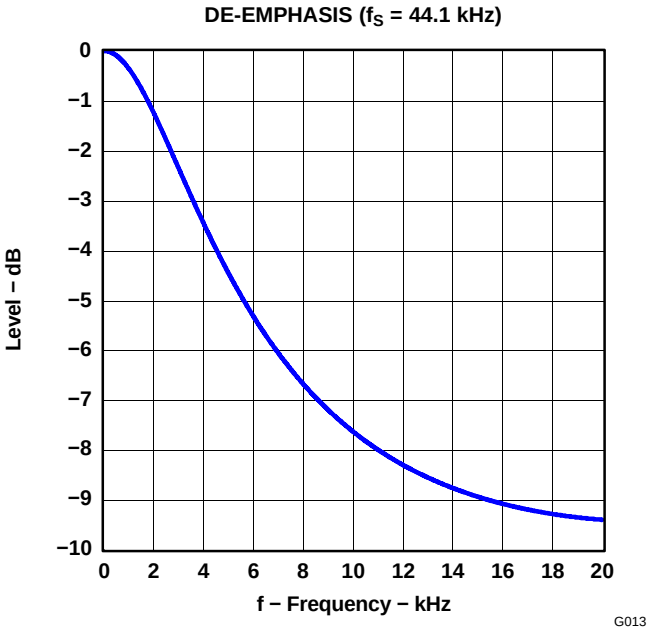
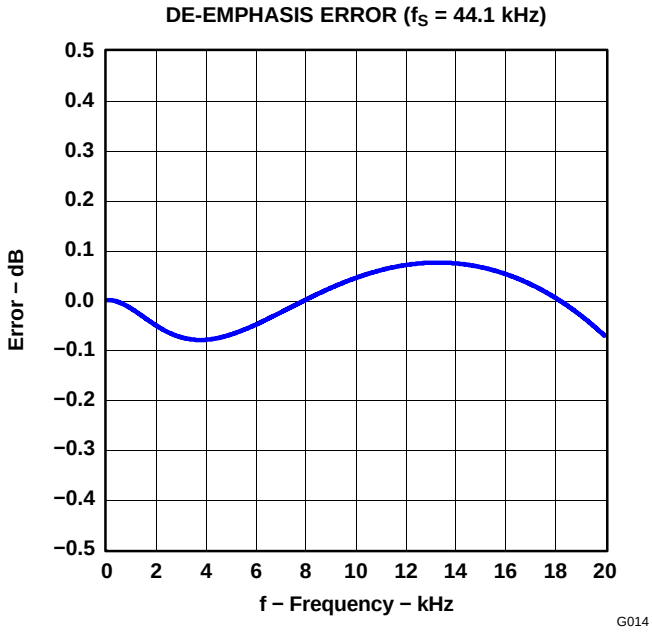


Figure 13.



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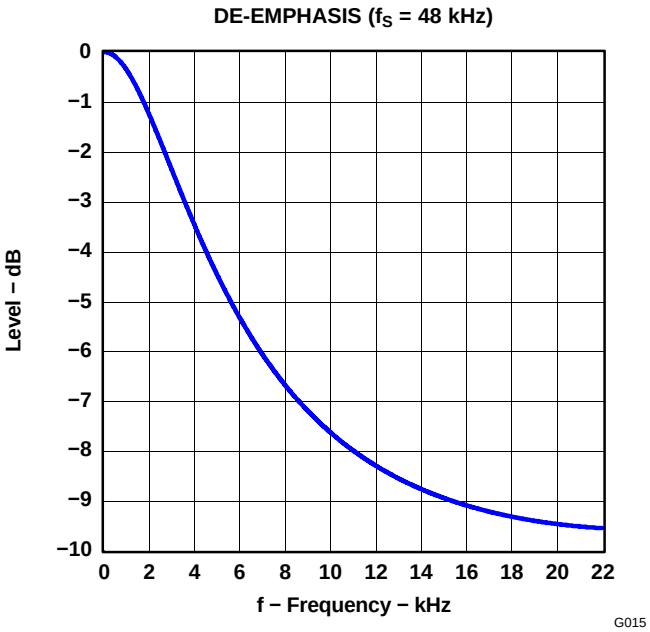

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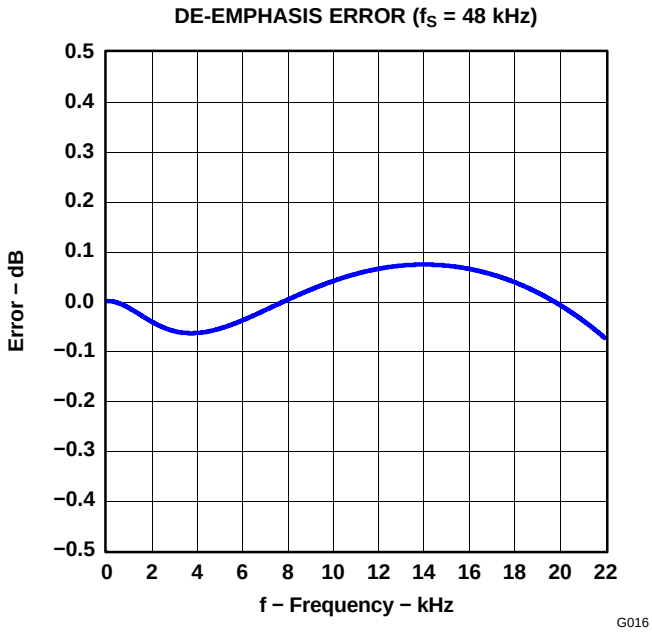


Figure 16.

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTER (DAC SECTION) (continued)

All specifications at T_A = 25°C, $V_{CC}1 = V_{CC}2 = V_{CC}3$ = 5 V, V_{DD} = 3.3 V, f_S = 48 kHz, SCKI = 256f_S, 24-bit data, unless otherwise noted.

ANALOG FILTER

STOP-BAND CHARACTERISTICS (1 kHz–10 MHz)

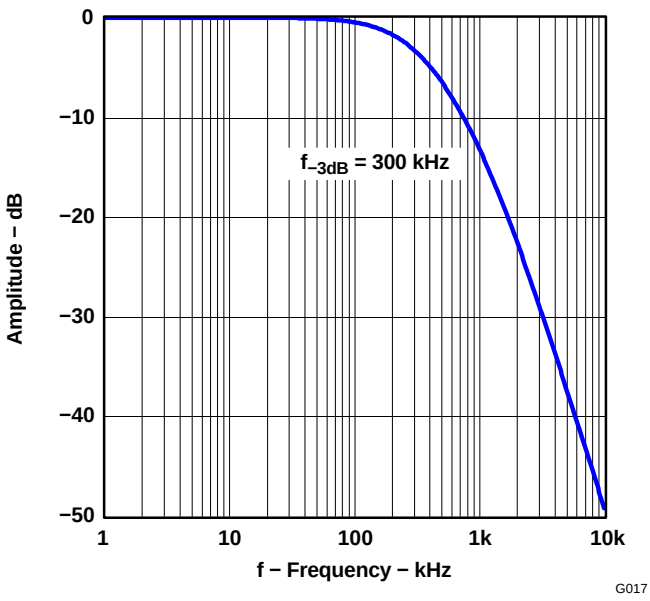


Figure 17.

PASS-BAND CHARACTERISTICS (100 Hz–1 MHz)

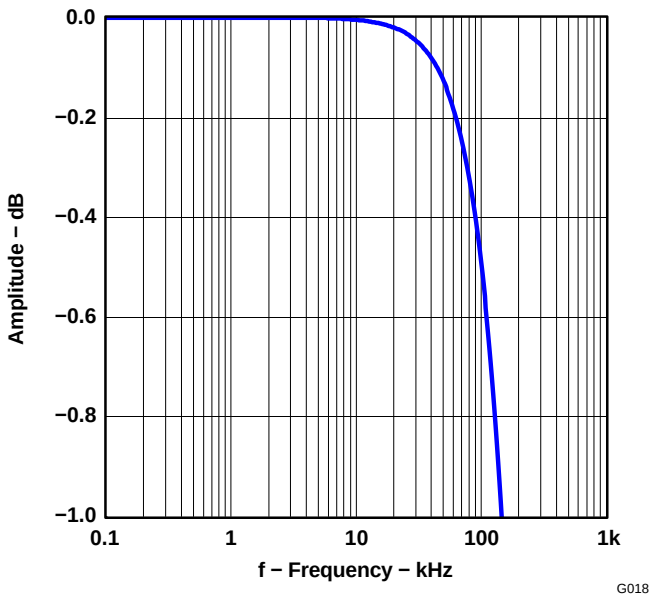


Figure 18.

TYPICAL PERFORMANCE CURVES (ADC SECTION)

All specifications at T_A = 25°C, $V_{CC}1 = V_{CC}2 = V_{CC}3$ = 5 V, V_{DD} = 3.3 V, f_S = 48 kHz, SCKI = 256 f_S, 24-bit data, unless otherwise noted.

LINE INPUT (at PGA Gain = 0 dB)

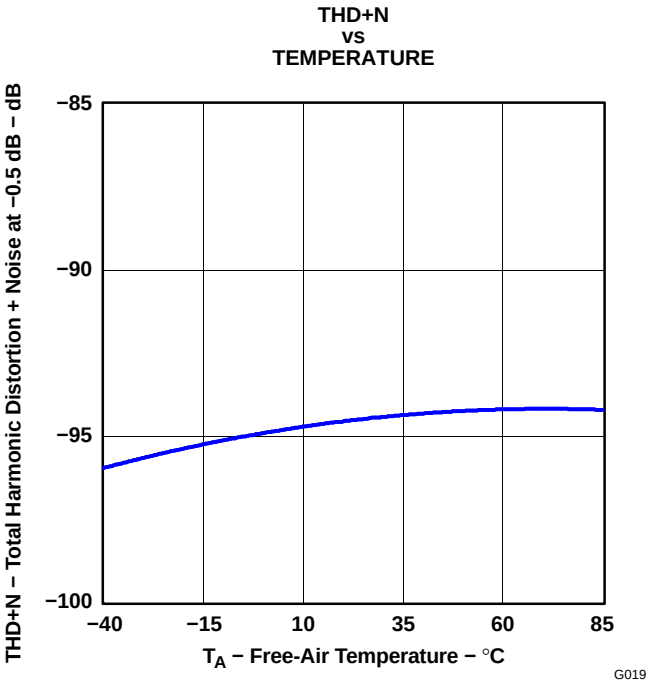


Figure 19.

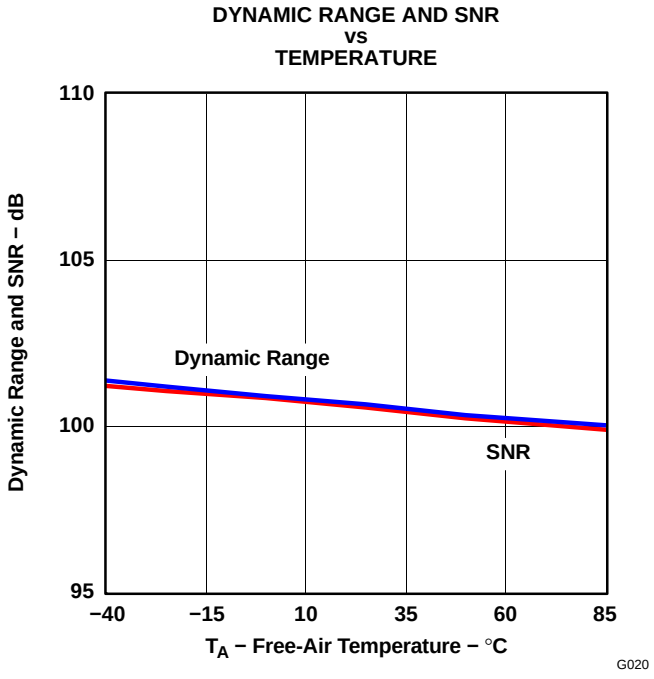


Figure 20.

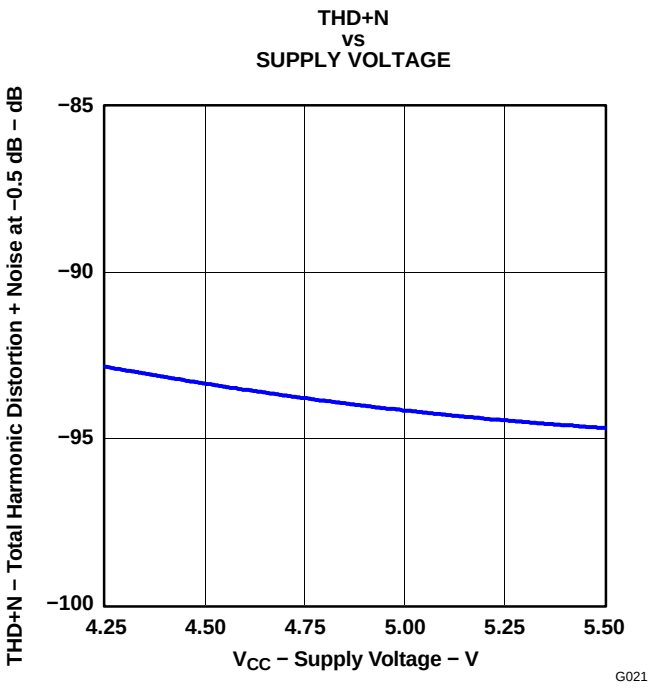


Figure 21.

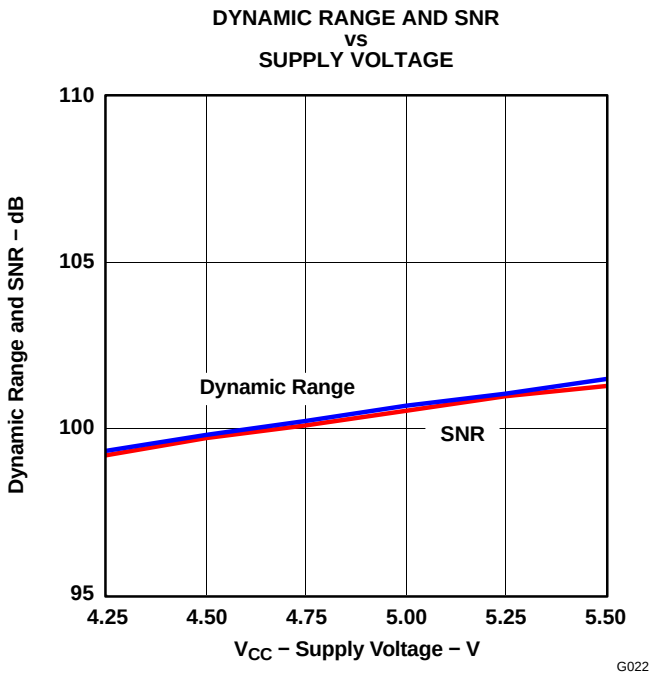


Figure 22.

TYPICAL PERFORMANCE CURVES (ADC SECTION) (continued)

All specifications at T_A = 25°C, $V_{CC}1 = V_{CC}2 = V_{CC}3$ = 5 V, V_{DD} = 3.3 V, f_S = 48 kHz, SCKI = 256 f_S, 24-bit data, unless otherwise noted.

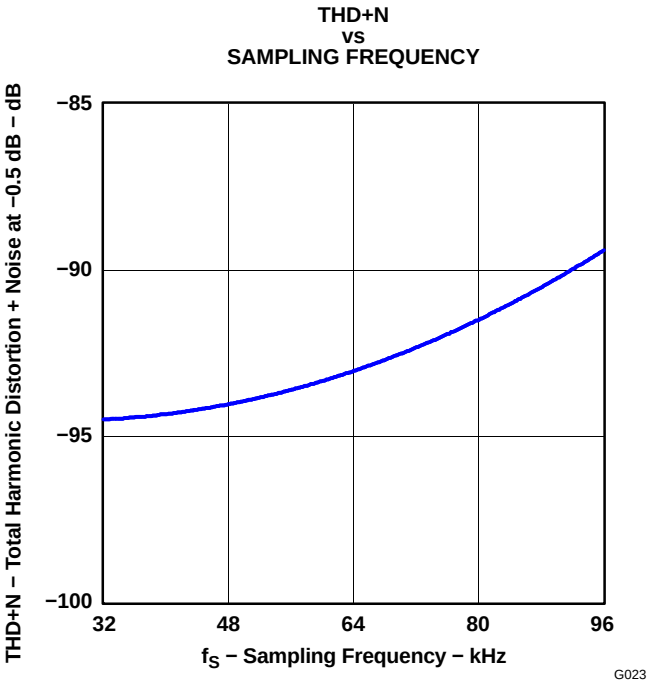


Figure 23.

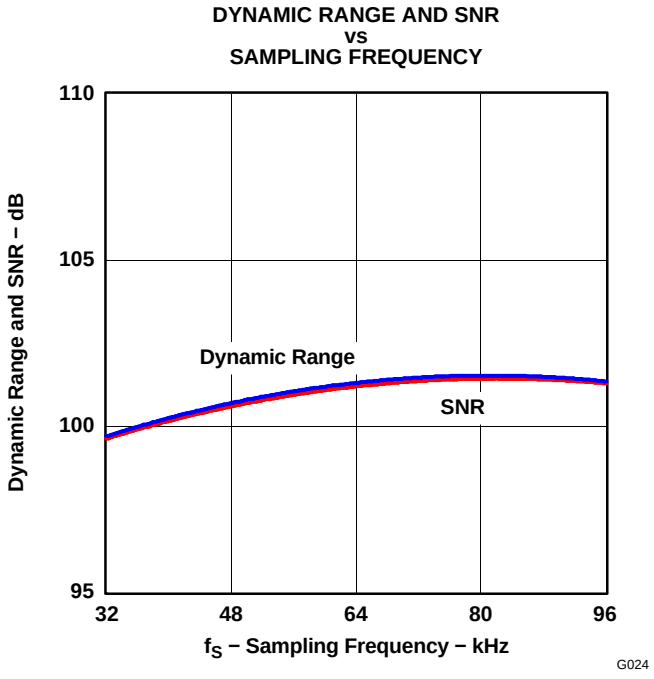


Figure 24.

TYPICAL PERFORMANCE CURVES (DAC SECTION)

All specifications at T_A = 25°C, $V_{CC}1 = V_{CC}2 = V_{CC}3$ = 5 V, V_{DD} = 3.3 V, f_S = 48 kHz, SCKI = 256 f_S, 24-bit data, unless otherwise noted.

THD+N
vs
TEMPERATURE

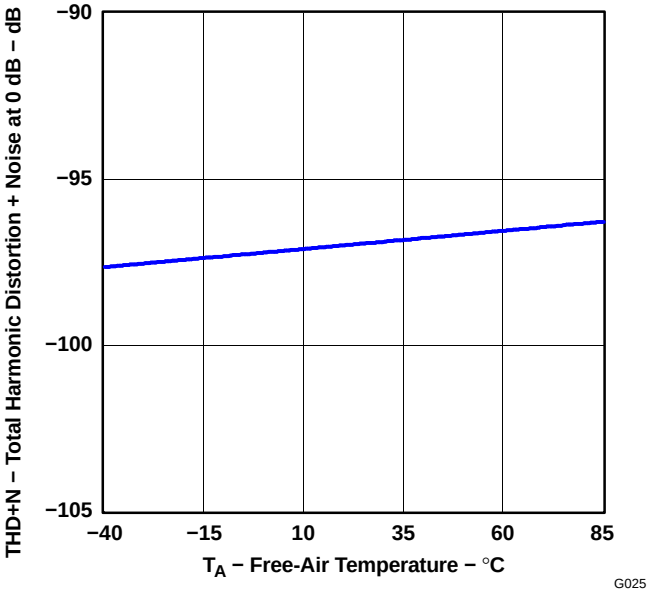


Figure 25.

DYNAMIC RANGE AND SNR
vs
TEMPERATURE

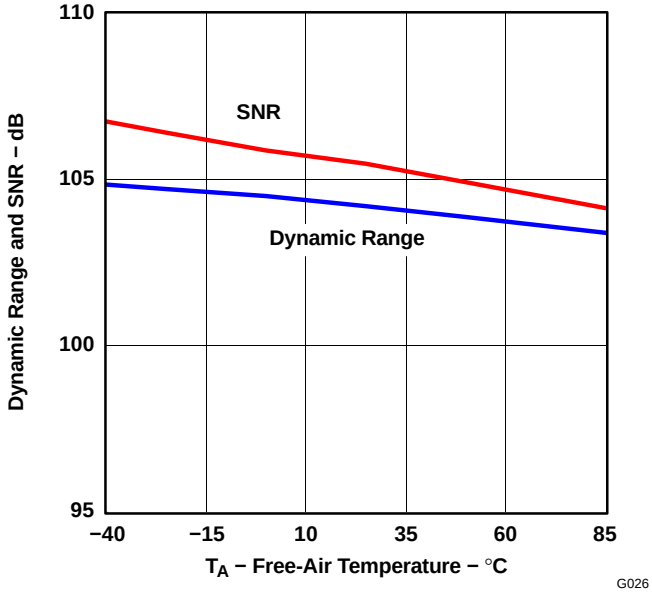


Figure 26.

THD+N
vs
SUPPLY VOLTAGE

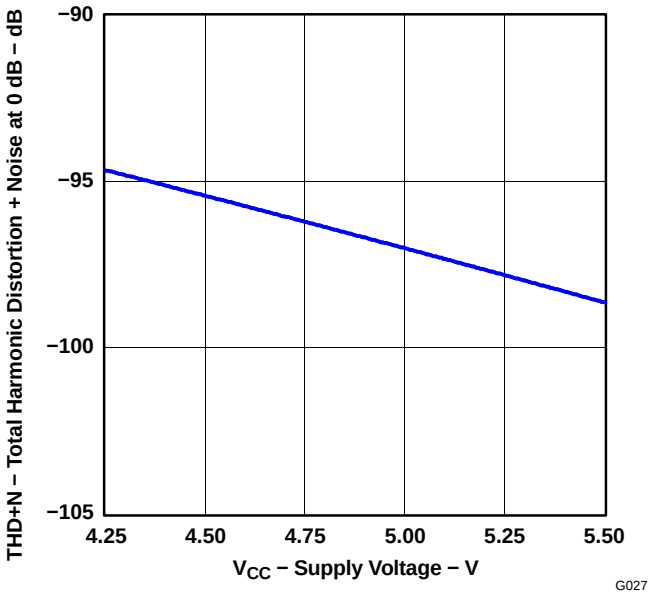


Figure 27.

DYNAMIC RANGE AND SNR
vs
TEMPERATURE

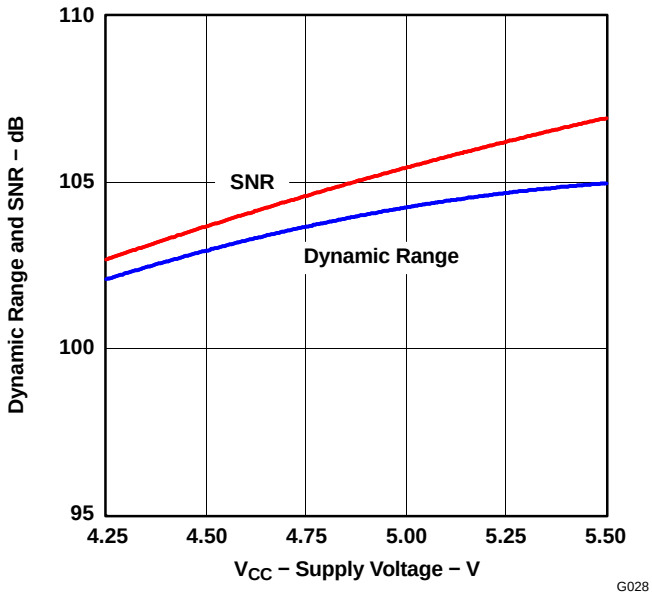


Figure 28.

TYPICAL PERFORMANCE CURVES (DAC SECTION) (continued)

All specifications at T_A = 25°C, $V_{CC}1 = V_{CC}2 = V_{CC}3$ = 5 V, V_{DD} = 3.3 V, f_S = 48 kHz, SCKI = 256 f_S, 24-bit data, unless otherwise noted.

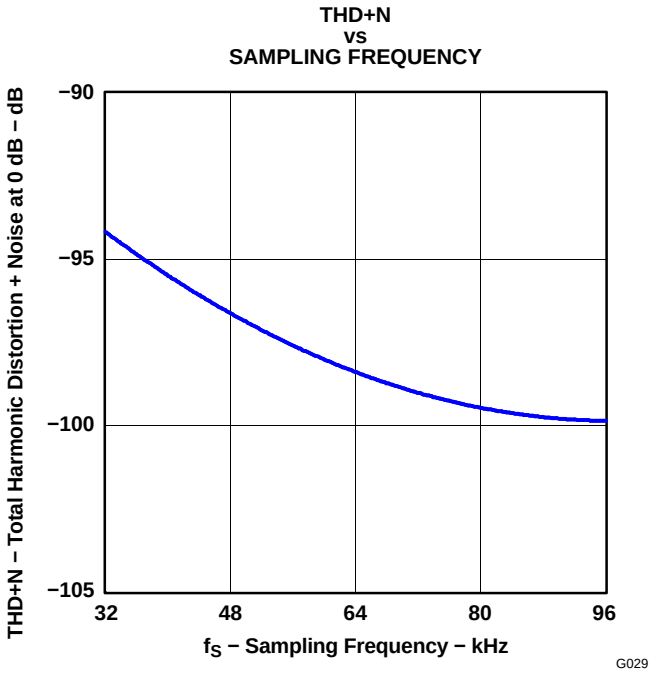


Figure 29.

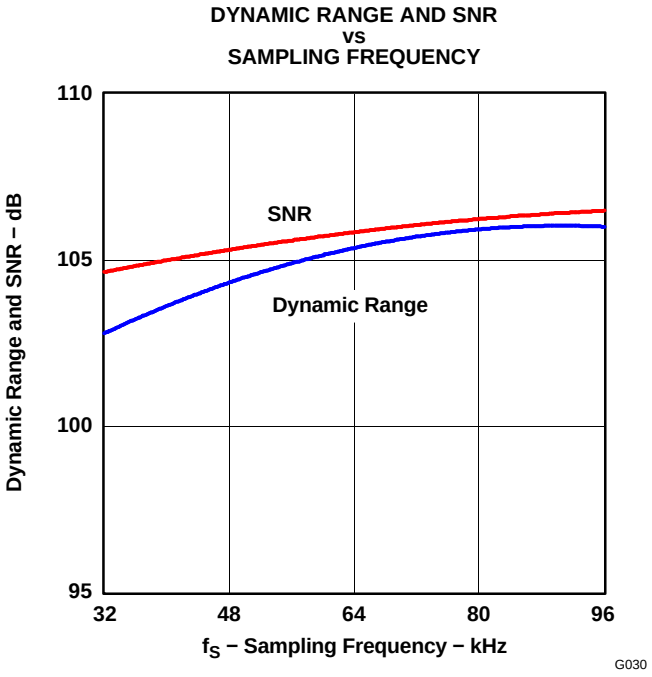


Figure 30.

TYPICAL PERFORMANCE CURVES

All specifications at T_A = 25°C, $V_{CC}1 = V_{CC}2 = V_{CC}3$ = 5 V, V_{DD} = 3.3 V, f_S = 48 kHz, SCKI = 256 f_S, 24-bit data, unless otherwise noted.

ADC OUTPUT SPECTRUM (Line Input, at PGA Gain = 0 dB)

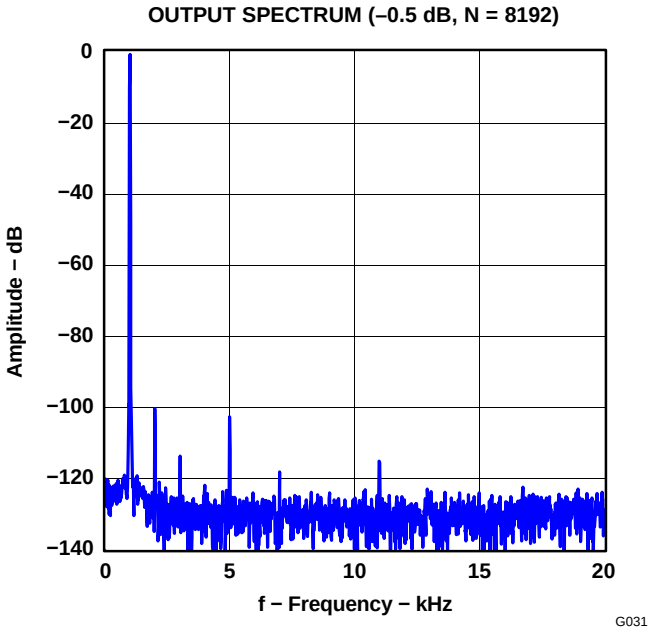


Figure 31.

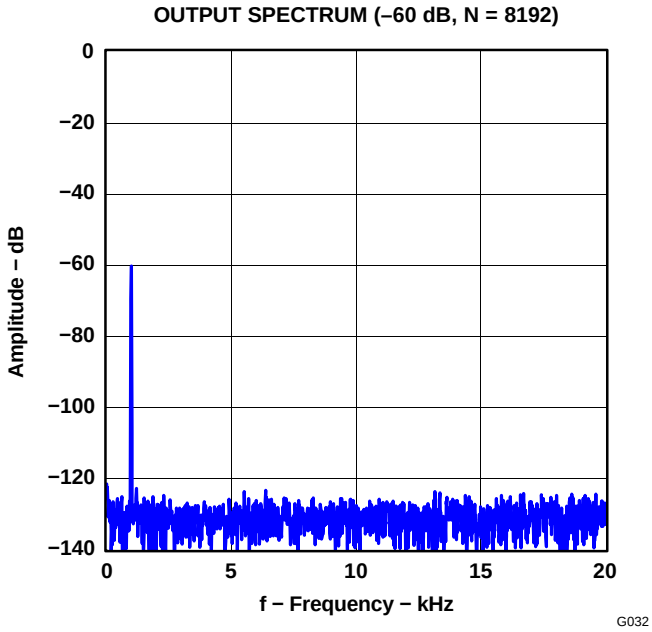


Figure 32.

DAC OUTPUT SPECTRUM

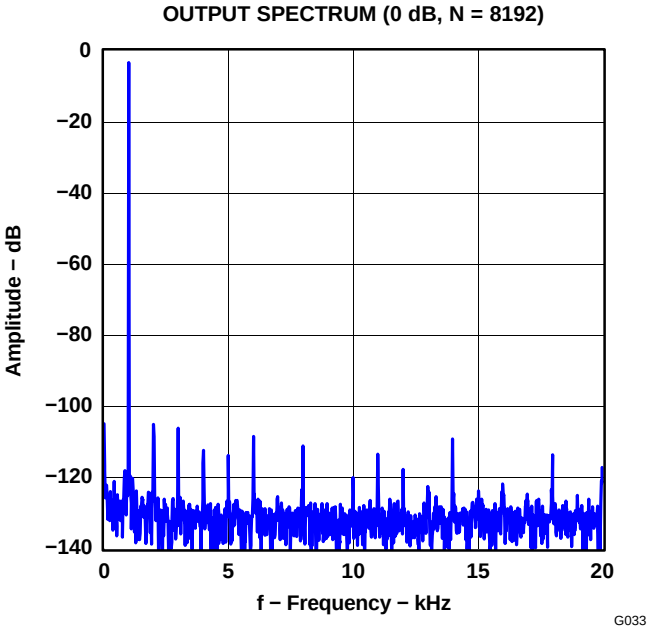


Figure 33.

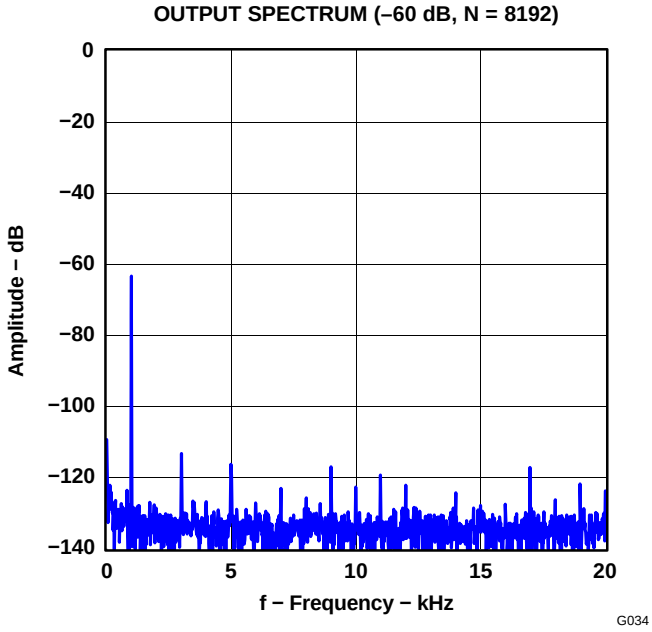


Figure 34.

TYPICAL PERFORMANCE CURVES (continued)

All specifications at T_A = 25°C, $V_{CC}1 = V_{CC}2 = V_{CC}3$ = 5 V, V_{DD} = 3.3 V, f_S = 48 kHz, SCKI = 256 f_S, 24-bit data, unless otherwise noted.

SUPPLY CURRENT

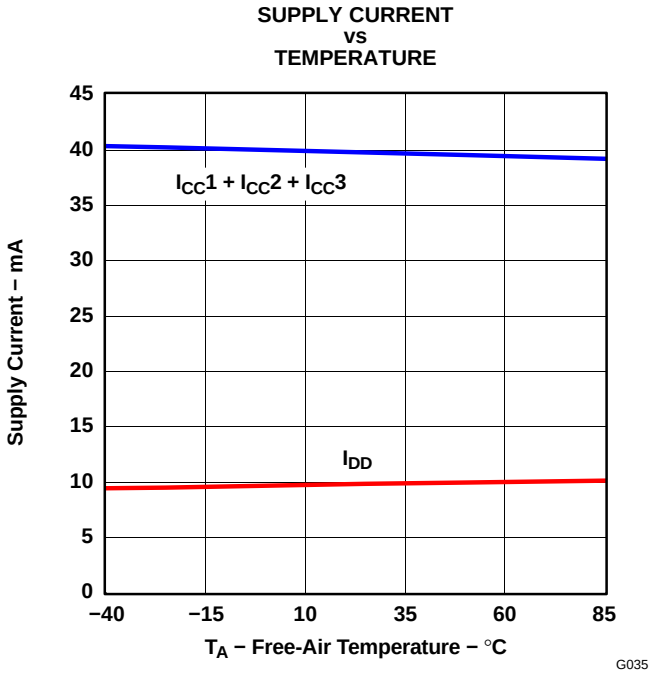


Figure 35.

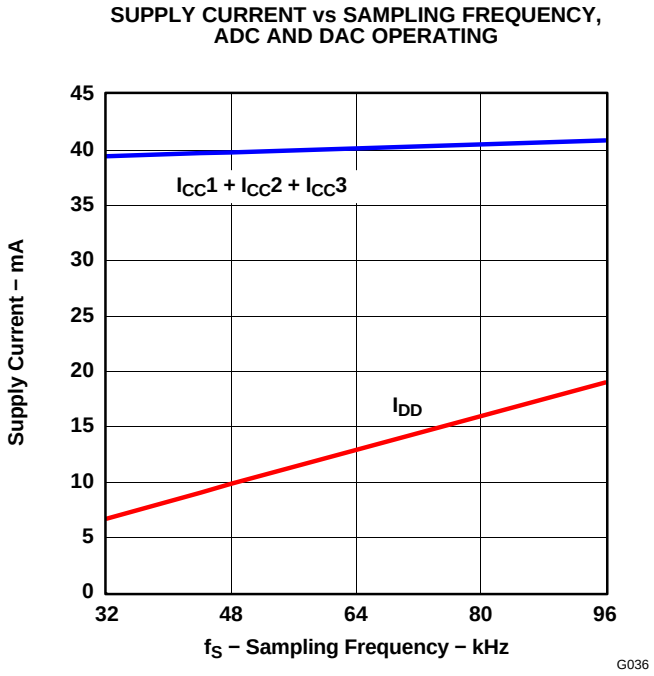


Figure 36.

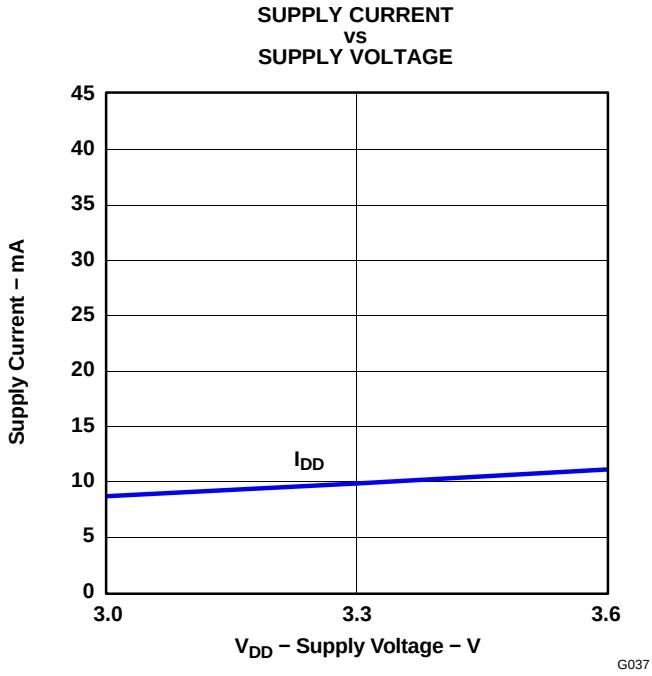


Figure 37.

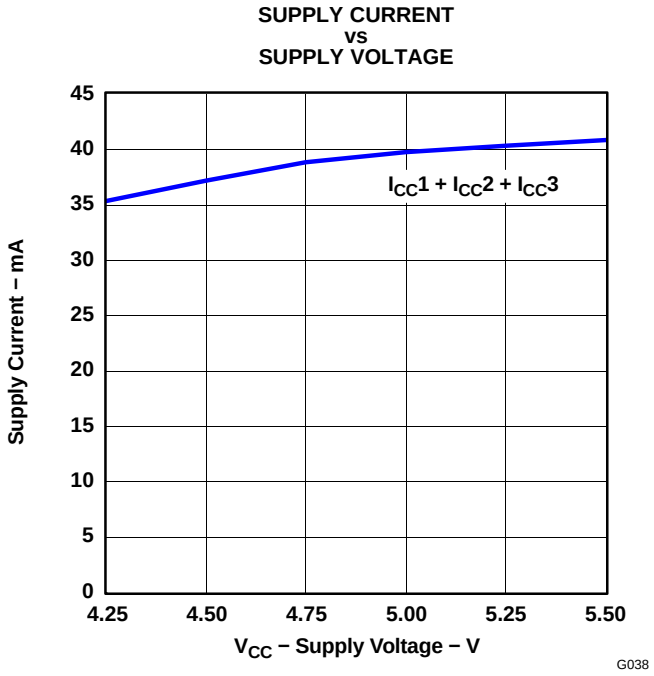


Figure 38.

THEORY OF OPERATION

ADC SECTION

The ADC block consists of a reference circuit, two channels of single-ended to differential converter, a fifth-order delta-sigma modulator with fully differential architecture, a decimation filter with high-pass filter, and a serial interface circuit which is also used as the serial interface for the DAC input signal as shown in the block diagram.

Figure 39 is the block diagram of the fifth-order delta-sigma modulator and transfer function.

An on-chip reference circuit with two external capacitors provides all reference voltages that are needed in the ADC section, and defines the full-scale voltage range of both channels.

An on-chip, single-ended to differential signal converter saves the design, space, and extra parts cost of an external signal converter.

Full differential architecture provides a wide dynamic range and excellent power supply rejection performance.

The input signal is sampled at ×64 oversampling rate and an on-chip antialiasing filter eliminates the need for an external sample-hold amplifier. A fifth-order delta-sigma noise shaper, which consists of five integrators using the switched-capacitor technique and a comparator, shapes the quantization noise generated outside of audio signal band by the comparator and 1-bit DAC.

The high-order delta-sigma modulation randomizes the modulator outputs and reduces idle-tone level.

The 64 f_S, 1-bit stream from the delta-sigma modulator is converted to a 1-f_S, 24-bit digital signal by removing high-frequency noise components with the decimation filter.

The dc component of the signal is removed by the HPF, and the HPF output is converted to a time-multiplexed serial signal through the serial interface.

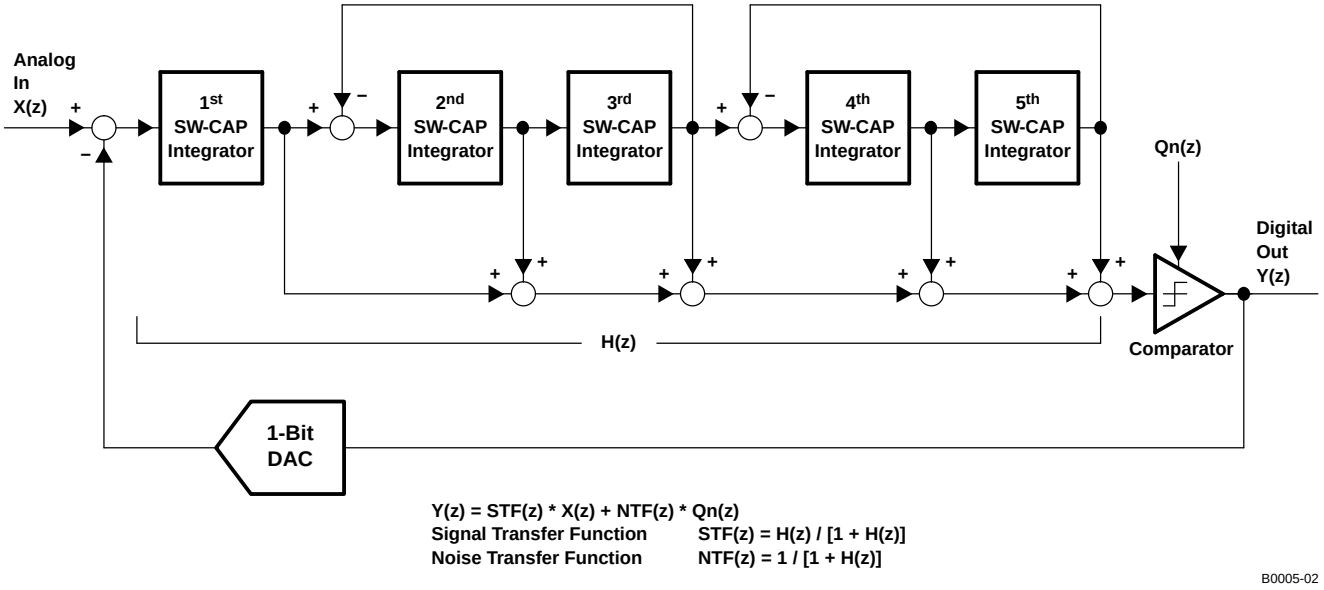


Figure 39. Block Diagram of Fifth-Order Delta-Sigma Modulator

DAC SECTION

The DAC section is based on the delta-sigma modulator, which consists of an 8-level amplitude quantizer and a fourth-order noise shaper. This section converts the oversampled input data to 8-level delta-sigma format. A block diagram of the 8-level delta-sigma modulator is shown in Figure 40. This 8-level delta-sigma modulator has the advantage of stability and clock jitter over the typical one-bit (2-level) delta-sigma modulator. The combined oversampling rate of the delta-sigma modulator and the internal 8× interpolation filter is 64 f_S for all system clocks. The theoretical quantization-noise performance of the 8-level delta-sigma modulator is shown in Figure 41.

THEORY OF OPERATION (continued)

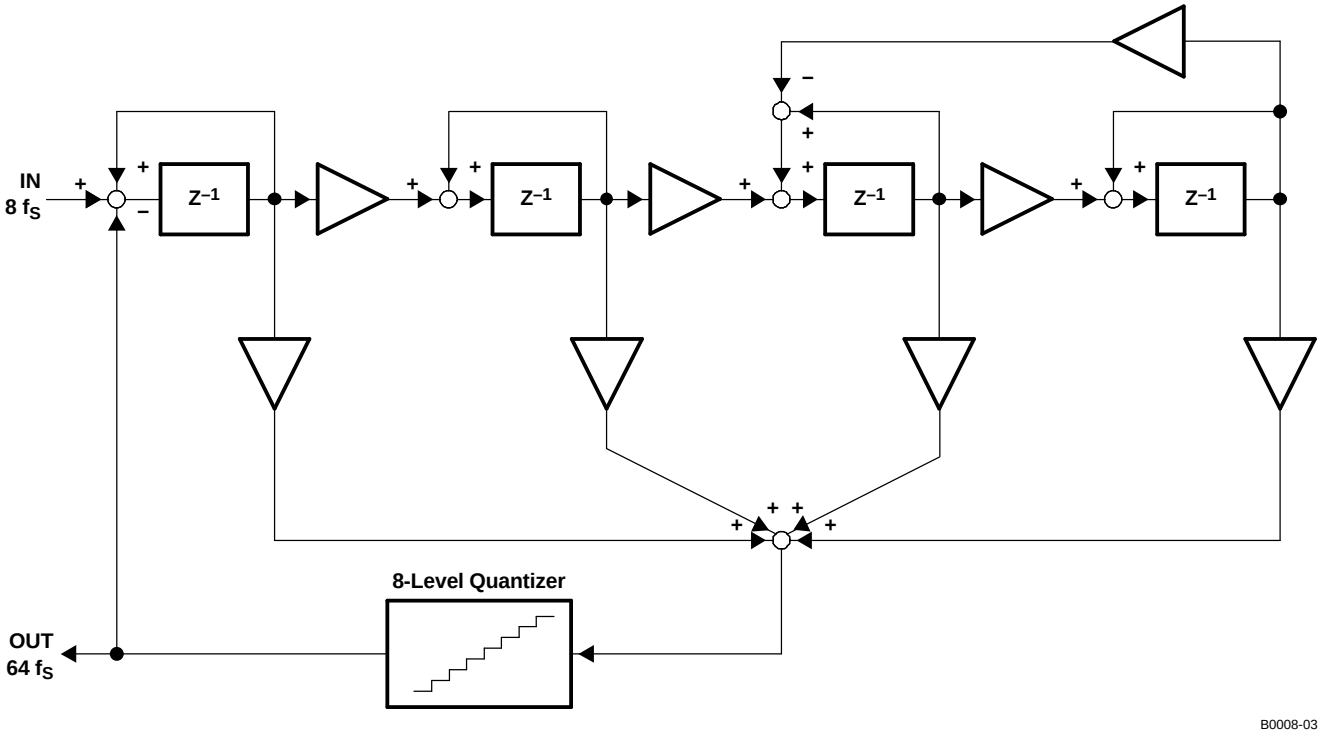


Figure 40. 8-Level Delta-Sigma Modulator Block Diagram

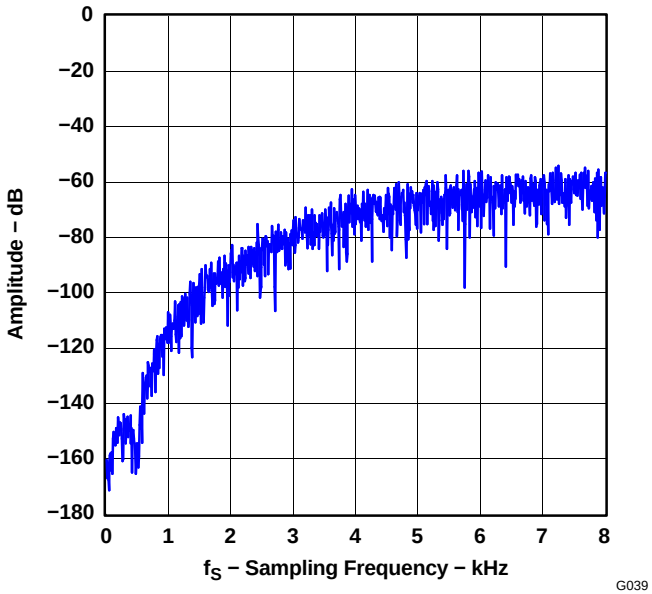


Figure 41. Quantization Noise Spectrum

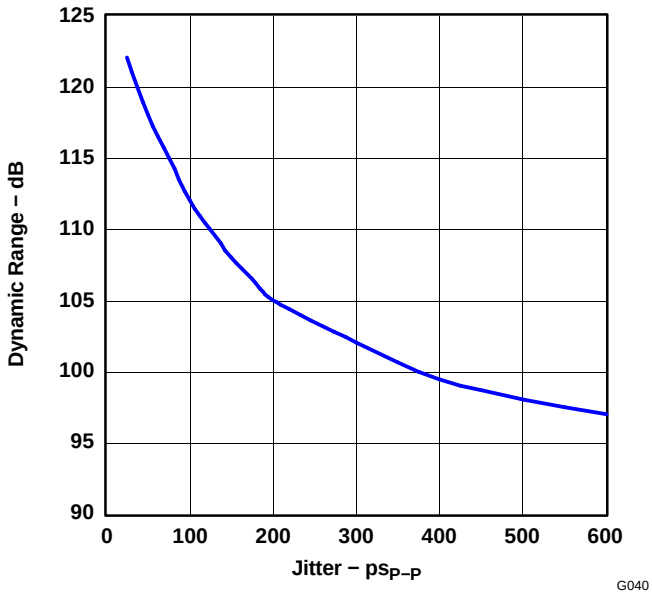


Figure 42. Clock Jitter

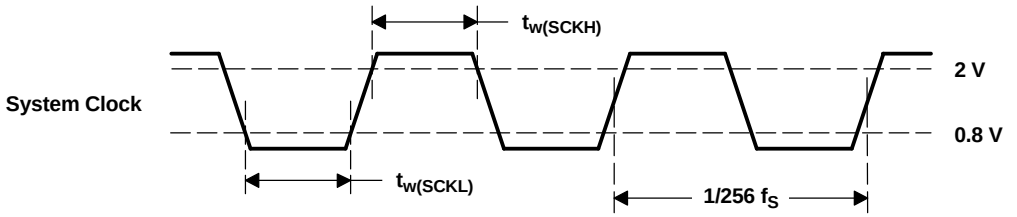
THEORY OF OPERATION (continued)

SYSTEM CLOCK

The system clock for the PCM3052A must be 256 f_S, where f_S is the audio sampling rate, 16 kHz to 96 kHz. Table 1 lists typical system clock frequencies, and Figure 43 illustrates the system clock timing.

Table 1. Typical System Clock

SAMPLING RATE FREQUENCY (f_S) – LRCK	SYSTEM CLOCK FREQUENCY – MHz
	256 f_S
16 kHz	4.096
32 kHz	8.192
44.1 kHz	11.2896
48 kHz	12.288
96 kHz	24.576



PARAMETER		MIN	MAX	UNIT
$t_{w(SCKH)}$	System clock pulse duration, HIGH	16		ns
$t_{w(SCKL)}$	System clock pulse duration, LOW	16		ns

Figure 43. System Clock Timing

POWER SUPPLY ON, EXTERNAL RESET, AND POWER DOWN

The PCM3052A has both an internal power-on-reset circuit and an external reset circuit. The sequences for both resets are shown as follows.

Figure 44 is the timing chart of the internal power-on reset. Two power-on-reset circuits are implemented, one each for for $V_{CC}1$ and V_{DD}. Initialization (reset) is performed automatically at the time when $V_{CC}1$ and V_{DD} exceed 3.9 V (typical) and 2.2 V (typical), respectively.

Internal reset is released after 1024 SCKI from power-on-reset release, and the PCM3052A begins normal operation. $V_{OUT}L$ and $V_{OUT}R$ from the DAC are forced to the V_{COM} (= 0.5 $V_{CC}2$) level as $V_{CC}2$ rises. When synchronization between SCKI, BCK, and LRCK is maintained, $V_{OUT}L$ and $V_{OUT}R$ go into the fade-in sequence. Then $V_{OUT}L$ and $V_{OUT}R$ provide outputs corresponding to DIN after $t_{(DACDLY1)}$ = 2100/f_S from power-on-reset release. On the other hand, DOUT from the ADC provides an output corresponding to $V_{IN}L$ and $V_{IN}R$ after $t_{(ADCDLY1)}$ = 4500/f_S from power-on-reset release. If synchronization is not maintained, the internal reset is not released, and operation is kept in the power-down mode. After resynchronization, the DAC goes into the fade-in sequence, and the ADC goes into normal operation after internal initialization.

DOUTS can provide S/PDIF data after the power-on-reset release if the SPDIF bit is HIGH (see serial control port for mode control section).

Figure 45 shows timing chart for external reset. The $\overline{\text{PDWN}}$ pin (pin 9) initiates external forced reset when $\overline{\text{PDWN}}$ = LOW, and it provides the power-down mode, which is the lowest power-dissipation state in the PCM3052A.

When $\overline{\text{PDWN}}$ transitions from HIGH to LOW while SCKI, BCK, and LRCK are synchronized, $V_{OUT}L$ and $V_{OUT}R$ are faded out and forced into V_{COM} (= 0.5 $V_{CC}2$) level after $t_{DACDLY1}$ = 2100/f_S. At the same time as the internal reset becomes LOW, DOUT becomes ZERO, the PCM3052A enters the power-down mode. To return to normal operation, set $\overline{\text{PDWN}}$ to HIGH. Then the power-on reset sequence, Figure 44, is performed.

DOUTS is driven LOW immediately after $\overline{PDWN}$ is asserted and recovers about $40/f_S$ following $\overline{PDWN}$ release.

Notes:

1. Large pop noises can be generated on $V_{OUT}L$ and $V_{OUT}R$ if the power supply is turned off during normal operation.
2. To switch $\overline{PDWN}$ during fade-in or fade-out causes an immediate change between fade-in and fade-out.
3. Changing mode controls during normal operation can degrade analog performance. It is recommended that mode controls be changed through the serial control port, and that changing or stopping the clock, switching the power supply off, etc., be done in the power-down mode.

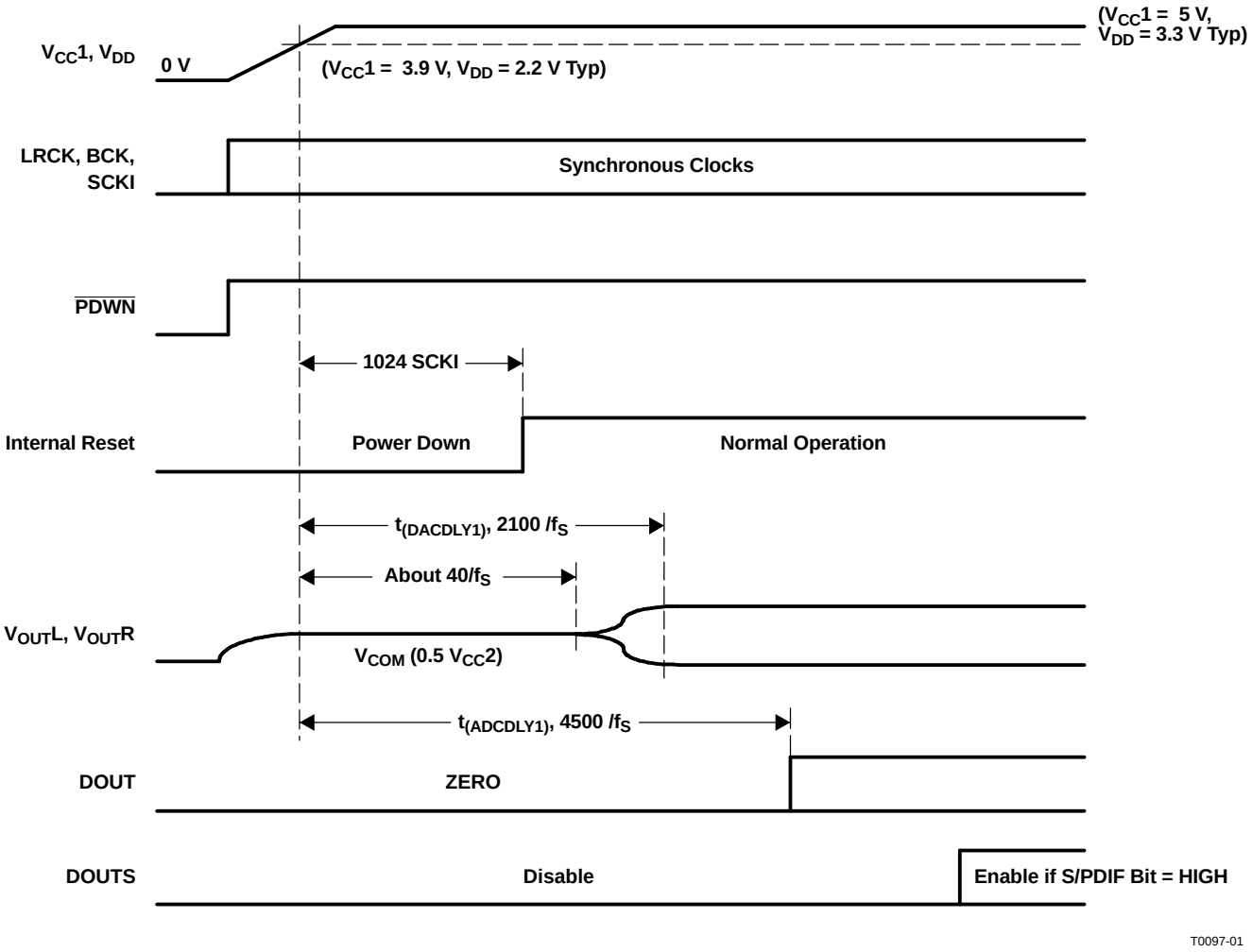


Figure 44. DAC Output and ADC Output for Power-On Reset

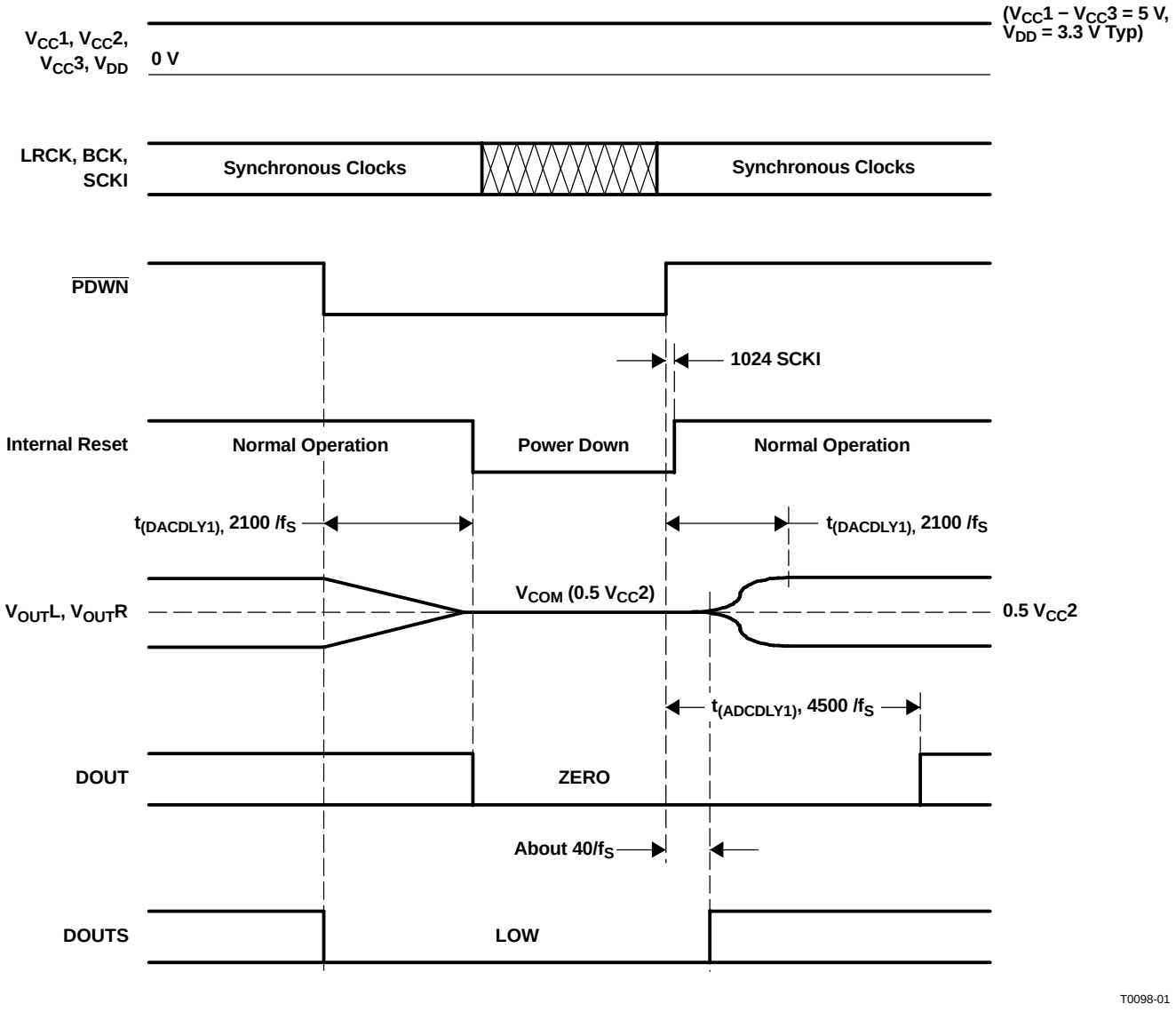


Figure 45. DAC Output and ADC Output for External Reset ($\overline{\text{PDWN}}$ Pin)

PCM AUDIO INTERFACE

Digital audio data is interfaced to the PCM3052A on LRCK (pin 10), BCK (pin 11), DIN (pin 12), DOUT (pin 13), and DOUTS (pin 14). The PCM3052A can accept 24-bit I^2S format only. In case of AC-3 type output data for DOUTS, bits 17 to 24 of DIN must be held LOW. See the *Digital Audio Interface Transmitter (DIT)* section of this data sheet.

Table 2. Audio Data Format

DATA FORMAT
24-bit, MSB-first, I^2S

The PCM3052A accepts only 64 clocks of BCK during one clock of LRCK. Figure 46 and Figure 47 illustrate audio data input/output format and timing.

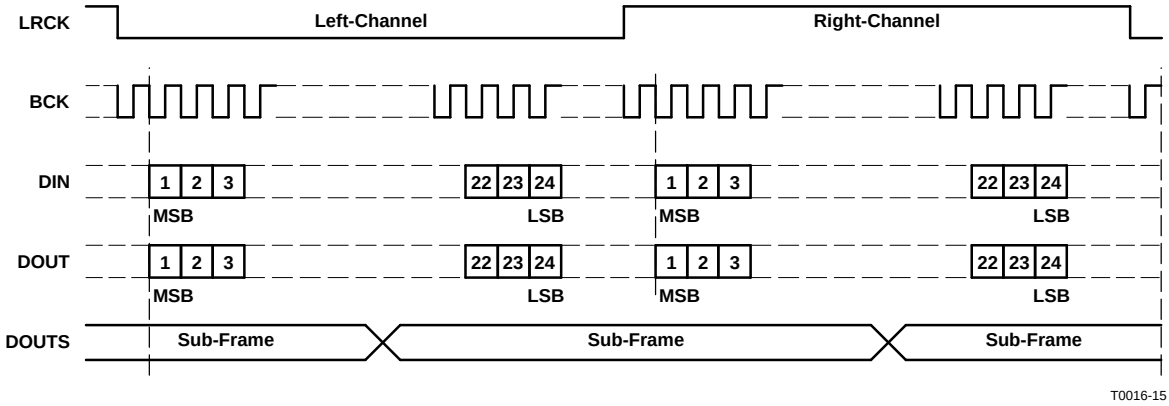
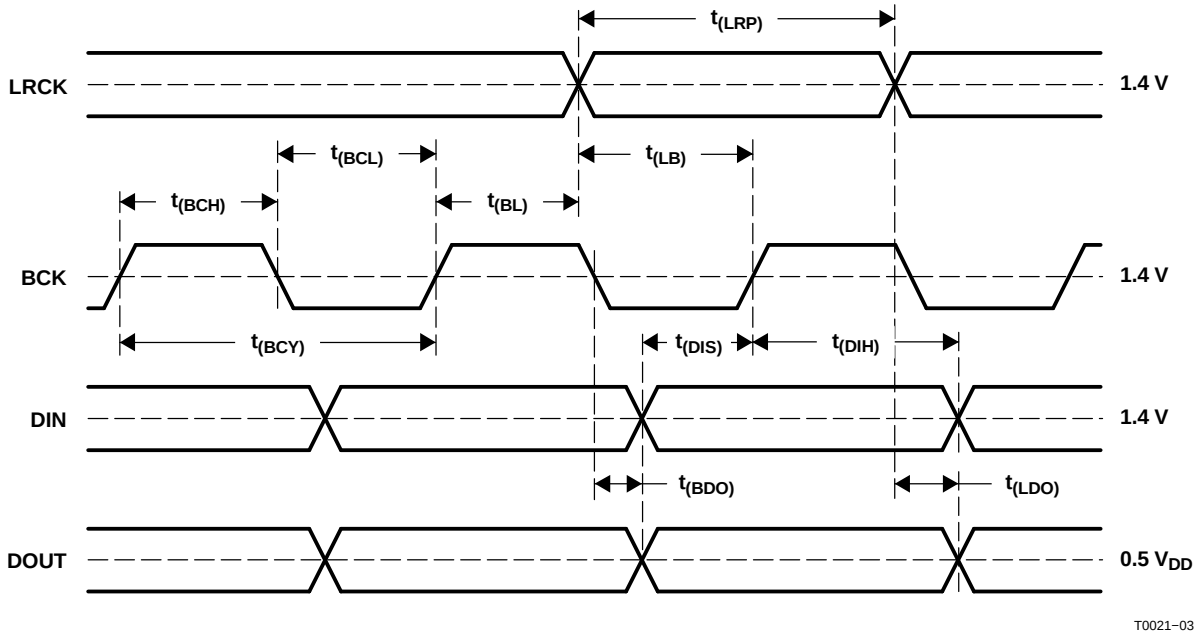


Figure 46. Audio Data Input/Output Format



PARAMETER		MIN	MAX	UNIT
t_{BCY}	BCK pulse cycle time	160		ns
t_{BCH}	BCK pulse duration, HIGH	70		ns
t_{BCL}	BCK pulse duration, LOW	70		ns
t_{BL}	BCK rising edge to LRCK edge	20		ns
t_{LB}	LRCK edge to BCK rising edge	20		ns
t_{LRP}	LRCK pulse duration	4.2		µs
t_{DIS}	DIN setup time to BCK rising edge	20		ns
t_{DIH}	DIN hold time to BCK rising edge	20		ns
t_{BDO}	DOUT delay time from BCK falling edge		20	ns
t_{LDO}	DOUT delay time from LRCK edge		20	ns
t_R	Rising time of all signals		10	ns
t_F	Falling time of all signals		10	ns

NOTE: Load capacitance at DOUT is 20 pF. Rising and falling time is measured from 10% to 90% of IN/OUT signal swing.

Figure 47. Audio Data Input/Output Timing

SYNCHRONIZATION WITH DIGITAL AUDIO SYSTEM

The PCM3052A operates with LRCK and BCK synchronized to the system clock in slave mode. The PCM3052A does not need specific phase relationship among LRCK, BCK, and the system clock, but does require the synchronization of LRCK, BCK, and the system clock.

If the relationship between system clock and LRCK changes more than ±6 BCKs during one sample period due to LRCK jitter, etc., internal operation of DAC halts within $6/f_S$, and the analog output is forced to 0.5 $V_{CC}2$ until re-synchronization of the system clock to LRCK and BCK has completed and then the time of $t_{(DACDLY2)}$ has elapsed.

DOUTS is also held LOW during the same period.

Internal operation of the ADC also halts within $6/f_S$, and digital output is forced into ZERO code until re-synchronization of the system clock to LRCK and BCK has completed and then the time of $t_{(ADCDLY2)}$ has elapsed.

In case of changes less than ±5 BCKs, re-synchronization does not occur and the previously described analog/digital output control and discontinuity does not occur.

Figure 48 illustrates the DAC analog output, ADC digital output, and DOUTS output for loss of synchronization.

During undefined data, the PCM3052A can generate some noise in audio signal. Also, the transition of normal to undefined data and undefined or zero data to normal creates a discontinuity of data on analog and digital outputs, which could generate some noise in audio signal.

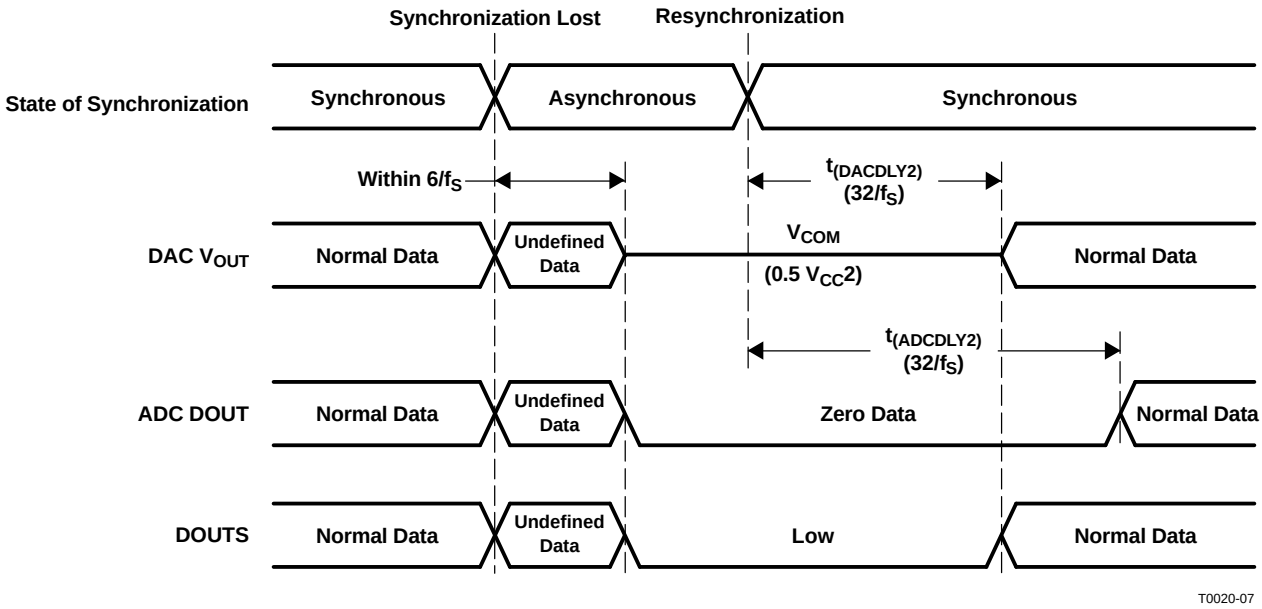


Figure 48. DAC Output and ADC Output for Loss of Synchronization

MICROPHONE AMPLIFIER AND MICROPHONE BIAS GENERATOR

The PCM3052A has a built-in, high-performance differential-input microphone amplifier with 34-dB gain, 5-kΩ (minimum) input resistance, and 59-dB SNR at 100-mVrms output. Bandwidth is 20 kHz for –3-dB attenuation. The PCM3052A also has a low-noise microphone bias generator with 0.75-$V_{CC}1$ and 1-mA current-source capability for electret microphones. Output impedance is 48 Ω for external noise reduction. The output of the microphone amplifier and the line input are connected as inputs to the multiplexer. The serial control port can be used to control which input the multiplexer selects (see Figure 50).

REFERENCE OUTPUT

The PCM3052A has a reference output pin (RFFO, pin 32) to supply reference voltage (0.5 $V_{CC}1$) to external components. The pin has 10-mA sink/source capability with 6-Ω output impedance.

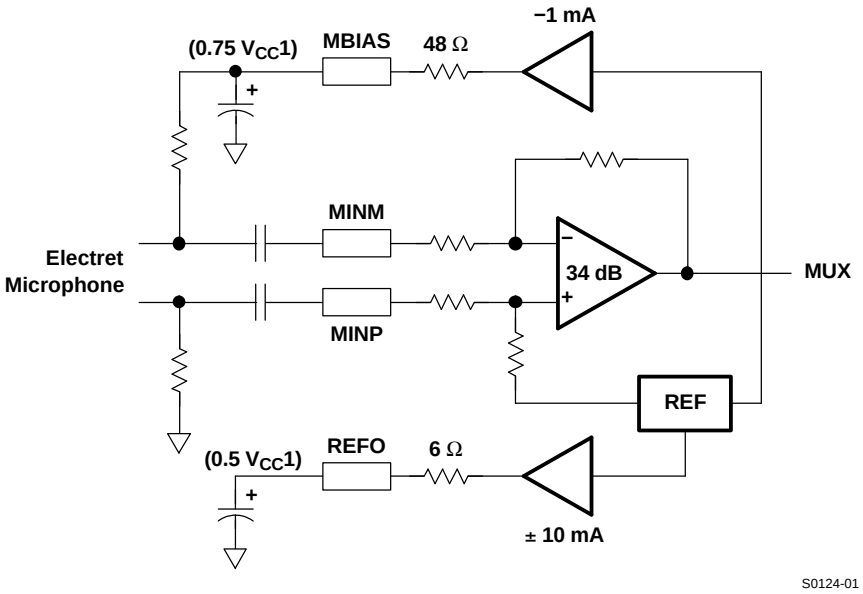


Figure 49. Microphone Amplifier, Microphone Bias Generator, and Reference Output

LINE AND MICROPHONE INPUT SELECT INDICATOR

The PCM3052A employs an indicator pin (L/$\overline{M}$, pin 3) to show which analog input is selected, line or microphone.

Table 3. Line and Microphone Select Indicator

L/$\overline{M}$	LINE/MIC SELECT INDICATOR
LOW	Microphone
HIGH	Line

MULTIPLEXER AND PGA

The PCM3052A has built-in analog front-end circuit which is shown in Figure 50. Multiplexer input and PGA gain are selected by mode control via the serial port, as shown in the *Serial Control Port for Mode Control* section. The full-scale input voltage range is 0.1 Vrms to 1.5 Vrms, and it can be adjusted to an adequate level for following the ADC sections.

$V_{IN}L$ and $V_{IN}R$ input resistance is maintained above 22 kΩ for all PGA gains. The input resistance value for each gain can be calculated by Equation 1.

$$R_{IN}(k\Omega,\ \text{typical}) = \frac{286}{1 + 10^{(\text{PGA Gain}/20)}} \quad (1)$$

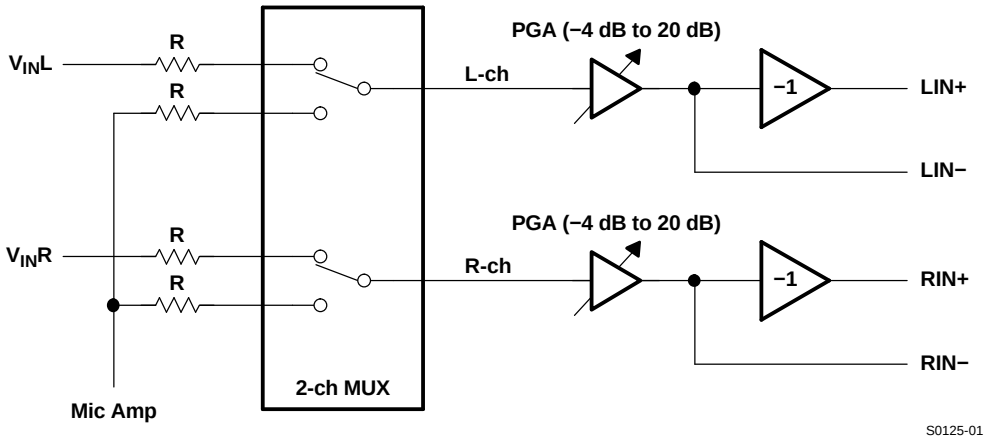


Figure 50. Multiplexer and PGA

ANALOG OUTPUTS FROM DAC

The PCM3052A has two independent output channels, $V_{OUT}L$ and $V_{OUT}R$. These are unbalanced outputs, each capable of driving 4 Vp-p (typical) into a 5-kΩ ac-coupled load. The internal output amplifiers for $V_{OUT}L$ and $V_{OUT}R$ are biased to the dc common-mode (or bipolar zero) voltage, equal to 0.5 $V_{CC}2$

The output amplifiers include an RC continuous-time filter, which helps to reduce the out-of-band noise energy present at the DAC outputs due to the noise-shaping characteristics of the PCM3052A delta-sigma modulators. The frequency response of this filter is shown in the typical performance curves. By itself, this filter is not adequate to attenuate the out-of-band noise to an acceptable level for many applications. An external low-pass filter is required to provide sufficient out-of-band noise rejection. Further discussion of DAC post-filter circuits is provided in the PCM1742 data sheet (SBAS176).

VCOM OUTPUT FOR DAC

One unbuffered common-mode voltage output pin, V_{COM} (pin 26), is brought out for decoupling purposes. This pin is nominally biased to a dc voltage level equal to 0.5 $V_{CC}2$. This pin can be used to bias external circuits. Output resistance of this pin is 21 kΩ (typical).

DIGITAL AUDIO INTERFACE TRANSMITTER (DIT)

The PCM3052A employs S/PDIF output from DOUTS (pin 14). The data (I^2S format only) from DAC digital data input (DIN, pin 12) is encoded to S/PDIF format with preambles according to IEC958. S/PDIF output is controlled through the serial control port. The output data type (linear PCM or AC-3) can be also selected through the serial control port. For the output data type of AC-3, the word length is limited to 16 bits in the PCM3052A. Therefore, bits 17 to 24 in the I^2S format data must be set to LOW.

Each bit after the audio sample word is assigned in the PCM3052A as follows.

Validity bit:	Writable through serial control port
User data:	Fixed to 0
Channel status [0]:	Fixed to 0 (consumer use)
Channel status [1]:	Writable through serial control port (audio sample word type)
Channel status [2]:	Writable through serial control port (copyright flag)
Channel status [3:5]:	Writable through serial control port (additional format information)
Channel status [6:7]:	Fixed to 00 (mode 0)
Channel status [8:15]:	Writable through serial control port (category code)
Channel status [16:19]:	Fixed to 0000 (source number)
Channel status [20:23]:	Fixed to 0000 (channel number)
Channel status [24:27]:	Writable through serial control port (sampling frequency)
Channel status [28:29]:	Writable through serial control port (clock accuracy)
Channel status [30:31]:	Fixed to 00
Channel status [32:35]:	Writable through serial control port (word length)
Channel status [36:191]:	Fixed to all 0s
Parity bit:	Even parity for preceding data from preamble to channel status bit

S/PDIF output timing is shown in Figure 51. The S/PDIF block starts with a preamble after $32/f_S$ from the frame where S/PDIF output control bit becomes HIGH. The behavior of DOUTS for power-on reset, external reset, and loss of synchronization is shown in Figure 44, Figure 45, and Figure 48, respectively.

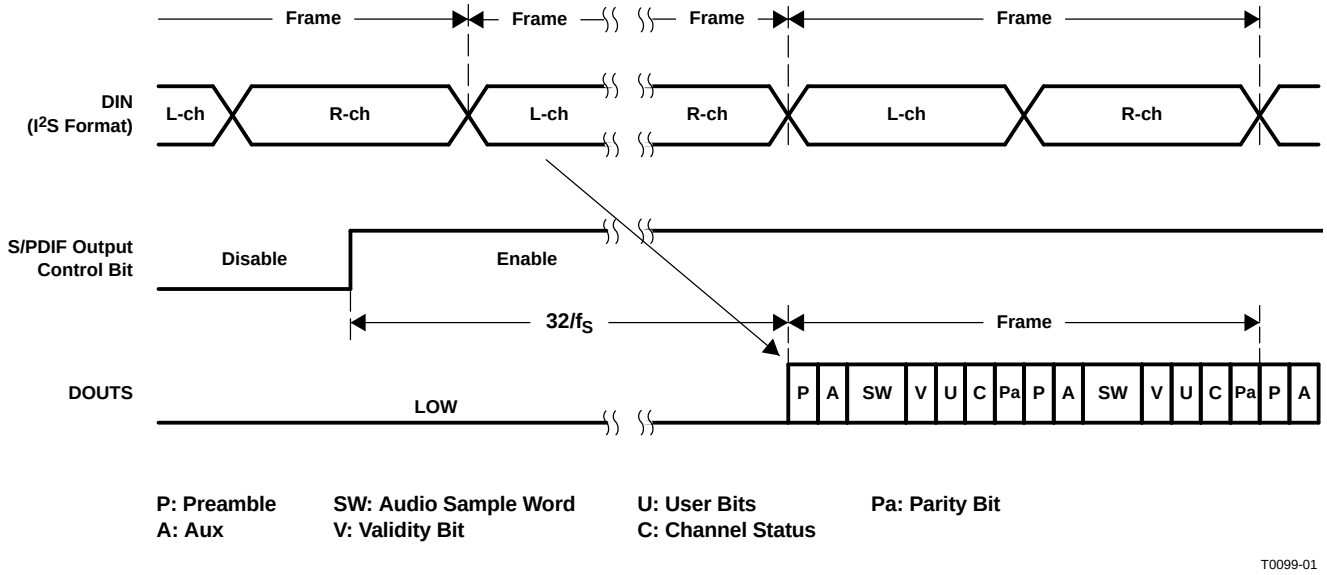


Figure 51. S/PDIF Output Timing

SERIAL CONTROL PORT FOR MODE CONTROL

The several built-in functions of the PCM3052A can be controlled through the I^2C format serial-control port, SDA (pin 18) and SCL (pin 19). The PCM3052A supports the I^2C serial bus and the data transmission protocol for standard mode as a slave device. This protocol is explained in I^2C specification 2.0.

Serial control is available even during the power-down state and without a system clock, except when the MRST bit = 0 or I2CEN (pin 21) = LOW.

Slave Address

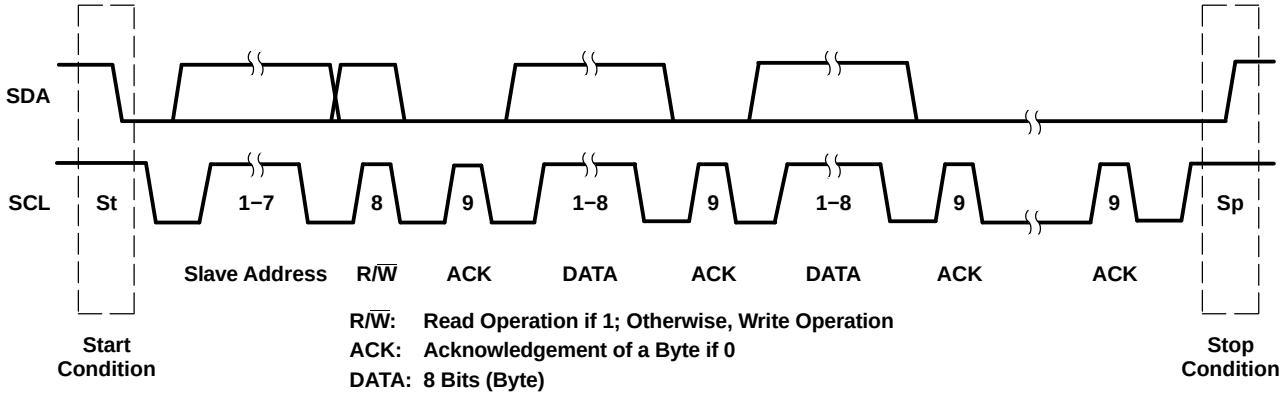
MSB LSB

1	0	0	0	1	1	ADR	R/$\overline{W}$

The PCM3052A has seven bits for its own slave address. The first six bits (MSBs) of the slave address are factory preset to 100011. The next bit of the address byte is the device select bit which can be user-defined by ADR (pin 20). A maximum of two PCM3052As can be connected on the same bus at one time. Each PCM3052A responds when it receives its own slave address.

Packet Protocol

A master device must control packet protocol, which consists of start condition, slave address with read/write bit, data if write or acknowledgement if read, and stop condition. The PCM3052A supports slave receiver function.



R/$\overline{W}$: Read Operation if 1; Otherwise, Write Operation
ACK: Acknowledgement of a Byte if 0
DATA: 8 Bits (Byte)
NACK: Not Acknowledgement of a bite if 1

Write Operation

Transmitter	*M*	*M*	*M*	*S*	*M*	*S*	*M*	*S*		*S*	*M*
Data Type	St	Slave Address	$\overline{W}$	ACK	DATA	ACK	DATA	ACK		ACK	Sp

M: Master Device S: Slave Device
St: Start Condition $\overline{W}$: Write Sp: Stop Condition

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Figure 52. Basic I^2C Framework

Write Operation

The PCM3052A supports receiver function. A master can write to any PCM3052A registers using single or multiple accesses. The master sends a PCM3052A slave address with a write bit, a register address, and the data. If multiple access is required, the address is that of the starting register, followed by the data to be transferred. When the data are received properly, the index register is incremented by 1 automatically. When the index register reaches 50h, the next value is 41h. When undefined registers are accessed, the PCM3052A does not send an acknowledgement. Figure 53 is a diagram of the write operation. The register address and the write data are 8 bits and MSB-first format.

Transmitter	*M*	*M*	*M*	*S*	*M*	*S*	*M*	*S*	*M*	*S*		*S*	*M*
Data Type	St	Slave Address	$\overline{W}$	ACK	Reg Address	ACK	Write Data 1	ACK	Write Data 2	ACK		ACK	Sp

M: Master Device S: Slave Device

St: Start Condition ACK: Acknowledge $\overline{W}$: Write Sp: Stop Condition

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Figure 53. Framework for Write Operation

Serial Control Enable/Disable

The PCM3052A supports I^2C serial control enable/disable function by I2CEN (pin 21) to avoid an unstable start condition. When the I2CEN pin transitions from LOW to HIGH, both SDA (pin 18) and SCL (pin 19) must be HIGH stable and the ADR (pin 20) must be also stable.

While I2CEN = LOW, the write operation is disabled. A timing chart of I2CEN is shown in Figure 54.

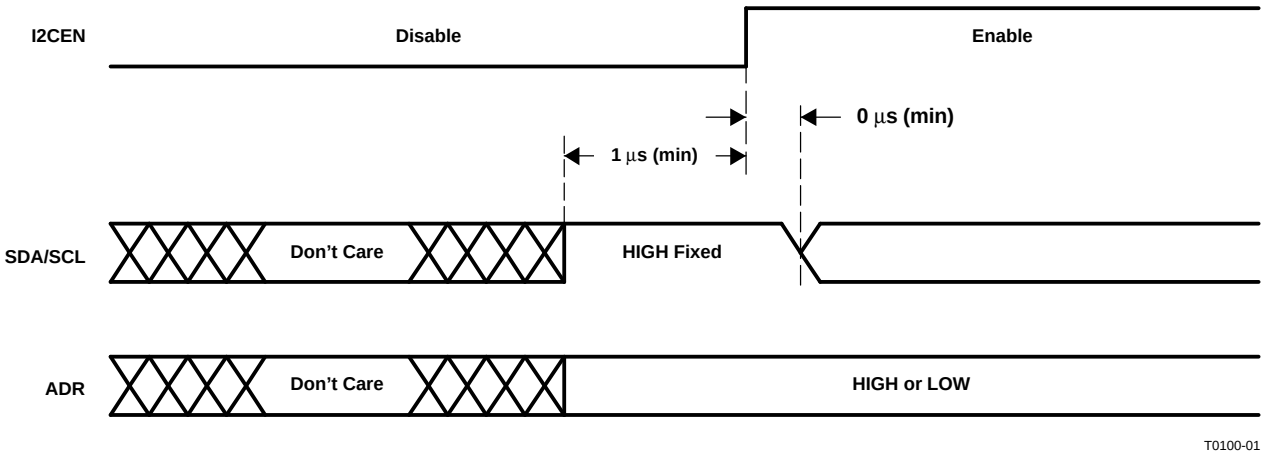
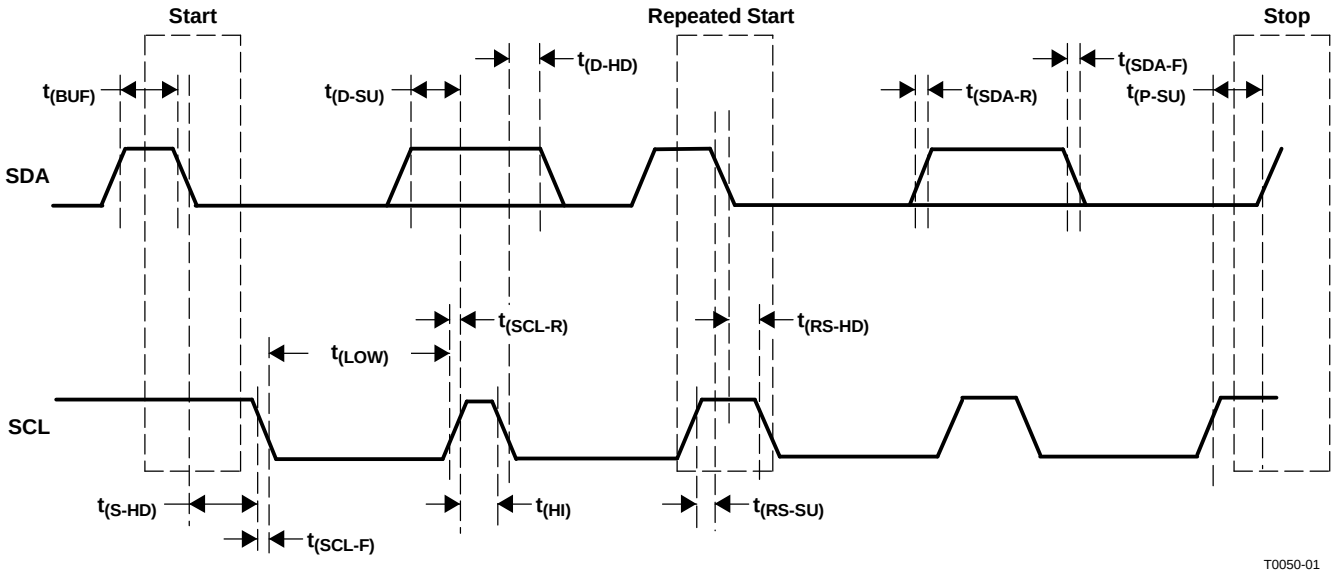


Figure 54. I2CEN Timing Chart

TIMING DIAGRAM



PARAMETER		CONDITIONS	MIN	MAX	UNIT
$f_{(SCL)}$	SCL clock frequency	Standard mode		100	kHz
$t_{(BUF)}$	Bus free time between STOP and START condition	Standard mode	4.7		µs
$t_{(LOW)}$	Low period of the SCL clock	Standard mode	4.7		µs
$t_{(HI)}$	High period of the SCL clock	Standard mode	4		µs
t_{RS-SU}	Setup time for START/repeated START condition	Standard mode	4.7		µs
$t_{(S-HD)}$ $t_{(RS-HD)}$	Hold time for START/repeated START condition	Standard mode	4		µs
$t_{(D-SU)}$	Data setup time	Standard mode	250		ns
$t_{(D-HD)}$	Data hold time	Standard mode	0	900	ns
$t_{(SCL-R)}$	Rise time of SCL signal	Standard mode	20 + 0.1 C_B	1000	ns
$t_{(SCL-R1)}$	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	Standard mode	20 + 0.1 C_B	1000	ns
$t_{(SCL-F)}$	Fall time of SCL signal	Standard mode	20 + 0.1 C_B	1000	ns
$t_{(SDA-R)}$	Rise time of SDA signal	Standard mode	20 + 0.1 C_B	1000	ns
$t_{(SDA-F)}$	Fall time of SDA signal	Standard mode	20 + 0.1 C_B	1000	ns
$t_{(P-SU)}$	Setup time for STOP condition	Standard mode	4		µs
C_B	Capacitive load for SDA and SCL line			400	pF
V_{NH}	Noise margin at high level for each connected device (including hysteresis)	Standard mode	0.2 V_{DD}		V

Figure 55. Control Interface Timing

MODE CONTROL REGISTERS

User-Programmable Mode Controls

The PCM3052A has several user programmable functions which are accessed via control registers. The registers are programmed using the I^2C serial control port, which was previously discussed in this data sheet. Table 4 lists the available mode control functions, along with their reset default conditions and associated register addresses. The register map is shown in Table 5.

Table 4. User-Programmable Mode Controls

FUNCTION	RESET DEFAULT	REGISTER	BIT(S)
Digital attenuation control, 0 dB to –63 dB in 0.5-dB steps (DAC)	0 dB, no attenuation	65 and 66	AT1[7:0], AT2[7:0]
Mode control register reset (ADC and DAC)	Normal operation	67	MRST
System reset (ADC and DAC)	Normal operation	67	SRST
ADC power-save control (ADC)	Normal operation	67	ADPSV
DAC Power Save Control (DAC)	Normal operation	67	DAPSV
Soft-mute control (DAC)	Mute disabled	68	MUT[2:1]
Oversampling rate control (DAC)	64-f_S oversampling	68	OVR1
De-emphasis function control (DAC)	De-emphasis disabled	69	DM12
De-emphasis sampling rate selection (DAC)	48 kHz	69	DMF[1:0]
Digital filter rolloff control (DAC)	Sharp rolloff	70	FLT0
Output phase select (DAC)	Normal	71	DREV
Multiplexer input channel control (ADC)	LINE IN	72	AML
PGA gain control (ADC)	–4 dB	72	PG[4:0]
HPF bypass control (ADC)	HPF enabled	75	BYP
DAC output control (DAC)	Disabled	77	DACMSK
Additional format information (DIT)	Two audio channels without pre-emphasis	77	AFI[5:3]
Copyright flag (DIT)	Asserted	77	COPY
Audio sample word type (DIT)	PCM	77	AUDIO
DIT output control (DIT)	Disable	77	DITMSK
Category code (DIT)	General	78	CAT[15:8]
Clock accuracy (DIT)	Level II	79	CLK[29:28]
Sampling frequency (DIT)	44.1kHz	79	SF[27:24]
Validity bit for L-channel (DIT)	Valid	80	VALIDL
Validity bit for R-channel (DIT)	Valid	80	VALIDR
S/PDIF output control (DIT)	Disabled	80	SPDIF
Word Length (DIT)	24 bits	80	WL[35:32]

Table 5. Register Map

REGISTER ADDRESS										DATA							
IDX (B8–B14)	REGISTER	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
41h	65	0	1	0	0	0	0	0	1	AT17	AT16	AT15	AT14	AT13	AT12	AT11	AT10
42h	66	0	1	0	0	0	0	1	0	AT27	AT26	AT25	AT24	AT23	AT22	AT21	AT20
43h	67	0	1	0	0	0	0	1	1	MRST	SRST	ADPSV	DAPSV	RSV(1)	RSV(1)	RSV(1)	RSV(1)
44h	68	0	1	0	0	0	1	0	0	RSV(1)	OVR1	RSV(1)	RSV(1)	RSV(1)	RSV(1)	MUT2	MUT1
45h	69	0	1	0	0	0	1	0	1	RSV(1)	DMF1	DMF0	DM12	RSV(1)	RSV(1)	RSV(1)	RSV(1)
46h	70	0	1	0	0	0	1	1	0	RSV(1)	RSV(1)	FLT0	RSV(1)	RSV(1)	1	RSV(1)	RSV(1)
47h	71	0	1	0	0	0	1	1	1	RSV(1)	RSV(1)	RSV(1)	RSV(1)	RSV(1)	RSV(1)	RSV(1)	DREV
48h	72	0	1	0	0	1	0	0	0	RSV(1)	RSV(1)	AML	PG4	PG3	PG2	PG1	PG0
4Bh	75	0	1	0	0	1	0	1	1	RSV(1)	RSV(1)	RSV(1)	RSV(1)	BYP	1	RSV(1)	RSV(1)
4Dh	77	0	1	0	0	1	1	0	1	DACMSK	RSV(1)	AFI5	AFI4	AFI3	COPY	AUDIO	DITMSK
4Eh	78	0	1	0	0	1	1	1	0	CAT15	CAT14	CAT13	CAT12	CAT11	CAT10	CAT9	CAT8
4Fh	79	0	1	0	0	1	1	1	1	RSV(1)	RSV(1)	CLK29	CLK28	SF27	SF26	SF25	SF24
50h	80	0	1	0	1	0	0	0	0	VALIDL	VALIDR	SPDIF	RSV(1)	WL35	WL34	WL33	WL32

(1) *RSV* means *reserved* for test operation or future extension, and these bits should be set 0 during regular operation. Do not write any values in other addresses than those listed in the table.

REGISTER DEFINITIONS

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 65	0	1	0	0	0	0	0	1	AT17	AT16	AT15	AT14	AT13	AT12	AT11	AT10
REGISTER 66	0	1	0	0	0	0	1	0	AT27	AT26	AT25	AT24	AT23	AT22	AT21	AT20

ATx[7:0]: Digital Attenuation Level Setting (DAC)

Where x = 1 or 2, corresponding to the DAC output $V_{OUT}L$ (x = 1) and $V_{OUT}R$ (x = 2).

Default value: 1111 1111b

ATX[7:0]	DECIMAL VALUE	ATTENUATION LEVEL SETTING
1111 1111b	255	0 dB, No Attenuation. (default)
1111 1110b	254	–0.5 dB
1111 1101b	253	–1.0 dB
:	:	:
1000 0011b	131	–62.0 dB
1000 0010b	130	–62.5 dB
1000 0001b	129	–63.0 dB
1000 0000b	128	Mute
:	:	:
0000 0000b	0	Mute

Each DAC channel ($V_{OUT}L$ and $V_{OUT}R$) includes a digital attenuation function. The attenuation level can be set from 0 dB to –63 dB in 0.5-dB steps, and also can be set to infinite attenuation (mute). The attenuation level change from current value to target value is performed by incrementing or decrementing by one small step size for every $1/f_S$ time interval during $2048/f_S$. The small step size is determined automatically so that it can provide a transition in attenuation level with a characteristic S-shaped curve from the current value to the target value. While the attenuation level change sequence is in progress for $2048/f_S$, processing of the attenuation level change for any new command is ignored, and the new command is overwritten into command buffer. The last command for an attenuation level change is performed after present attenuation level change sequence is finished.

The attenuation data for each channel can be set individually. The attenuation level can be calculated using the following formula:

$$\text{Attenuation level (dB)} = 0.5 \times (\text{ATx}[7:0]_{DEC} - 255)$$

where $\text{ATx}[7:0]_{DEC}$ = 0 through 255.

For $\text{ATx}[7:0]_{DEC}$ = 0 through 128, attenuation is set to infinite attenuation.

The preceding table shows attenuation levels for various settings.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 67	0	1	0	0	0	0	1	1	MRST	SRST	ADPSV	DAPSV	RSV	RSV	RSV	RSV

MRST: Mode Control Register Reset (ADC and DAC)

Default value: 1

MRST = 0	Set default value
MRST = 1	Normal operation (default)

The MRST bit controls mode control register reset. Pop-noise may be generated.

SRST: System Reset (ADC and DAC)

Default value: 1

SRST = 0	Re-synchronization
SRST = 1	Normal operation (default)

The SRST bit controls system reset. The PCM3052A does not go into power-down state. The mode control register is not reset by this control. Also pop-noise may be generated.

ADPSV: ADC Power-Save Control (ADC)

Default value: 0

ADPSV = 0	Normal operation (default)
ADPSV = 1	Power-save mode

The ADPSV bit controls ADC power-save mode. In power-save mode, ADC goes into power-down state, the data in ADC are reset, and DOUT is forced into ZERO immediately. I^2C control is enabled.

DAPSV: DAC Power-Save Control (DAC)

Default value: 0

DAPSV = 0	Normal operation (default)
DAPSV = 1	Power-save mode

The DAPSV bit controls the DAC power-save mode. In the power-save mode, the DAC output is faded out and DAC goes into the power-down state. I^2C control is enabled. A waiting time of more than $2100/f_S$ from power-save-mode assertion is required for the release of the power-save mode.

DIT function is available if SPDIF bit = 1, even though DAPSV = 1.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 68	0	1	0	0	0	1	0	0	RSV	OVR1	RSV	RSV	RSV	RSV	MUT2	MUT1

OVR1: Oversampling Rate Control (DAC)

Default value: 0

OVR1 = 0	64× oversampling (default)
OVR1 = 1	128× oversampling

The OVR1 bit is used to control the oversampling rate of the delta-sigma D/A converters. To write over this register during normal operation may generate noise.

MUTx: Soft-Mute Control (DAC)

where, x = 1 or 2, corresponding to the DAC output $V_{OUT}L$ (x = 1) and $V_{OUT}R$ (x = 2).

Default value: 0

MUTx = 0	Mute disabled (default)
MUTx = 1	Mute enabled

The mute bits, MUT1 and MUT2, are used to enable or disable the soft-mute function for the corresponding DAC outputs, $V_{OUT}L$ and $V_{OUT}R$. The soft-mute function is incorporated into the digital attenuators. When mute is disabled (MUTx = 0), the attenuator and DAC operate normally. When mute is enabled by setting MUTx = 1, the digital attenuator for the corresponding output is decreased from the current setting to infinite attenuation, one attenuator step (0.5 dB) for every $8/f_S$ seconds. This provides *pop-free* muting of the DAC output.

By setting MUTx = 0, the attenuator is increased one step for every $8/f_S$ seconds to the previously programmed attenuation level.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 69	0	1	0	0	0	1	0	1	RSV	DMF1	DMF0	DM12	RSV	RSV	RSV	RSV

DMF[1:0]: Sampling Frequency Selection for the De-Emphasis Function (DAC)

Default value: 01

DMF[1:0]	DE-EMPHASIS SAMPLING RATE SELECTION
0 0	44.1 kHz
0 1	48 kHz (default)
1 0	32 kHz
1 1	Reserved

The DMF[1:0] bits are used to select the sampling frequency used for the digital de-emphasis function when it is enabled.

DM12: Digital De-Emphasis Function Control (DAC)

Default value: 0

DM12 = 0	De-emphasis disabled (default)
DM12 = 1	De-emphasis enabled

The DM12 bit is used to enable or disable the digital de-emphasis function. See the plots shown in the *Typical Performance Curves* section of this data sheet.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 70	0	1	0	0	0	1	1	0	RSV	RSV	FLT0	RSV	RSV	1	RSV	RSV

FLT0: Digital Filter Rolloff Control (DAC)

Default value: 0

FLT0 = 0	Sharp rolloff (default)
FLT0 = 1	Slow rolloff

The FLT0 bit allows the user to select the digital filter rolloff that is best suited to their application. Two filter rolloff selections are available: Sharp and Slow. The filter responses for these selections are shown in the Typical Performance Curves section of this data sheet.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 71	0	1	0	0	0	1	1	1	RSV	RSV	RSV	RSV	RSV	RSV	RSV	DREV

DREV: Output Phase Select (DAC)

Default value: 0

DREV = 0	Normal output (default)
DREV = 1	Inverted output

The DREV bit is used to control the output analog signal phase control.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 72	0	1	0	0	1	0	0	0	RSV	RSV	AML	PG4	PG3	PG2	PG1	PG0

AML: Multiplexer Input Channel Selection (ADC)

Default value: 0

AML	MULTIPLEXER INPUT CHANNEL SELECTION
0	Line (default)
1	Microphone

The AML bit selects the input channel of multiplexer.

PG[4:0]: PGA Gain Selection (ADC)

Default value: 0 0100 (–4 dB)

PG[4:0]	PGA Gain Selection	PG[4:0]	PGA Gain Selection
11111	Digital mute	01111	7 dB
11110	Digital mute	01110	6 dB
11101	Digital mute	01101	5 dB
11100	20 dB	01100	4 dB
11011	19 dB	01011	3 dB
11010	18 dB	01010	2 dB
11001	17 dB	01001	1 dB
11000	16 dB	01000	0 dB
10111	15 dB	00111	– 1 dB
10110	14 dB	00110	–2 dB
10101	13 dB	00101	–3 dB
10100	12 dB	00100	–4 dB (default)
10011	11 dB	00011	Digital mute
10010	10 dB	00010	Digital mute
10001	9 dB	00001	Digital mute
10000	8 dB	00000	Digital mute

The PG[4:0] bits control the gain of PGA for adjusting the signal level for ADC.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 75	0	1	0	0	1	0	1	1	RSV	RSV	RSV	RSV	BYP	1	RSV	RSV

BYP: HPF Bypass Control (ADC)

Default value: 0

BYP = 0	Normal output, HPF enable (default)
BYP = 1	Bypass output, HPF disable

The BYP bit controls HPF function; dc components of input and dc offset are converted in bypass mode.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 77	0	1	0	0	1	1	0	1	DACMSK	RSV	AFI5	AFI4	AFI3	COPY	AUDIO	DITMSK

DACMSK: DAC Output Control (DAC)

Default value: 0

DACMSK = 0	Mask disable (default)
DACMSK = 1	Mask DIN to BPZ level

The DACMSK bit is used to mask DIN to BPZ level. The analog outputs from DAC is forced to BPZ level immediately. Larger noise may be generated by this control.

AFI[5:3]: Additional Format Information (DIT)

Default value: 000 (2 audio channels without pre-emphasis)

The AFI[5:3] bits control bits[5:3] of channel status bits in compliance with IEC958.

COPY: Copyright Flag (DIT)

Default value: 0 (Asserted)

The COPY bit controls bit[2] of channel status bits in compliance with IEC958.

AUDIO: Audio Sample Word Type (DIT)

Default value: 0 (PCM)

The AUDIO bit controls bit[1] of channel status bits in compliance with IEC958.

DITMSK: DIT Output Control (DIT)

Default value: 0

DITMSK = 0	Mask disable (default)
DITMSK = 1	Force DOUTS to encoded ZERO status

The DITMSK bit forces only aux and audio sample words on DOUTS to encoded ZERO status. As for validity and channel status bits, the values in the register are output.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 78	0	1	0	0	1	1	1	0	CAT15	CAT14	CAT13	CAT12	CAT11	CAT10	CAT9	CAT8

CAT[15:8]: Category Code (DIT)

Default value: 0000 0000 (general)

The CAT[15:8] bits control bits[15:8] of channel status bits in compliance with IEC958.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 79	0	1	0	0	1	1	1	1	RSV	RSV	CLK29	CLK28	SF27	SF26	SF25	SF24

CLK[29:28]: Clock Accuracy (DIT)

Default value: 00 (level II)

The CLK[29:28] bits control bits[29:28] of channel status bits in compliance with IEC958.

SF[27:24]: Sampling Frequency (DIT)

Default value: 0000 (44.1 kHz)

The SF[27:24] bits control bits[27:24] of channel status bits in compliance with IEC958.

	B15	B14	B13	B12	B11	B10	B9	B8 •	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 80	0	1	0	1	0	0	0	0	VALIDL	VALIDR	SPDIF	RSV	WL35	WL34	WL33	WL32

VALIDL: Validity Bit for L-channel (DIT)

Default value: 0 (valid)

The VALIDL bit controls the validity bit for L-channel in compliance with IEC958.

VALIDR: Validity Bit for R-channel (DIT)

Default value: 0 (valid)

The VALIDR bit controls validity bit for R-channel in compliance with IEC958.

SPDIF: S/PDIF Output Control (DIT)

Default value: 0

SPDIF = 0	DOUTS disabled (default)
SPDIF = 1	DOUTS enabled

The SPDIF bit controls output from DOUTS pin. In case of default, DOUTS always becomes LOW status.

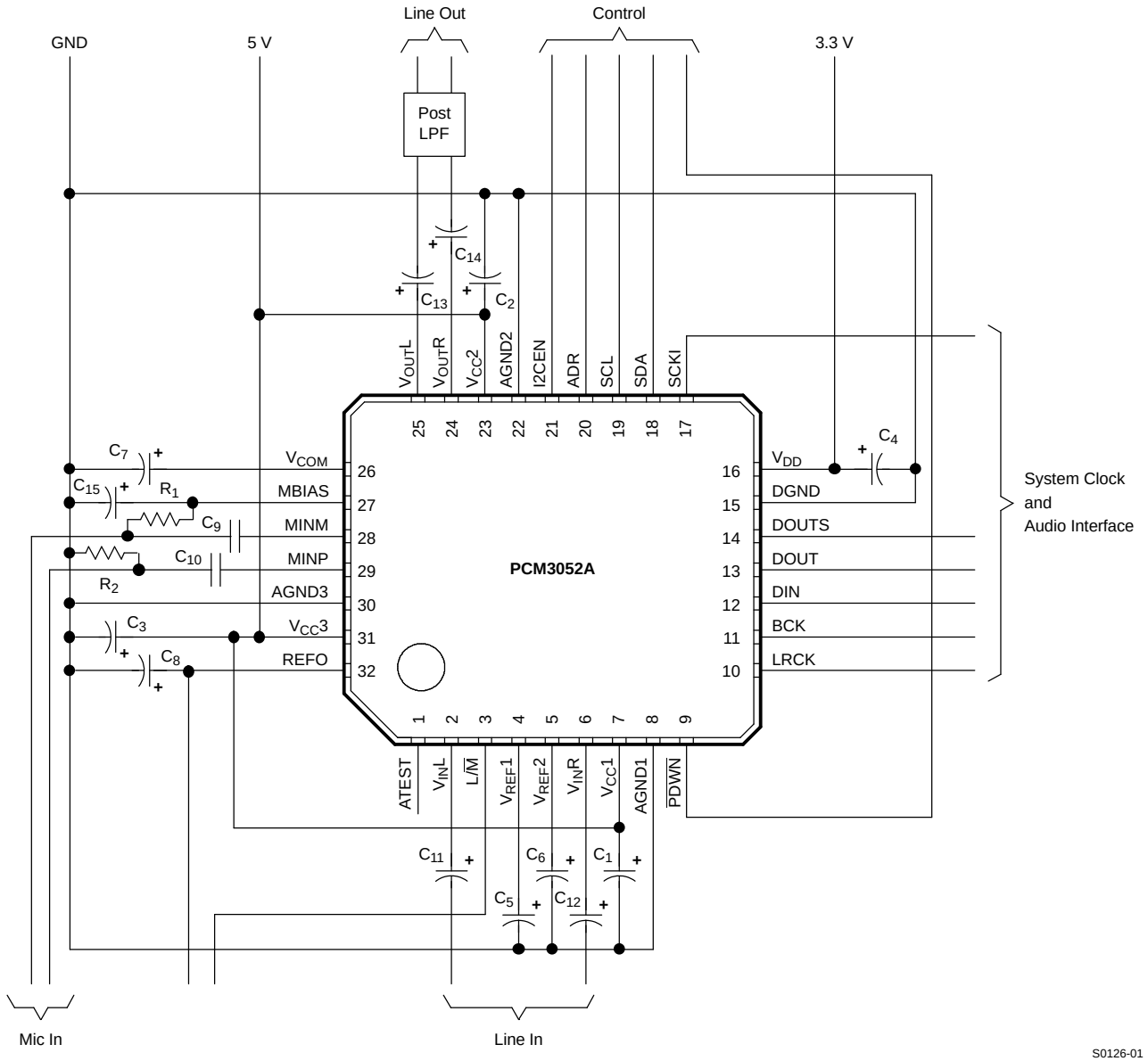
WL[35:32]: Word Length (DIT)

Default value: 0001 (24 bits)

The WL[35:32] bits control bits[35:32] of channel status bits and the actual data word length of audio sample word including auxiliary 4-bits from DOUTS pin in compliance with IEC958. If the WL[35:32] bits indicate 16 bits, the actual data word length of audio sample word is limited to 16 bits even though data input on DIN pin is 24-bits, for example.

TYPICAL CIRCUIT CONNECTION

Figure 56 illustrates typical circuit connection.



NOTE: C_1– C_4: 0.1-µF ceramic and 10-µF electrolytic capacitors typical, depending on power supply quality and pattern layout.
C_5– C_8: 0.1-µF ceramic and 10-µF electrolytic capacitors are recommended.
C_9, C_{10}: 1-µF non-polar electrolytic capacitors are recommended, which give 27-Hz cutoff frequency.
C_{11}, C_{12}: 0.22-µF electrolytic capacitors are recommended, which give 5-Hz cutoff frequency at PGA gain = 0 dB.
C_{13}, C_{14}: 2.2-µF electrolytic capacitors are typical.
C_{15}: 10-µF electrolytic capacitor is recommended.
R_1, R_2: 1-kΩ typical is recommended.

Figure 56. Typical Application Diagram

DESIGN AND LAYOUT CONSIDERATIONS IN APPLICATION

Power Supply Pins ($V_{CC}1$, $V_{CC}2$, $V_{CC}3$, V_{DD})

The digital and analog power supply lines to the PCM3052A should be bypassed to the corresponding ground pins with 0.1-μF ceramic and 10-μF electrolytic capacitors as close to the pins as possible to maximize the dynamic performance of the ADC and DAC.

Although the PCM3052A has four power lines to maximize the potential of dynamic performance, using one common 5-V power supply for $V_{CC}1$, $V_{CC}2$, and $V_{CC}3$. A 3.3-V power supply for V_{DD}, which is generated from the 5-V power supply for $V_{CC}1$, $V_{CC}2$, and $V_{CC}3$, is recommended to avoid unexpected power supply trouble like latch-up or power supply sequencing problems.

Grounding (AGND1, AGND2, AGND3, DGND)

To maximize the dynamic performance of the PCM3052A, the analog and digital grounds are not connected internally. These points should have low impedance to avoid digital noise and signal components feeding back into the analog ground. They should be connected directly to each other under the parts to reduce the potential of noise problems.

$V_{IN}L$, $V_{IN}R$ Pins

A 0.22-μF electrolytic capacitor is recommended as an ac-coupling capacitor, which gives a 5-Hz cutoff frequency at PGA gain = 0 dB. If higher full-scale input voltage is required, it can be adjusted by adding only one series resistor to $V_{IN}X$ pins.

$V_{REF}1$, $V_{REF}2$, V_{COM} Pins

Both 0.1-μF ceramic and 10-μF electrolytic capacitors are recommended from $V_{REF}1$ and $V_{REF}2$ to AGND1, and from V_{COM} to AGND2, to ensure low source impedance of the ADC and DAC references. These capacitors should be located as close as possible to the $V_{REF}1$, $V_{REF}2$, and V_{COM} pins to reduce dynamic errors on the ADC and DAC references.

MBIAS Pin

A 10-μF electrolytic capacitor is recommended between MBIAS and AGND3 to ensure low noise on MBIAS.

REFO Pin

Both 0.1-μF ceramic and 10-μF electrolytic capacitors are recommended between REFO and AGND1 to ensure low noise on REFO.

MINM, MINP Pins

A 1-μF non-polar electrolytic capacitor which gives a 27-Hz cutoff frequency, is recommended as coupling capacitor.

System Clock

The quality of SCKI can influence dynamic performance, as the PCM3052A (both of DAC and ADC) operates based on SCKI. Therefore, it might be necessary to consider the jitter, duty, rise and fall time, etc. of the system clock.

External Mute Control

For power-down ON/OFF control without click noise which is generated by DAC output dc level changes, the external mute control is generally required. The control sequence, which is described as *External Mute ON, CODEC Power Down ON, SCKI stop and resume if necessary, CODEC Power Down OFF, and External Mute OFF*, is recommended.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCM3052ARTF	ACTIVE	VQFN	RTF	32	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCM3052A	Samples
PCM3052ARTFR	ACTIVE	VQFN	RTF	32	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCM3052A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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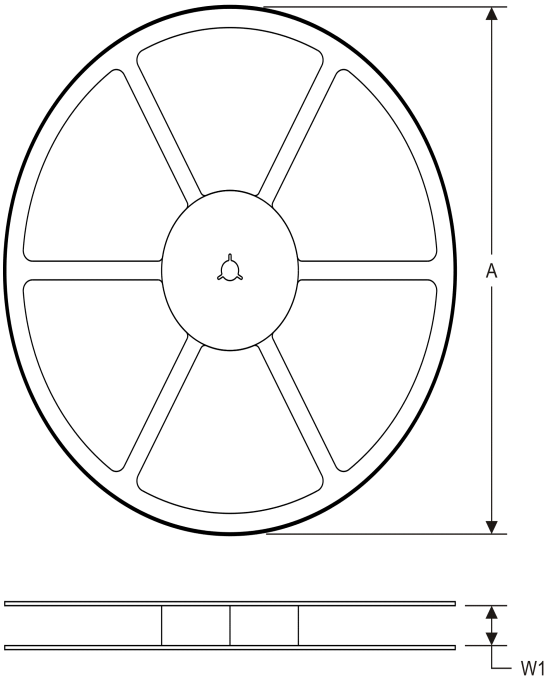
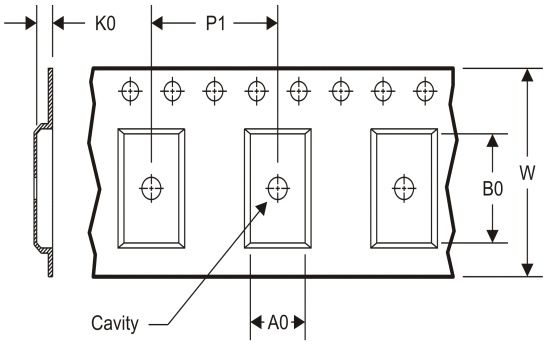
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



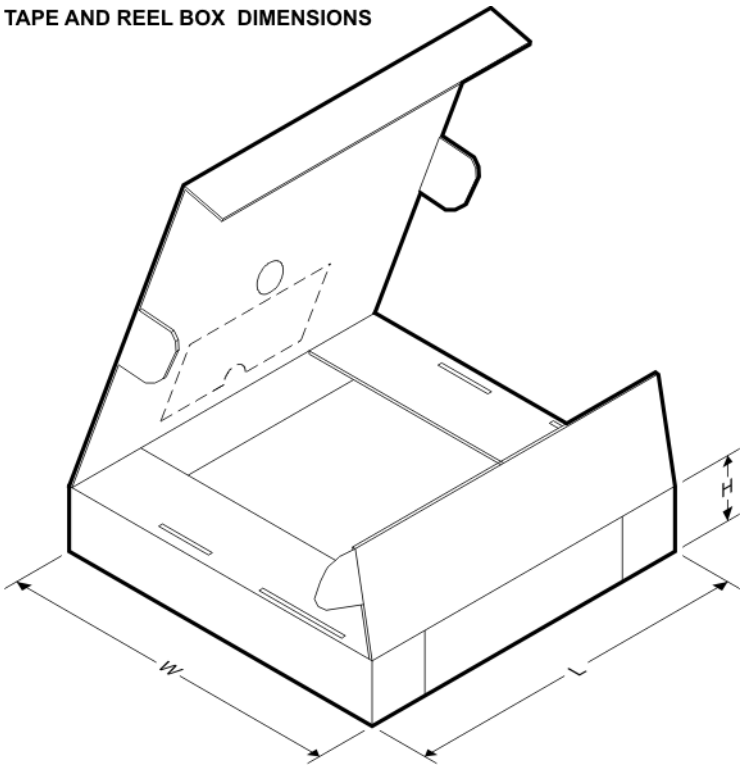
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM3052ARTFR	VQFN	RTF	32	2000	330.0	13.4	5.5	6.5	1.55	8.0	12.0	Q1

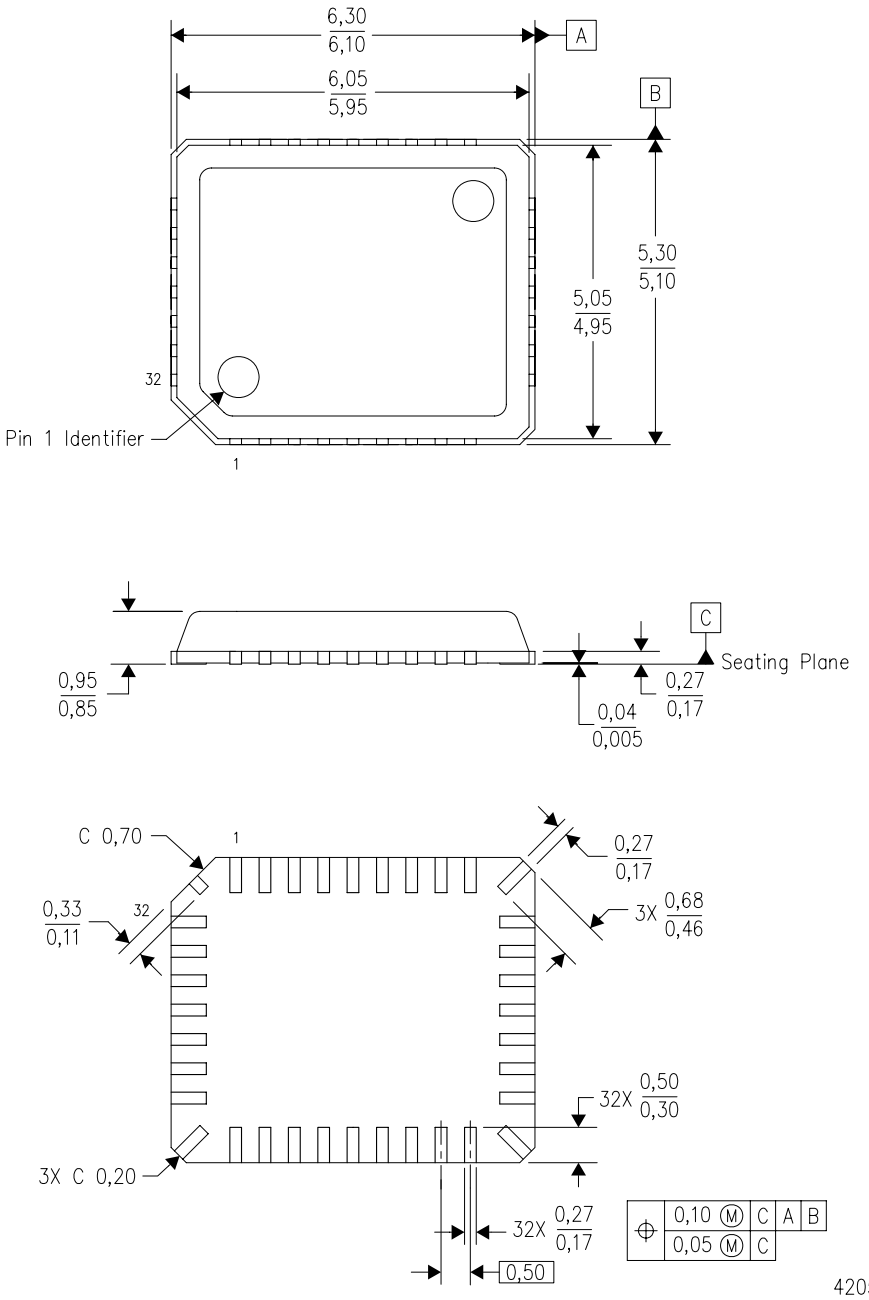
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM3052ARTFR	VQFN	RTF	32	2000	367.0	367.0	35.0

RTF (R–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. These dimensions include package bend.

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