SLAS332 – APRIL 2001

LOW POWER AND LOW VOLTAGE 16-BIT, SINGLE-ENDED ANALOG INPUT/OUTPUT STEREO AUDIO CODEC

FEATURES

- **16-Bit Delta-Sigma ADC and DAC**
- **Stereo ADC:**
  - **Single-Ended Voltage Input**
  - **Anti-Aliasing Filter Included**
  - **High Performance**
    - **THD+N: –84 dB**
    - **SNR: 88 dB**
    - **Dynamic Range: 88 dB**
  - **1/64× Decimation Digital Filter**
    - **Passband Ripple: ±0.05 dB**
    - **Stopband Attenuation: –65 dB**
  - **Digital HPF Included**
- **Stereo DAC:**
  - **Single-Ended Voltage Output**
  - **Analog LPF and FIR Filter Included**
  - **High Performance**
    - **THD+N: –88 dB**
    - **SNR: 92 dB**
    - **Dynamic Range: 92 dB**
  - **8× Oversampling Digital Filter**
    - **Passband Ripple: ±0.1 dB**
    - **Stopband Attenuation: –43 dB**
- **Audio Data Format:**
  - **ADC: 16-bit, Left-Justified**
  - **DAC: 16-bit, Right-Justified**
- **Special Built-In Functions:**
  - **Digital De-Emphasis: 32, 44.1, 48 kHz**
  - **ADC/DAC Independent Power Down With Pop-Noise Free Muting**
- **Sampling Rate: 8 kHz to 48 kHz**
- **System Clock: 256f_S, 384f_S, 512f_S**
- **Low Voltage Power Supply:**
  - **2.4 V TYP, 2.1 V MIN to 3.6 V MAX**
- **Low Power Dissipation:**
  - **32 mW at V_{CC} = 2.4 V**
- **Package: 16-Pin TSSOP**

APPLICATIONS

- **Digital Video Camera**
- **Portable MD Player**
- **Other Portable System**

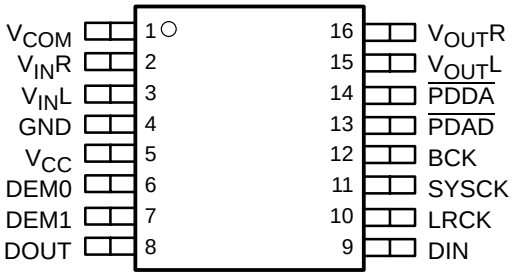
DESCRIPTION

The PCM3008 is a low cost single chip 16-bit stereo audio codec with single-ended analog voltage input and output.

Both ADCs and DACs employ delta-sigma modulation with 64-times oversampling. ADCs include a digital decimation filter and digital high pass filter. DACs include an 8-times oversampling digital interpolation filter, digital de-emphasis filter and pop-noise free muting which works during the power down ON/OFF sequence. The PCM3008 accepts left-justified format for ADC, and right-justified format for DAC. Independent power-down modes for ADC and DAC are provided.

The PCM3008 is suitable for a wide variety of cost-sensitive consumer applications where good performance is required. It is fabricated using a highly advanced CMOS process and is available in a small 16-pin TSSOP package.

PCM3008
PACKAGE
(TOP VIEW)



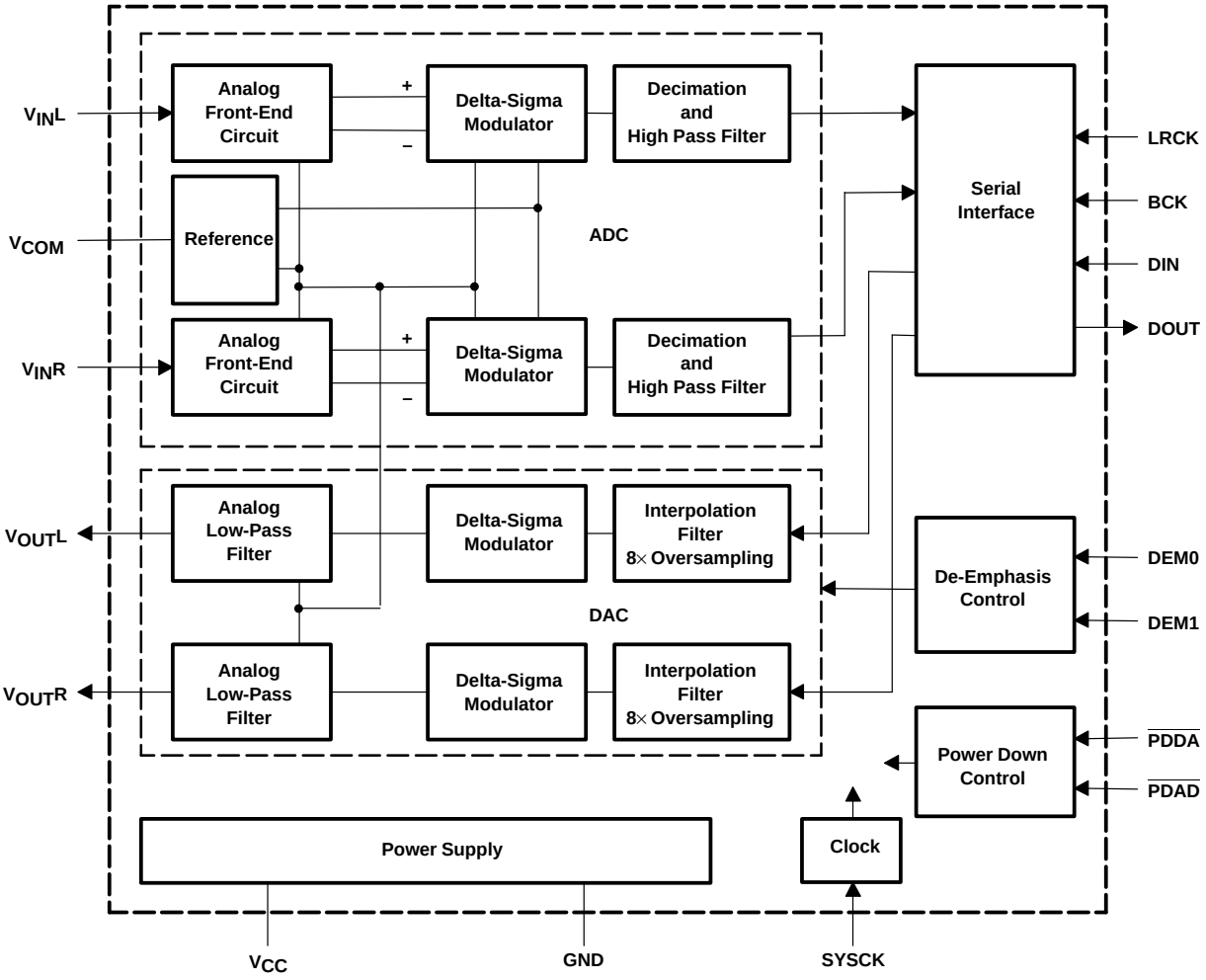
PACKAGE/ORDERING INFORMATION

PRODUCT PACKAGE	PACKAGE	DRAWING NUMBER	OPERATION TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(1)	TRANSPORT MEDIA
PCM3008T	TSSOP–16	ZZ363†	–25 °C to +85 °C	PCM3008T	PCM3008T	Rails
					PCM3008T/2K	Tape and Reel

† TI equivalent no. 4040064.

NOTE: Models with a slash (/) are available only in tape and reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of PCM3008T/2K will get a single 2000-piece tape and reel.

block diagram



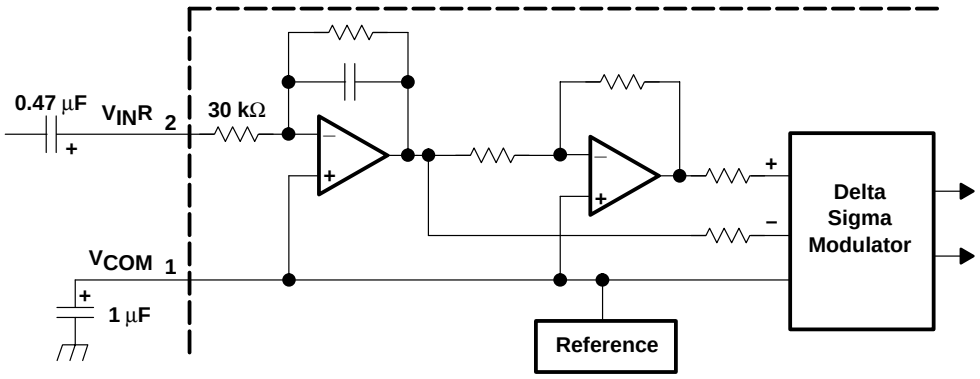


Figure 1. Analog Front-End (right-channel)

Terminal Assignments

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
V_{COM}	1	–	ADC/DAC common decouple (see Note 1)
$V_{IN}R$	2	I	ADC analog input, R-channel.
$V_{IN}L$	3	I	ADC analog input, L-channel.
GND	4	–	Ground.
V_{CC}	5	–	Power supply.
DEM0	6	I	De-emphasis control 0 (see Note 2)
DEM1	7	I	De-emphasis control 1 (see Note 2)
DOUT	8	O	Data output
DIN	9	I	Data input (see Note 2)
LRCK	10	I	Sampling clock input (see Note 2)
SYSCK	11	I	System clock input (see Note 2)
BCK	12	I	Bit clock input (see Note 2)
$\overline{PDAD}$	13	I	ADC power down, active low (see Note 2)
$\overline{PDDA}$	14	I	DAC power down, active low (see Note 2)
$V_{OUT}L$	15	O	DAC analog output, L-channel.
$V_{OUT}R$	16	O	DAC analog output, R-channel.

NOTES: 1. Connect decouple capacitor to GND.
2. Schmitt trigger input, open state can not be allowed because of no internal pullup or pulldown.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC}		4 V
Digital input voltage:	DEM0, DEM1, DIN, LRCK, SYSCK, BCK, $\overline{PDAL}$, $\overline{PDDA}$	–0.3 V to 4 V
	DOUT	–0.3 V to V_{CC} +0.3 V
Analog input voltage		–0.3 V to V_{CC} +0.3 V
Input current (any pins except supplies)		±10 mA
Ambient temperature under bias		–40°C to 125°C
Storage temperature		–55°C to 150°C
Junction temperature		150°C
Lead temperature (soldering)		260°C, 5 s
Package temperature (IR reflow, peak)		235°C, 10 s

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

electrical characteristics, all specifications at T_A = 25°C, V_{CC} = 2.4 V, f_S = 44.1 kHz, system clock = 384f_S, f_{IN} = 1 kHz, 16-bit data, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	PCM3008T			UNIT
			MIN	TYP	MAX	
DIGITAL INPUT/OUTPUT						
V_{IH}(3)	Input logic level		0.7 V_{CC}		3.6	VDC
V_{IL}(3)					0.3V_{CC}	
I_{IN}(3)	Input logic current				±10	µA
V_{OH}(4)	Output logic level	I_O = –400 µA	V_{CC}–0.2			VDC
V_{OL}(4)		I_O = 400 µA			0.2	
CLOCK FREQUENCY						
f_S	Sampling frequency		8	44.1	48	kHz
	System clock frequency	256 f_S	2.0480	11.2896	12.2880	MHz
		384 f_S	3.0720	16.9344	18.4320	
		512 f_S	4.0960	22.5792	24.5760	
ADC CHARACTERISTICS						
	Resolution			16		Bits
DC ACCURACY						
	Gain mismatch channel to channel			±1	±5	% of FSR
	Gain error			±2	±10	
	Bipolar zero error			±0		
DYNAMIC PERFORMANCE(5)						
	THD+N	V_{IN} = –0.5 dB		–84	–74	dB
		V_{IN} = –60 dB		–26		
	Dynamic range	A-weighted	82	88		
	S/N ratio	A-weighted	82	88		
	Channel separation		80	86		
ANALOG INPUT						
	Input voltage			0.6 V_{CC}		$V_{p–p}$
	Center voltage			0.5 V_{CC}		V
	Input impedance			30		kΩ
	Antialiasing filter frequency response	–3 dB		150		kHz
		f_{IN} = 20 kHz		–0.08		dB
DIGITAL FILTER PERFORMANCE						
	Passband				0.454 f_S	Hz
	Stopband		0.583 f_S			
	Passband ripple				±0.05	dB
	Stopband attenuation		–65			
	Delay time			17.4 f_S		s
	HPF frequency response	–3 dB		0.078 f_S		mHz
DAC CHARACTERISTICS						
	Resolution			16		Bits

NOTES: 3. Pins 6, 7, 9, 10–14: DEM0, DEMI, DIN, LRCK, SYSCK, BCK, $\overline{PDAD}$, $\overline{PDDA}$, (Schmitt trigger input, 3.3 V tolerant.
4. Pin 8: DOUT
5. f_{IN} = 1 kHz, using audio precision system II, RMS mode with 20 kHz LPF, 400 Hz HPF in calculation.

electrical characteristics, all specifications at T_A = 25°C, V_{CC} = 2.4 V, f_S = 44.1 kHz, system clock = 384f_S, f_{IN} = 1 kHz, 16-bit data, (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		PCM3008T			UNIT
				MIN	TYP	MAX	
DC ACCURACY							
	Gain mismatch channel to channel				±1	±5	%of FSR
	Gain error				±2	±10	
	Bipolar zero error				±2		
DYNAMIC PERFORMANCE(6)							
	THD+N	V_{OUT} = 0 dB			–88	–78	dB
		V_{OUT} = –60 dB			–30		
	Dynamic range	EIAJ, A-weighted		86	92		
	S/N ratio	EIAJ, A-weighted		86	92		
	Channel separation			84	90		
ANALOG OUTPUT							
	Output voltage				0.6 V_{CC}		$V_{p–p}$
	Center voltage				0.5 V_{CC}		V
	Load impedance	AC coupling		10			kΩ
	LPF frequency response	–3 dB			250		kHz
		f_{IN} = 20 kHz			–0.03		dB
DIGITAL FILTER PERFORMANCE							
	Passband					0.445 f_S	Hz
	Stopband			0.555 f_S			
	Passband ripple					±0.1	dB
	Stopband attenuation			–43			
	Delay time				14.3 f_S		s
POWER SUPPLY REQUIREMENTS							
V_{CC}	Voltage range			2.1	2.4	3.6	VDC
	Supply current	ADC, DAC operation,	V_{CC} = 2.4 V		13.2	17	mA
		ADC operation			8.1	10.5	
		DAC operation			5.6	7.5	
		ADC, DAC power down(7)			20	50	µA
	Power dissipation	ADC, DAC operation,	V_{CC} = 2.4 V		31.7	40.8	mW
		ADC operation			19.4	25.2	
		DAC operation			13.4	18	
		ADC, DAC power down(7)			48	120	µW
TEMPERATURE RANGE							
	Operation temperature	V_{CC} = V_{MIN} to V_{MAX}	f_S > 24 kHz	–25		85	°C
			f_S < 24 kHz	–25		70	
θ_{JA}	Thermal resistance	16-pin TSSOP			150		°C/W

6. f_{IN} = 1 kHz, using audio precision system II, RMS mode with 20 kHz LPF, 400 Hz HPF.
7. SYSCK, BCK, LRCK are stopped.

theory of operation

ADC section

The PCM3008 ADC consists of a reference circuit, a stereo single-to-differential converter, a stereo fully differential 5th-order delta-sigma modulator, a digital decimation filter with high pass filter function and a serial interface circuit. The block diagram in this data sheet illustrates the architecture of the ADC section and Figure 1 shows the single-to-differential converter.

An internal reference circuit with one external capacitor provides all reference voltages required by the ADC and DAC. The internal single-to-differential voltage converter saves the design, space and extra parts needed for external circuitry required by many delta-sigma converters. The internal full-differential signal processing architecture provides a wide dynamic range and excellent power supply rejection performance. The input signal is sampled at 64× oversampling rate, eliminating the need for a sample-and-hold circuit, and simplifying anti-alias filtering requirements. The 5th-order delta-sigma noise shaper consists of five integrators that use a switched-capacitor topology, a comparator and a feedback loop consisting of a one-bit DAC. The delta-sigma modulator shapes the quantization noise, shifting it out of the audio band in the frequency domain.

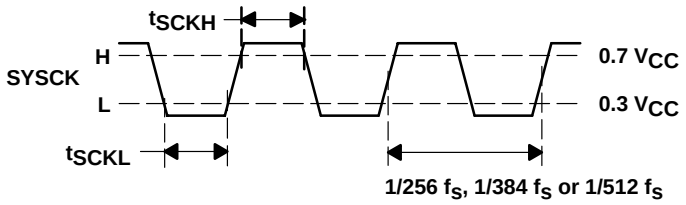
The $64f_S$ one-bit data stream from the modulator is converted to $1f_S$ 16-bit data words by the decimation filter, which also acts as a low pass filter to remove the shaped quantization noise. The dc components are removed by a high pass filter function contained within the decimation filter.

DAC section

The PCM3008 DAC consists of a serial interface circuit, a 8× digital interpolation filter with de-emphasis filter function, a stereo 5th-order delta-sigma modulator, and a stereo analog FIR filter with LPF and output buffer amplifier. The block diagram in this data sheet illustrates the architecture of the DAC section. $1f_S$ 16-bit audio data is converted to $8f_S$ 18-bit data by an 8× oversampling interpolation filter, and then converted to $64f_S$ one-bit data by delta-sigma modulator. One-bit digital data is converted to an analog signal by a current source D to A, and then high frequency components of the shaped quantization noise out of band is reduced by the analog FIR filter and LPF. The fade in, fade out function in digital domain, and V_{OUT} control circuit in analog domain provide a pop-noise free muting function that is required for the power down on/off control sequence.

system clock

The system clock for PCM3008 must be either $256f_S$, $384f_S$ or $512f_S$, where f_S is the audio sampling frequency. The system clock must be supplied on SYSCK (pin 11). PCM3008 also has a system clock detection circuit that automatically senses $256f_S$, $384f_S$ or $512f_S$ mode, and when $384f_S$ or $512f_S$ system clock is used, the clock is divided into $256f_S$ automatically. The $256f_S$ clock is used to operate the digital filter and the modulator. The system clock must be supplied whenever power is applied and either $\overline{\text{PDAD}}$ or $\overline{\text{PDDA}}$ is HIGH, as the PCM3008 uses dynamic circuits internally. Table 1 lists the relationship of typical sampling frequency and system clock frequency, and Figure 2 illustrates the system clock timing.



SYMBOL	DEFINITION	MIN	UNIT
t_{SCKH}	System clock pulse width HIGH	15	ns
t_{SCKL}	System clock pulse width LOW	15	ns

Figure 2. System Clock Timing

system clock (continued)

Table 1. System Clock Frequencies

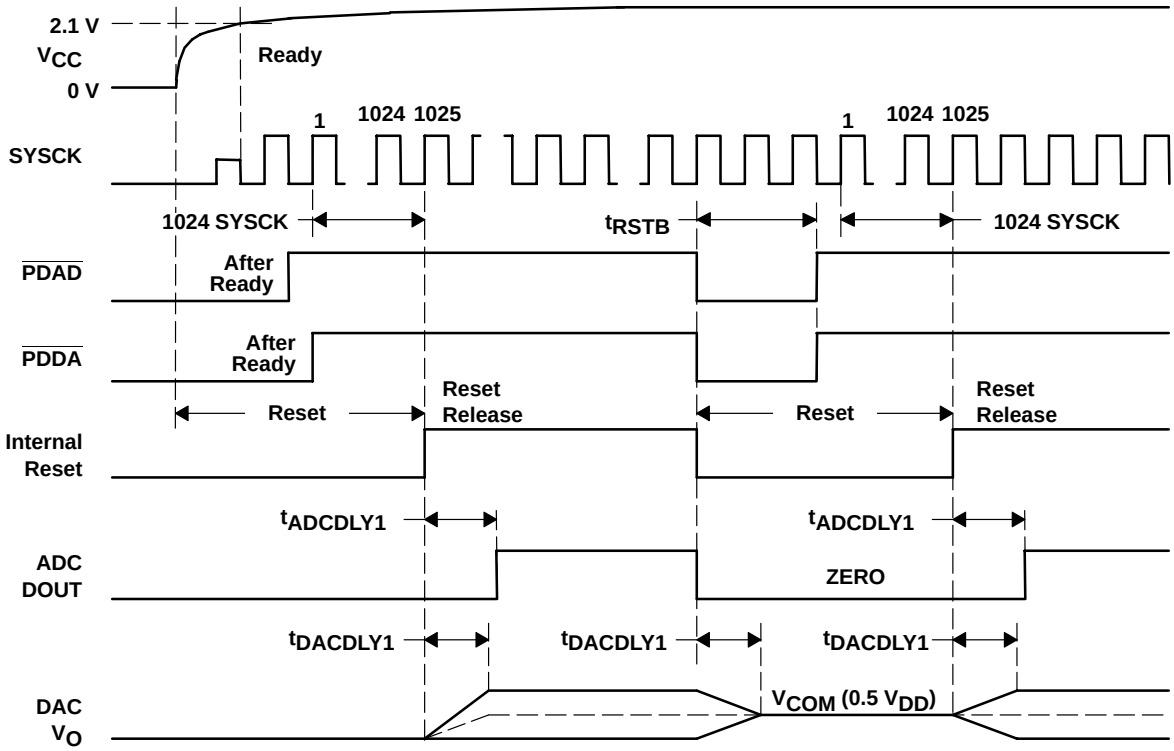
SAMPLING RATE FREQUENCY (kHz)	SYSTEM CLOCK FREQUENCY (MHz)		
	$256f_S$	$384f_S$	$512f_S$
32.0	8.1920	12.2880	16.3840
44.1	11.2896	16.9340	22.5792
48.0	12.2880	18.4320	24.5760

reset

The ADC and DAC portions of the PCM3008 can be reset simultaneously by the power down control pins, $\overline{\text{PDAD}}$ and $\overline{\text{PDDA}}$. This external reset using $\overline{\text{PDAD}}$ and $\overline{\text{PDDA}}$ must be always done at least once after the power is applied. Internal state is kept in reset during $\overline{\text{PDAD}}$ = low and $\overline{\text{PDDA}}$ = low and for 1024 system clock counts after $\overline{\text{PDAD}}$ = high or $\overline{\text{PDDA}}$ = high, and then the initialization sequence for ADC and DAC is started. For the ADC, DOUT is kept in ZERO during the initialization sequence and DOUT outputs normal data corresponding to the input analog signal after $t_{ADCDLY1}$. In the case of the DAC, the fade-in function is started, the signal level on V_{OUT} increases gradually and reaches to full level corresponding to the input digital signal after $t_{DACDLY1}$. The following figure illustrates the reset timing for power-on and the ADC/DAC output response for the power-on and reset sequence.

PCM audio interface

Digital audio data is interfaced to the PCM3008 on LRCK (pin 10), BCK (pin 12), DIN (pin 9), and DOUT (pin 8). PCM3008 can accept 16-bit standard format, right-justified 16 bit for DAC and left-justified 16 bit for ADC. PCM3008 accepts 3 types of BCK and LRCK combination, with 64, 48 or 32 clocks of BCK in one clock of LRCK. The following figures illustrate audio data input/output format and timing.



SYMBOL	DEFINITION	MIN	TYP	MAX	UNIT
t_{RSTB}	$\overline{PDAD}$ = LOW and $\overline{PDDA}$ = LOW pulse width	40			ns
$t_{ADCDLY1}$	Initial delay time		$2240/f_S$		s
$t_{DACDLY1}$	Fade in, fade out time		$2080/f_S$		s

Figure 3. Power-On Reset Timing

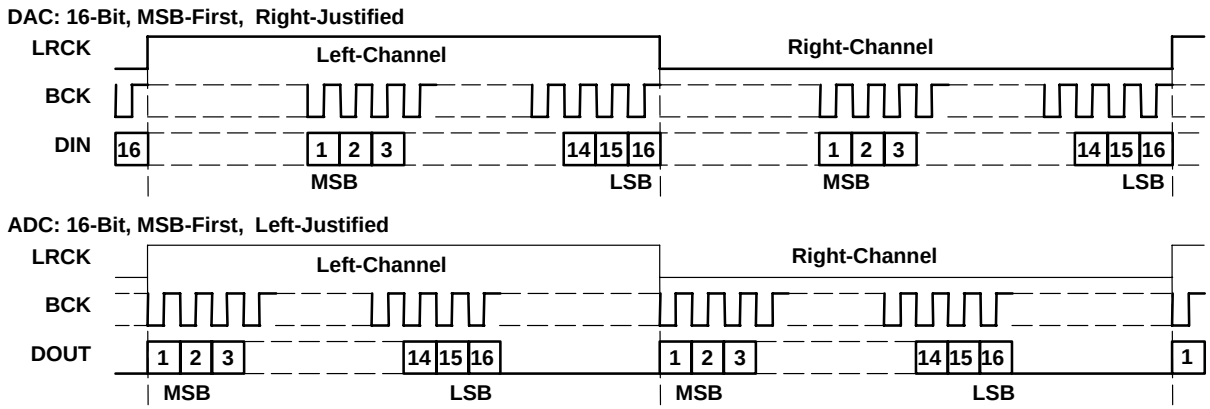
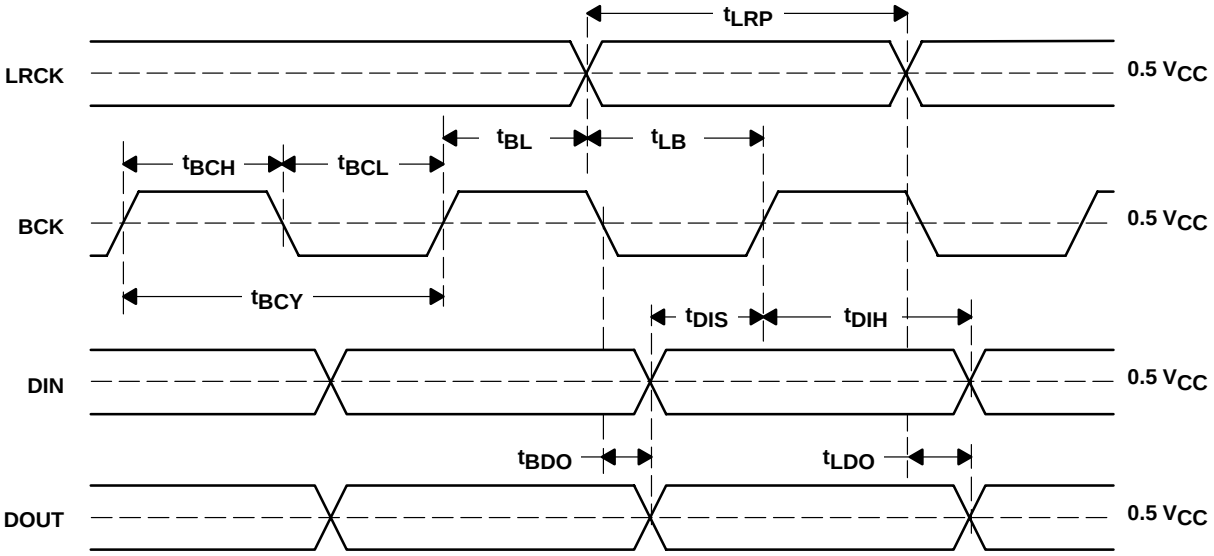


Figure 4. Audio Data Input/Output Format

PCM audio interface (continued)



SYMBOL	DEFINITION	MIN	TYP	MAX	UNITS
t_{BCY}	BCK pulse cycle time	300			ns
t_{BCH}	BCK pulse width high	120			ns
t_{BCL}	BCK pulse width low	120			ns
t_{BL}	BCK rising edge to LRCK edge	40			ns
t_{LB}	LRCK edge to BCK rising edge	40			ns
t_{LRP}	LRCK pulse width	t_{BCY}			
t_{DIS}	DIN setup time	40			ns
t_{DIH}	DIN hold time	40			ns
t_{BDO}	DOUT delay time to BCK falling edge			40	ns
t_{LDO}	DOUT delay time to LRCK edge			40	ns
t_R	Rising time of all signals			20	ns
t_F	Falling time of all signals			20	ns

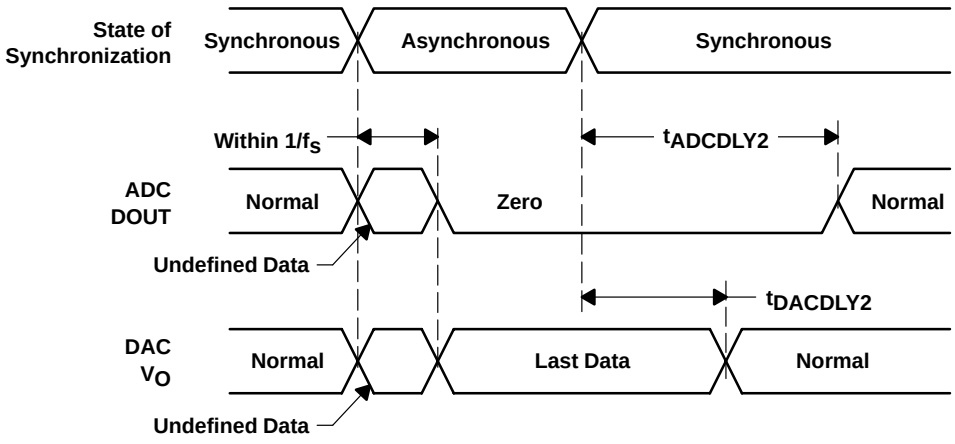
Figure 5. Audio Data Input/Output Timing

synchronization with digital audio system

PCM3008 operates with LRCK synchronized to the system clock. PCM3008 does not need a specific phase relationship between LRCK and system clock, but does require the synchronization of LRCK and system clock. If the relationship between system clock and LRCK changes more than ±4 BCK during one sample period, internal operation of DAC halts within $1/f_S$, and analog output is held at the last data until re-synchronization between system clock and LRCK is completed, and $t_{DACDLY2}$ has elapsed.

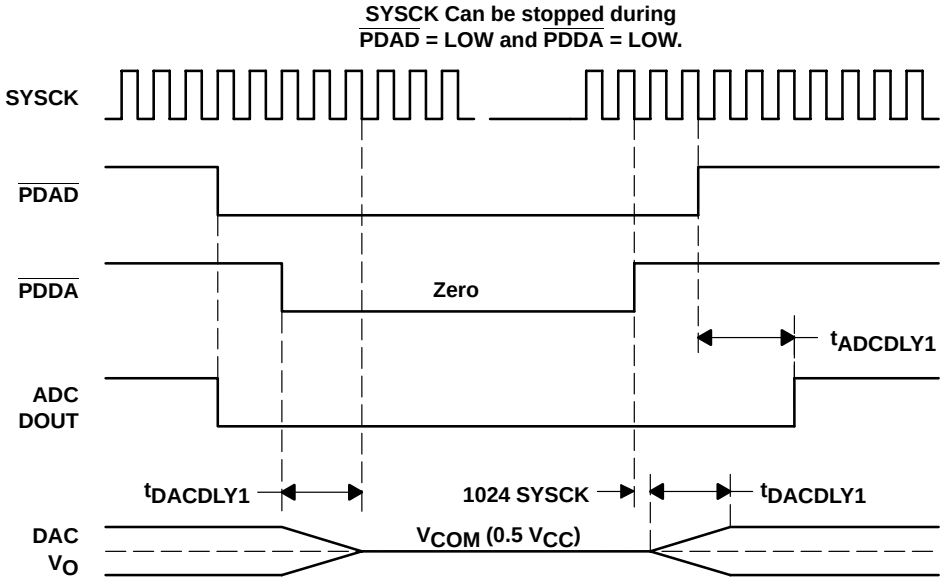
Internal operation of ADC also halts within $1/f_S$, and digital output is forced into ZERO code until re-synchronization between system clock and LRCK is completed and $t_{ADCDLY2}$ has elapsed. In case of changes less than ±4 BCK, re-synchronization does not occur and the above analog/digital output control and discontinuity do not occur. The following figure illustrates the DAC analog output and ADC digital output for loss of synchronization. During undefined data periods, some noise may be generated in the audio signal. Also, the transition of normal to undefined data and undefined data to normal makes a discontinuity of data on analog and digital output, which also may generate some noise in the audio signal.

synchronization with digital audio system (continued)



SYMBOL	DEFINITION	MIN	TYP	MAX	UNIT
$t_{ADCDLY2}$	Delay time from synchronization		$32/f_S$		s
$t_{DACDLY2}$	Delay time from synchronization		$32/f_S$		s

Figure 6. ADC and DAC Output for Loss of Synchronization



SYMBOL	DEFINITION	MIN	TYP	MAX	UNIT
$t_{ADCDLY1}$	Initial delay time		$2240/f_S$		s
$t_{DACDLY1}$	Fade in, fade out time		$2080/f_S$		s

Figure 7. ADC and DAC Output for Power Down Control

function control

The PCM3008 has the following functions which are controlled by $\overline{\text{PDAD}}$ (pin 13), $\overline{\text{PDDA}}$ (pin 14), DEM0 (pin 6) and DEM1 (pin 7).

power-down control

$\overline{\text{PDAD}}$: ADC power-down control pin places the ADC portion in the lowest power consumption mode. The ADC operation is stopped by disabling the clock and bias to the ADC portion, and DOUT is forced to zero during ADC power-down mode. Figure 7 illustrates the ADC DOUT response for ADC power-down ON/OFF. This does not affect the DAC operation.

$\overline{\text{PDAD}}$	ADC OPERATION MODE
Low	ADC power down mode enable
High	ADC power down mode disable

$\overline{\text{PDDA}}$: DAC power-down control pin places the DAC portion in the lowest power consumption mode. The DAC operation is stopped by disabling the clock and bias to the DAC portion, and V_{OUT} is forced to V_{COM} (0.5 V_{CC}) during DAC power-down mode. Figure 7 illustrates the DAC V_{OUT} response for DAC power-down ON/OFF. This does not affect the ADC operation.

$\overline{\text{PDDA}}$	DAC OPERATION MODE
Low	DAC power down mode enable
High	DAC power down mode disable

$\overline{\text{PDAD}}$ = low and $\overline{\text{PDDA}}$ = low places PCM3008 into reset state and either $\overline{\text{PDAD}}$ = high or $\overline{\text{PDDA}}$ = high returns PCM3008 to operational state.

de-emphasis control

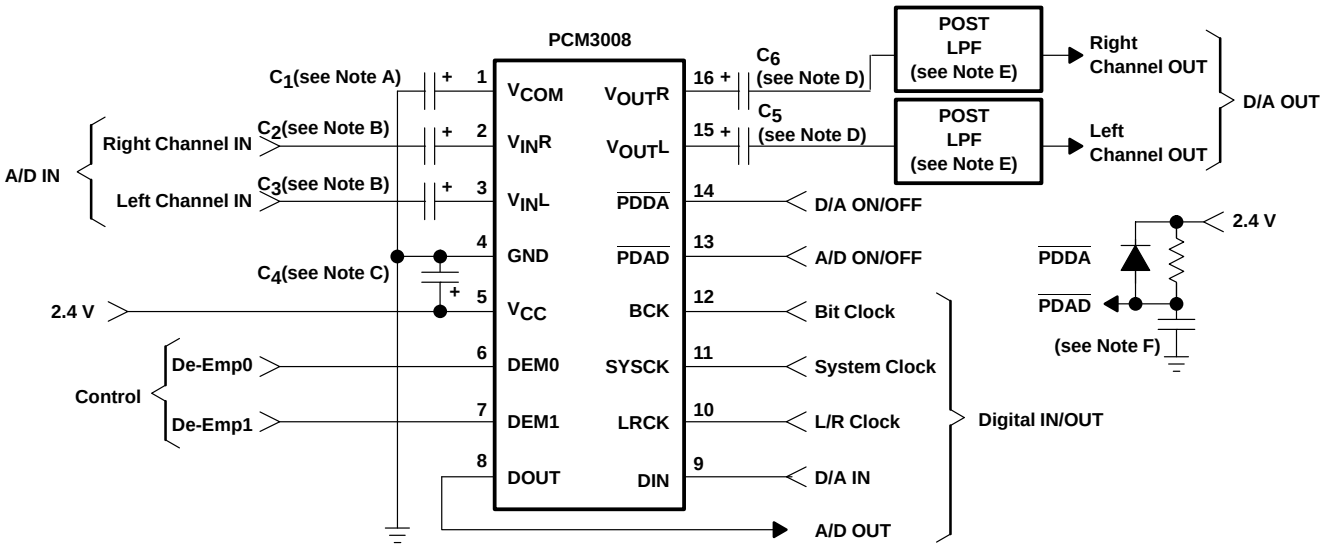
DEM1, DEM0: DAC de-emphasis control pins select the de-emphasis mode as shown below.

DEM1	DEM0	DE-EMPHASIS MODE
Low	Low	De-emphasis 44.1 kHz ON
Low	High	De-emphasis OFF
High	Low	De-emphasis 48 kHz ON
High	High	De-emphasis 32 kHz ON

TYPICAL CHARACTERISTICS

typical circuit connection

The following figure illustrates a typical PCM3008 circuit connection.



NOTES: A. C_1: 0.1 μF ceramic and 1 μF chemical typical, gives settling time with 15 ms (1 μF × 15 kΩ) time constant in power on period.
B. C_2, C_3: 0.47 μF typical, gives 11 Hz cutoff frequency of input HPF in normal operation and gives settling time with 14 ms (0.47 μF × 30 kΩ) time constant in power on and power down off period.
C. C_4: 0.1 μF ceramic and 10 μF chemical typical, depending on power supply quality and pattern layout.
D. C_5, C_6: 1 μF typical, gives 16 Hz cut-off frequency of output HPF in normal operation and gives settling time with 10 ms (1 μF × 10 kΩ) time constant in power on period.
E. Post low pass filter with R_{IN} > 10 kΩ, depending on requirement of system performance.
F. Power on reset circuit in case of no power-down control requirement.

board design and layout considerations

power supply and grounding (V_{CC}, GND)

The analog and digital power supply lines are internally tied, and the analog and digital grounds are internally tied due to pin count limitation. The power supply V_{CC} pin must be bypassed to the GND pin with 0.1 μF ceramic and 10 μF chemical capacitors as close to the pins as possible to maximize the dynamic performance of ADC and DAC.

V_{IN} pins

A chemical capacitor from 0.47 μF to 4.7 μF is recommended as an ac coupling capacitor. Capacitance of 0.47 μF gives 11 Hz cut-off frequency at input HPF. If higher full scale input voltage is required, it can be adjusted by adding only one series resistor to V_{IN} pins.

V_{COM} input

A 0.1 μF ceramic and a 1 μF or larger chemical capacitor are recommended between V_{COM} and GND to ensure low source impedance of ADC and DAC common voltage. This capacitor should be located as close as possible to the V_{COM} pin to reduce dynamic errors on the ADC and DAC common voltage.

TYPICAL CHARACTERISTICS

system clock

Dynamic performance may be influenced by the quality of SYSCK. Therefore the duty cycle, jitter and threshold voltage at the SYSCK pin must be carefully managed. The SYSCK and BCK, LRCK must be supplied whenever the power is applied and either $\overline{\text{PDAD}}$ or $\overline{\text{ODDA}}$ is HIGH, as the PCM3008 uses dynamic circuits internally.

reset control

The PCM3008 does not have an internal power-on reset circuit. Therefore external reset control by $\overline{\text{PDAD}}$ and $\overline{\text{PDDA}}$ must always done at least once after the power is turned on. If neither $\overline{\text{PDAD}}$ nor $\overline{\text{PDDA}}$ is needed in the application, the standard reset circuit which consists of one resistor, one capacitor and one diode is recommended on $\overline{\text{PDAD}}$ and $\overline{\text{PDDA}}$ pins.

external mute control

Although the PCM3008 has an internal muting function for power-down ON/OFF control, if external muting control is required, the recommended control sequence is described by External Mute ON, CODEC Power Down ON, SYSCK stop and resume if necessary, CODEC Power Down OFF and External Mute OFF.

TYPICAL CHARACTERISTICS

ADC

TOTAL HARMONIC DISTORTION PLUS NOISE AT –0.5 dB
vs
FREE-AIR TEMPERATURE

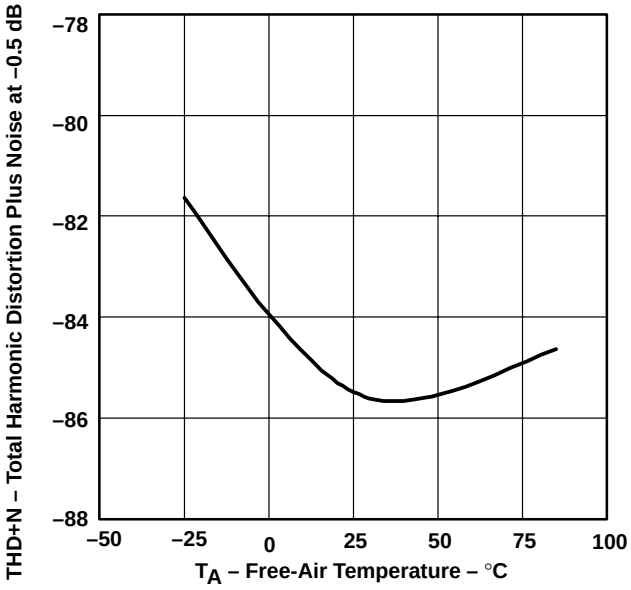


Figure 8

DYNAMIC RANGE AND SNR
vs
FREE-AIR TEMPERATURE

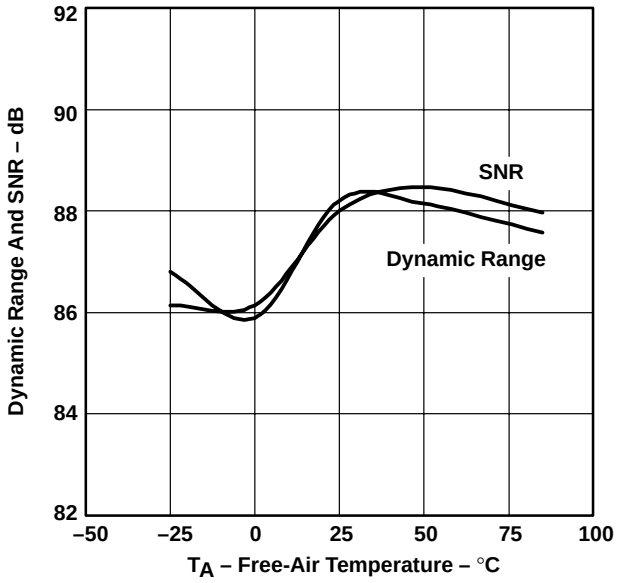


Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE AT –0.5 dB
vs
SUPPLY VOLTAGE

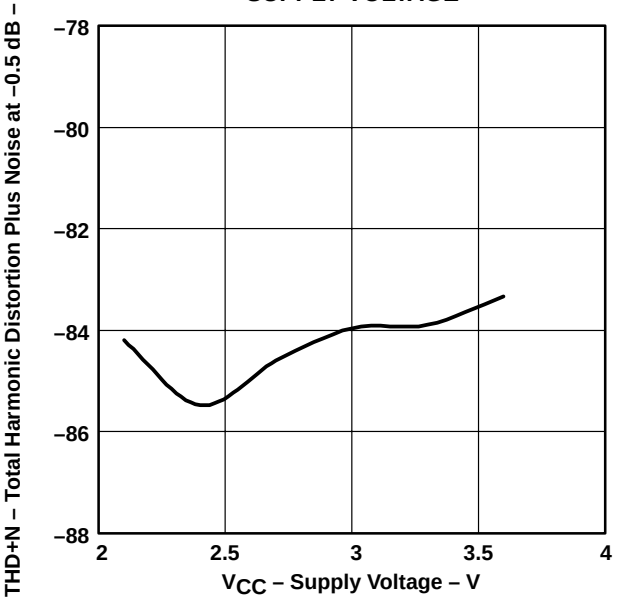


Figure 10

DYNAMIC RANGE AND SNR
vs
SUPPLY VOLTAGE

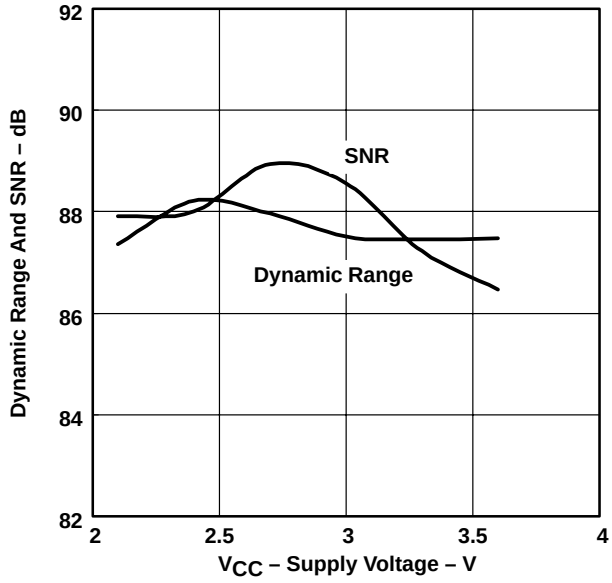


Figure 11

TYPICAL CHARACTERISTICS

ADC

TOTAL HARMONIC DISTORTION PLUS NOISE AT –0.5 dB
vs
SAMPLING FREQUENCY

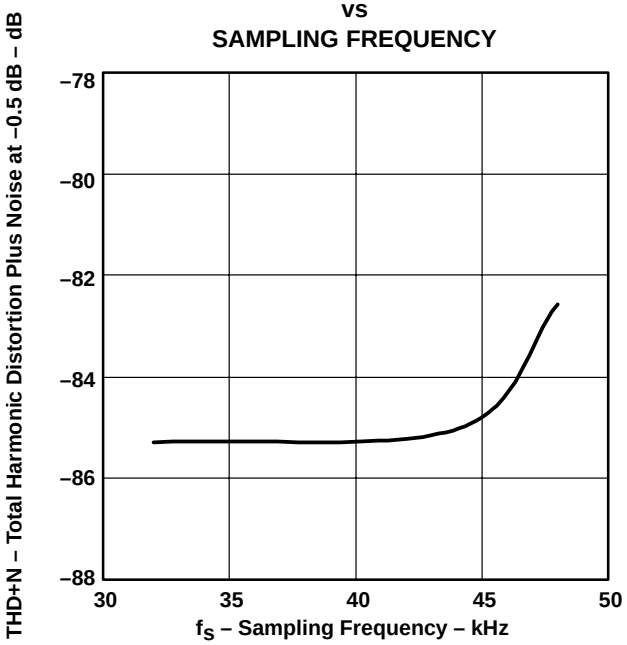


Figure 12

DYNAMIC RANGE AND SNR
vs
SAMPLING FREQUENCY

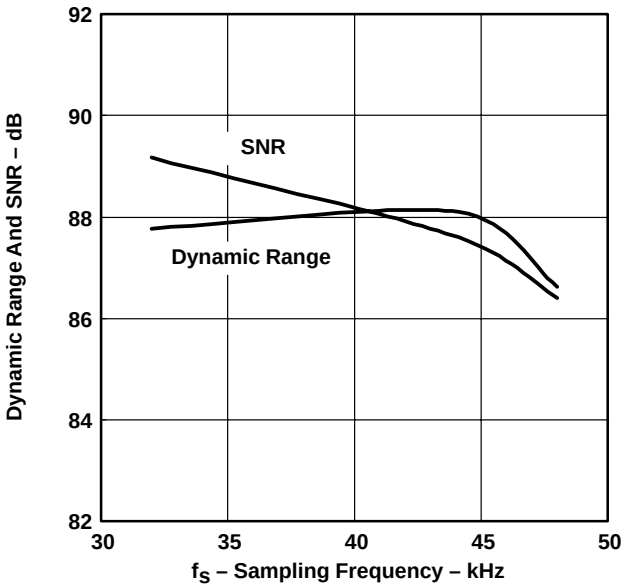


Figure 13

DAC

TOTAL HARMONIC DISTORTION PLUS NOISE AT 0 dB
vs
FREE-AIR TEMPERATURE

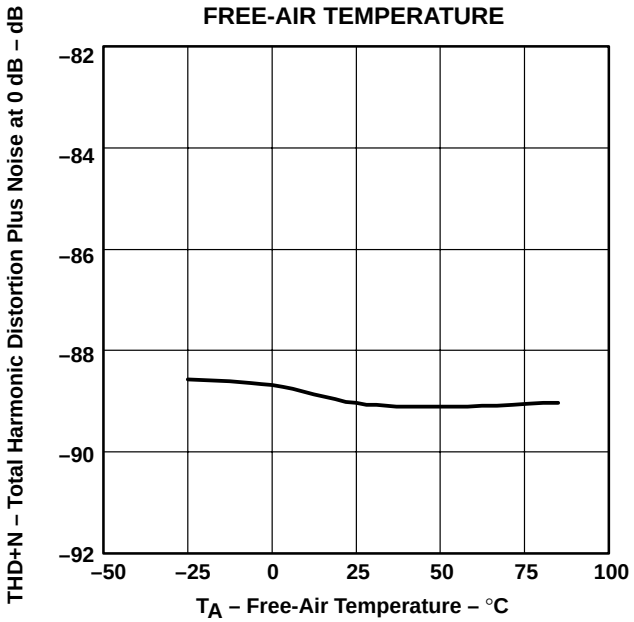


Figure 14

DYNAMIC RANGE AND SNR
vs
FREE-AIR TEMPERATURE

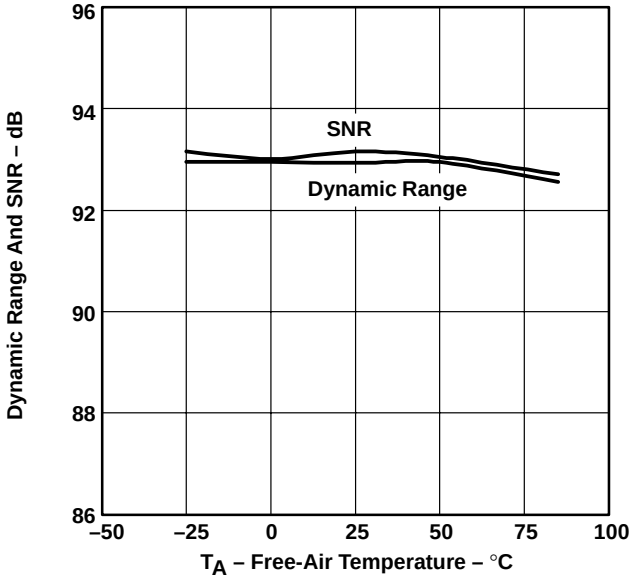


Figure 15

TYPICAL CHARACTERISTICS

DAC

TOTAL HARMONIC DISTORTION PLUS NOISE AT 0 dB vs SUPPLY VOLTAGE

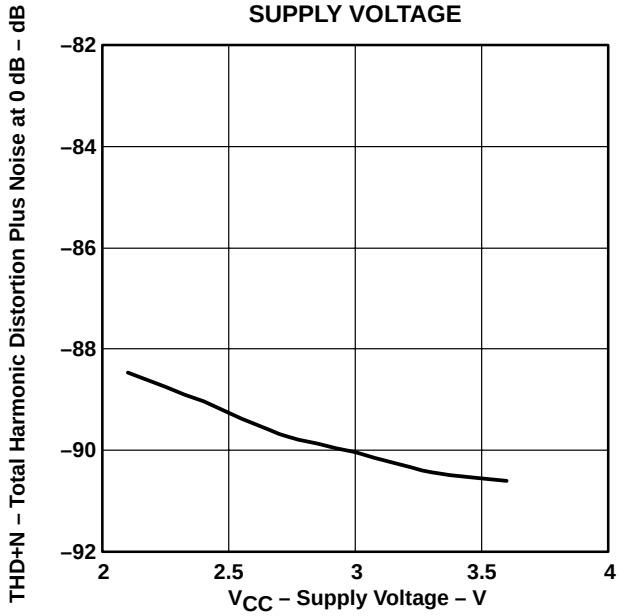


Figure 16

DYNAMIC RANGE AND SNR vs SUPPLY VOLTAGE

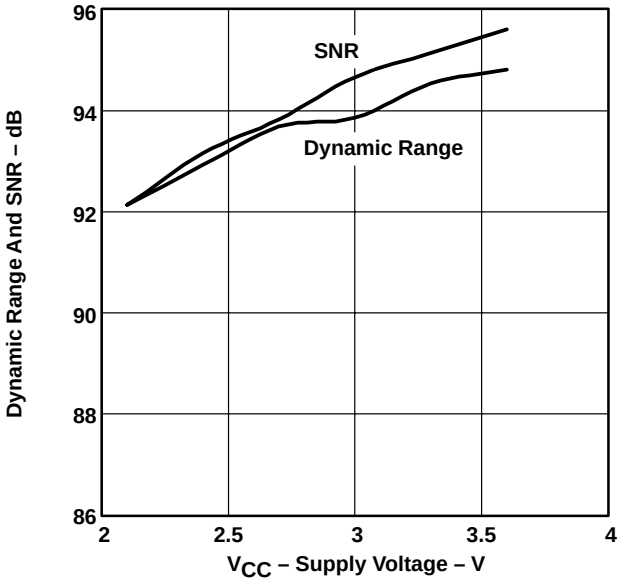


Figure 17

TOTAL HARMONIC DISTORTION PLUS NOISE AT 0 dB vs SAMPLING FREQUENCY

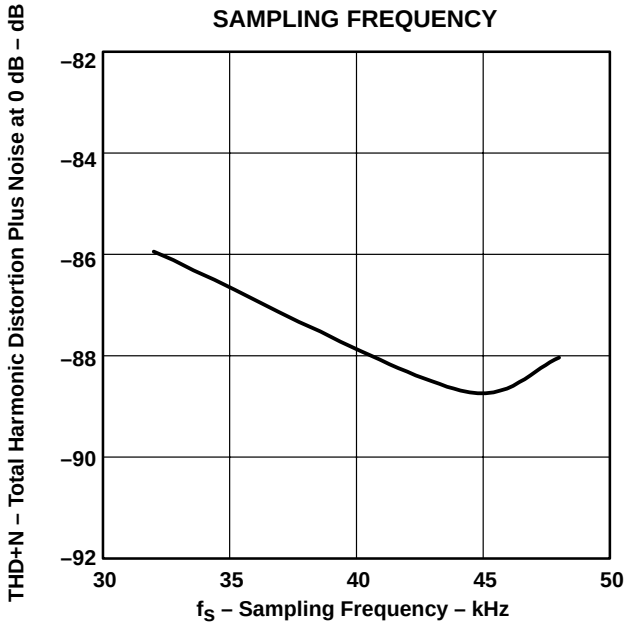


Figure 18

DYNAMIC RANGE AND SNR vs SAMPLING FREQUENCY

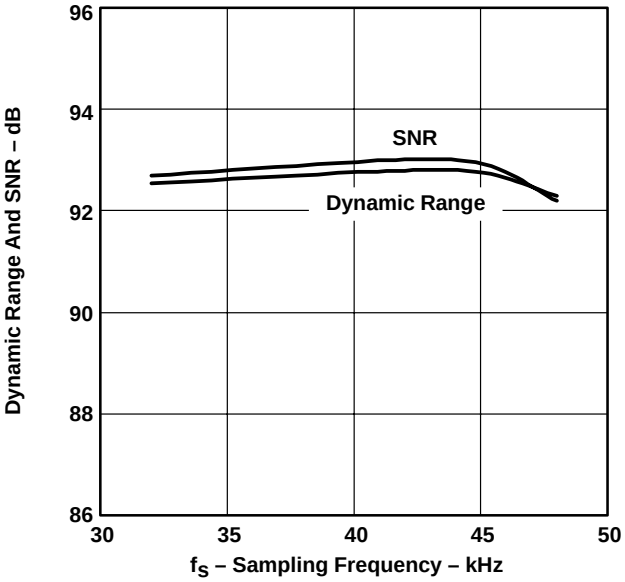


Figure 19

TYPICAL CHARACTERISTICS

ADC

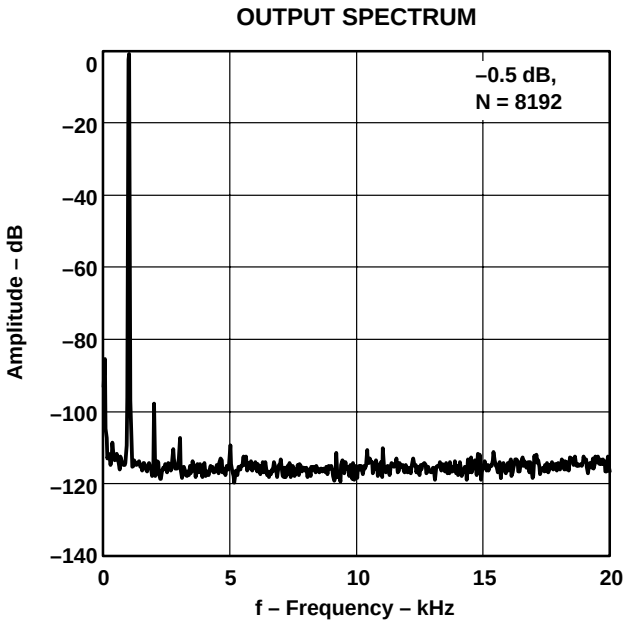


Figure 20

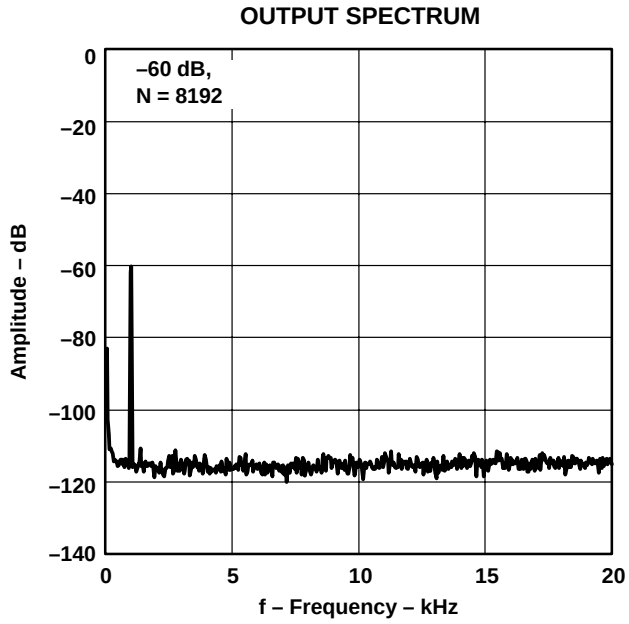


Figure 22

DAC

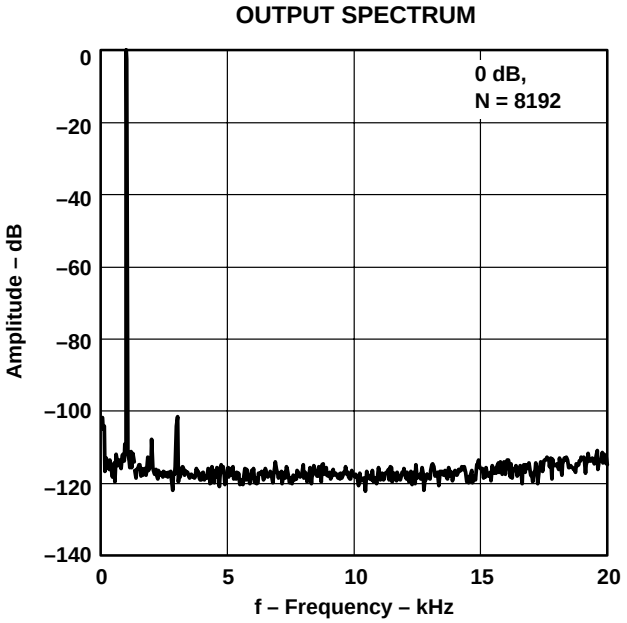


Figure 21

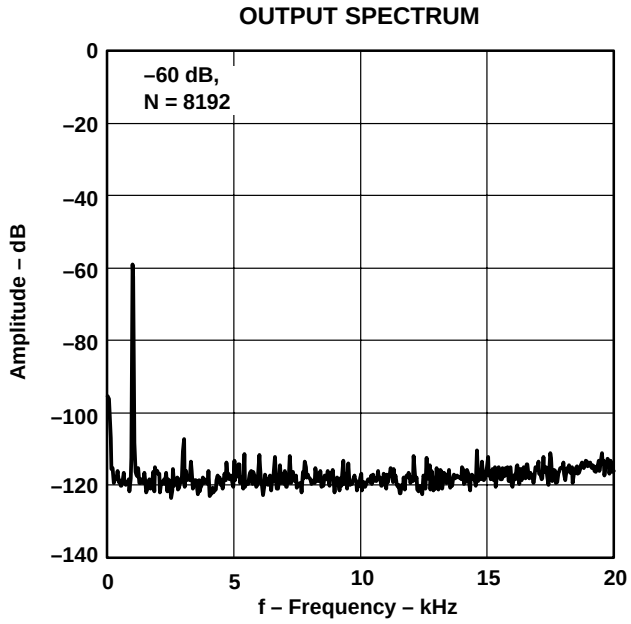


Figure 23

TYPICAL CHARACTERISTICS

ADC

TOTAL HARMONIC DISTORTION PLUS NOISE vs SIGNAL LEVEL

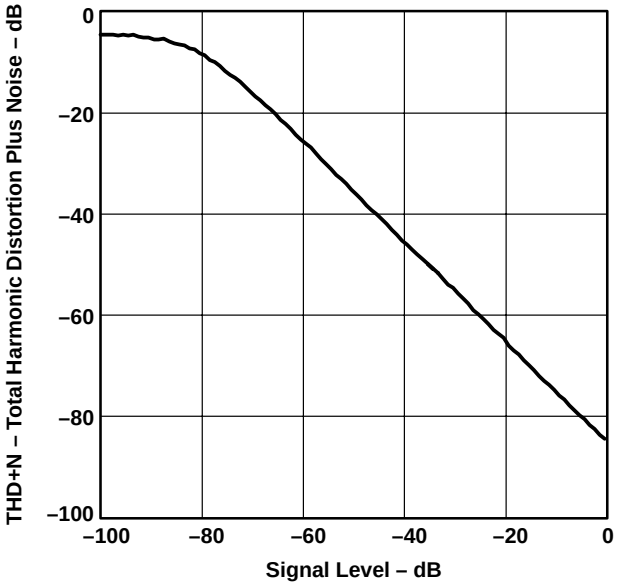


Figure 24

DAC

TOTAL HARMONIC DISTORTION PLUS NOISE vs SIGNAL LEVEL

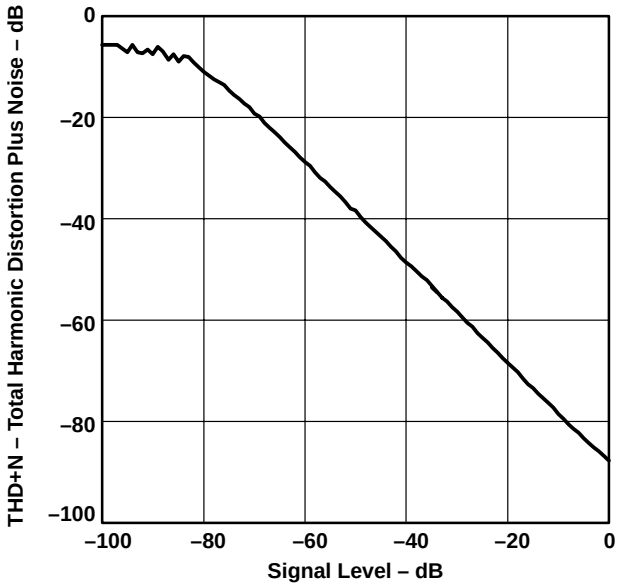


Figure 25

SUPPLY CURRENT vs SUPPLY VOLTAGE

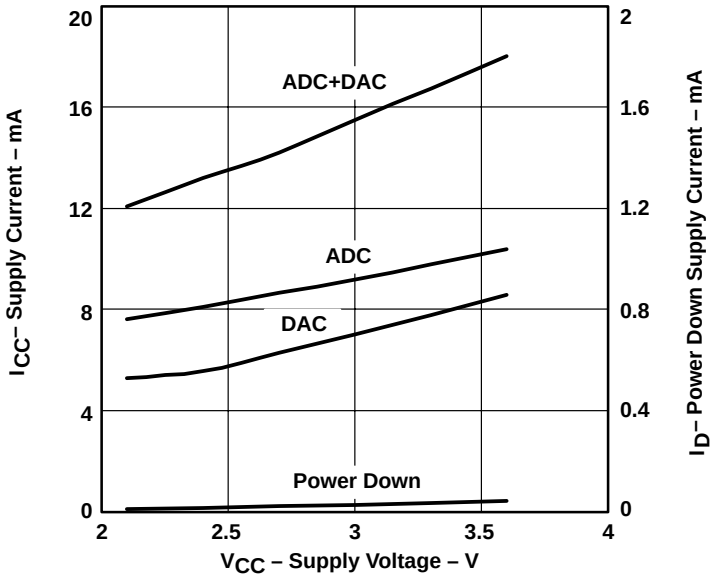


Figure 26

TYPICAL CHARACTERISTICS

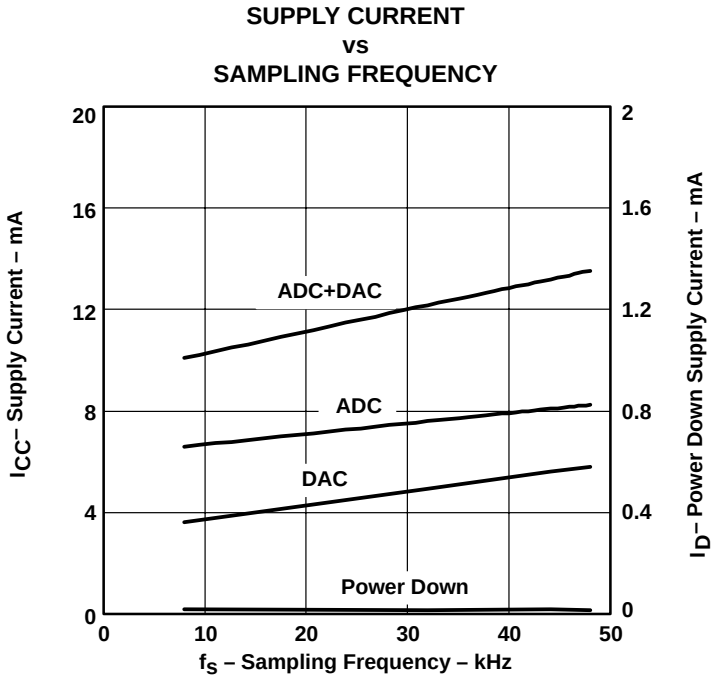


Figure 27

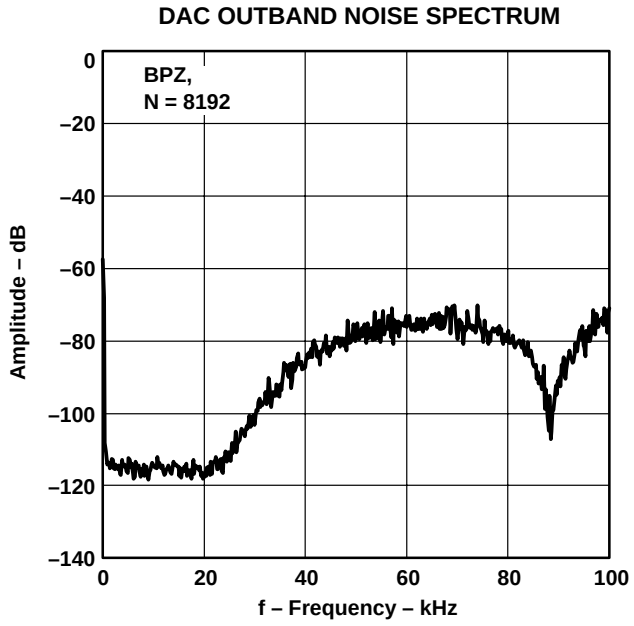


Figure 28

TYPICAL CHARACTERISTICS

ADC digital decimation filter frequency response

OVERALL CHARACTERISTIC

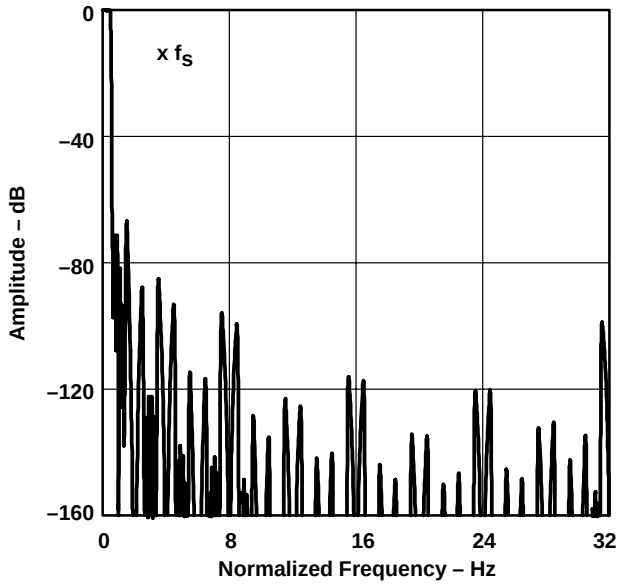


Figure 29

STOPBAND ATTENUATION

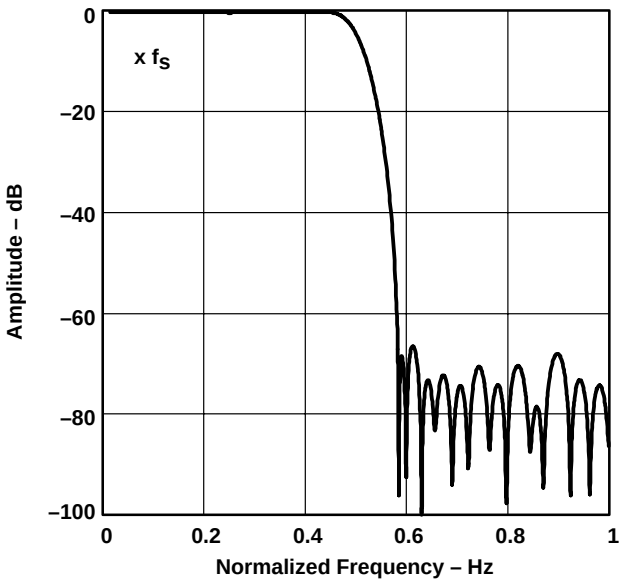


Figure 30

PASSBAND RIPPLE

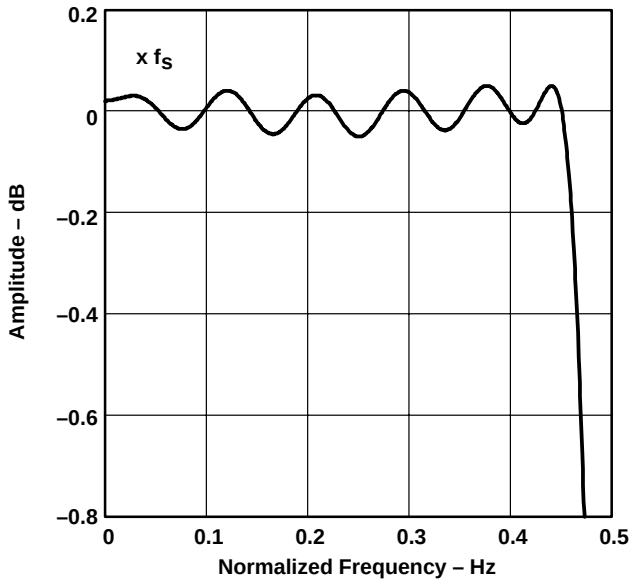


Figure 31

TRANSIENT BAND RESPONSE

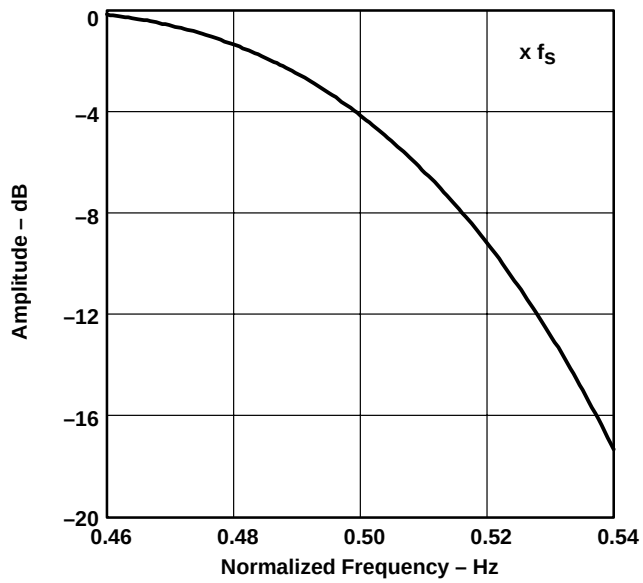


Figure 32

TYPICAL CHARACTERISTICS

digital high pass filter frequency response

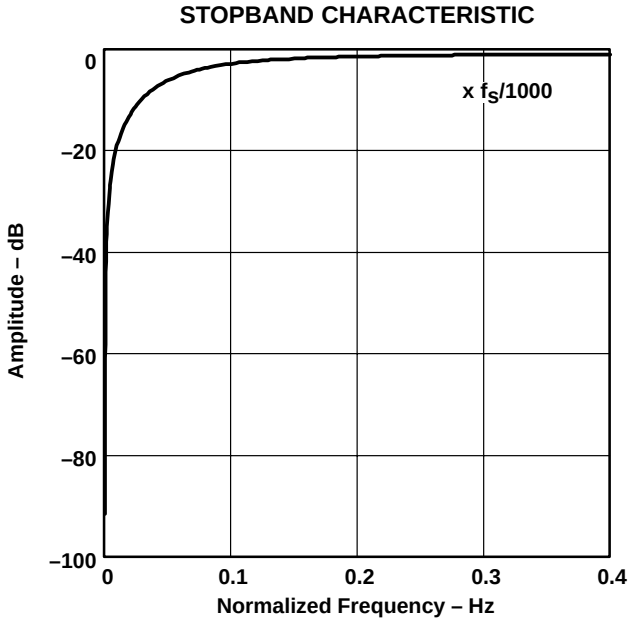


Figure 33

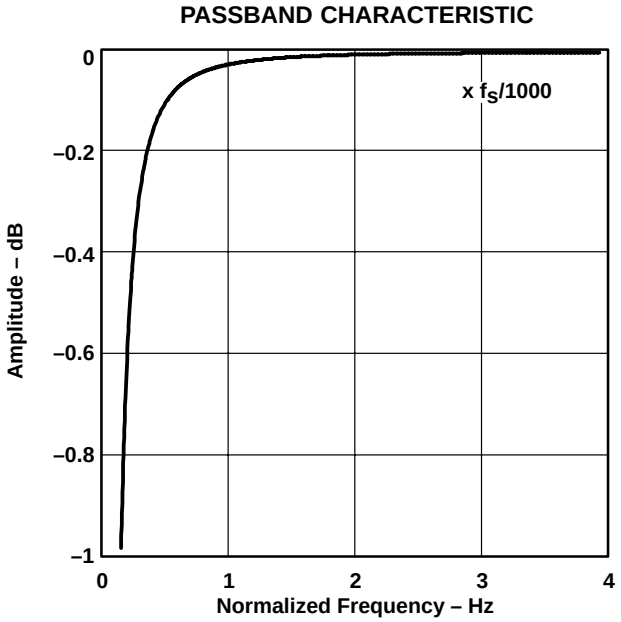


Figure 34

analog antialiasing filter frequency response

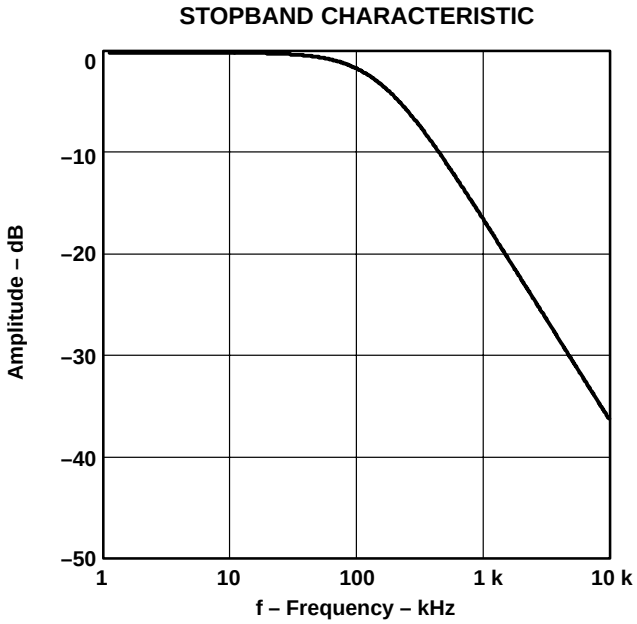


Figure 35

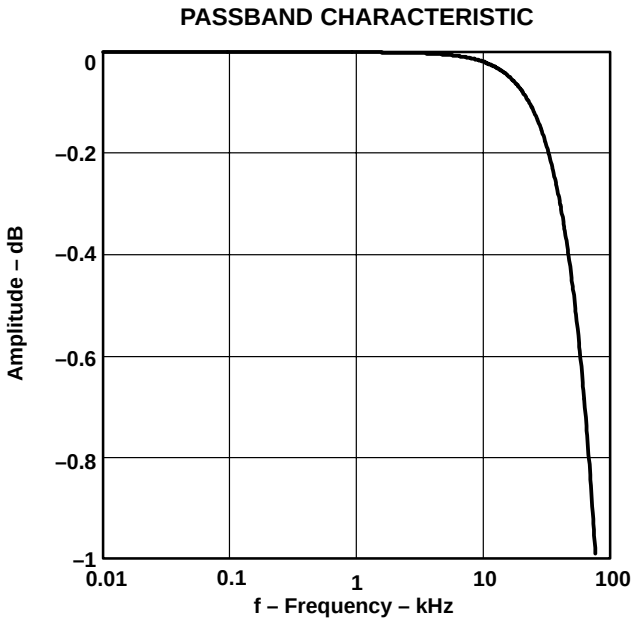


Figure 36

TYPICAL CHARACTERISTICS

DAC digital interpolation and de-emphasis filter frequency response

STOPBAND ATTENUATION

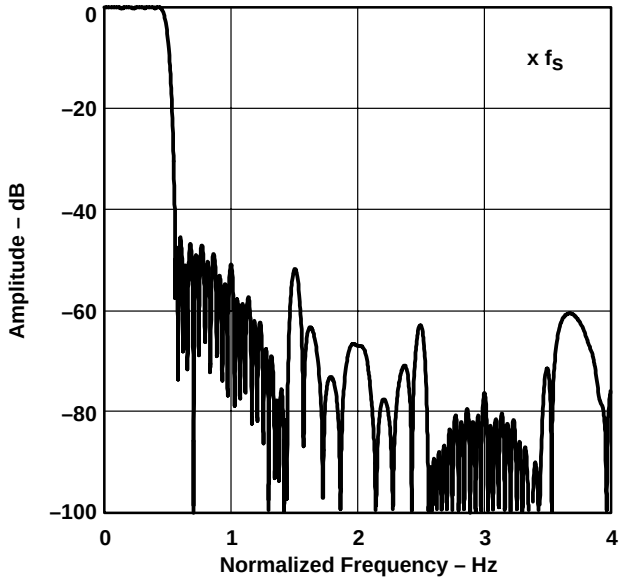


Figure 37

DE-EMPHASIS CHARACTERISTIC (32 kHz)

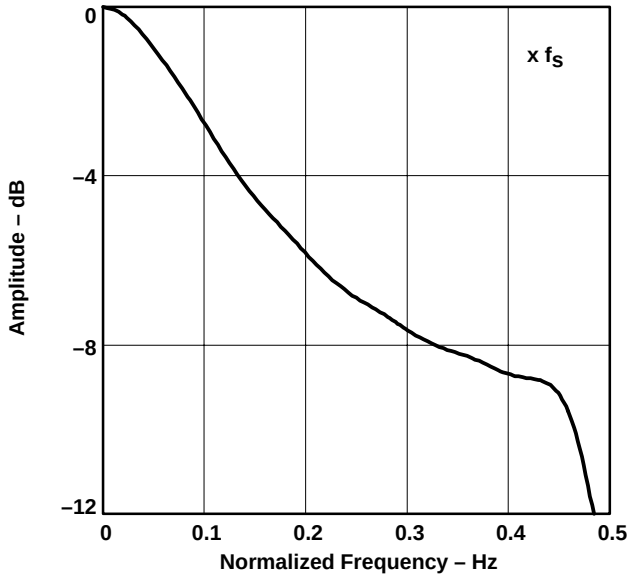


Figure 38

PASSBAND RIPPLE

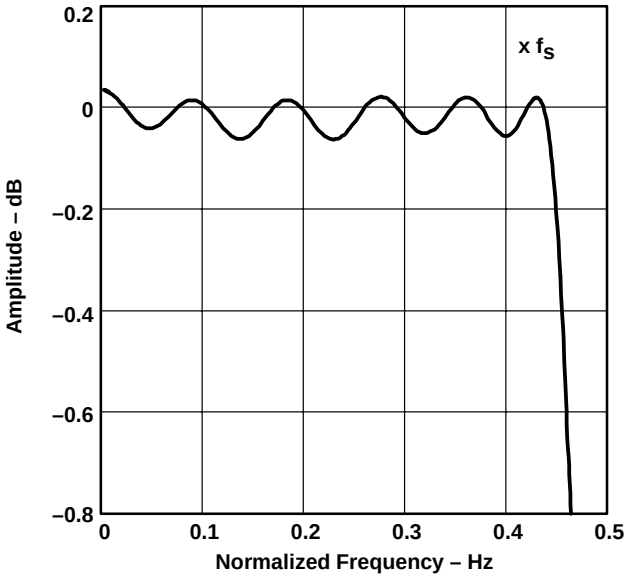


Figure 39

DE-EMPHASIS CHARACTERISTIC (44.1 kHz)

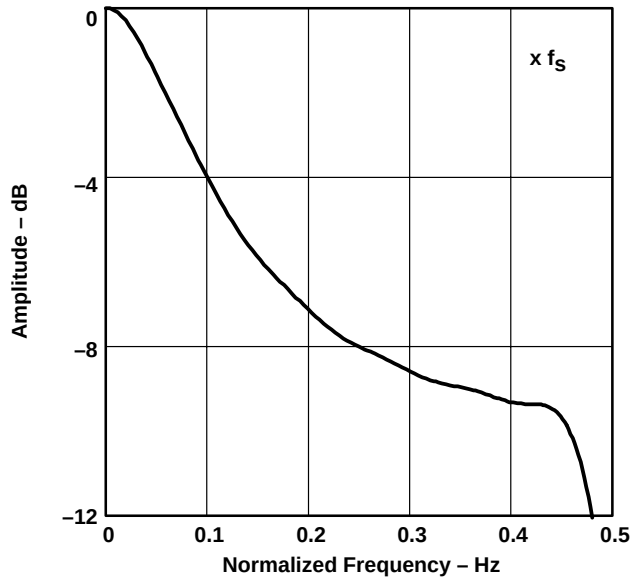


Figure 40

TYPICAL CHARACTERISTICS

DAC digital interpolation and de-emphasis filter frequency response (continued)

TRANSIENT BAND RESPONSE

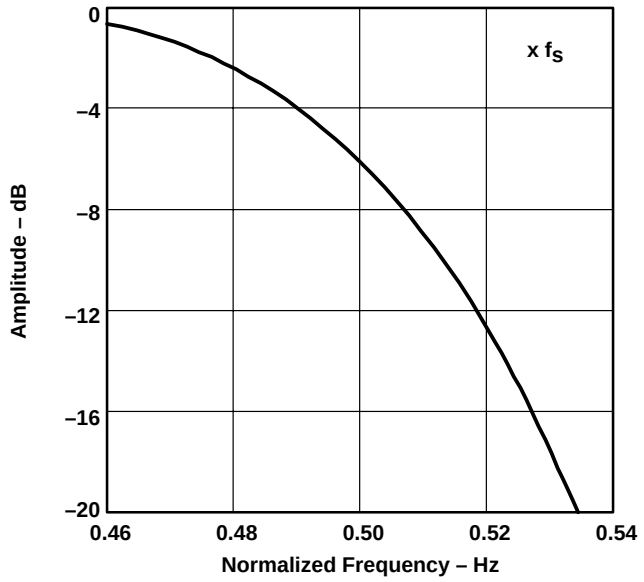


Figure 41

DE-EMPHASIS CHARACTERISTIC (48 kHz)

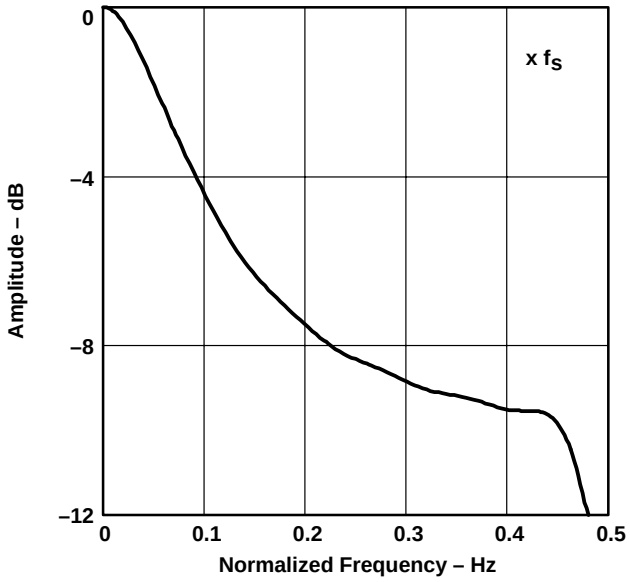


Figure 42

analog FIR filter frequency response

STOPBAND CHARACTERISTIC

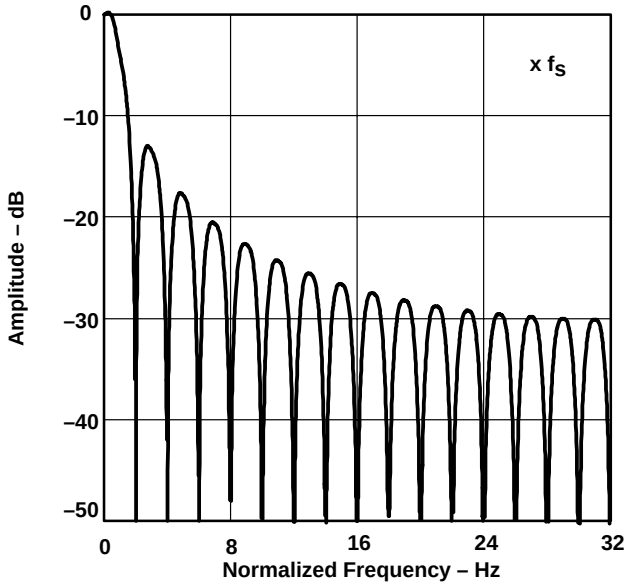


Figure 43

PASSBAND CHARACTERISTIC

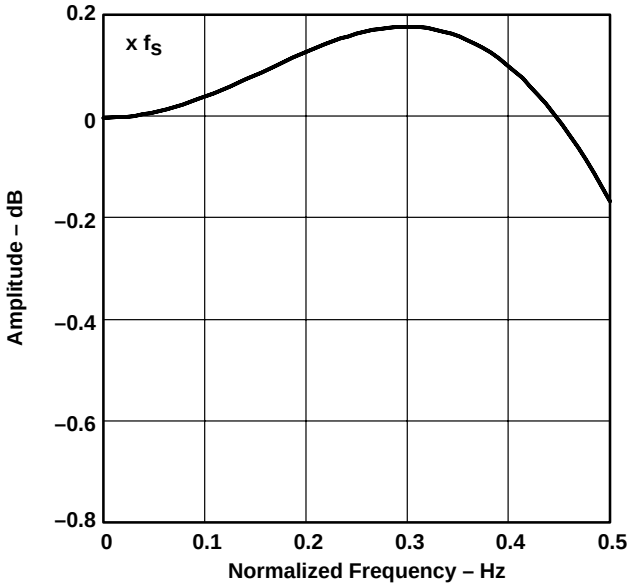


Figure 44

TYPICAL CHARACTERISTICS

analog low pass filter frequency response

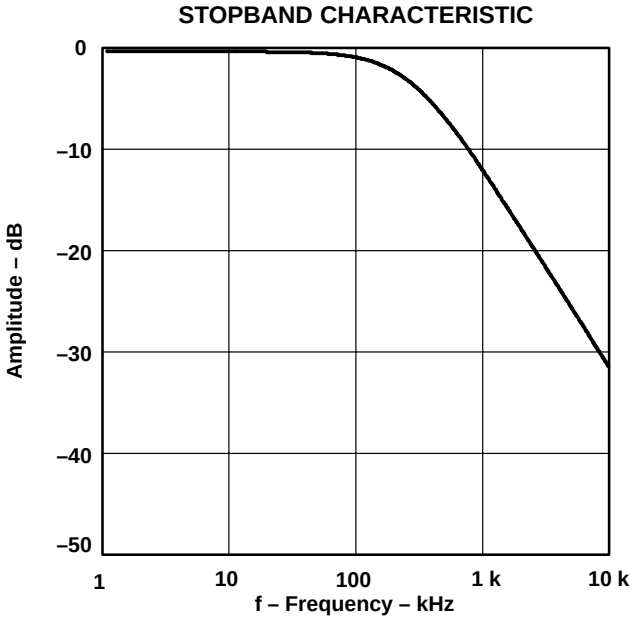


Figure 45

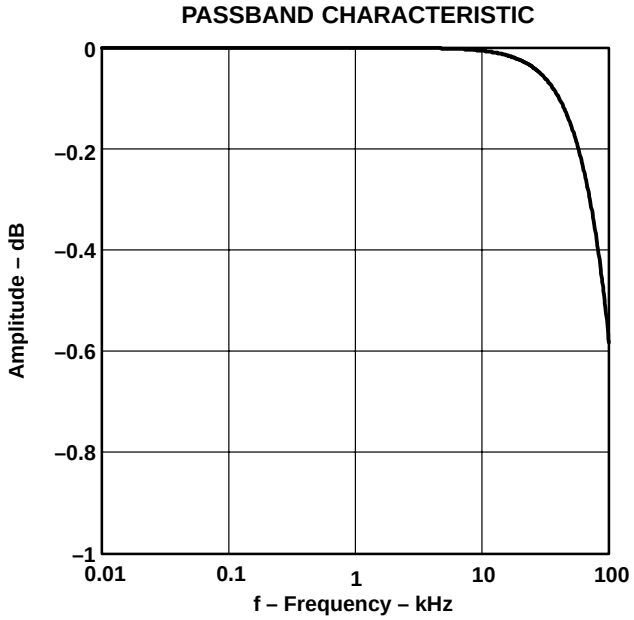
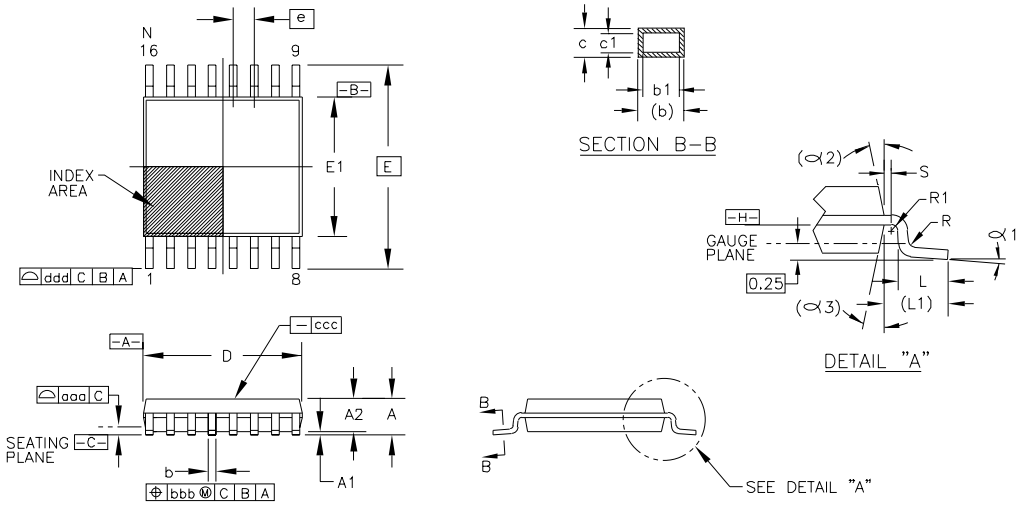


Figure 46

Package Number 363 - 16-Lead TSSOP, .173 Wide



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	--	.047	--	1.20	
A1	.002	.006	0.05	0.15	
A2	.031	.041	0.80	1.05	
b	.007	.012	0.19	0.30	5
b1	.007	.010	0.19	0.25	
c	.004	.008	0.09	0.20	
c1	.004	.006	0.09	0.16	
D	.193	.201	4.90	5.10	3,8
E	.252	BASIC	6.40	BASIC	
E1	.169	.177	4.30	4.50	4,8
e	.0256	BASIC	0.65	BASIC	
L	.018	.030	0.45	0.75	
L1	.039	REF.	1.00	REF.	
N	16		16		6

DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
R	.004	--	0.09	--	
R1	.004	--	0.09	--	
S	.008	--	0.20	--	
aaa	.004	NOM.	0.10	NOM.	
bbb	.004	NOM.	0.10	NOM.	
ccc	.002	NOM.	0.05	NOM.	
ddd	.008	NOM.	0.20	NOM.	
∝1	0°	8°	0°	8°	
∝2	12°	REF.	12°	REF.	
∝3	12°	REF.	12°	REF.	

NOTES:

1. MILLIMETERS SHALL BE CONTROLLING UNIT.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15mm (.006 IN) PER SIDE.
4. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25mm(.010 IN) PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm(.003 IN) TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
6. N IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS.
7. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
8. DIMENSIONS D AND E1 TO BE DETERMINED AT DATUM PLANE -H-.
9. SECTION B-B TO BE DETERMINED AT 0.10mm TO 0.25mm FROM LEAD TIP.
10. PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE CROSSHATCHED INDEX AREA.

PACKAGE NUMBER: ZZ363	REV.: B
JEDEC NUMBER: MO-153-AB	

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