

SLES023B – DECEMBER 2001 – REVISED MARCH 2002

SINGLE-ENDED ANALOG-INPUT 24-BIT, 96-kHz STEREO A/D CONVERTER

FEATURES

- 24-Bit Delta-Sigma Stereo A/D Converter
- Single-Ended Voltage Input: 3 V p-p
- Antialiasing Filter Included
- Oversampling Decimation Filter
  - Oversampling Frequency: ×64, ×128
  - Passband Ripple: ±0.05 dB
  - Stopband Attenuation: –65 dB
  - On-Chip HPF (Low Cut Filter): 0.84 Hz (44.1 kHz)
- High Performance
  - THD+N: 96 dB (Typical)
  - SNR: 105 dB (Typical)
  - Dynamic Range: 105 dB (Typical)
- PCM Audio Interface
  - Master/Slave Mode Selectable
  - Data Formats: 24-Bit Left-Justified; 24-Bit I^2S; 20-, 24-Bit Right-Justified
- Sampling Rate: 16 kHz to 96 kHz
- System Clock: 256 f_S, 384 f_S, 512 f_S, 768 f_S
- Dual Power Supplies: 5 V for Analog, 3.3 V for Digital
- Package: 20-Pin SSOP
- Lead-Free Product

APPLICATIONS

- AV Amp Receiver
- MD Player
- CD Recorder
- Multitrack Receiver
- Electric Musical Instrument

DESCRIPTION

The PCM1802 is a high-performance, low-cost, single-chip stereo analog-to-digital converter with single-ended analog voltage input. The PCM1802 uses a delta-sigma modulator with 64- or 128-times oversampling, and includes a digital decimation filter and HPF (low cut filter) which removes the dc component of the input signal. For various applications, the PCM1802 supports master and slave modes and four data formats in serial interface. The PCM1802 is suitable for a wide variety of cost-sensitive consumer applications where good performance, 5-V analog supply, and 3.3-V digital supply operation is required. The PCM1802 is fabricated using a highly advanced CMOS process and is available in the DB 20-pin SSOP package.



This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriated logic voltage level, preferably either V_{CC} or ground. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.



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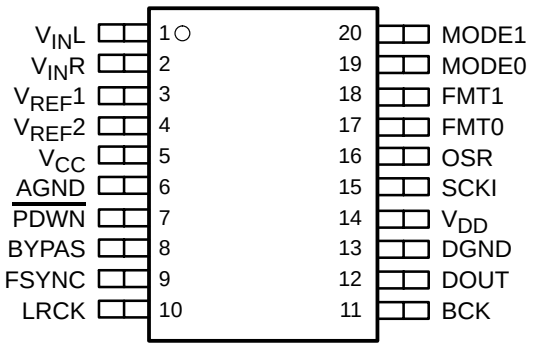
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PACKAGE/ORDERING INFORMATION

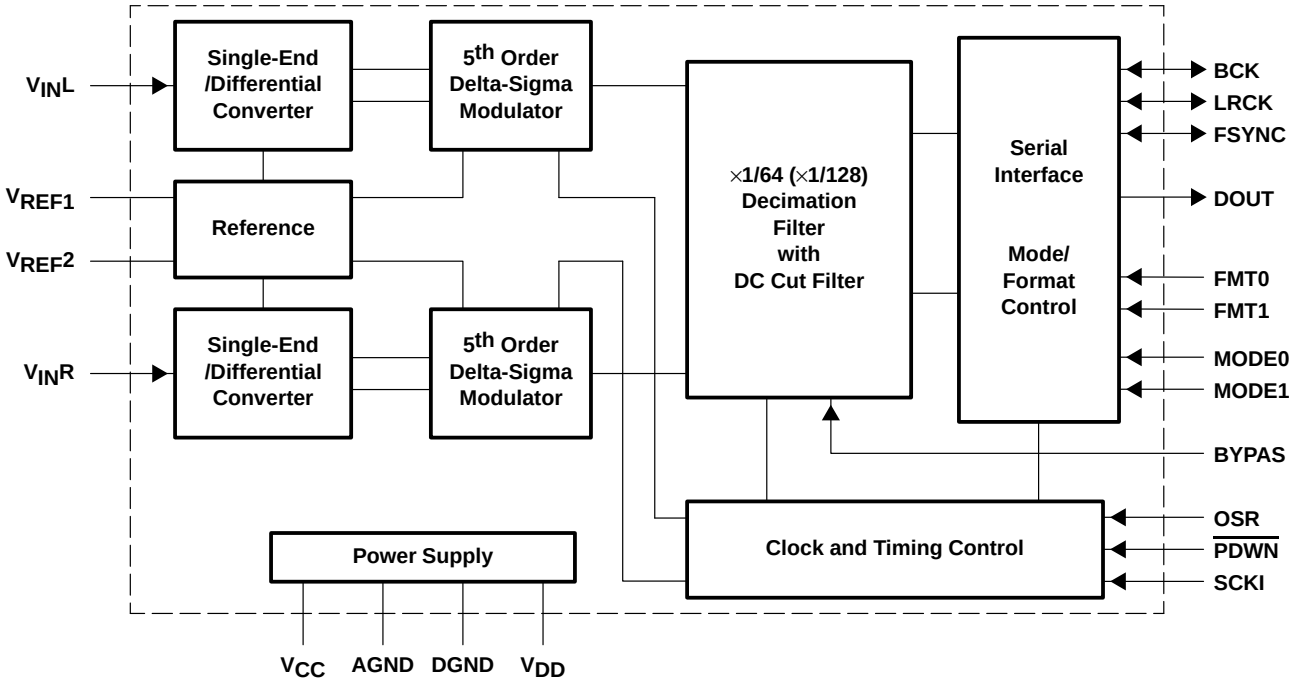
PRODUCT	PACKAGE	PACKAGE CODE	OPERATION TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA
PCM1802DB	20-Lead SSOP	20DB	–40°C to 85°C	PCM1802	PCM1802DB	Tube
					PCM1802DBR	Tape and reel

pin assignments

PCM1802
(TOP VIEW)



block diagram



Terminal Functions

TERMINAL NAME	TERMINAL PIN	I/O	DESCRIPTIONS
AGND	6	–	Analog GND
BCK	11	I/O	Bit clock input/output‡
BYPAS	8	I	HPF bypass control. Low: normal mode (dc cut); High: bypass mode (through)†
DGND	13	–	Digital GND
DOUT	12	O	Audio data output
FMT0	17	I	Audio data format select 0. See *data format*†
FMT1	18	I	Audio data format select 1. See *data format*†
FSYNC	9	I/O	Frame synchronous clock input/output‡
LRCK	10	I/O	Sampling clock input/output‡
MODE0	19	I	Mode select 0. See *interface mode*†
MODE1	20	I	Mode select 1. See *interface mode*†
OSR	16	I	Oversampling ratio select. Low: ×64 f_S; High: ×128 f_S†
$\overline{\text{PDWN}}$	7	I	Power-down control, active low†
SCKI	15	I	System clock input; 256 f_S, 384 f_S, 512 f_S or 768 f_S§
V_{CC}	5	–	Analog power supply, 5 V
V_{DD}	14	–	Digital power supply, 3.3 V
$V_{IN}L$	1	I	Analog input, L-channel
$V_{IN}R$	2	I	Analog input, R-channel
$V_{REF}1$	3	–	Reference 1 decoupling capacitor
$V_{REF}2$	4	–	Reference 2 voltage input, normally connected to V_{CC}

† Schmitt-trigger input with internal pulldown (50 kΩ typically), 5-V tolerant
‡ Schmitt-trigger input
§ Schmitt-trigger input, 5-V tolerant

absolute maximum ratings over operating free-air temperature (unless otherwise noted)¶

Supply voltage: V_{CC} . . . . . 6.5 V
V_{DD} . . . . . 4.0 V
Ground voltage differences: AGND, DGND . . . . . ±0.1 V
Digital input voltage: FSYNC, LRCK, BCK, DOUT . . . . . –0.3 V to (V_{DD} + 0.3 V)
$\overline{\text{PDWN}}$, BYPAS, SCKI, OSR, FMT0, FMT1, MODE0, MODE1 . . . . . –0.3 V to 6.5 V
Analog input voltage: $V_{IN}L$, $V_{IN}R$, $V_{REF}1$, $V_{REF}2$ . . . . . –0.3 V to (V_{CC} + 0.3 V)
Input current (any pins except supplies) . . . . . ±10 mA
Ambient temperature under bias . . . . . –40°C to 125°C
Storage temperature . . . . . –55°C to 150°C
Junction temperature . . . . . 150°C
Lead temperature (soldering) . . . . . 260°C, 5 s
Package temperature (IR reflow, peak) . . . . . 260°C

¶ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

electrical characteristics, all specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 44.1 kHz, system clock = 384 f_S, over sampling ratio = ×128, 24-bit data (unless otherwise noted)

			TEST CONDITIONS	PCM1802DB			UNIT
				MIN	TYP	MAX	
	Resolution				24		bits
DATA FORMAT							
	Audio data interface format				Left justified, I²S, right justified		
	Audio data bit length				20, 24		bits
	Audio data format				MSB first, 2s complement		
f_S	Sampling frequency			16	44.1	96	kHz
	System clock frequency		256 f_S	4.096	11.2896	24.576	MHz
			384 f_S	6.144	16.9344	36.864	
			512 f_S	8.192	22.5792	49.152	
			768 f_S	12.288	33.8688		
INPUT LOGIC							
V_{IH}	See Note 1	Input logic level		2		V_{DD}	VDC
V_{IL}				0		0.8	
V_{IH}	See Note 2			2		5.5	
V_{IL}				0		0.8	
I_{IH}	See Note 3	Input logic current	V_{IN} = V_{DD}			±10	µA
I_{IL}			V_{IN} = 0 V			±10	
I_{IH}	See Note 4		V_{IN} = V_{DD}		65	100	
I_{IL}			V_{IN} = 0 V			±10	
OUTPUT LOGIC							
V_{OH}	See Note 5	Output logic level	I_{OUT} = –1 mA	2.8			VDC
V_{OL}			I_{OUT} = 1 mA			0.5	
DC ACCURACY							
	Gain mismatch channel-to-channel				±1	±4	%FSR
	Gain error				±2	±6	%FSR
	Bipolar zero error		LCF bypass (see Note 6)		±2		%FSR

NOTES: 1. Pins 9–11: FSYNC, LRCK, BCK (Schmitt-trigger input, in slave mode)
2. Pins 7–8, 15–20: $\overline{\text{PDWN}}$, BYPAS, SCKI, OSR, FMT0, FMT1, MODE0, MODE1 (Schmitt-trigger input, 5-V tolerant).
3. Pins 9–11, 15: FSYNC, LRCK, BCK (Schmitt-trigger input in slave mode), SCKI (Schmitt-trigger input).
4. Pins 7–8, 16–20: $\overline{\text{PDWN}}$, BYPAS, OSR, FMT0, FMT1, MODE0, MODE1 (Schmitt-trigger input, with 50-kΩ typical pulldown resistor).
5. Pins 9–12: FSYNC, LRCK, BCK (in master mode), DOUT
6. Low cut filter

electrical characteristics, all specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 44.1 kHz, system clock = 384 f_S, over sampling ratio = ×128, 24-bit data (unless otherwise noted) (continued)

		TEST CONDITIONS	PCM1802DB			UNIT
			MIN	TYP	MAX	
DYNAMIC PERFORMANCE (see Note 7)						
	THD+N (V_{IN} = –0.5 dB)	f_S = 44.1 kHz		0.0015%	0.003%	
		f_S = 96 kHz (see Note 8)		0.0025%		
	THD+N (V_{IN} = –60 dB)	f_S = 44.1 kHz		0.7%		
		f_S = 96 kHz (see Note 8)		1.2%		
	Dynamic range	f_S = 44.1 kHz, A-weighted	100	105		dB
		f_S = 96 kHz, A-weighted (see Note 8)		103		
	S/N ratio	f_S = 44.1 kHz, A-weighted	100	105		dB
		f_S = 96 kHz, A-weighted (see Note 8)		103		
	Channel separation	f_S = 44.1 kHz	96	103		dB
		f_S = 96 kHz (see Note 8)		98		
ANALOG INPUT						
	Input voltage			0.6 V_{CC}		Vp–p
	Center voltage (V_{REF}1)			0.5 V_{CC}		V
	Input impedance			20		kΩ
	Antialiasing filter frequency response	–3 dB		300		kHz
DIGITAL FILTER PERFORMANCE						
	Passband				0.454 f_S	Hz
	Stopband		0.583 f_S			Hz
	Passband ripple				±0.05	dB
	Stopband attenuation		–65			dB
	Delay time			17.4/f_S		s
	HPF frequency response	–3 dB		0.019 f_S		mHz
POWER SUPPLY REQUIREMENTS						
V_{CC}	Voltage range		4.5	5	5.5	VDC
V_{DD}			2.7	3.3	3.6	
I_{CC}	Supply current (see Note 9)	V_{CC} = 5 V, V_{DD} = 3.3 V		24	30	mA
I_{DD}		f_S = 44.1 kHz V_{CC} = 5 V, V_{DD} = 3.3 V		8.3	10	
		f_S = 96 kHz, V_{CC} = 5 V, V_{DD} = 3.3 V (see Note 8)		17		
P_D	Power dissipation; operation	f_S = 44.1 kHz, V_{CC} = 5 V, V_{DD} = 3.3 V		147	183	mW
		f_S = 96 kHz, V_{CC} = 5 V, V_{DD} = 3.3 V (see Note 8)		176		
	Power dissipation; power down	V_{CC} = 5 V, V_{DD} = 3.3 V		0.5		mW
TEMPERATURE RANGE						
	Operation temperature		–40		85	°C
	Thermal resistance (θ_{JA})	20-pin SSOP		115		°C/W

NOTES: 7. Analog performance specs are tested with System Two™ audio measurement system by Audio Precision™, using 400-Hz HPF, 20-kHz LPF at 44.1-kHz operation, 40-kHz LPF at 96-kHz operation in RMS mode.
8. f_S = 96 kHz, system clock = 256 f_S, oversampling ratio = ×64.
9. Minimum load on DOUT (pin 12), BCK (pin 11), LRCK (pin 10), FSYNC (pin 9).

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTER

digital filter—decimation filter frequency response

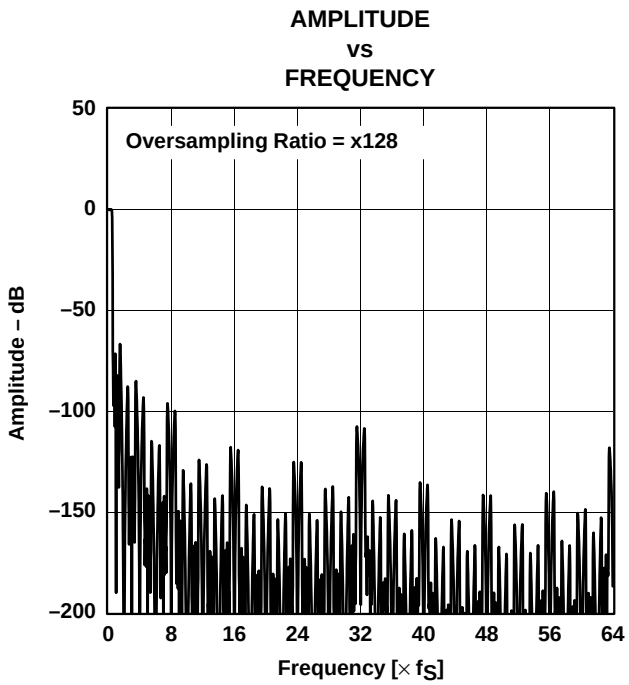


Figure 1. Overall Characteristics

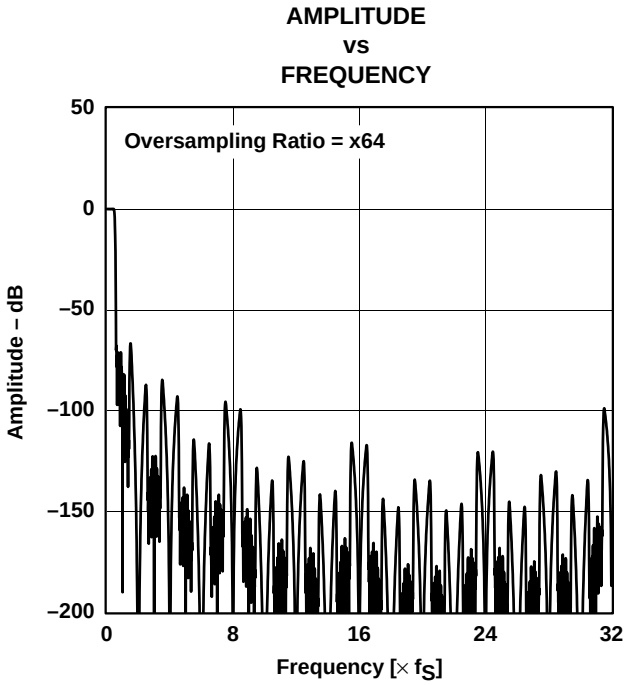


Figure 2. Overall Characteristics

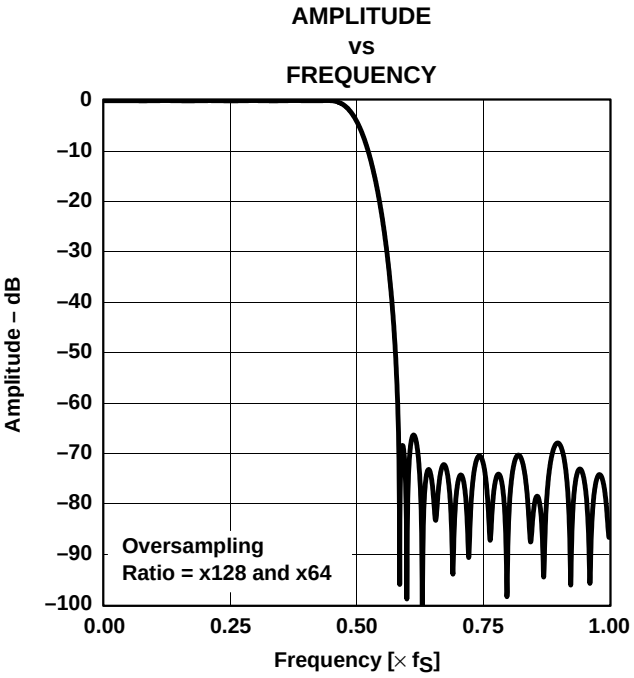


Figure 3. Stopband Attenuation Characteristics

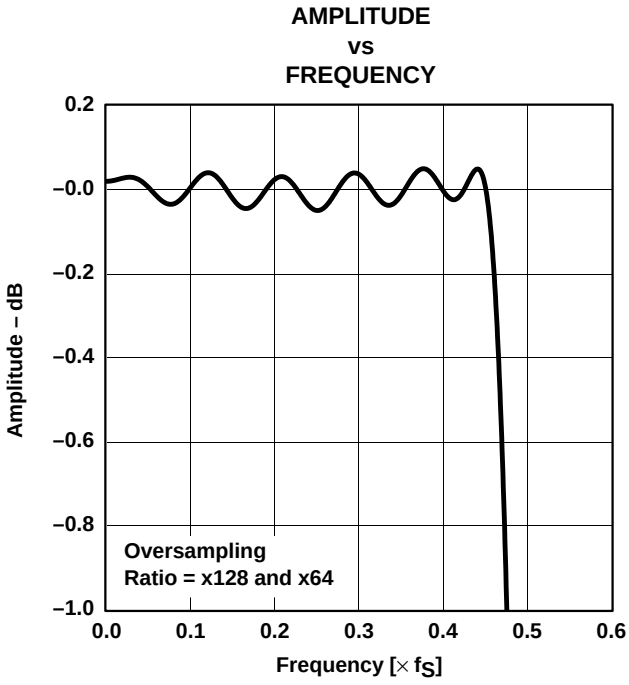


Figure 4. Passband Ripple Characteristics

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 44.1 kHz, system clock = 384 f_S, oversampling ratio = ×128, 24-bit data, unless otherwise noted.

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTER

HPF (low cut filter) frequency response

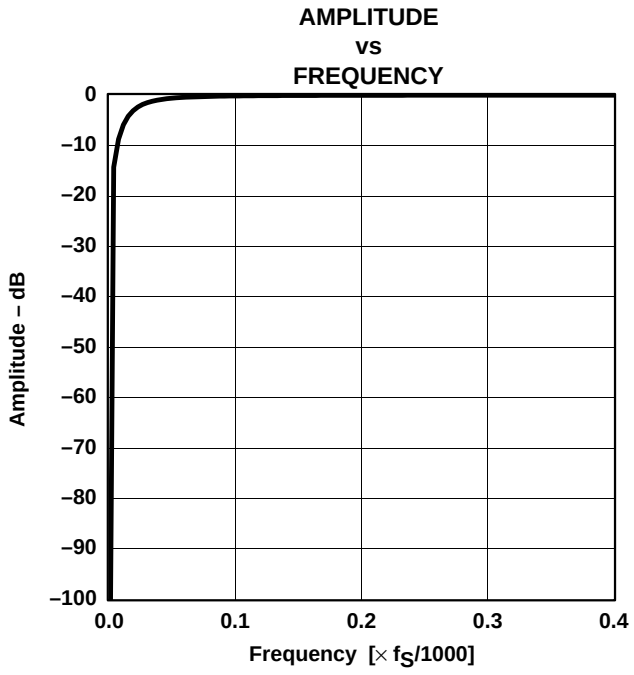


Figure 5. LCF Stopband Characteristics

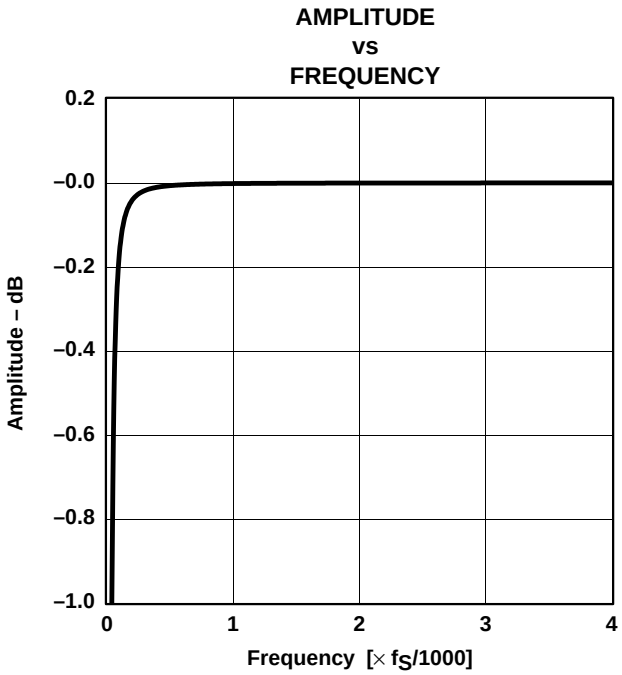


Figure 6. LCF Passband Characteristics

analog filter—antialiasing filter frequence response

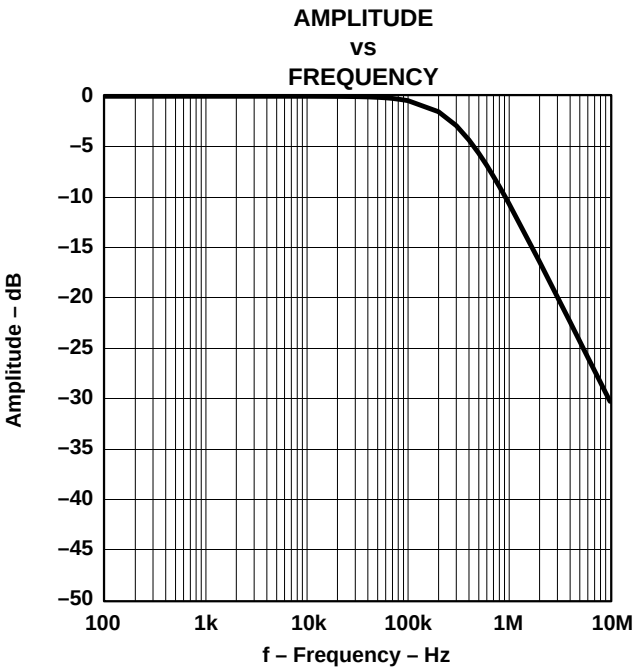


Figure 7. Antialias Filter Stopband Characteristics

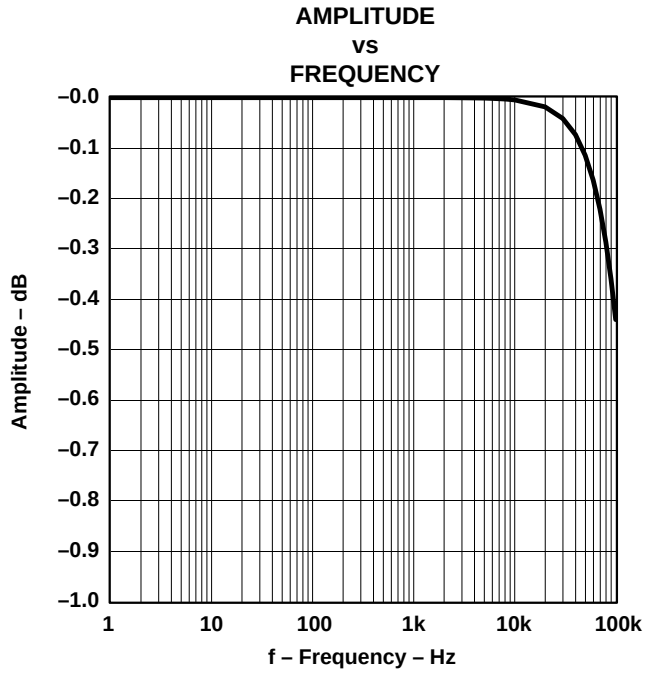


Figure 8. Antialias Filter Passband Characteristics

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 44.1 kHz, system clock = 384 f_S, oversampling ratio = ×128, 24-bit data, unless otherwise noted.

TYPICAL PERFORMANCE CURVES

TOTAL HARMONIC DISTORTION + NOISE vs FREE-AIR TEMPERATURE

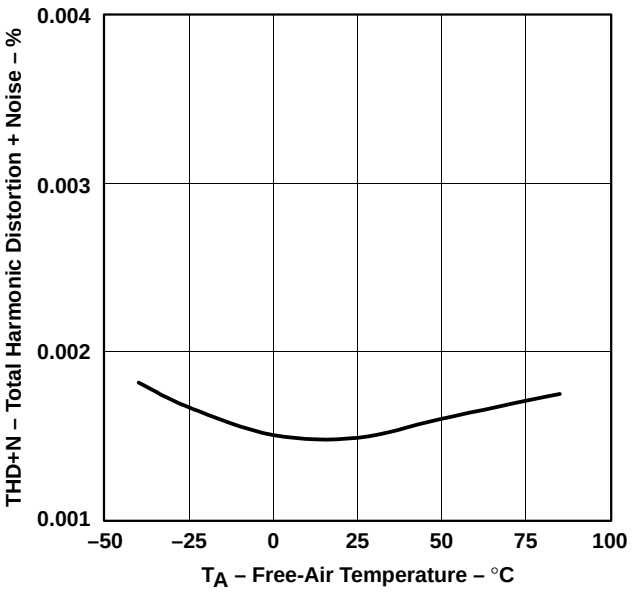


Figure 9

DYNAMIC RANGE and SNR vs FREE-AIR TEMPERATURE

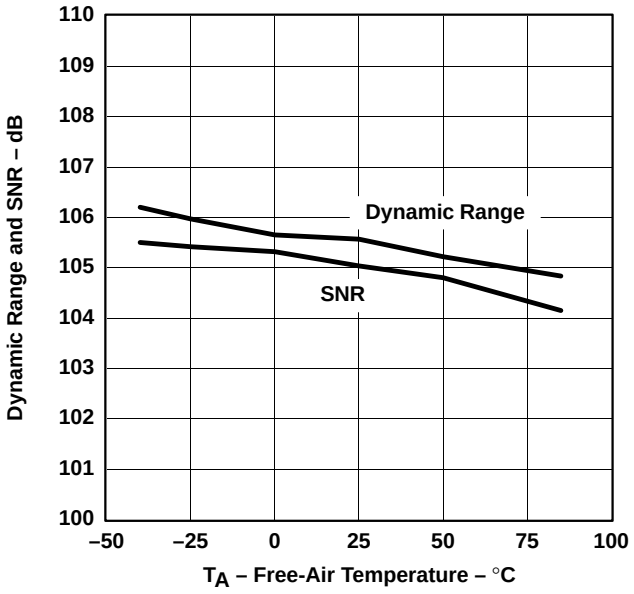


Figure 10

TOTAL HARMONIC DISTORTION + NOISE vs SUPPLY VOLTAGE

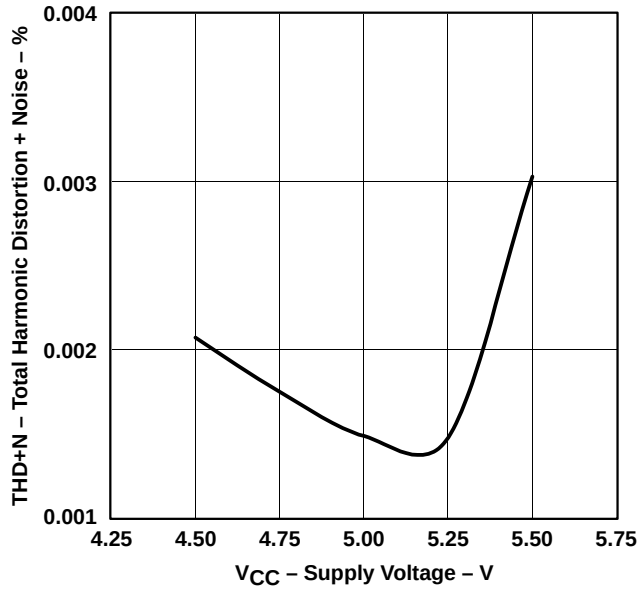


Figure 11

DYNAMIC RANGE and SNR vs SUPPLY VOLTAGE

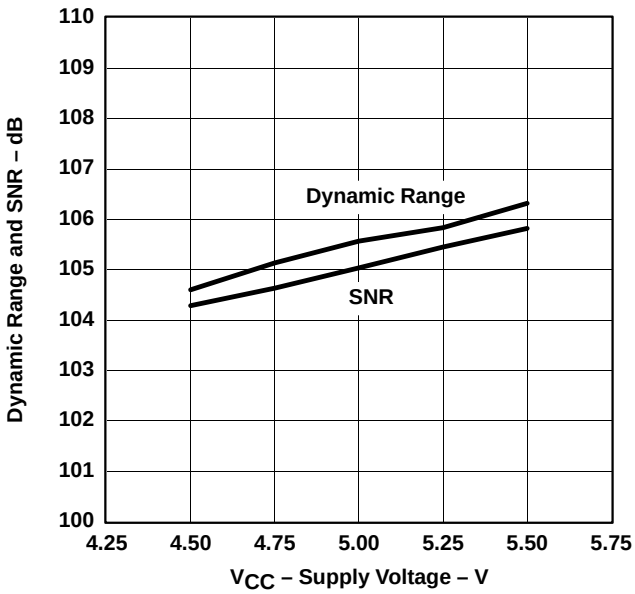


Figure 12

All specifications at T_A = 25°C, V_{CC} = 5.0 V, V_{DD} = 3.3 V, master mode, f_S = 44.1 kHz, system clock = 384 f_S, oversampling ratio = ×128, 24-bit data, unless otherwise noted.

TYPICAL PERFORMANCE CURVES

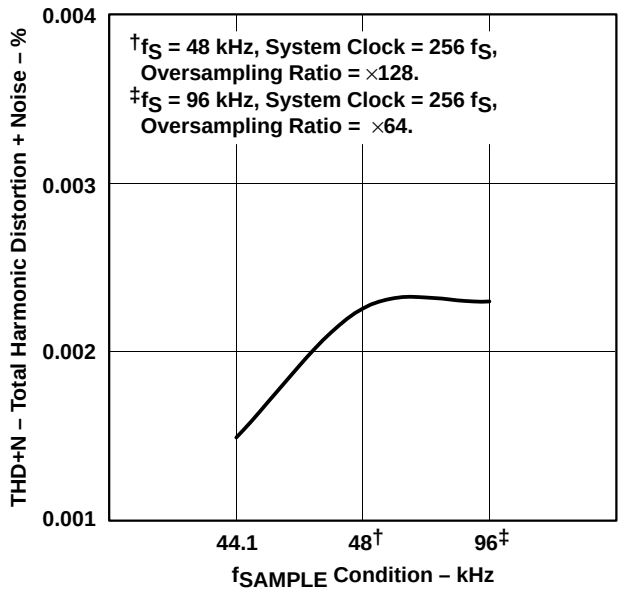


Figure 13

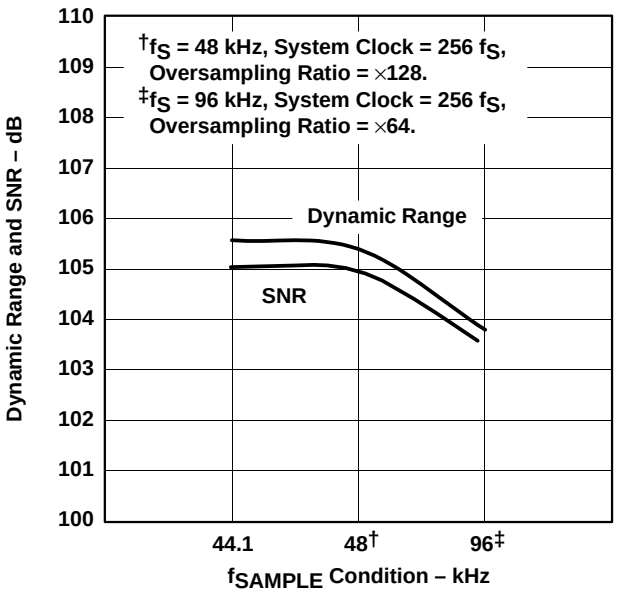


Figure 14

output spectrum

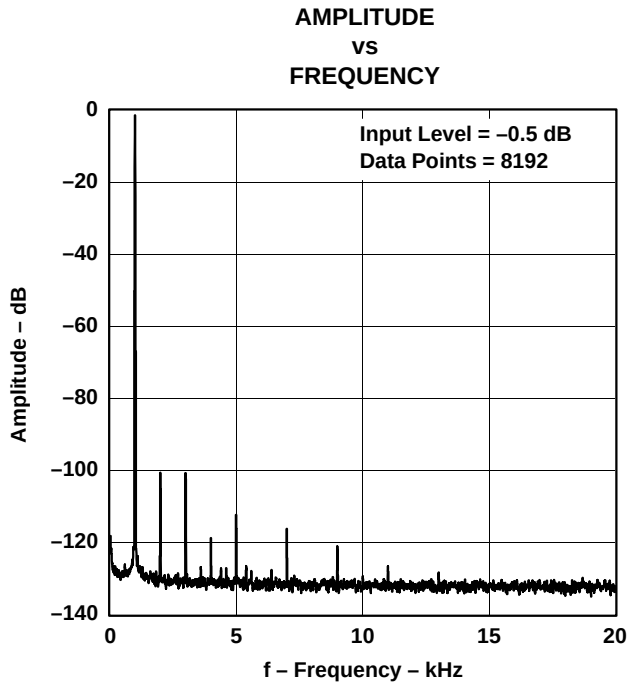


Figure 15

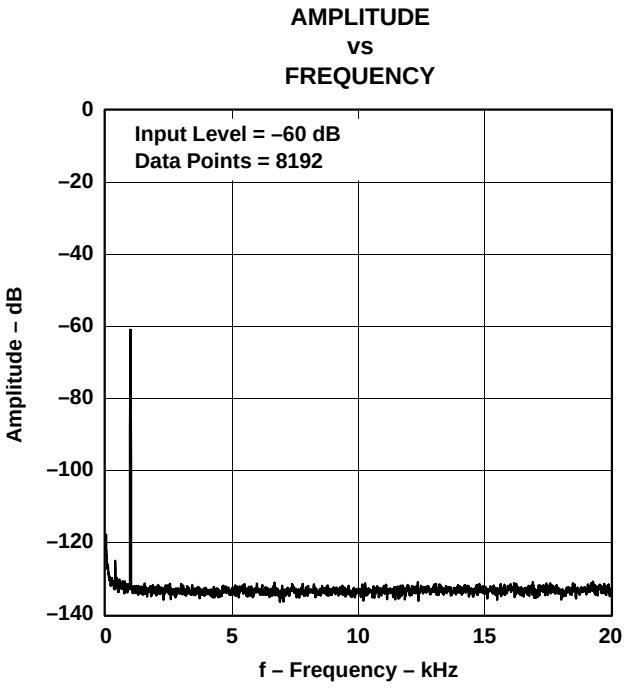


Figure 16

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 44.1 kHz, system clock = 384 f_S, oversampling ratio = ×128, 24-bit data, unless otherwise noted.

TYPICAL PERFORMANCE CURVES

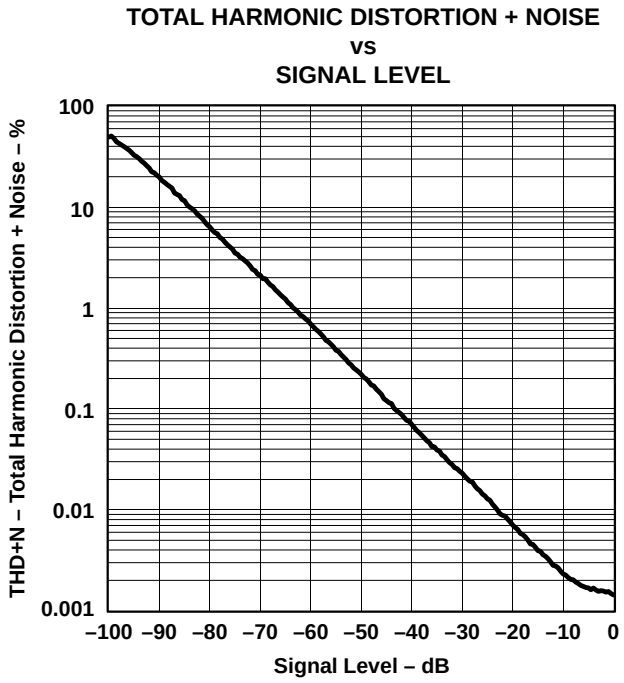


Figure 17

supply current

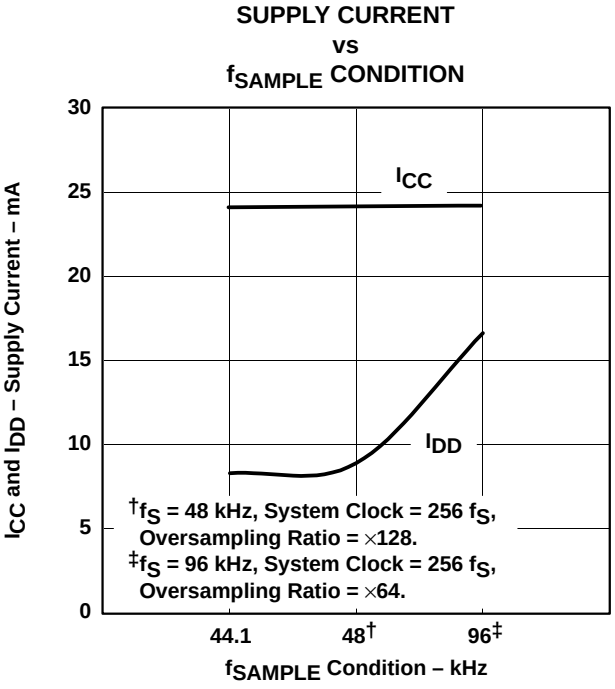


Figure 18

All specifications at T_A = +25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, Master Mode, f_S = 44.1 kHz, system clock = 384f_S, oversampling ratio = ×128, 24-bit data, unless otherwise noted.

PRINCIPLES OF OPERATION

PCM1802 consists of a reference circuit, two channels of single-ended-to-differential converter, fifth-order delta-sigma modulator with full differential architecture, decimation filter with low cut filter, and a serial interface circuit. Figure 19 illustrates the total architecture of PCM1802, Figure 20 illustrates the architecture of single-ended-to-differential converter and antialiasing filter, and Figure 21 illustrates the block diagram of fifth-order delta-sigma modulator and transfer function. An on-chip high-precision reference with one external capacitor provides all reference voltages that are needed in the PCM1802, and defines the full scale voltage range for both channels. On-chip single-ended-to-differential signal converters save the design, space, and extra parts cost for external signal converters. Full differential architecture provides a wide dynamic range and excellent power supply rejection performance. The input signal is sampled at a ×64 or ×128 oversampling rate, thus eliminating an external sample-hold amplifier. A fifth-order delta-sigma noise shaper, which consists of five integrators using the switched capacitor technique and a comparator, shapes the quantization noise generated by the comparator and 1-bit DAC outside of the audio signal band. The high-order delta-sigma modulation randomizes the modulator outputs and reduces the idle tone level. The 64-f_S or 128-f_S, 1-bit stream from the delta-sigma modulator is converted to a 1-f_S, 24-bit or 20-bit digital signal by removing high-frequency noise components with a decimation filter. The dc component of the signal is removed by the LCF, and the LCF output is converted to a time-multiplexed serial signal through the serial interface, which provides flexible serial formats.

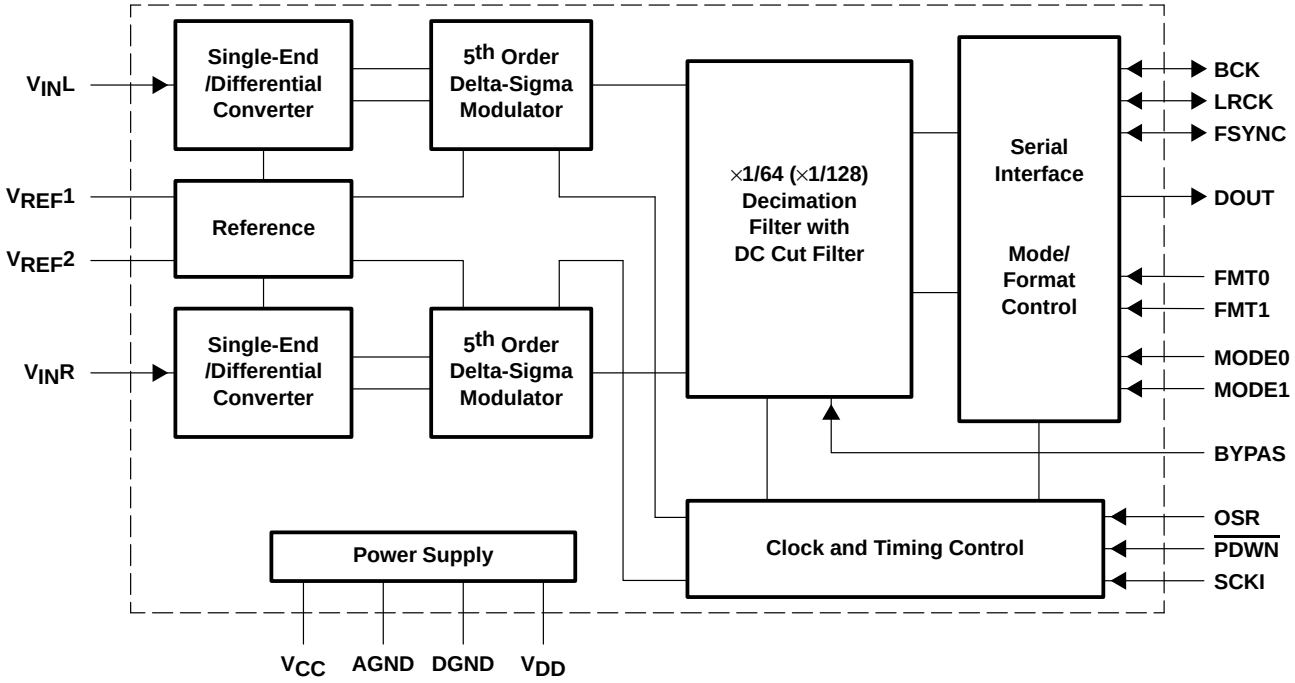


Figure 19. Block Diagram

PRINCIPLES OF OPERATION

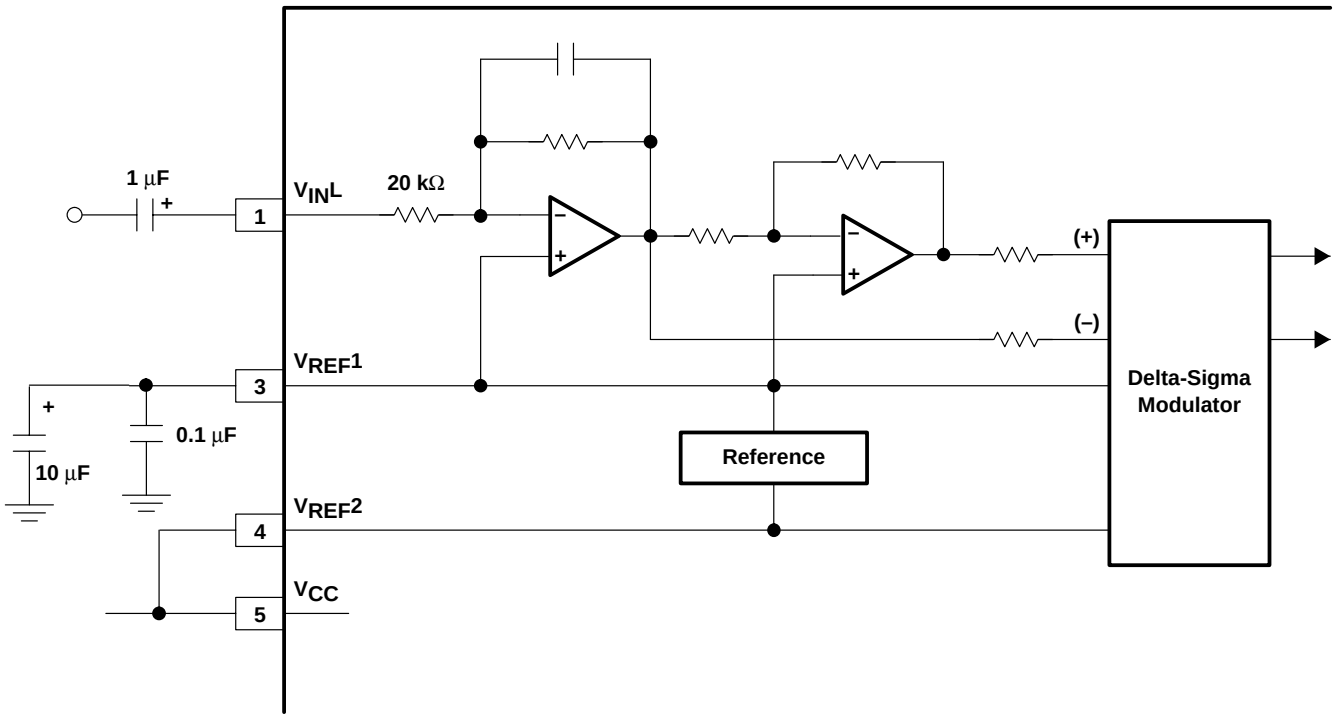
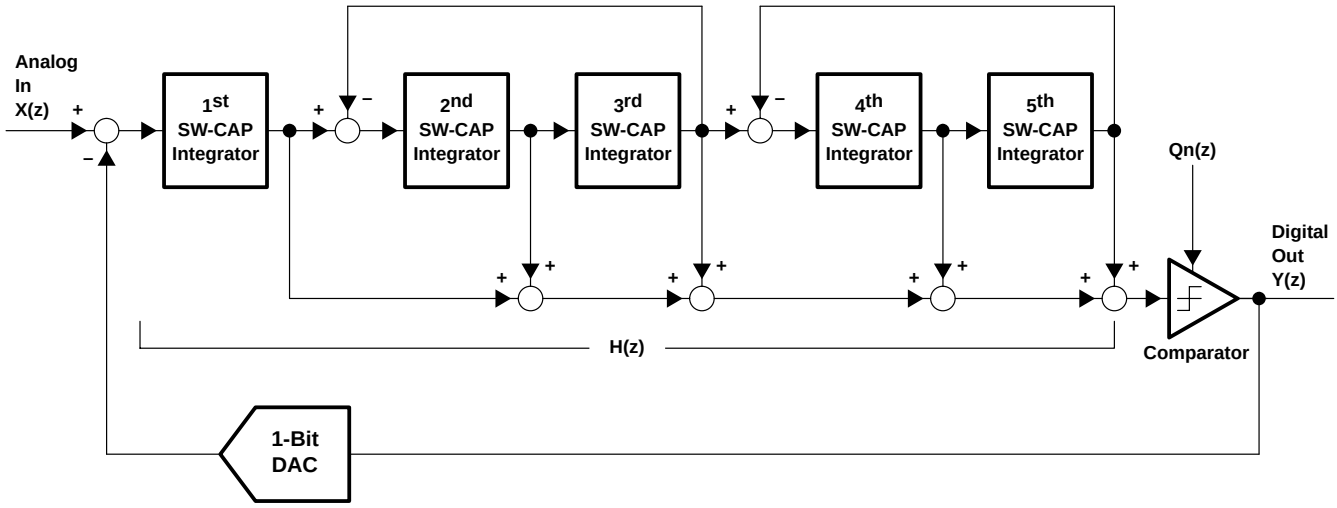


Figure 20. Analog Front End (Left Channel)



$Y(z) = STF(z) * X(z) + NTF(z) * Qn(z)$

Signal Transfer Function $STF(z) = H(z) / [1 + H(z)]$

Noise Transfer Function $NTF(z) = 1 / [1 + H(z)]$

Figure 21. Block Diagram of Fifth-Order Delta-Sigma Modulator

PRINCIPLES OF OPERATION

system clock

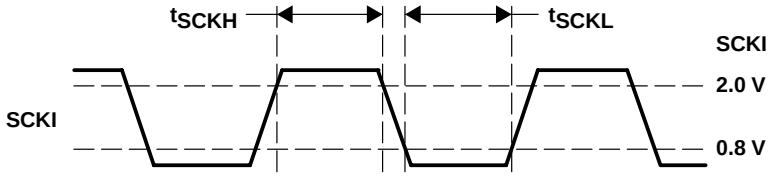
The PCM1802 supports 256 f_S, 384 f_S, 512 f_S, and 768 f_S as the system clock, where f_S is the audio sampling frequency. The system clock must be supplied on SCKI (pin 15).

The PCM1802 has a system clock detection circuit which automatically senses if the system clock is operating at 256 f_S, 384 f_S, 512 f_S, or 768 f_S in slave mode. In master mode, the system clock frequency must be selected by MODE0 (pin 19) and MODE1 (pin 20), and 768 f_S is not available. For system clock inputs of 384 f_S, 512 f_S, and 768 f_S, the system clock is divided to 256 f_S automatically, and the 256 f_S clock is used to operate the delta-sigma modulator and the digital filter.

Table 1 shows the relationship of typical sampling frequencies and system clock frequencies, and Figure 22 shows system clock timing.

Table 1. Sampling Frequency and System Clock Frequency

SAMPLING RATE FREQUENCY (kHz)	SYSTEM CLOCK FREQUENCY (MHz)			
	256 f_S	384 f_S	512 f_S	768 f_S
32	8.192	12.288	16.384	24.576
44.1	11.2896	16.9344	22.5792	33.8688
48	12.288	18.432	24.576	36.864
64	16.384	24.576	32.768	49.152
88.2	22.5792	33.8688	45.1584	—
96	24.576	36.864	49.152	—



PARAMETER		MIN	MAX	UNIT
t_{SCKH}	System clock pulse width, high	7		ns
t_{SCKL}	System clock pulse width, low	7		ns

Figure 22. System Clock Timing

PRINCIPLES OF OPERATION

power-on reset sequence

The PCM1802 has an internal power-on reset circuit and initialization (reset) is performed automatically when the power supply (V_{DD}) exceeds 2.2 V (typ). While V_{DD} < 2.2 V (typ), and for 1024 system-clock counts after V_{DD} > 2.2 V (typ), the PCM1802 stays in the reset state and the digital output is forced to zero. The digital output is valid after the reset state is released and the time of 4480/f_S has passed. Figure 23 illustrates the internal power-on reset timing and the digital output for power-on reset.

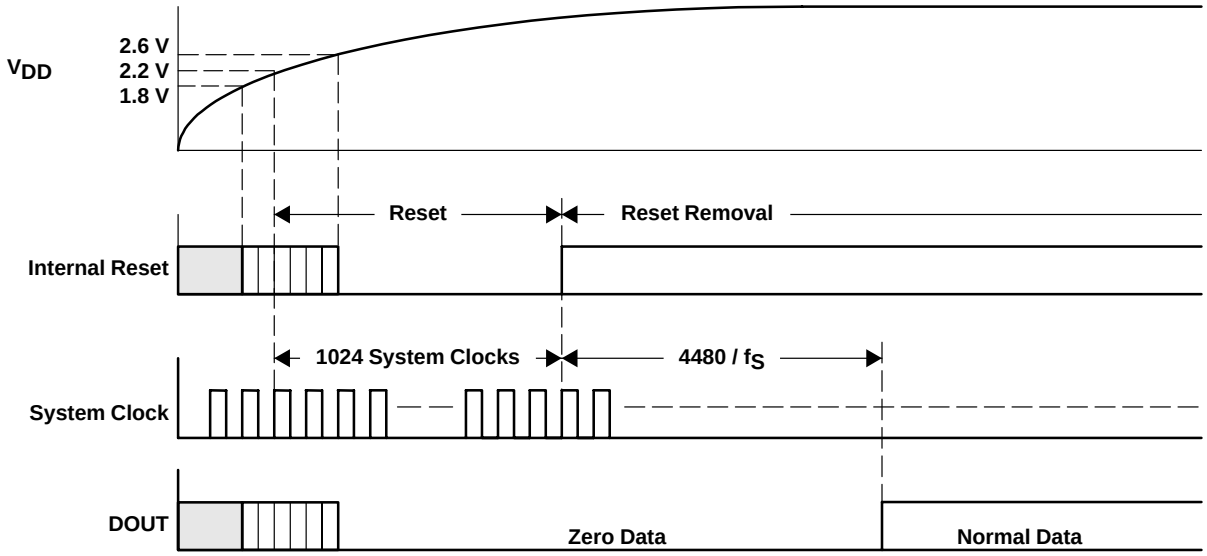


Figure 23. Internal Power-On Reset Timing

serial audio data interface

The PCM1802 interfaces with the audio system through BCK (pin 11), LRCK (pin 10), FSYNC (pin 9), and DOUT (pin 12).

PRINCIPLES OF OPERATION

interface mode

The PCM1802 supports master mode and slave mode as interface modes, and they are selected by MODE1 (pin 20) and MODE0 (pin 19) as shown in Table 2.

In master mode, the PCM1802 provides the timing for serial audio data communications between the PCM1802 and the digital audio processor or external circuit. In slave mode, the PCM1802 receives the timing for data transfer from an external controller.

Table 2. Interface Mode

MODE1	MODE0	INTERFACE MODE
0	0	Slave mode (256 f_S, 384 f_S, 512 f_S, 768 f_S)
0	1	Master mode (512 f_S)
1	0	Master mode (384 f_S)
1	1	Master mode (256 f_S)

(1) Master mode

In master mode, BCK, LRCK and FSYNC work as output pins, and these pins are controlled by timing which is generated in the clock circuit of the PCM1802. FSYNC is used to designate the valid data from the PCM1802. The rising edge of FSYNC indicates the starting point of the converted audio data and the falling edge of this signal indicates the ending point of the data. The frequency of this signal is fixed at 2 × LRCK. The duty cycle ratio depends on data bit length. The frequency of BCK is fixed at 64 × LRCK. The 768 f_S system clock is not available in master mode.

(2) Slave mode

In slave mode, BCK, LRCK and FSYNC work as input pins. FSYNC is used to enable the BCK signal, and the PCM1802 can shift out the converted data while FSYNC is HIGH. The PCM1802 accepts either the 64 BCK/LRCK or the 48 BCK/LRCK format. The delay of FSYNC from the LRCK transition must be within 16 BCKs for the 64 BCK/LRCK format and within 12 BCKs for the 48 BCK/LRCK format.

data format

The PCM1802 supports four audio data formats in both master and slave modes, and they are selected by FMT1 (pin 18) and FMT0 (pin 17) as shown in Table 3. Figure 24 and Figure 26 illustrate the data formats in slave mode and master mode, respectively.

Table 3. Data Format

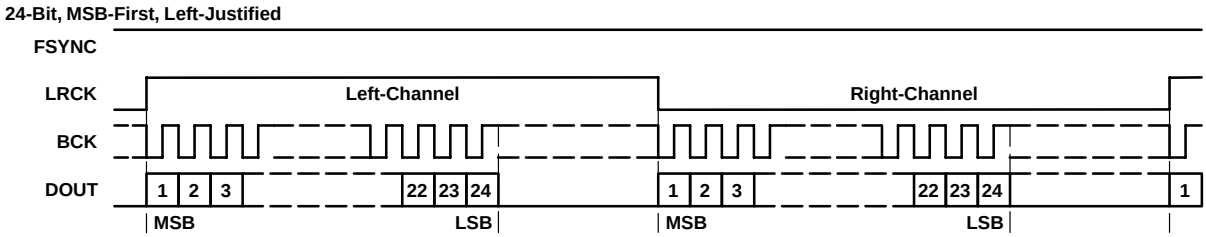
FORMAT#	FMT1	FMT0	FORMAT
0	0	0	Left justified, 24 bit
1	0	1	I^2S, 24 bit
2	1	0	Right justified, 24 bit
3	1	1	Right justified, 20 bit

PRINCIPLES OF OPERATION

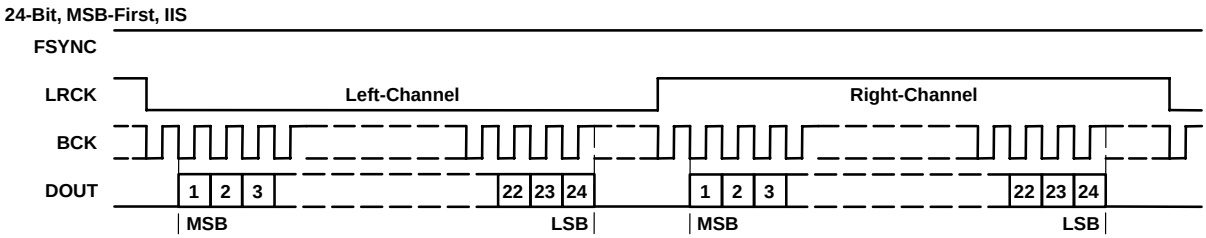
interface timing

Figure 25 and Figure 27 illustrate the interface timing in slave mode and master mode, respectively.

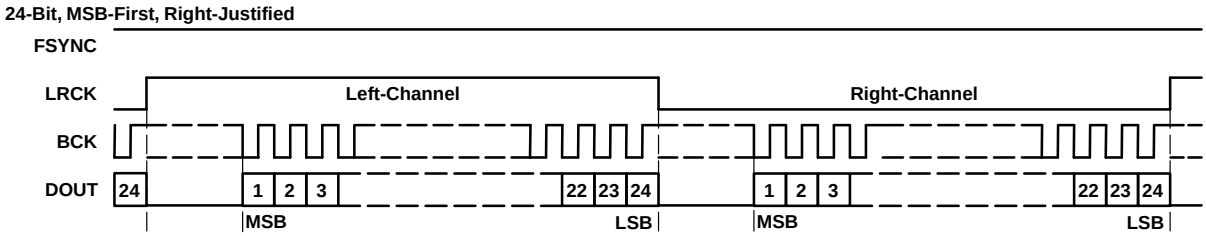
FORMAT 0: FMT[1:0] = 00



FORMAT 1: FMT[1:0] = 01



FORMAT 2: FMT[1:0] = 10



FORMAT 3: FMT[1:0] = 11

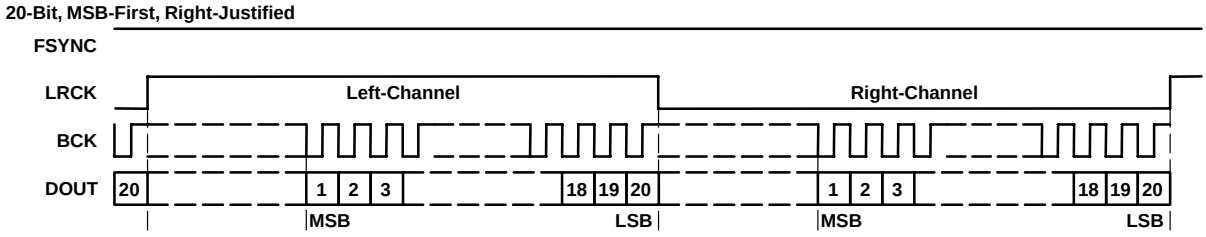
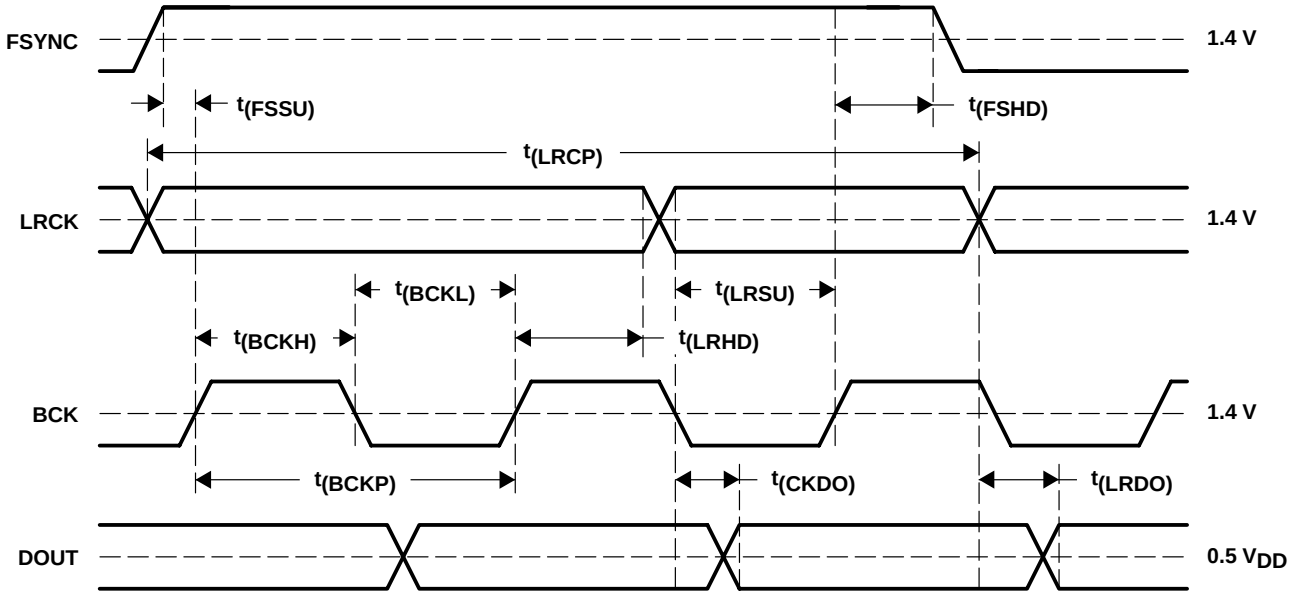


Figure 24. Audio Data Format (Slave Mode: FSYNC, LRCK, BCK Work as Inputs)

PRINCIPLES OF OPERATION

interface timing (continued)



PARAMETER		MIN	TYP	MAX	UNIT
$t_{(BCKP)}$	BCK period	150			ns
$t_{(BCKH)}$	BCK pulse duration high	60			ns
$t_{(BCKL)}$	BCK pulse duration low	60			ns
$t_{(LRSU)}$	LRCK setup time to BCK rising edge	40			ns
$t_{(LRHD)}$	LRCK hold time to BCK rising edge	20			ns
$t_{(LRCP)}$	LRCK period	10			μs
$t_{(FSSU)}$	FSYNC setup time to BCK rising edge	20			ns
$t_{(FSHD)}$	FSYNC hold time to BCK rising edge	20			ns
$t_{(CKDO)}$	Delay time, BCK falling edge to DOUT valid	–10		20	ns
$t_{(LRDO)}$	Delay time, LRCK edge to DOUT valid	–10		20	ns
t_r	Rise time of all signals			10	ns
t_f	Fall time of all signals			10	ns

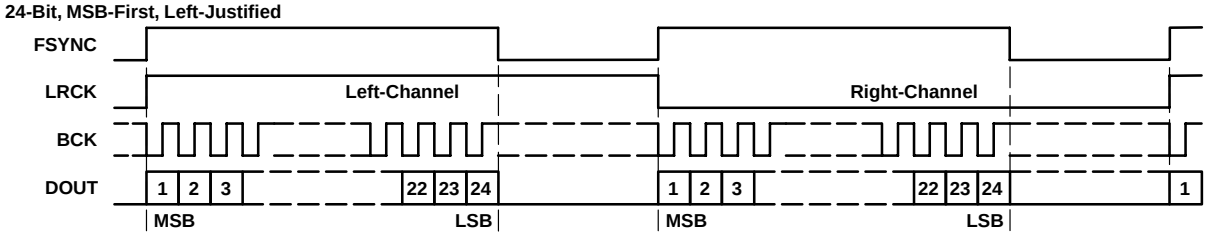
NOTE: Timing measurement reference level is $(V_{IH}/V_{IL})/2$. Rise and fall times are measured from 10% to 90% of IN/OUT signal swing. Load capacitance of DOUT is 20 pF.

Figure 25. Audio Data Interface Timing (Slave Mode: FSYNC, LRCK, BCK Work as Inputs)

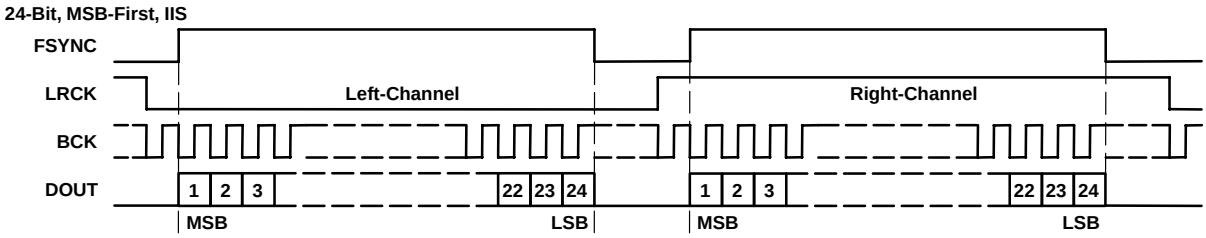
PRINCIPLES OF OPERATION

interface timing (continued)

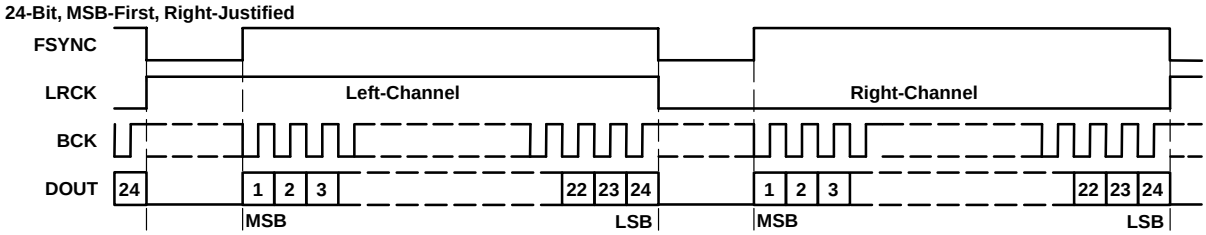
FORMAT 0: FMT[1:0] = 00



FORMAT 1: FMT[1:0] = 01



FORMAT 2: FMT[1:0] = 10



FORMAT 3: FMT[1:0] = 11

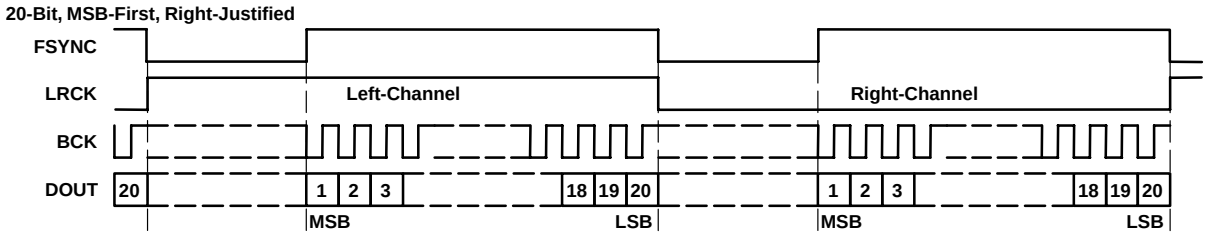
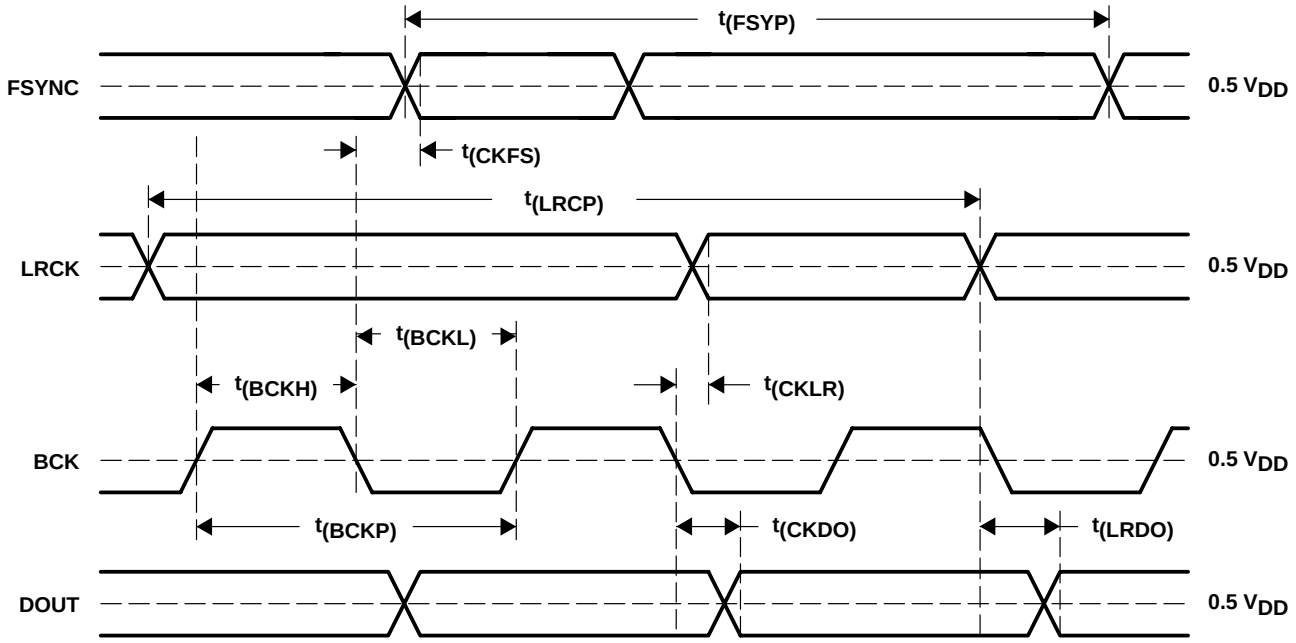


Figure 26. Audio Data Format (Master Mode: FSYNC, LRCK, BCK Work as Outputs)

PRINCIPLES OF OPERATION

interface timing (continued)



PARAMETER		MIN	TYP	MAX	UNIT
$t_{(BCKP)}$	BCK period	150	1/(64 f_S)	1200	ns
$t_{(BCKH)}$	BCK pulse width high	75		600	ns
$t_{(BCKL)}$	BCK pulse width low	75		600	ns
$t_{(CKLR)}$	Delay time BCK falling edge to LRCK valid	–10		20	ns
$t_{(LRCP)}$	LRCK period	10	1/ f_S	80	µs
$t_{(CKFS)}$	Delay time BCK falling edge to FSYNC valid	–10		20	ns
$t_{(FSYP)}$	FSYNC period	5	1/(2 f_S)	40	µs
$t_{(CKDO)}$	Delay time, BCK falling edge to DOUT valid	–10		20	ns
$t_{(LRDO)}$	Delay time, LRCK edge to DOUT valid	–10		20	ns
t_r	Rise time of all signals			10	ns
t_f	Fall time of all signals			10	ns

NOTE: Timing measurement reference level is (V_{IH}/V_{IL}) / 2. Rise and fall times are measured from 10% to 90% of IN/OUT signal swing. Load capacitance of all signals is 20 pF.

Figure 27. Audio Data Interface Timing (Master Mode: FSYNC, LRCK, BCK Work as Outputs)

PRINCIPLES OF OPERATION

synchronization with digital audio system

In slave mode, the PCM1802 operates under LRCK, synchronized with system clock SCKI. The PCM1802 does not need a specific phase relationship between LRCK and SCKI, but does require the synchronization of LRCK and SCKI.

If the relationship between LRCK and SCKI changes more than ±6 BCKs for 64 BCK/frame (±5 BCKs for 48 BCK/frame) during one sample period due to LRCK or SCKI jitter, internal operation of the ADC halts within $1/f_S$ and digital output is forced into BPZ code until re-synchronization between LRCK and SCKI is completed.

In the case of changes less than ±5 BCKs for 64 BCK/frame (±4 BCKs for 48 BCK/frame), resynchronization does not occur.

Figure 28 illustrates digital output response for loss of synchronization and resynchronization. During undefined data, some noise might be generated in the audio signal. Also, the transition of normal to undefined data and undefined or zero data to normal creates a data discontinuity in the digital output, which can generate some noise in the audio signal.

It is recommended to set $\overline{\text{PDWN}}$ low to get stable analog performance when the sampling rate, interface mode, data format, or oversampling control is changed.

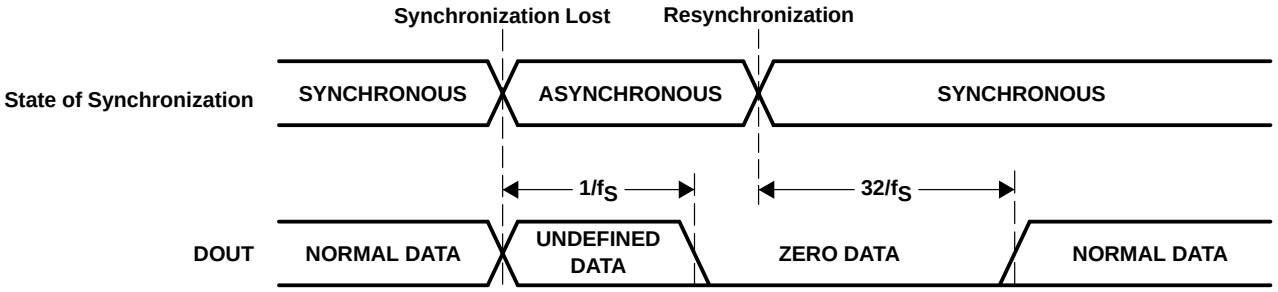


Figure 28. ADC Digital Output for Loss of Synchronization and Resynchronization

power down, LCF bypass, oversampling control

$\overline{\text{PDWN}}$ (pin 7) controls the entire ADC operation. During power-down mode, both the supply current for the analog portion and the clock signal for the digital portion are shut down, and power dissipation is minimized. Also, DOUT (pin 12) is disabled and no system clock is accepted during power-down mode.

Table 4. Power-Down Control

$\overline{\text{PDWN}}$	Power-down mode
LOW	Power-down mode
HIGH	Normal operation mode

The built-in function for dc component rejection can be bypassed using the BYPAS (pin 8) control. In bypass mode, the dc components of the analog input signal, internal dc offset, etc., are also converted and included in the digital output data.

Table 5. LCF Bypass Control

BYPAS	LCF (low-cut filter) mode
LOW	Normal (no dc component on DOUT) mode
HIGH	Bypass (dc component on DOUT) mode

PRINCIPLES OF OPERATION

power down, LCF bypass, oversampling control (continued)

OSR (pin 16) controls the oversampling ratio of the delta-sigma modulator, ×64 or ×128. The ×128 mode is available for f_S < 50 kHz, and must be used carefully as performance is affected by the duty cycle of the 384 f_S system clock.

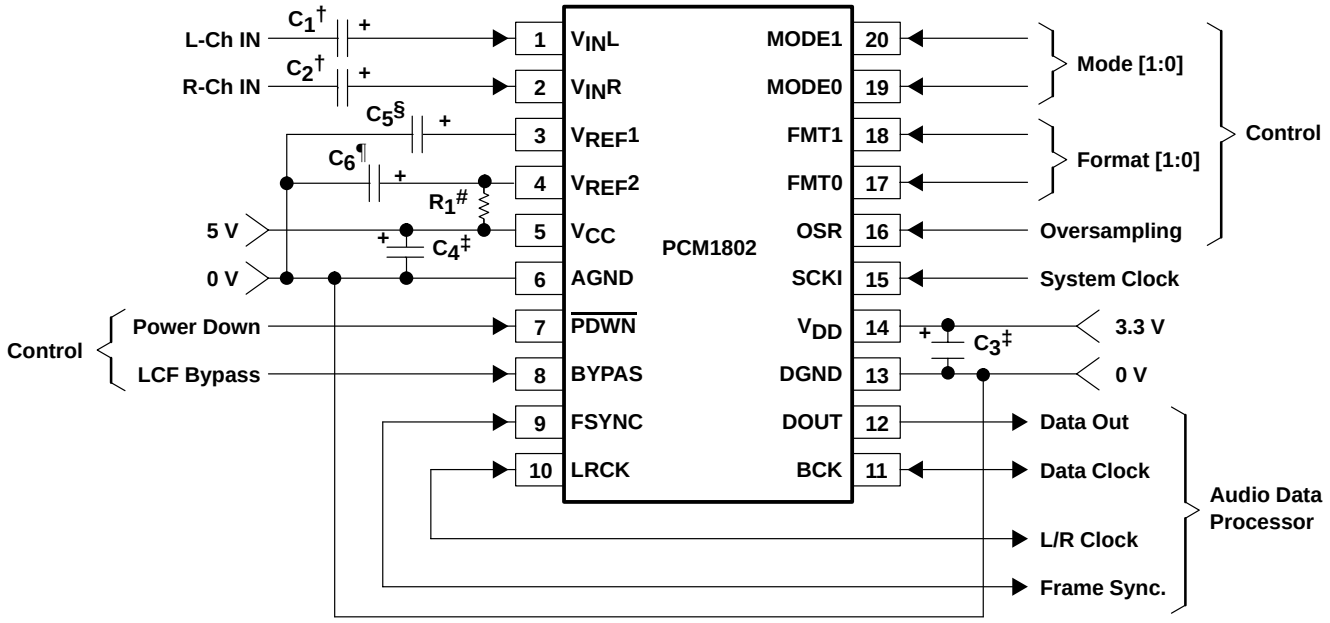
Table 6. Oversampling Control

OSR	Oversampling ratio
LOW	×64
HIGH	×128 (f_S < 50 kHz)

APPLICATION INFORMATION

typical circuit connection diagram

Figure 29 illustrates a typical circuit connection diagram in which the cutoff frequency of the input HPF is about 8 Hz.



† C_1, C_2: A 1-µF capacitor gives 8-Hz (τ = 1 µF × 20 kΩ) cutoff frequency for input HPF in normal operation, and requires a power-on settling time with 20-ms time constant in the power-on initialization period.
‡ C_3, C_4: Bypass capacitors, 0.1-µF ceramic and 10-µF tantalum, depending on layout and power supply.
§ C_5: 0.1-µF ceramic and 4.7-µF tantalum capacitors are recommended.
¶ C_6: 0.1-µF ceramic and 4.7-µF tantalum capacitors are recommended for using a noise analog power supply. These capacitor are not required for clean analog supply.
# R_1: 1-kΩ resistor is recommended for using a noisy analog power supply. This resistor is shorted for a clean analog supply.

Figure 29. Typical Circuit Connection

APPLICATION INFORMATION

board design and layout considerations

V_{CC}, V_{DD} pins

The digital and analog power supply lines to the PCM1802 should be bypassed to the corresponding ground pins with 0.1-μF ceramic and 10-μF tantalum capacitors as close to the pins as possible to maximize the dynamic performance of the ADC.

AGND, DGND pins

To maximize the dynamic performance of the PCM1802, the analog and digital grounds are not connected internally. These grounds should have very low impedance to avoid digital noise feeding back into the analog ground. They should be connected directly to each other under the parts to reduce the potential noise problem.

V_{IN} pins

A 1-μF capacitor is recommended as an ac-coupling capacitor which gives 8-Hz cutoff frequency. If a higher full-scale input voltage is required, it can be accommodated by adding only one series resistor to each V_{IN} pin.

$V_{REF}1$ pin

A 0.1-μF ceramic and 10-μF chemical capacitors are recommended between $V_{REF}1$ and AGND to insure low source impedance of ADC references. These capacitors should be located as close as possible to the $V_{REF}1$ pin to reduce the dynamic errors on ADC references.

$V_{REF}2$ pin

The differential voltage between $V_{REF}2$ and AGND sets the analog input full-scale range. A 0.1-μF ceramic and 10-μF chemical capacitors are recommended between $V_{REF}2$ and AGND with insertion of a 1-kΩ resistor between VCC and VREF2 for using a noisy analog power supply. These capacitors and resistor are not required for clean analog supply. These capacitors should be located as close as possible to the $V_{REF}2$ pin to reduce the dynamic errors on ADC references. Full-scale input level is affected by this 1-kΩ resistor and decreases by 3%.

DOUT pin

The DOUT pin has enough load drive capability, but locating a buffer near the PCM1802 and minimizing load capacitance is recommended if the DOUT line is long, in order to minimize the digital-analog crosstalk and maximize the dynamic performance of the ADC.

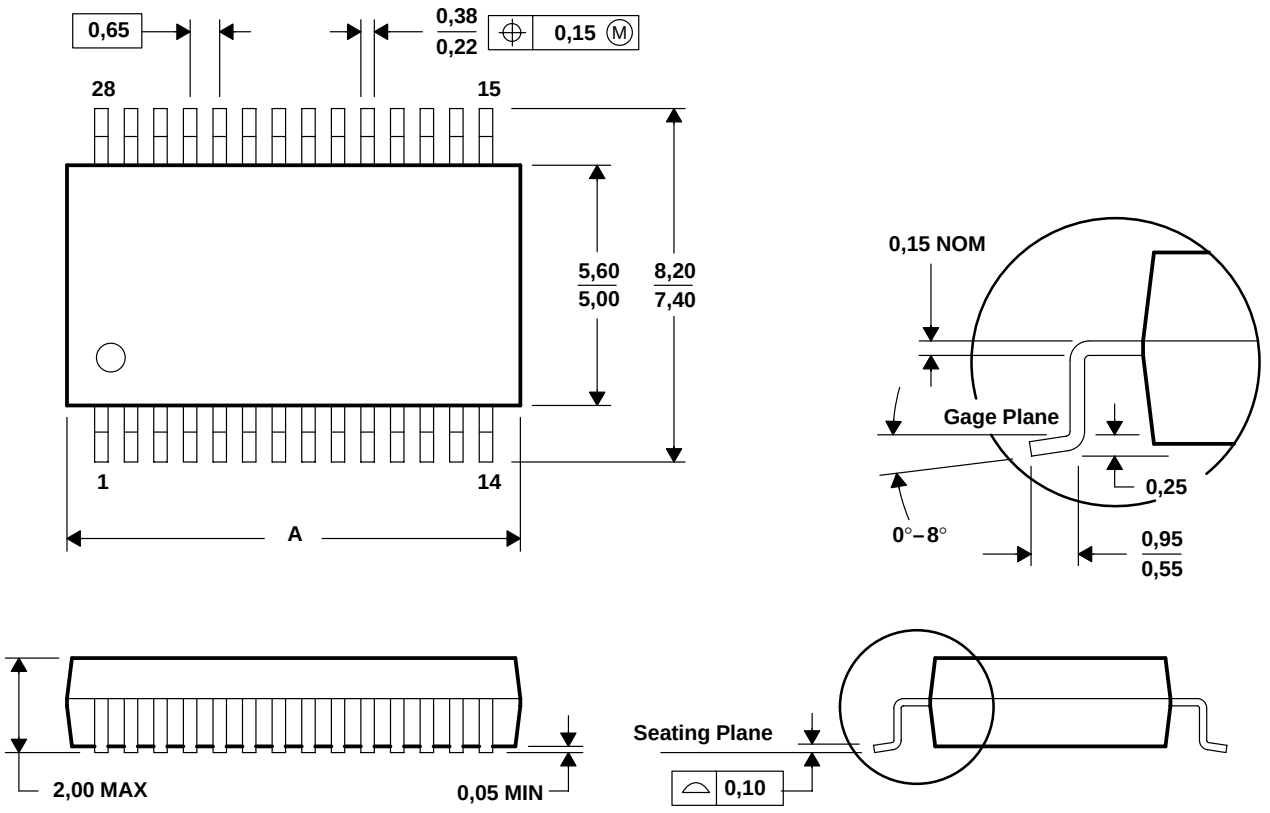
system clock

The quality of the system clock can influence dynamic performance, as the PCM1802 operates based on the system clock. In slave mode, it may be necessary to consider the system-clock duty cycle, jitter, and the time difference between the system clock transition and the BCK or LRCK transition.

MECHANICAL DATA

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /D 09/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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