24-Bit, 96-kHz Sampling, Enhanced Multilevel, Delta-Sigma, Audio Digital-to-Analog Converter

FEATURES

- 24-Bit Resolution
- Analog Performance (V_{CC} = 5 V):
  - Dynamic Range:
    - 106 dB, Typical (PCM1748KE)
    - 100 dB, Typical (PCM1748E)
  - SNR:
    - 106 dB, Typical (PCM1748KE)
    - 100 dB, Typical (PCM1748E)
  - THD+N:
    - 0.002%, Typical (PCM1748KE)
    - 0.003%, Typical (PCM1748E)
  - Full-Scale Output: 3.1 Vp-p, Typical
- 8× Oversampling Digital Filter:
  - Stop-Band Attenuation: –55 dB
  - Pass-Band Ripple: ±0.03 dB
- Sampling Frequency: 5 kHz to 100 kHz
- System Clock: 256 f_S, 384 f_S, 512 f_S, 768 f_S With Autodetect
- Accepts 16-, 18-, 20-, and 24-Bit Audio Data
- Data Formats: Standard, I^2S, and Left-Justified
- User-Programmable Mode Controls:
  - Digital Attenuation: 0 dB to –63 dB, 0.5 dB/Step
  - Digital De-Emphasis
  - Digital Filter Rolloff: Sharp or Slow
  - Soft Mute
  - Zero Flags for Each Output
- Dual-Supply Operation:
  - 5-V Analog
  - 3.3-V Digital
- 5-V Tolerant Digital Inputs
- Small SSOP-16 Package

APPLICATIONS

- AV Receivers
- DVD Movie Players
- DVD Add-On Cards for High-End PCs
- HDTV Receivers
- Car Audio Systems
- Other Applications Requiring 24-Bit Audio

DESCRIPTION

The PCM1748 is a CMOS, monolithic, integrated circuit which includes stereo digital-to-analog converters (DAC) and support circuitry in a small SSOP-16 package. The data converters use Texas Instruments' enhanced multilevel delta-sigma architecture that employs fourth-order noise shaping and 8-level amplitude quantization to achieve excellent dynamic performance and improved tolerance to clock jitter. The PCM1748 accepts industry-standard audio data formats with 16- to 24-bit data, providing easy interfacing to audio DSP and decoder chips. Sampling rates up to 100 kHz are supported. A full set of user-programmable functions is accessible through a 3-wire serial-control port that supports register write functions.

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ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

Power supply voltage, V_{DD}	–0.3 to 4 V
Power supply voltage, V_{CC}	–0.3 to 6.5 V
Supply voltage difference, V_{CC}, V_{DD}	$V_{CC} - V_{DD} < 3$ V
Ground voltage differences	±0.1 V
Digital input voltage	–0.3 V to 6.5 V
Input current (except power supply)	±10 mA
Ambient temperature under bias	–40°C to 125°C
Storage temperature, T_{stg}	–55°C to 150°C
Junction temperature, T_J	150°C
Lead temperature (soldering)	260°C, 5 s
Package temperature (IR reflow, peak)	235°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range

		MIN	NOM	MAX	UNIT
Digital supply voltage, V_{DD}		3	3.3	3.6	V
Analog supply voltage, V_{CC}		4.5	5	5.5	V
Digital input logic family			TTL		
Digital input clock frequency	System clock	8.192		36.864	MHz
	Sampling clock	32		96	kHz
Analog output load resistance		5			kΩ
Analog output load capacitance				50	pF
Digital output load capacitance				20	pF
Operating free-air temperature, T_A		–25		85	°C

ELECTRICAL CHARACTERISTICS

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, f_S = 44.1 kHz, system clock = 384 f_S, and 24-bit data, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESOLUTION				24		Bits
DATA FORMAT						
	Audio data interface formats			Standard, I^2S, left-justified		
	Audio data bit length			16-, 18-, 20-, 24-bit selectable		
	Audio data format			MSB-first, binary 2s complement		
f_S	Sampling frequency		5		100	kHz
	System clock frequency			256 f_S, 384 f_S, 512 f_S, 768 f_S		
DIGITAL INPUT/OUTPUT						
	Logic family			TTL-compatible		
Input Logic Level						
V_{IH}	High-level input votlage		2			VDC
V_{IL}	Low-level input voltage				0.8	VDC

ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, f_S = 44.1 kHz, system clock = 384 f_S, and 24-bit data, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Logic Current						
I_{IH}	High-level input current(1)	$V_{IN} = V_{DD}$			10	µA
I_{IL}	Low-level input current(1)	V_{IN} = 0 V			–10	µA
I_{IH}	High-level input current(2)	$V_{IN} = V_{DD}$		65	100	µA
I_{IL}	Low-level input current(2)	V_{IN} = 0 V			–10	µA
Output Logic Level						
V_{OH}	High-level output votlage(3)	I_{OH} = –2 mA	2.4			VDC
V_{OL}	Low-level output voltage(3)	I_{OL} = 2 mA			1	VDC
DYNAMIC PERFORMANCE(4)						
	PCM1748E					
THD+N	Total harmonic distortion + noise	V_{OUT} = 0 dB, f_S = 44.1 kHz		0.003%	0.008%	
		V_{OUT} = 0 dB, f_S = 96 kHz		0.004%		
		V_{OUT} = –60 dB, f_S = 44.1 kHz		1.2%		
		V_{OUT} = –60 dB, f_S = 96 kHz		1.6%		
	Dynamic range	EIAJ, A-weighted, f_S = 44.1 kHz	94	100		dB
		A-weighted, f_S = 96 kHz		98		
SNR	Signal-to-noise ratio	EIAJ, A-weighted, f_S = 44.1 kHz	94	100		dB
		A-weighted, f_S = 96 kHz		98		
	Channel separation	f_S = 44.1 kHz	91	98		dB
		f_S = 96 kHz		96		
	Level linearity error	V_{OUT} = –90 dB		±0.5		dB
	PCM1748KE					
THD+N	Total harmonic distortion + noise	V_{OUT} = 0 dB, f_S = 44.1 kHz		0.002%	0.006%	
		V_{OUT} = 0 dB, f_S = 96 kHz		0.003%		
		V_{OUT} = –60 dB, f_S = 44.1 kHz		0.65%		
		V_{OUT} = –60 dB, f_S = 96 kHz		0.8%		
	Dynamic range	EIAJ, A-weighted, f_S = 44.1 kHz	100	106		dB
		A-weighted, f_S = 96 kHz		104		
SNR	Signal-to-noise ratio	EIAJ, A-weighted, f_S = 44.1 kHz	100	106		dB
		A-weighted, f_S = 96 kHz		104		
	Channel separation	f_S = 44.1 kHz	97	103		dB
		f_S = 96 kHz		101		
	Level linearity error	V_{OUT} = –90 dB		±0.5		dB
DC ACCURACY						
	Gain error			±1	±6	% of FSR
	Gain mismatch, channel-to-channel			±1	±3	% of FSR
	Bipolar zero error	V_{OUT} = 0.5 V_{CC} at bipolar zero		±30	±60	mV

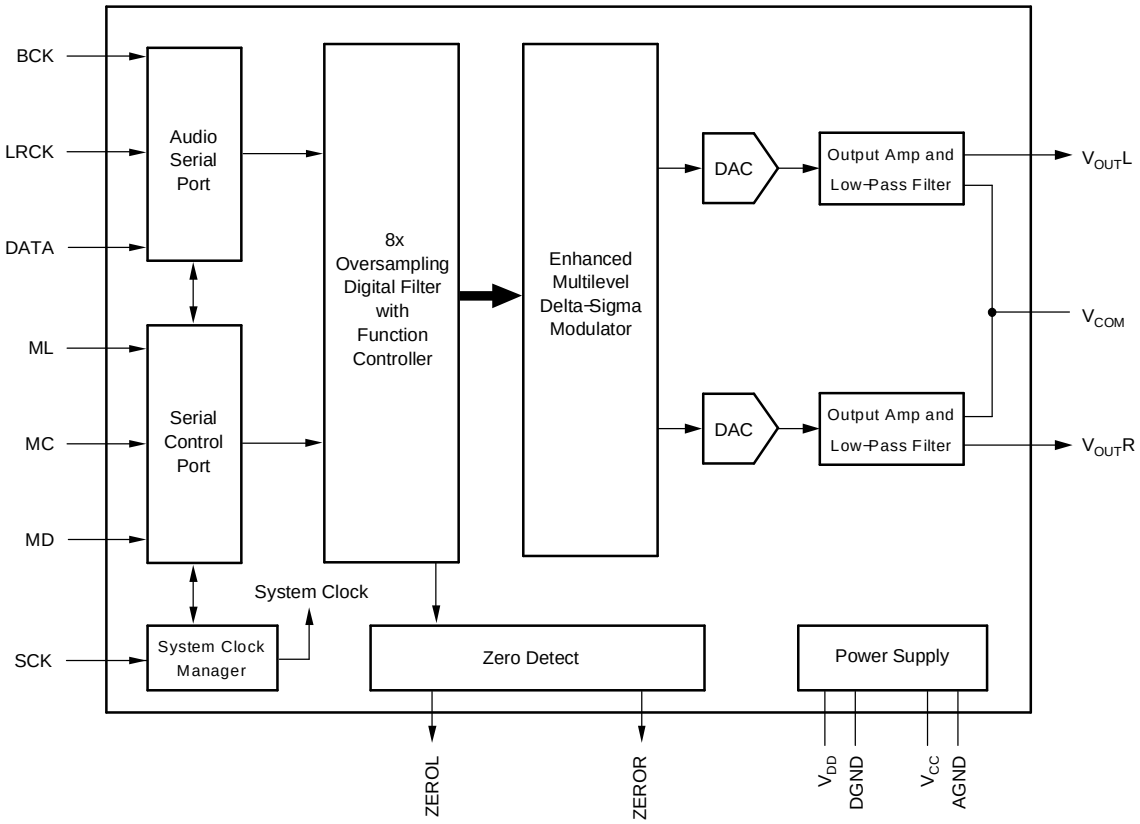
(1) Pins 1, 2, 3, 16 (BCK, DATA, LRCK, SCK)
(2) Pins 13–15 (MD, MC, ML)
(3) Pins 11, 12 (ZEROR, ZEROL)
(4) Analog performance specifications are tested with a Shibasoku #725 THD meter with 400-Hz HPF on, 30-kHz LPF on, and an average mode with 20-kHz bandwidth limiting. The load connected to the analog output is 5 kΩ or larger, via capacitive coupling.

ELECTRICAL CHARACTERISTICS (continued)

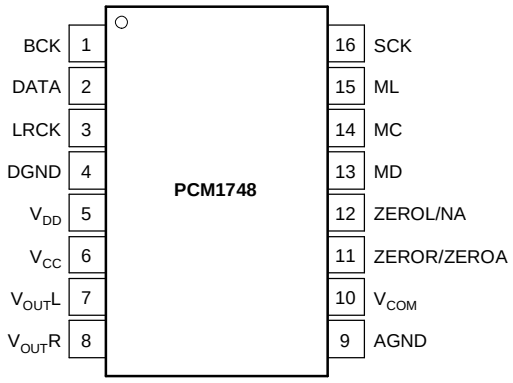
All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, f_S = 44.1 kHz, system clock = 384 f_S, and 24-bit data, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG OUTPUT						
	Output voltage	Full scale (0 dB)		0.62 V_{CC}		Vp-p
	Center voltage			0.5 V_{CC}		VDC
	Load impedance	AC load	5			kΩ
DIGITAL FILTER PERFORMANCE						
Filter Characteristics, Sharp Rolloff						
	Pass band	±0.03 dB			0.454 f_S	
	Pass band	–3 dB			0.487 f_S	
	Stop band		0.546 f_S			
	Pass-band ripple				±0.03	dB
	Stop-band attenuation	Stop band = 0.546 f_S	–50			dB
		Stop band = 0.567 f_S	–55			
Filter Characteristics, Slow Rolloff						
	Pass band	±0.5 dB			0.198 f_S	
	Pass band	–3 dB			0.39 f_S	
	Stop band		0.884 f_S			
	Pass-band ripple				±0.5	dB
	Stop-band attenuation	Stop band = 0.884 f_S	–40			dB
	Delay time			20/f_S		s
	De-emphasis error			±0.1		dB
ANALOG FILTER PERFORMANCE						
	Frequency response	f = 20 kHz		–0.03		dB
		f = 44 kHz		–0.20		
POWER SUPPLY REQUIREMENTS						
V_{DD}	Supply voltage		3	3.3	3.6	VDC
V_{CC}			4.5	5	5.5	
I_{DD}	Supply current	f_S = 44.1 kHz		6	10	mA
		f_S = 96 kHz		13		
I_{CC}		f_S = 44.1 kHz		8.5	13	
		f_S = 96 kHz		9		
	Power dissipation	f_S = 44.1 kHz		62	98	mW
		f_S = 96 kHz		88		
TEMPERATURE RANGE						
T_A	Operation temperature		–25		85	°C
θ_{JA}	Thermal resistance			115		°C/W

Functional Block Diagram



PIN ASSIGNMENTS



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND	9	–	Analog ground
BCK	1	I	Audio data bit clock input (1)
DATA	2	I	Audio data digital input (1)
DGND	4	–	Digital ground
LRCK	3	I	L-channel and R-channel audio data latch enable input (1)
MC	14	I	Mode control clock input (2)
MD	13	I	Mode control data input (2)
ML	15	I	Mode control latch input (2)
SCK	16	I	System clock input (1)
V_{CC}	6	–	Analog power supply, 5-V
V_{COM}	10	–	Common voltage decoupling
V_{DD}	5	–	Digital power supply, 3.3-V
$V_{OUT}L$	7	O	Analog output for L-channel
$V_{OUT}R$	8	O	Analog output for R-channel
ZEROL/NA	12	O	Zero-flag output for L-channel/Not assigned
ZEROR/ZEROA	11	O	Zero-flag output for R-channel/Zero-flag output for L-/R-channels

(1) Schmitt-trigger input, 5-V tolerant
(2) Schmitt-trigger input with internal pulldown, 5-V tolerant

TYPICAL PERFORMANCE CURVES

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, f_S = 44.1 kHz, system clock = 384 f_S, and 24-bit input data, unless otherwise noted

Digital Filter (De-Emphasis Off)

FREQUENCY RESPONSE (SHARP ROLLOFF)

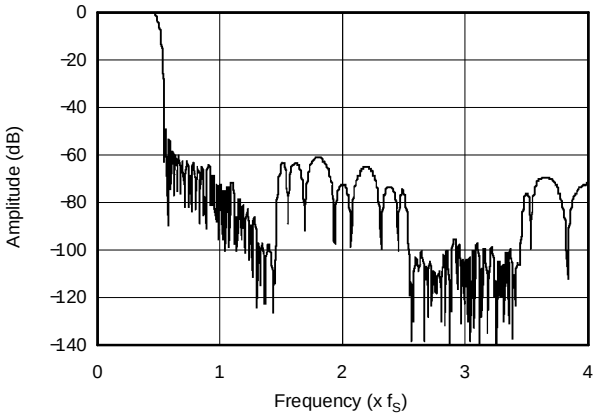


Figure 1.

PASS-BAND FREQUENCY RESPONSE (SHARP ROLLOFF)

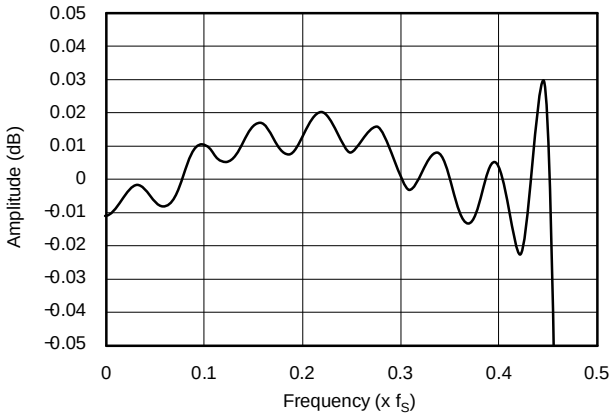


Figure 2.

FREQUENCY RESPONSE (SLOW ROLLOFF)

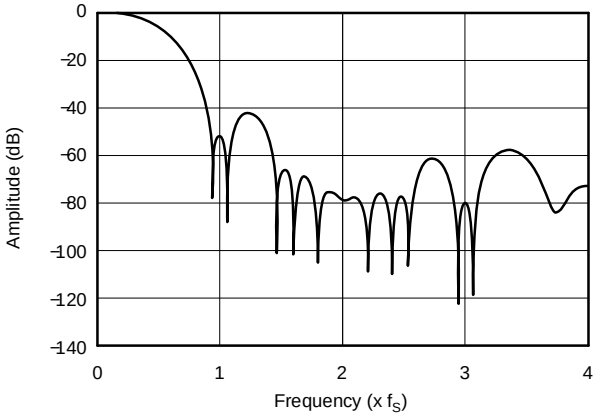


Figure 3.

TRANSITION CHARACTERISTICS (SLOW ROLLOFF)

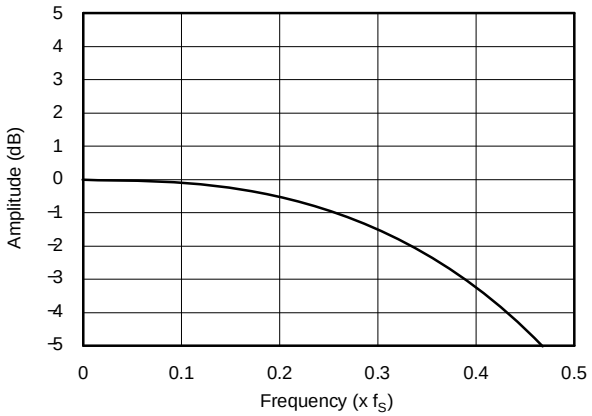


Figure 4.

TYPICAL PERFORMANCE CURVES (continued)

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, f_S = 44.1 kHz, system clock = 384 f_S, and 24-bit input data, unless otherwise noted

Digital Filter (De-Emphasis Curves)

DE-EMPHASIS (f_S = 32 kHz)

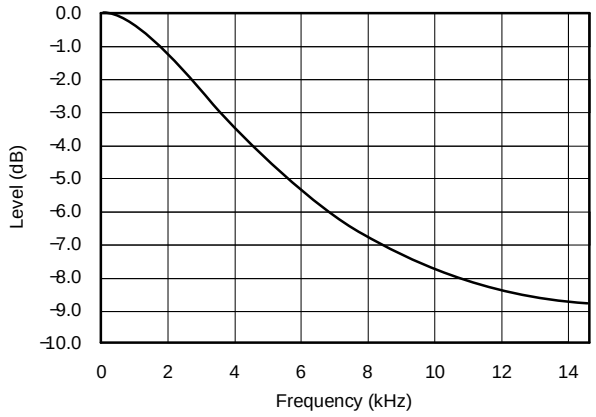


Figure 5.

DE-EMPHASIS ERROR (f_S = 32 kHz)

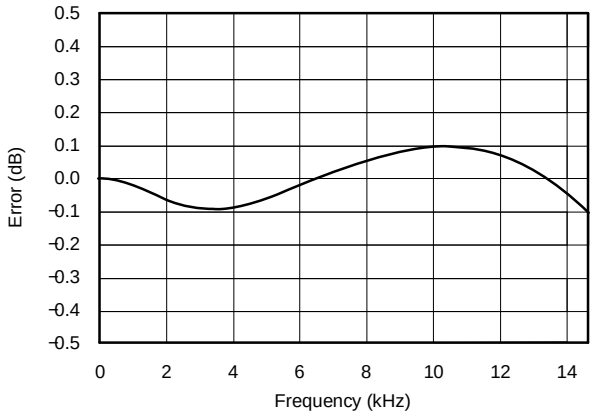


Figure 6.

DE-EMPHASIS (f_S = 44.1 kHz)

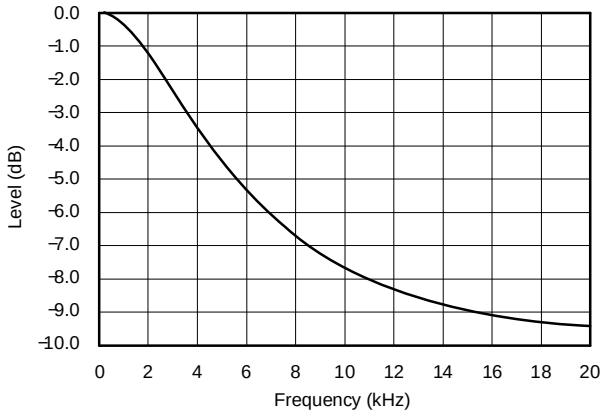


Figure 7.

DE-EMPHASIS ERROR (f_S = 44.1 kHz)

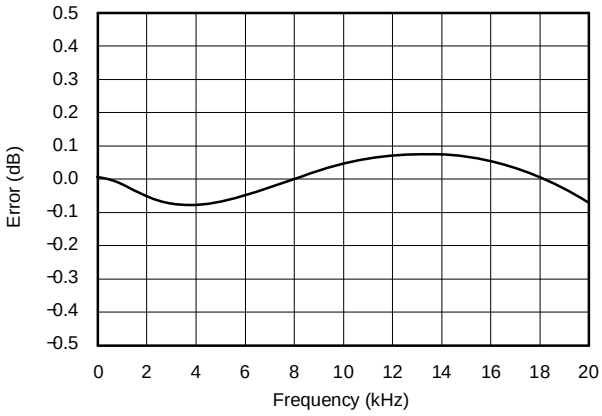


Figure 8.

DE-EMPHASIS (f_S = 48 kHz)

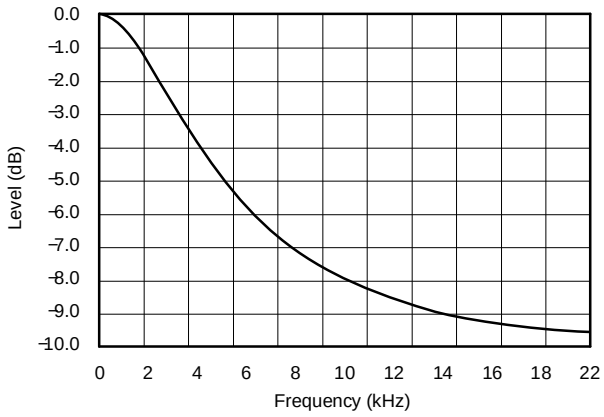


Figure 9.

DE-EMPHASIS ERROR (f_S = 48 kHz)

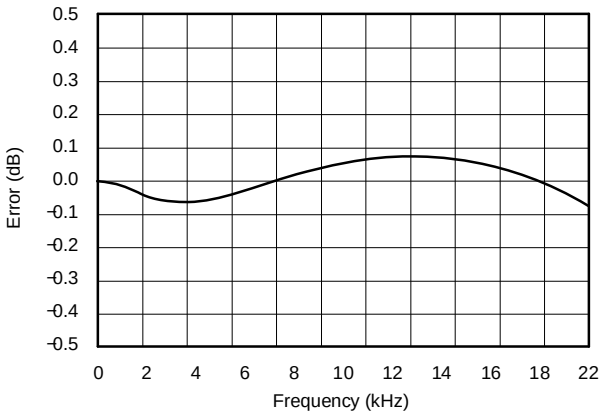


Figure 10.

TYPICAL PERFORMANCE CURVES (continued)

ANALOG DYNAMIC PERFORMANCE

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, and 24-bit input data, unless otherwise noted

Supply-Voltage Characteristics

TOTAL HARMONIC DISTORTION + NOISE vs V_{CC} (V_{DD} = 3.3 V)

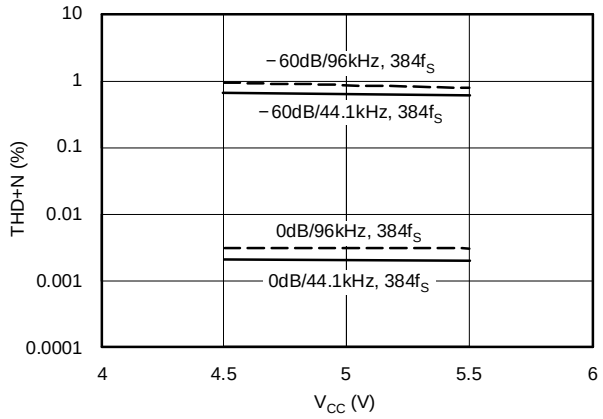


Figure 11.

DYNAMIC RANGE vs V_{CC} (V_{DD} = 3.3 V)

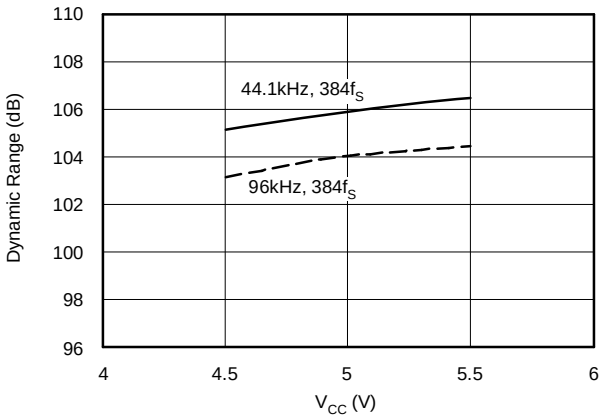


Figure 12.

SIGNAL-TO-NOISE RATIO vs V_{CC} (V_{DD} = 3.3 V)

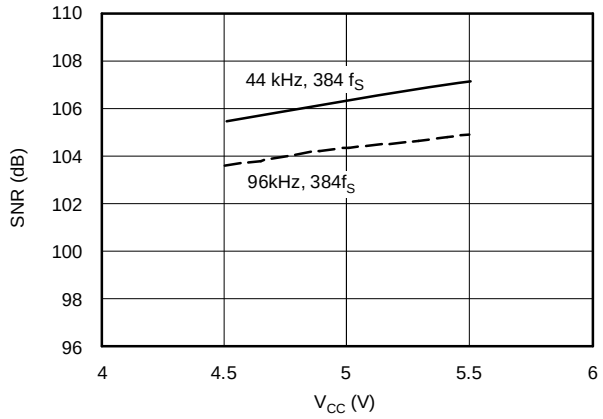


Figure 13.

CHANNEL SEPARATION vs V_{CC} (V_{DD} = 3.3 V)

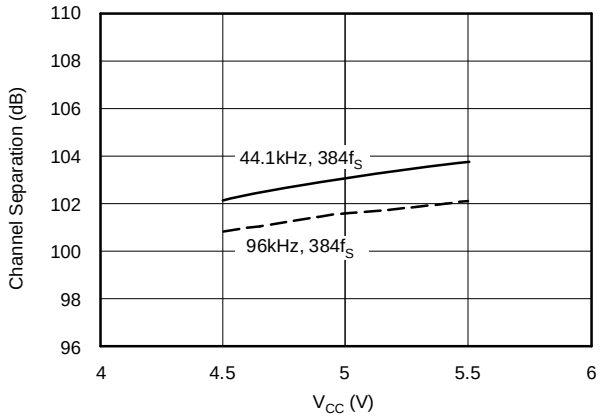


Figure 14.

TYPICAL PERFORMANCE CURVES (continued)

ANALOG DYNAMIC PERFORMANCE (continued)

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, and 24-bit input data, unless otherwise noted

Temperature Characteristics

TOTAL HARMONIC DISTORTION + NOISE vs TEMPERATURE (T_A)

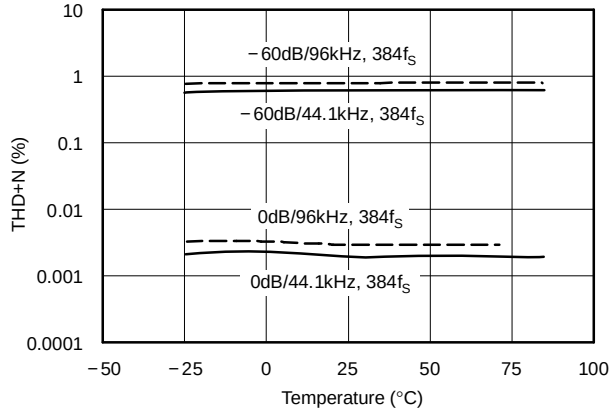


Figure 15.

DYNAMIC RANGE vs TEMPERATURE (T_A)

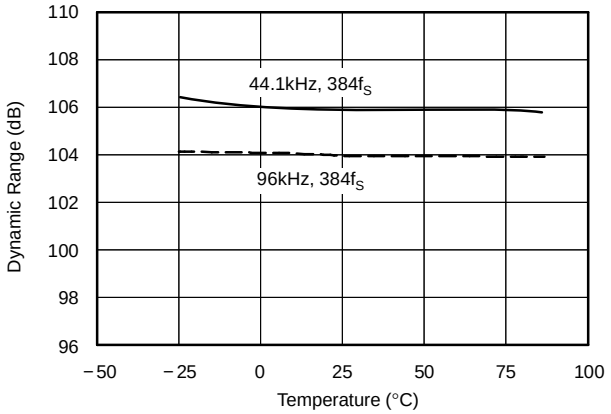


Figure 16.

SIGNAL-TO-NOISE RATIO vs TEMPERATURE (T_A)

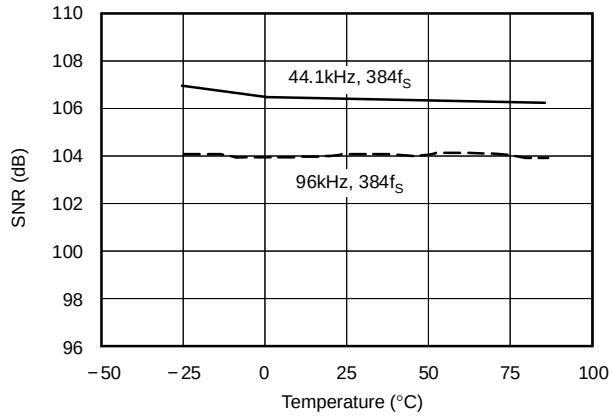


Figure 17.

CHANNEL SEPARATION vs TEMPERATURE (T_A)

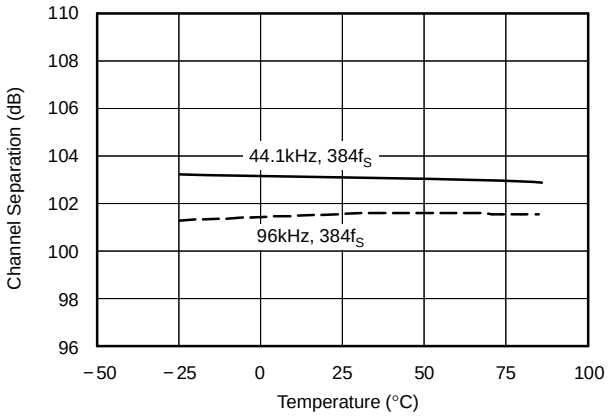


Figure 18.

SYSTEM CLOCK AND RESET FUNCTIONS

SYSTEM CLOCK INPUT

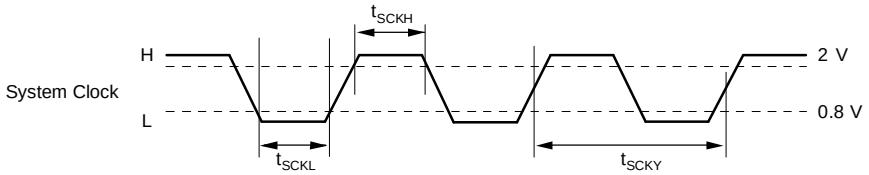
The PCM1748 requires a system clock for operating the digital interpolation filters and multilevel delta-sigma modulators. The system clock is applied at the SCK input (pin 16). Table 1 shows examples of system clock frequencies for common audio sampling rates.

Figure 19 shows the timing requirements for the system clock input. For optimal performance, it is important to use a clock source with low phase jitter and noise. The PLL1700 multiclock generator from Texas Instruments is an excellent choice for providing the PCM1748 system clock.

Table 1. System Clock Rates for Common Audio Sampling Frequencies

SAMPLING FREQUENCY (kHz)	SYSTEM CLOCK FREQUENCY (f_{SCLK}) (MHz)			
	256 f_S	**384 f_S**	**512 f_S**	**768 f_S**
8	2.048	3.072	4.096	6.144
16	4.096	6.144	8.192	12.288
32	8.192	12.288	16.384	24.576
44.1	11.2896	16.9344	22.5792	33.8688
48	12.288	18.432	24.576	36.864
88.2	22.5792	33.8688	45.1584	(1)
96	24.576	36.864	49.152	(1)

(1) This system clock is not supported for the given sampling frequency.



SYMBOL	DESCRIPTION	MIN	MAX	UNIT
t_{SCKY}	System clock cycle time (1)	20		ns
t_{SCKH}	System clock pulse duration, HIGH	7		ns
t_{SCKL}	System clock pulse duration, LOW	7		ns

(1) 1/256 f_S, 1/384 f_S, 1/512 f_S, or 1/768 f_S

Figure 19. System Clock Input Timing

POWER-ON-RESET FUNCTIONS

The PCM1748 includes a power-on-reset function, as shown in Figure 20. With the system clock active, and V_{DD} > 2 V (typical, 1.6 V to 2.4 V), the power-on-reset function is enabled. The initialization sequence requires 1024 system clocks from the time V_{DD} > 2 V. After the initialization period, the PCM1748 is set to its reset default state, as described in the *Mode Control Register*s section of this data sheet.

During the reset period (1024 system clocks), the analog outputs are forced to the bipolar zero level, or $V_{CC}/2$. After the reset period, all the mode control registers are initialized in the next $1/f_S$ period and, if SCK, BCK, and LRCK are provided continuously, the PCM1748 provides proper analog output with group delay corresponding to the input data.

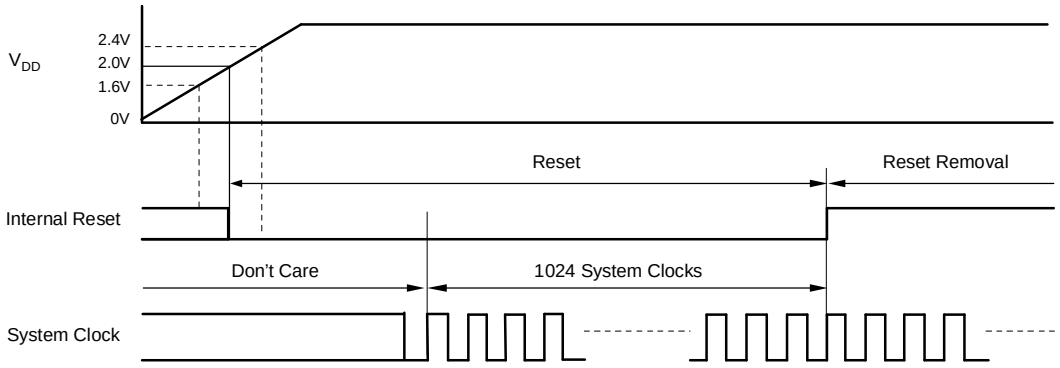


Figure 20. Power-On-Reset Timing

AUDIO SERIAL INTERFACE

The audio serial interface for the PCM1748 comprises a 3-wire synchronous serial port. It includes LRCK (pin 3), BCK (pin 1), and DATA (pin 2). BCK is the serial audio bit clock, and is used to clock the serial data present on DATA into the audio interface serial shift register. Serial data is clocked into the PCM1748 on the rising edge of BCK. LRCK is the serial audio left/right word clock used to latch serial data into the serial audio interface internal registers.

Both LRCK and BCK should be synchronous to the system clock. Ideally, it is recommended that LRCK and BCK be derived from the system clock input, SCK. LRCK is operated at the sampling frequency, f_S. BCK can be operated at 32 (16-bit, right-justified only), 48, or 64 times the sampling frequency. Internal operation of the PCM1748 is synchronized with LRCK. Accordingly, internal operation of the device is suspended when the sampling rate clock of LRCK is changed or SCK and/or BCK is interrupted at least for a 3-bit clock cycle. If SCK, BCK, and LRCK are provided continuously after this suspended state, the internal operation is resynchronized automatically within a period of less than $3/f_S$. During this resynchronization period and for a $3/f_S$ time thereafter, the analog output is forced to the bipolar zero level, or $V_{CC}/2$. External resetting is not required.

AUDIO DATA FORMATS AND TIMING

The PCM1748 supports industry-standard audio data formats, including standard, I^{2}S, and left-justified, as shown in Figure 21. Data formats are selected using the format bits, FMT[2:0], in control register 20. The default data format is 24-bit left justified. All formats require binary 2s complement, MSB-first audio data. See Figure 22 for a detailed timing diagram of the serial audio interface.

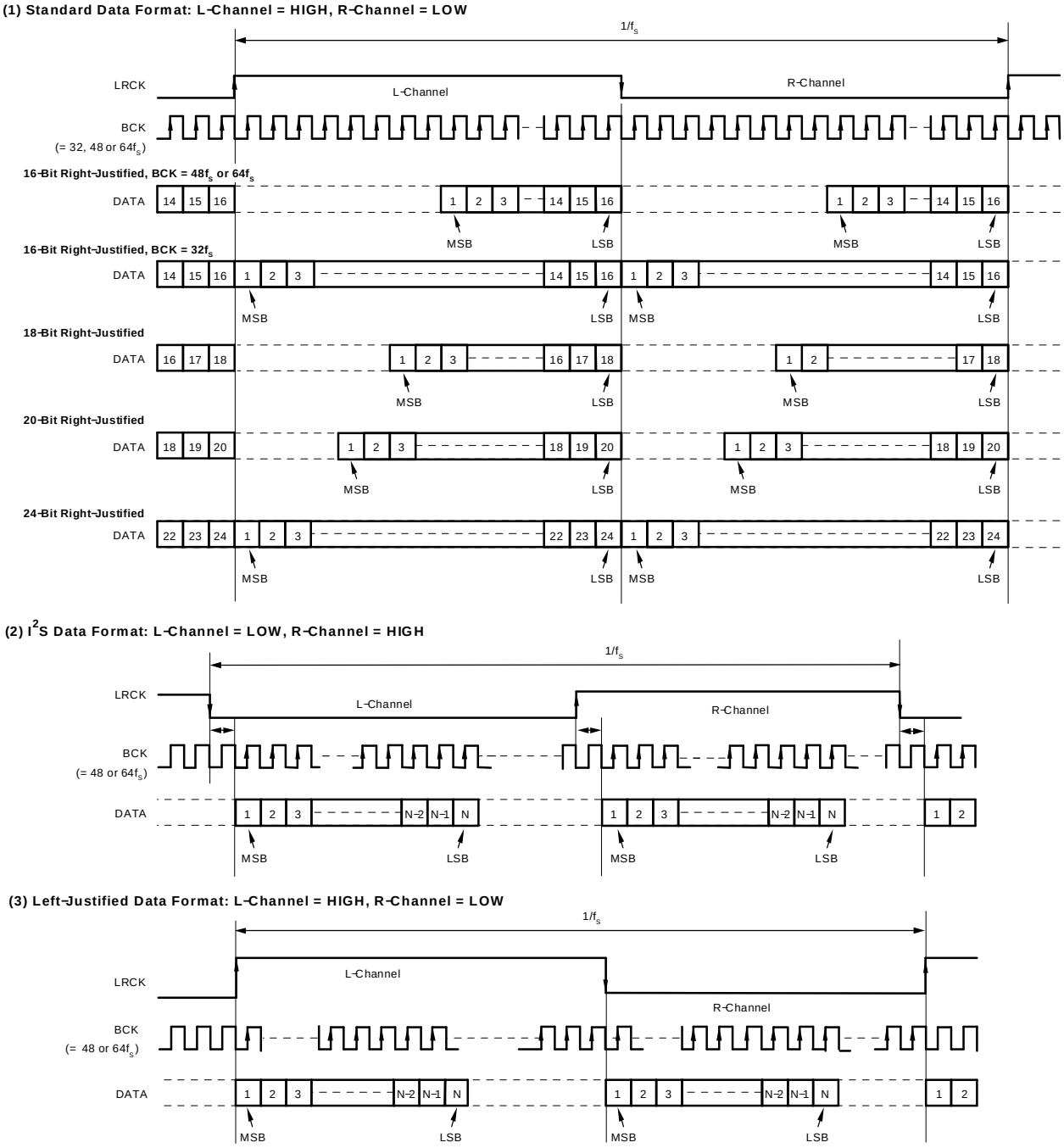
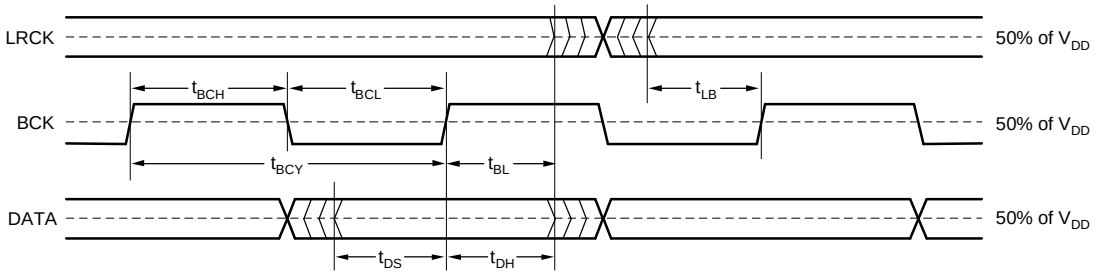


Figure 21. Audio Data Input Formats



SYMBOL	DESCRIPTION	MIN	MAX	UNIT
t_{BCY}	BCK pulse cycle time	1/(64 f_S)(1)		
t_{BCH}	BCK high-level time	35		ns
t_{BCL}	BCK low-level time	35		ns
t_{BL}	BCK rising edge to LRCK edge	10		ns
t_{LB}	LRCK falling edge to BCK rising edge	10		ns
t_{DS}	DATA setup time	10		ns
t_{DH}	DATA hold time	10		ns

(1) f_S is the sampling frequency (e.g., 44.1 kHz, 48 kHz, 96 kHz, etc.).

Figure 22. Audio Interface Timing

SERIAL CONTROL INTERFACE

The serial control interface is a 3-wire serial port that operates asynchronously to the serial audio interface. The serial control interface is used to program the on-chip mode registers. The control interface includes MD (pin 13), MC (pin 14), and ML (pin 15). MD is the serial data input, used to program the mode registers; MC is the serial bit clock, used to shift data into the control port; and ML is the control port latch clock.

REGISTER WRITE OPERATION

All write operations for the serial control port use 16-bit data words. Figure 23 shows the control data word format. The most significant bit must be a 0. Seven bits, labeled IDX[6:0], set the register index (or address) for the write operation. The least significant eight bits, D[7:0], contain the data to be written to the register specified by IDX[6:0].

Figure 24 shows the functional timing diagram for writing to the serial control port. ML is held at a logic-1 state until a register is to be written. To start the register write cycle, ML is set to logic-0. Sixteen clocks are then provided on MC, corresponding to the 16 bits of the control data word on MD. After the sixteenth clock cycle has completed, ML is set to logic-1 to latch the data into the indexed mode control register.

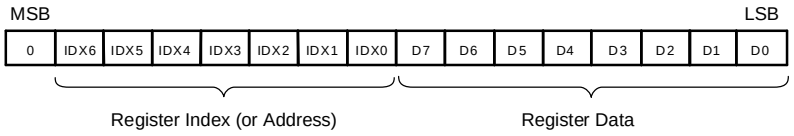


Figure 23. Control Data Word Format for MD

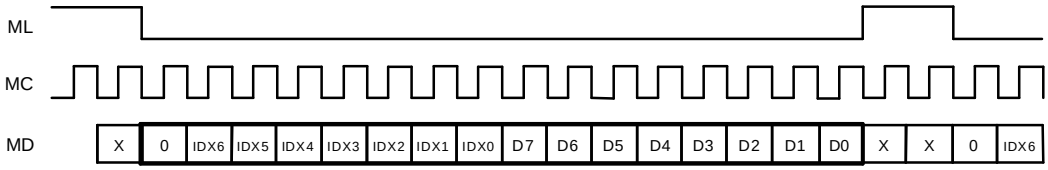
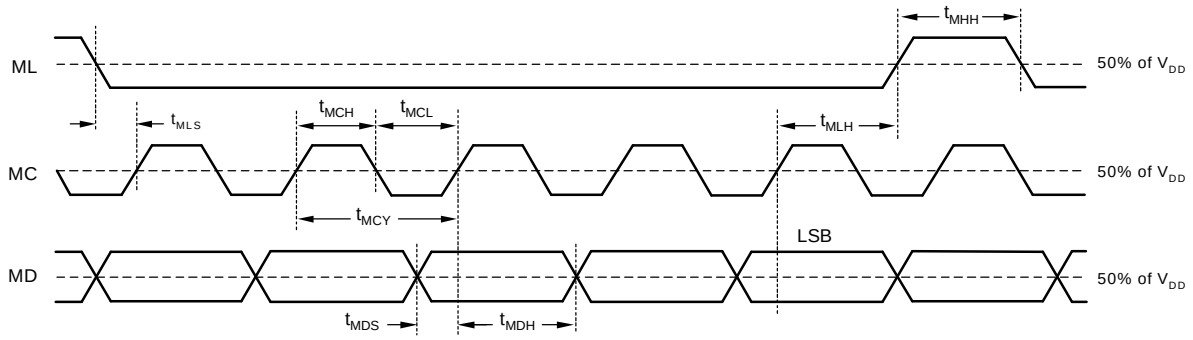


Figure 24. Register Write Operation

CONTROL INTERFACE TIMING REQUIREMENTS

See Figure 25 for a detailed timing diagram of the serial control interface. These timing parameters are critical for proper control port operation.



SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
t_{MCY}	MC pulse cycle time	100			ns
t_{MCL}	MC low-level time	50			ns
t_{MCH}	MC high-level time	50			ns
t_{MHH}	ML high-level time	$3/(256 \times f_S)$ (2)			ns
t_{MLS}	ML falling edge to MC rising edge	20			ns
t_{MLH}	ML hold time (1)	20			ns
t_{MDH}	MD hold time	15			ns
t_{MDS}	MD setup time	20			ns

(1) MC rising edge for LSB to ML rising edge

(2) f_S = sampling rate

Figure 25. Control Interface Timing

MODE CONTROL REGISTERS

User-Programmable Mode Controls

The PCM1748 includes a number of user-programmable functions that are accessed via control registers. The registers are programmed using the serial control interface that was previously discussed in this data sheet. Table 2 lists the available mode control functions, along with their reset default conditions and associated register index.

Table 2. User-Programmable Mode Controls

FUNCTION	RESET DEFAULT	CONTROL REGISTER	INDEX IDX[6:0]
Digital attenuation control, 0 dB to –63 dB in 0.5-dB steps	0 dB, no attenuation	16 and 17	AT1[7:0], AT2[7:0]
Soft mute control	Mute disabled	18	MUT[2:0]
Oversampling rate control (64 f_S or 128 f_S)	64-f_S oversampling	18	OVER
DAC operation control	DAC1 and DAC2 enabled	19	DAC[2:1]
De-emphasis function control	De-emphasis disabled	19	DM12
De-emphasis sample rate selection	44.1 kHz	19	DMF[1:0]
Audio data format control	24-bit left-justified	20	FMT[2:0]
Digital filter rolloff control	Sharp rolloff	20	FLT
Zero flag function select	L-/R-channels independent	22	AZRO
Output phase select	Normal phase	22	DREV
Zero-flag polarity select	High	22	ZREV

Register Map

The mode control register map is shown in Table 3. Each register includes an index (or address) indicated by the IDX[6:0] bits.

Table 3. Mode Control Register Map

IDX (B14–B8)	REGISTER	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
10h	16	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT17	AT16	AT15	AT14	AT13	AT12	AT11	AT10
11h	17	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT27	AT26	AT25	AT24	AT23	AT22	AT21	AT20
12h	18	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV(1)	OVER	RSV(1)	RSV(1)	RSV(1)	RSV(1)	MUT2	MUT1
13h	19	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV(1)	DMF1	DMF0	DM12	RSV(1)	RSV(1)	DAC2	DAC1
14h	20	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV(1)	RSV(1)	FLT	RSV(1)	RSV(1)	FMT2	FMT1	FMT0
15h	21	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV(1)	RSV(1)	RSV(1)	RSV(1)	RSV(1)	RSV(1)	RSV(1)	RSV(1)
16h	22	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV(1)	RSV(1)	RSV(1)	RSV(1)	RSV(1)	AZRO	ZREV	DREV

(1) Reserved for test operation. It should be set to 0 during normal operation.

REGISTER DEFINITIONS

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 16	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT17	AT16	AT15	AT14	AT13	AT12	AT11	AT10
REGISTER 17	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT27	AT26	AT25	AT24	AT23	AT22	AT21	AT20

ATx[7:0] – Digital Attenuation Level Setting

where x = 1 or 2, corresponding to the DAC output $V_{OUT}L$ (x = 1) and $V_{OUT}R$ (x = 2).

Default value: 1111 1111b

Each DAC channel ($V_{OUT}L$ and $V_{OUT}R$) includes a digital attenuator function. The attenuation level can be set from 0 dB to –63 dB in 0.5-dB steps. Changes in attenuation levels are made by incrementing or decrementing, by one step (0.5 dB), for every $8/f_S$ time interval until the programmed attenuator setting is reached. Alternatively, the attenuation level can be set to infinite attenuation, or mute. The attenuation data for each channel can be set individually.

The attenuation level is calculated using the following formula:

$$\text{Attenuation level (dB)} = 0.5\ (\text{ATx}[7:0]_{DEC} - 255)$$

where $\text{ATx}[7:0]_{DEC}$ = 0 through 255.

For $\text{ATx}[7:0]_{DEC}$ = 0 through 128, the attenuator is set to infinite attenuation.

The following table shows attenuator levels for various settings.

ATx[7:0]	DECIMAL VALUE	ATTENUATOR LEVEL SETTING
1111 1111b	255	0 dB, no attenuation (default)
1111 1110b	254	–0.5 dB
1111 1101b	253	–1 dB
:	:	:
1000 0011b	131	–62 dB
1000 0010b	130	–62.5 dB
1000 0001b	129	–63 dB
1000 0000b	128	Mute
:	:	:
0000 0000b	0	Mute

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 18	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	OVER	RSV	RSV	RSV	RSV	MUT2	MUT1

MUTx – Soft Mute Control

where x = 1 or 2, corresponding to the DAC output $V_{OUT}L$ (x = 1) and $V_{OUT}R$ (x = 2)

Default value: 0

MUTx = 0	Mute disabled (default)
MUTx = 1	Mute enabled

The mute bits, MUT1 and MUT2, are used to enable or disable the soft mute function for the corresponding DAC outputs, $V_{OUT}L$ and $V_{OUT}R$. The soft mute function is incorporated into the digital attenuators. When mute is disabled (MUTx = 0), the attenuator and DAC operate normally. When mute is enabled by setting MUTx = 1, the digital attenuator for the corresponding output is decreased from the current setting to the infinite attenuation setting by one attenuator step (0.5 dB) at a time for every $8/f_S$ period. This provides a quiet, pop-free muting of the DAC output.

By setting MUTx = 0, the attenuator is increased by one step for every $8/f_S$ period to the previously programmed attenuation level.

OVER – Oversampling Rate Control

Default value: 0

OVER = 0	64× oversampling (default)
OVER = 1	128× oversampling

The OVER bit is used to control the oversampling rate of the delta-sigma DACs.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 19	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	DMF1	DMF0	DM12	RSV	RSV	DAC2	DAC1

DACx – DAC Operation Control

where x = 1 or 2, corresponding to the DAC output $V_{OUT}L$ (x = 1) or $V_{OUT}R$ (x = 2)

Default value: 0

DACx = 0	DAC operation enabled (default)
DACx = 1	DAC operation disabled

The DAC operation controls are used to enable and disable the DAC outputs, $V_{OUT}L$ and $V_{OUT}R$. When DACx = 0, the corresponding output generates the audio waveform dictated by the data present on the DATA pin. When DACx = 1, the corresponding output is set to the bipolar zero level, or $V_{CC}/2$.

DM12 – Digital De-Emphasis Function Control

Default value: 0

DM12 = 0	De-emphasis disabled (default)
DM12 = 1	De-emphasis enabled

The DM12 bit is used to enable or disable the digital de-emphasis function. Refer to the *Typical Performance Curves* section of this data sheet for more information.

DMF[1:0] – Sampling Frequency Selection for the De-Emphasis Function

Default value: 00

DMF[1:0]	De-Emphasis Sample Rate Selection
00	44.1 kHz (default)
01	48 kHz
10	32 kHz
11	Reserved

The DMF[1:0] bits select the sampling frequency used for the digital de-emphasis function when it is enabled.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 20	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	FLT	RSV	RSV	FMT2	FMT1	FMT0

FMT[2:0] – Audio Interface Data Format

Default value: 101

The FMT[2:0] bits are used to select the data format for the serial audio interface. The following table shows the available format options.

FMT[2:0]	Audio Data Format Selection
000	24-bit standard format, right-justified data
001	20-bit standard format, right-justified data
010	18-bit standard format, right-justified data
011	16-bit standard format, right-justified data
100	I^2S format, 16- to 24-bit
101	Left-justified format, 16- to 24-bit (default)
110	Reserved
111	Reserved

FLT – Digital Filter Rolloff Control

Default value: 0

FLT = 0	Sharp rolloff (default)
FLT = 1	Slow rolloff

The FLT bit allows users to select the digital filter rolloff that is best suited to their application. Two filter rolloff selections are available: sharp or slow. The filter responses for these selections are shown in the *Typical Performance Curves* section of this data sheet.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 22	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	RSV	RSV	AZRO	ZREV	DREV

DREV – Output Phase Select

Default value: 0

DREV = 0	Normal output (default)
DREV = 1	Inverted output

The DREV bit is used to set the output phase of $V_{OUT}L$ and $V_{OUT}R$.

ZREV – Zero-Flag Polarity Select

Default value: 0

ZREV = 0	Zero-flag pins HIGH at a zero detect (default)
ZREV = 1	Zero-flag pins LOW at a zero detect

The ZREV bit allows the user to select the active polarity of zero-flag pins.

AZRO – Zero-Flag Function Select

Default value: 0

AZRO = 0	L-/R-channel independent zero flags (default)	Pin 11: ZEROR = zero-flag output for R-channel Pin 12: ZEROL = zero flag output for L-channel
AZRO = 1	L-/R-channel common zero flag	Pin 11: ZEROA = zero flag output for L-/R-channel Pin 12: NA, not assigned

The AZRO bit allows the user to select the function of the zero-flag pins

ANALOG OUTPUTS

The PCM1748 includes two independent output channels: $V_{OUT}L$ and $V_{OUT}R$. These are unbalanced outputs, each capable of driving 3.1 Vp-p typical into a 5-kΩ ac-coupled load. The internal output amplifiers for $V_{OUT}L$ and $V_{OUT}R$ are biased to the dc common-mode (or bipolar zero) voltage, equal to $V_{CC}/2$.

The output amplifiers include an RC continuous-time filter that helps to reduce the out-of-band noise energy present at the DAC outputs, due to the noise shaping characteristics of the PCM1748 delta-sigma DACs. The frequency response of this filter is shown in Figure 26. By itself, this filter is not enough to attenuate the out-of-band noise to an acceptable level for many applications; therefore, an external low-pass filter is required to provide sufficient out-of-band noise rejection. Further discussion of DAC post-filter circuits is provided in the *Application Information* section of this data sheet.

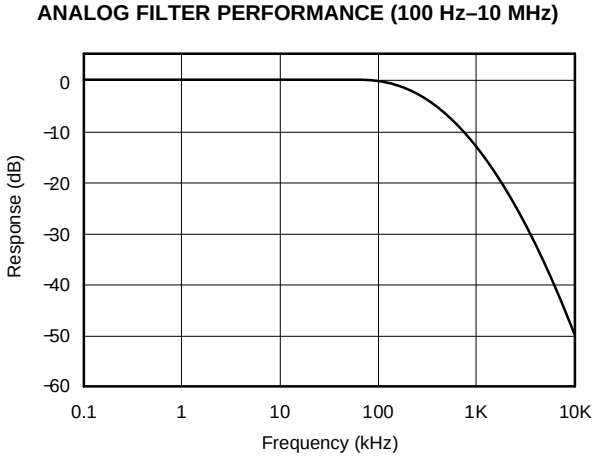
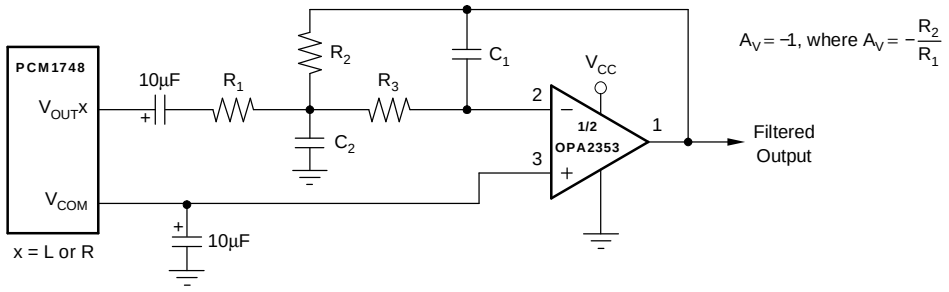


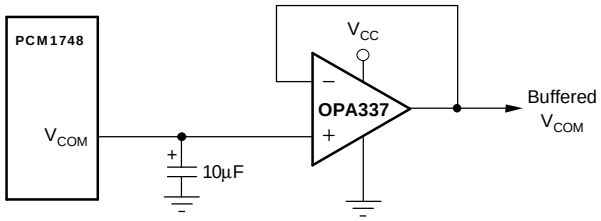
Figure 26. Output Filter Frequency Response

V_{COM} OUTPUT

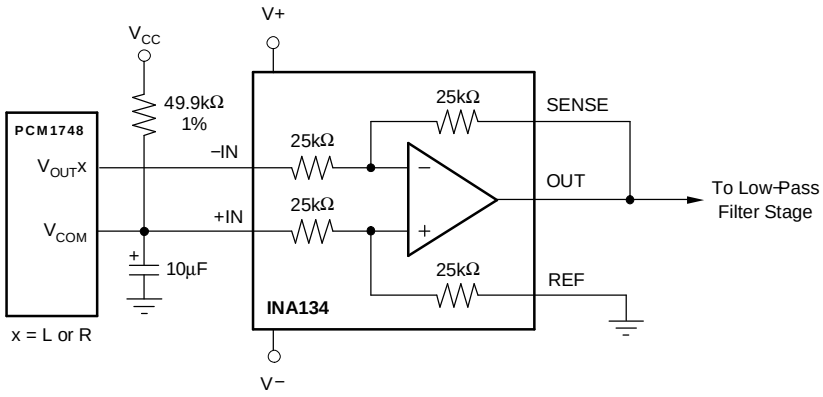
One unbuffered common-mode voltage output pin, V_{COM} (pin 10), is brought out for decoupling purposes. This pin is nominally biased to a dc voltage level equal to $V_{CC}/2$. This pin can be used to bias external circuits. An example of using the V_{COM} pin for external biasing applications is shown in Figure 27.



(a) Using V_{COM} to Bias a Single-Supply Filter Stage



(b) Using a Voltage Follower to Buffer V_{COM} when Biasing Multiple Nodes



(c) Using an INA134 for DC-Coupled Output

Figure 27. Biasing External Circuits Using the V_{COM} Pin

ZERO FLAGS

Zero-Detect Condition

Zero detection for each output channel is independent from the other. If the data for a given channel remains at a 0 level for 1024 sample periods (or LRCK clock periods), a zero-detect condition exists for that channel.

Zero Output Flags

Given that a zero-detect condition exists for one or more channels, the zero-flag pins for those channels are set to a logic-1 state. The zero-flag pins for each channel are ZEROL (pin 12) and ZEROR (pin 11). These pins can be used to operate external mute circuits, or used as status indicators for a microcontroller, audio signal processor, or other digitally controlled function.

The active polarity of the zero-flag output can be inverted by setting the ZREV bit of control register 22 to 1. The reset default is active-high output, or ZREV = 0.

The L-channel and R-channel common-zero flag can be selected by setting the AZRO bit of control register 22 to 1. The reset default is L-channel and R-channel independent zero flags, or AZRO = 0.

APPLICATION INFORMATION

Connection Diagram

A basic connection diagram is shown in Figure 28, with the necessary power-supply bypassing and decoupling components. Texas Instruments recommends using the component values shown in Figure 28 for all designs.

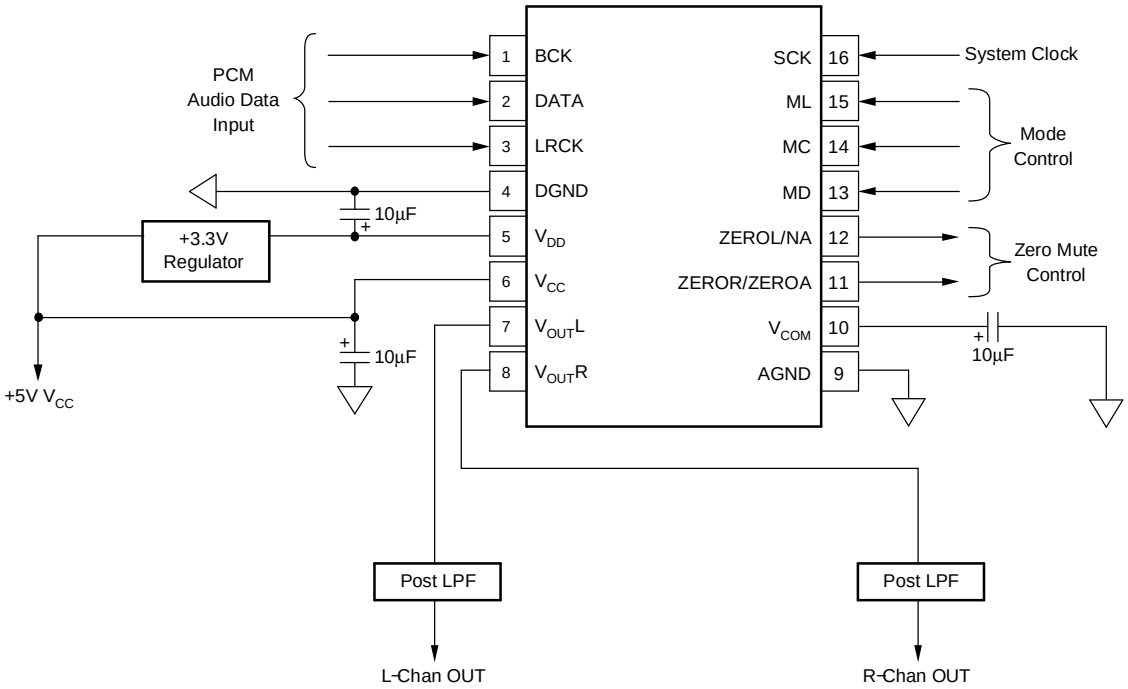


Figure 28. Basic Connection Diagram

The use of series resistors (22 Ω to 100 Ω) is recommended for the SCK, LRCK, BCK, and DATA inputs. The series resistor combines with stray PCB and device input capacitance to form a low-pass filter that reduces high-frequency noise emissions and helps to dampen glitches and ringing present on clock and data lines.

Power Supplies and Grounding

The PCM1748 requires a 5-V analog supply (V_{CC}) and a 3.3-V digital supply (V_{DD}). The 5-V supply is used to power the DAC analog and output filter circuitry, while the 3.3-V supply is used to power the digital filter and serial interface circuitry. For best performance, the 3.3-V supply should be derived from the 5-V supply using a linear regulator, as shown in Figure 28. The REG1117-3.3 from Texas Instruments is an ideal choice for this application.

Proper power-supply bypassing is shown in Figure 28. The 10-µF capacitors should be tantalum or aluminum electrolytic.

DAC Output Filter Circuits

Delta-sigma DACs use noise-shaping techniques to improve in-band signal-to-noise ratio (SNR) performance at the expense of generating increased out-of-band noise above the Nyquist frequency, or $f_S/2$. The out-of-band noise must be low-pass filtered in order to provide optimal converter performance. This is accomplished by a combination of on-chip and external low-pass filtering.

Figure 27(a) and Figure 29 show the recommended external low-pass active filter circuits for single- and dual-supply applications. These circuits are second-order Butterworth filters using a multiple feedback (MFB) circuit arrangement that reduces sensitivity to passive component variations over frequency and temperature. For more information regarding MFB active filter design, see *FilterPro™ MFB and Sallen-Key Low-Pass Filter Design Program* (SBFA001), available from the TI Web site at http://www.ti.com.

APPLICATION INFORMATION (continued)

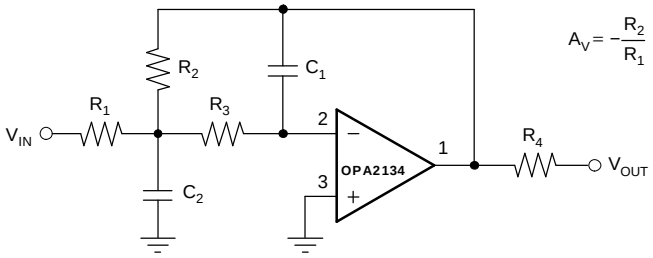


Figure 29. Dual-Supply Filter Circuit

Because the overall system performance is defined by the quality of the DACs and their associated analog output circuitry, high-quality audio operational amplifiers are recommended for the active filters. The OPA2353 and OPA2134 dual operational amplifiers from Texas Instruments are recommended for use with the PCM1748; see Figure 27(a) and Figure 29.

PCB LAYOUT GUIDELINES

A typical PCB floor plan for the PCM1748 is shown in Figure 30. A ground plane is recommended, with the analog and digital sections being isolated from one another using a split or cut in the circuit board. The PCM1748 should be oriented with the digital I/O pins facing the ground plane split/cut to allow for short, direct connections to the digital audio interface and control signals originating from the digital section of the board.

Separate power supplies are recommended for the digital and analog sections of the board. This prevents the switching noise present on the digital supply from contaminating the analog power supply and degrading the dynamic performance of the PCM1748. In cases where a common 5-V supply must be used for the analog and digital sections, an inductance (RF choke, ferrite bead) should be placed between the analog and digital 5-V supply connections to avoid coupling of the digital switching noise into the analog circuitry. Figure 31 shows the recommended approach for single-supply applications.

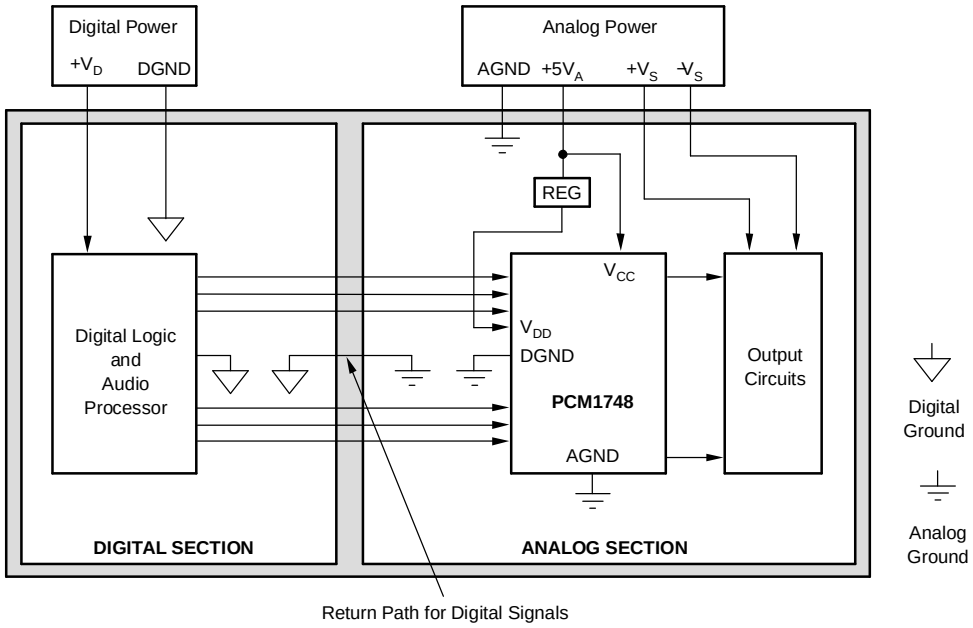


Figure 30. Recommended PCB Layout

APPLICATION INFORMATION (continued)

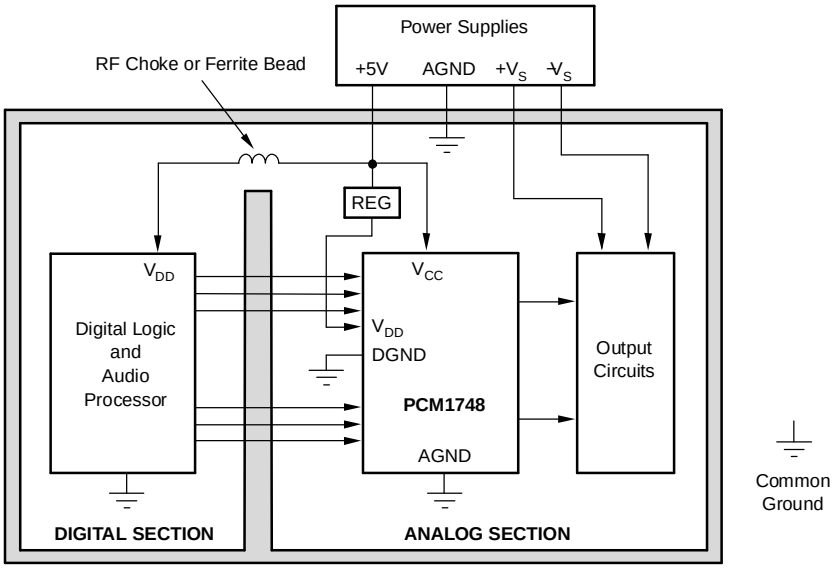


Figure 31. Single-Supply PCB Layout

THEORY OF OPERATION

The delta-sigma section of the PCM1748 is based on an 8-level amplitude quantizer and a fourth-order noise shaper. This section converts the oversampled input data to 8-level delta-sigma format. A block diagram of the 8-level delta-sigma modulator is shown in Figure 32. This 8-level delta-sigma modulator has the advantage of stability and clock jitter sensitivity over the typical one-bit (2-level) delta-sigma modulator. The combined oversampling rate of the delta-sigma modulator and the interpolation filter is 64 f_S.

The theoretical quantization noise performance of the 8-level delta-sigma modulator is shown in Figure 33. The enhanced multilevel delta-sigma architecture also has advantages for input clock-jitter sensitivity due to the multilevel quantizer, with the simulated jitter sensitivity as shown in Figure 34.

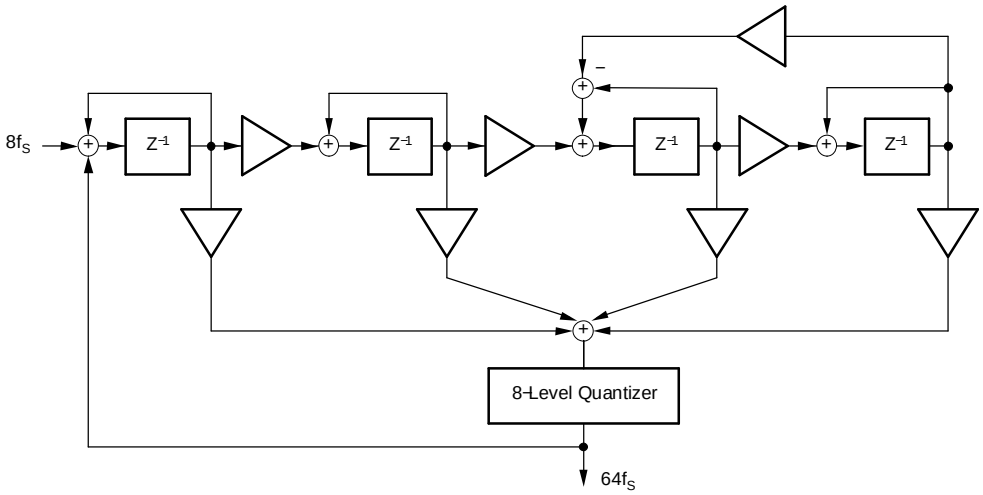


Figure 32. 8-Level Delta-Sigma Modulator

APPLICATION INFORMATION (continued)

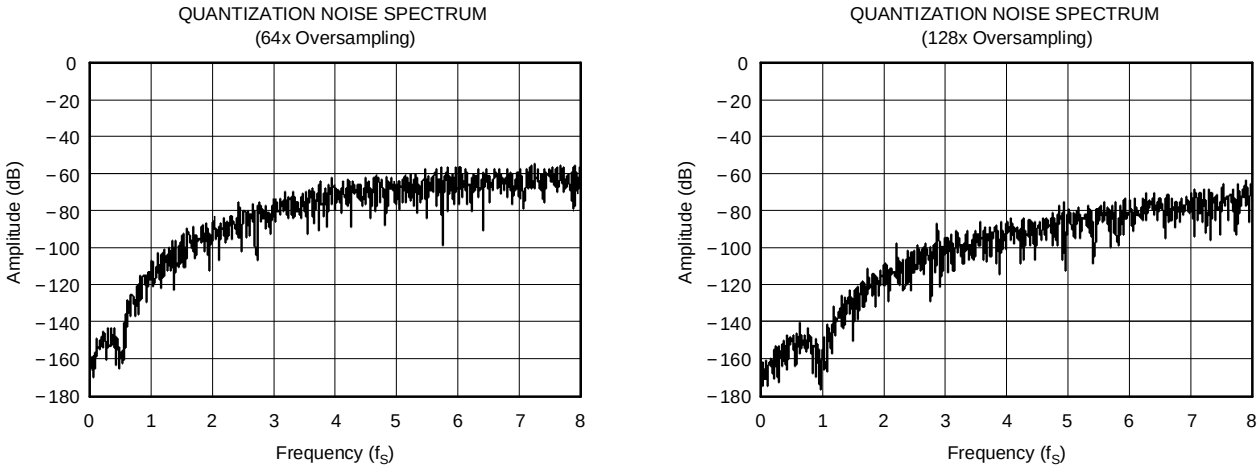


Figure 33. Quantization Noise Spectrum

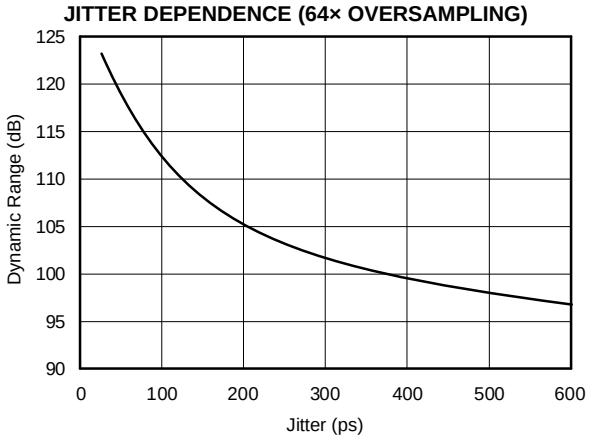


Figure 34. Jitter Sensitivity

KEY PERFORMANCE PARAMETERS AND MEASUREMENT

This section provides information on how to measure key dynamic performance parameters for the PCM1748. In all cases, a System Two™ Cascade audio measurement system by Audio Precision™, or equivalent, is used to perform the testing.

Total Harmonic Distortion + Noise

Total harmonic distortion + noise (THD+N) is a significant figure of merit for audio DACs, because it takes into account both harmonic distortion and all noise sources within a specified measurement bandwidth. The true rms value of the distortion and noise is referred to as THD+N. Figure 35 shows the test setup for THD+N measurements.

For the PCM1748, THD+N is measured with a full-scale, 1-kHz digital sine wave as the test stimulus at the input of the DAC. The digital generator is set to a 24-bit audio word length and a sampling frequency of 44.1 kHz or 96 kHz. The digital generator output is taken from the unbalanced S/PDIF connector of the measurement system. The S/PDIF data is transmitted via a coaxial cable to the digital audio receiver on the DEM-DAI1748 demonstration board. The receiver is then configured to output 24-bit data in either I^2S or left-justified data format. The DAC audio interface format is programmed to match the receiver output format. The analog output is then taken from the DAC post filter and connected to the analog analyzer input of the measurement system. The analog input is band-limited using filters resident in the analyzer. The resulting THD+N is measured by the analyzer and displayed by the measurement system.

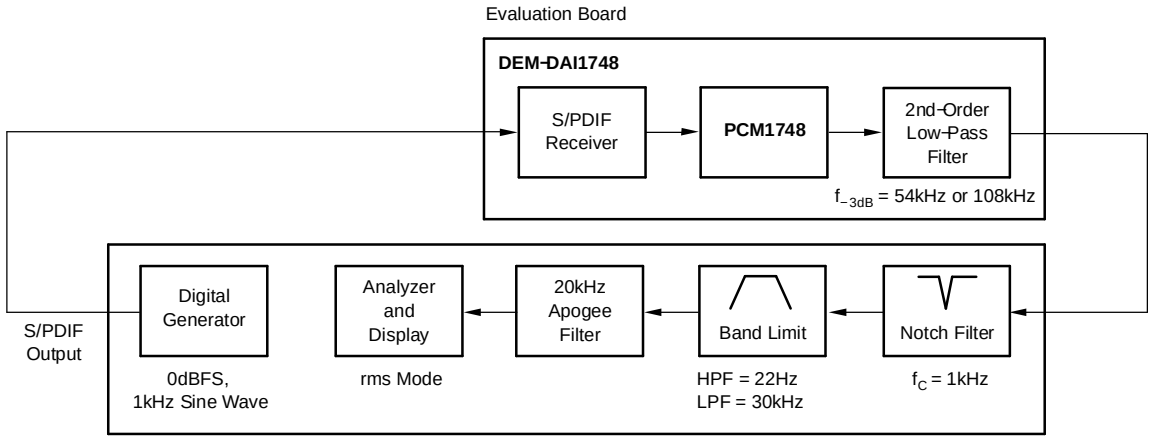


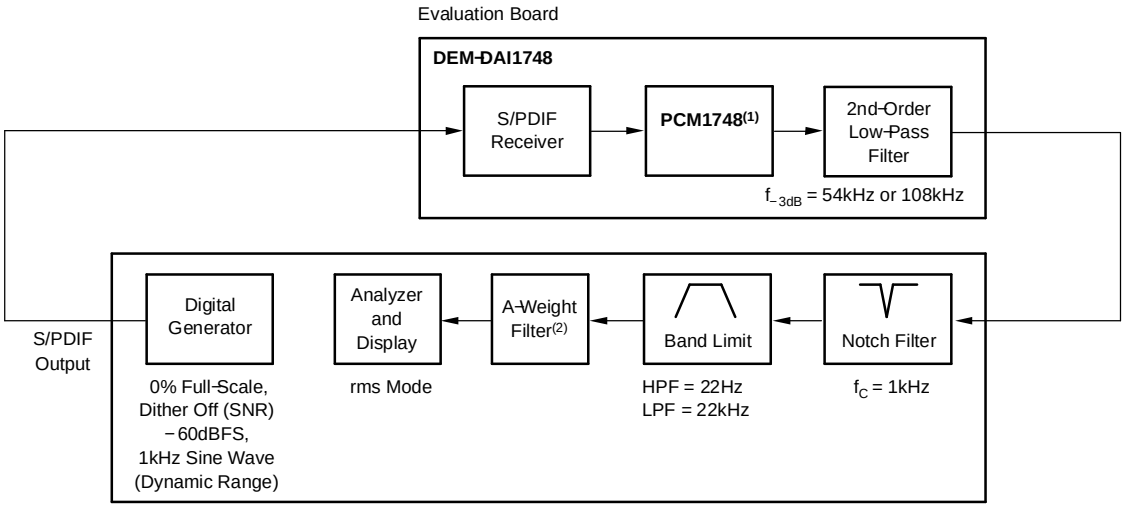
Figure 35. Test Setup for THD+N Measurements

KEY PERFORMANCE PARAMETERS AND MEASUREMENT (continued)

Dynamic Range

Dynamic range is specified as A-weighted, THD+N measured with a –60-dBFS, 1-kHz digital sine-wave stimulus at the input of the DAC. This measurement is designed to give a good indicator of how the DAC performs given a low-level input signal.

The measurement setup for the dynamic range measurement is shown in Figure 36 and is similar to the THD+N test setup discussed previously. The differences include the band-limit filter selection, the additional A-weighting filter, and the –60-dBFS input level.



(1) Infinite-zero-detect mute disabled

(2) Results without A-weighting are approximately 3 dB worse.

Figure 36. Test Setup Dynamic Range and SNR Measurements

Idle-Channel Signal-to-Noise Ratio

The SNR test provides a measure of the noise floor of the DAC. The input to the DAC is all-0s data, and the DAC infinite-zero-detect mute function must be disabled (default condition at power up for the PCM1748). This ensures that the delta-sigma modulator output is connected to the output amplifier circuit so that idle tones (if present) can be observed and affect the SNR measurement. The dither function of the digital generator must also be disabled to ensure an all-0s data stream at the input of the DAC. The measurement setup for SNR is identical to that used for dynamic range, with the exception of the input signal level (see the notes provided in Figure 36).

REVISION HISTORY

DATE	REV	PAGE	SECTION	DESCRIPTION
Apr 2005	B	–	Global	Changed to new format
		2	Absolute Maximum Ratings	Changed values for power supply voltage, digital input voltage, lead temperature, and package temperature. Added supply voltage difference, $V_{CC} – V_{DD} < 3$ V.
		2	Package/Ordering Information	Table removed from page 2, reformatted, and appended at end of data sheet.
		2	Recommended Operating Conditions	New table added to data sheet.
		4	Electrical Characteristics	Storage temperature removed from Temperature Range section of Electrical Characteristics (duplicate information in Absolute Maximum Ratings).
		6	Pin Assignments and Terminal Functions	Moved from page 2
		9	Typical Performance Curves	In Figure 12, changed Y-axis label from SNR to Dynamic Range.
		12	Power-On-Reset Functions	Added description about 1024-system-clock delay time shown in the Figure 20 timing diagram.
		12	Audio Serial Interface	Changed description of I^2S format and condition for synchronization from one SCK clock to three BCK clocks.
		13, 14	Audio Data Formats and Timing	In Figure 21, Audio Data Input Formats, removed 32-f_S availability from left-justified format. In Figure 22, Audio Interface Timing, corrected specification for BCK pulse cycle time.
		17	Register Map	For Table 3, Mode Control Register Map, added note to explain the RSV table entry.
		17, 18	Register Definitions	For ATx[7:0] – Digital Attenuation Level Setting and MUTx – Soft Mute Control, added description about incrementing/decrementing attenuation level by one step for every 8/f_S period.
		20	Register Definitions	For FMT[2:0] – Audio Interface Data Format, corrected default setting from 000, 24-bit standard format, right-justified data to 101, left-justified format, 16-to 24-bit.
		24	Zero Flags	Added description for L-channel/R-channel common zero flag.
		25	Connection Diagram	In Figure 28, corrected capacitor polarity for V_{DD} decoupling capacitor.
		26, 27	PCB Layout Guidelines	In Figure 30 and Figure 31, deleted extraneous signal lines. In Figure 31, changed leftmost block to Digital Logic and Audio Processor.
		30	Dynamic Range	Corrected parameters in test setup diagram, Figure 36.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCM1748E	ACTIVE	SSOP	DBQ	16	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM 1748E	Samples
PCM1748E/2K	ACTIVE	SSOP	DBQ	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM 1748E	Samples
PCM1748KE	ACTIVE	SSOP	DBQ	16	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM 1748KE	Samples
PCM1748KE/2K	ACTIVE	SSOP	DBQ	16	2000	Green (RoHS & no Sb/Br)	Call TI | NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM 1748KE	Samples
PCM1748KE/2KG4	ACTIVE	SSOP	DBQ	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM 1748KE	Samples
PCM1748KEG4	ACTIVE	SSOP	DBQ	16	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM 1748KE	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

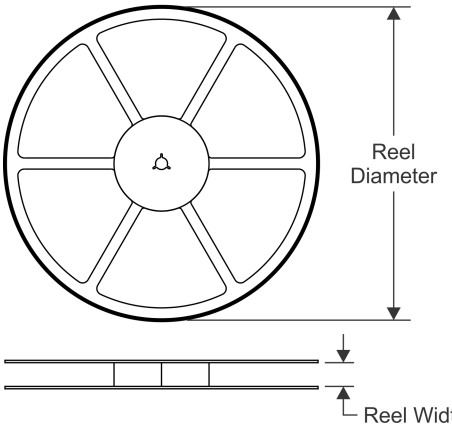
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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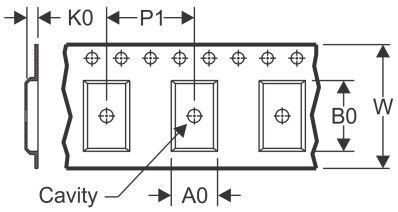
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

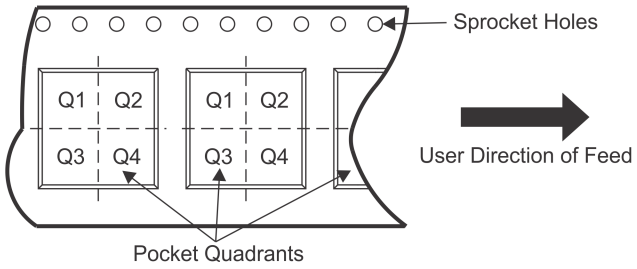


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

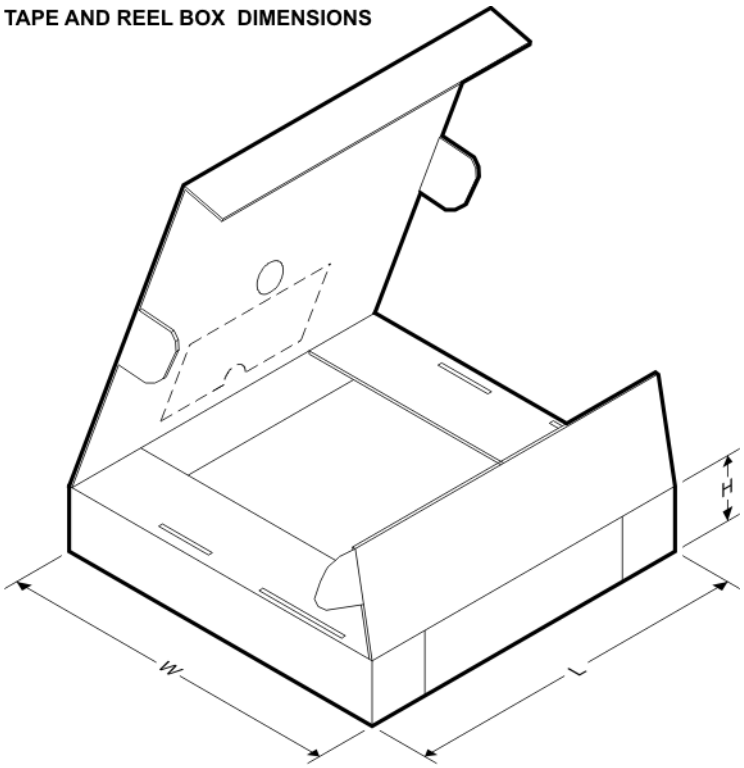
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM1748E/2K	SSOP	DBQ	16	2000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
PCM1748KE/2K	SSOP	DBQ	16	2000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



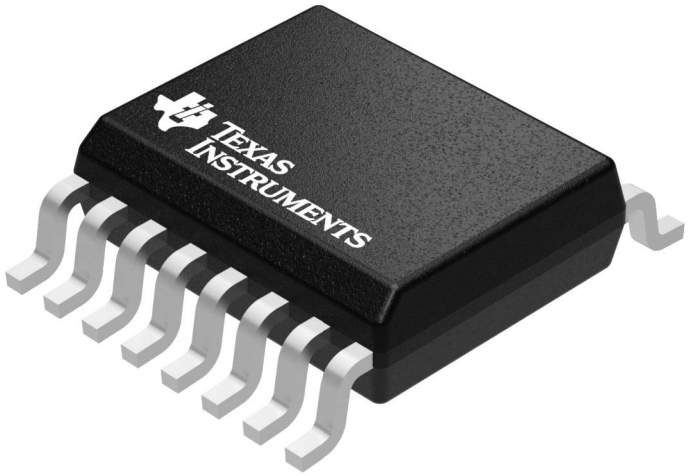
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM1748E/2K	SSOP	DBQ	16	2000	367.0	367.0	35.0
PCM1748KE/2K	SSOP	DBQ	16	2000	367.0	367.0	35.0

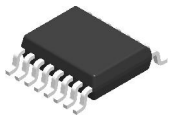
GENERIC PACKAGE VIEW

DBQ 16 SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

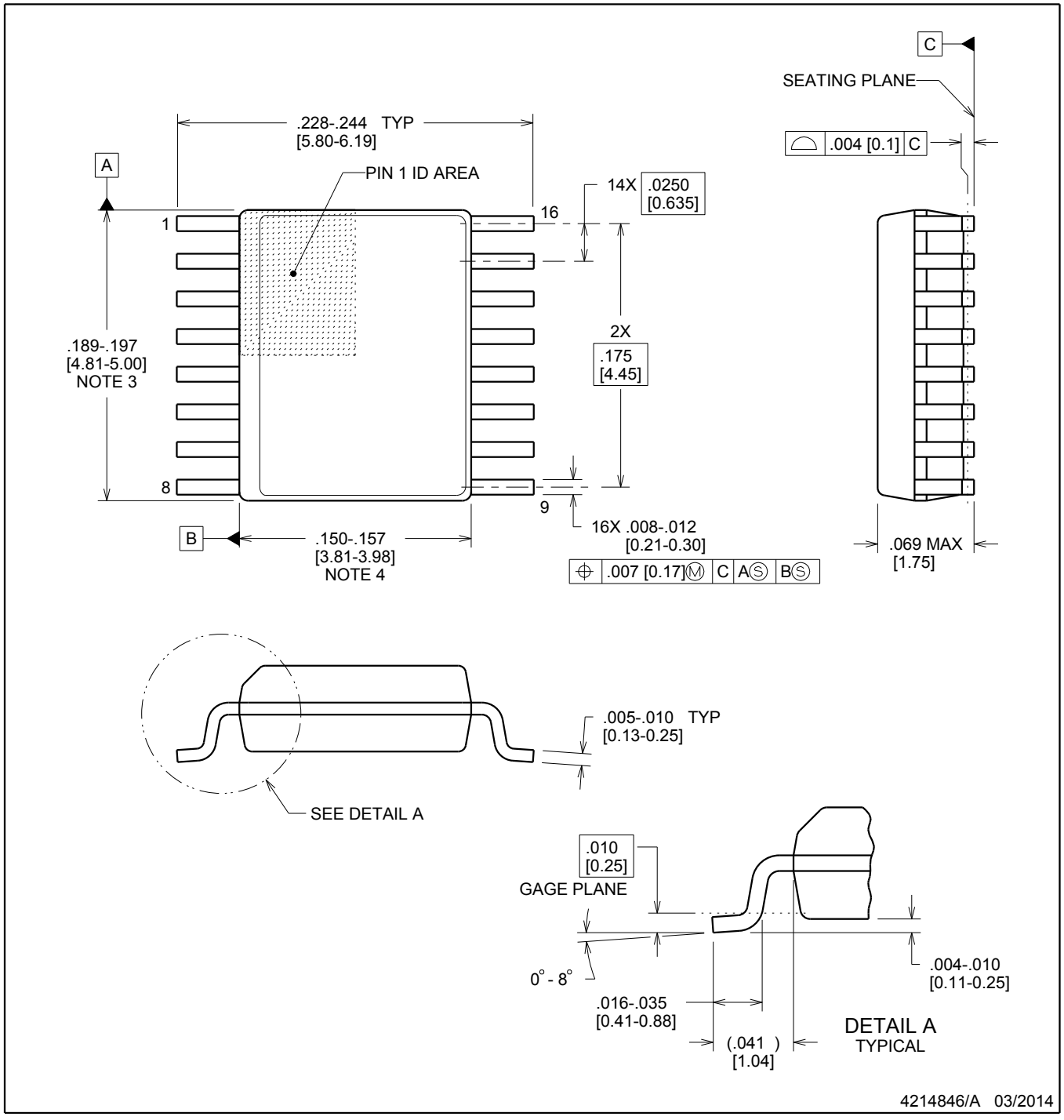


PACKAGE OUTLINE

DBQ0016A

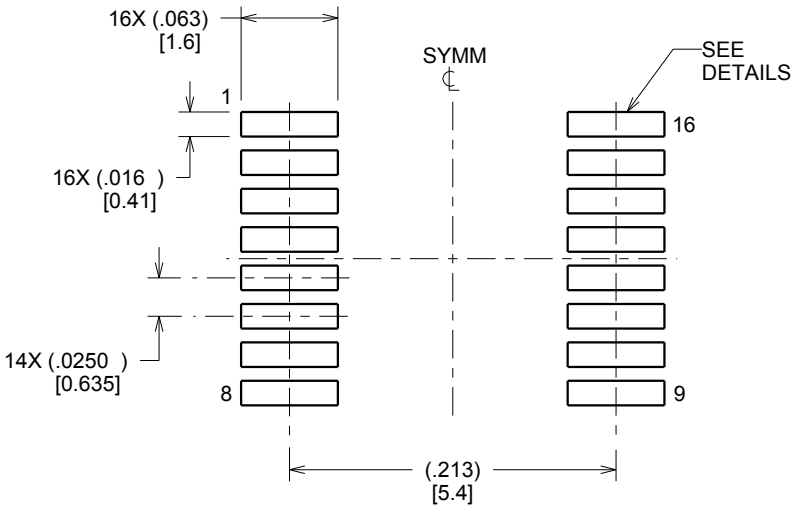
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

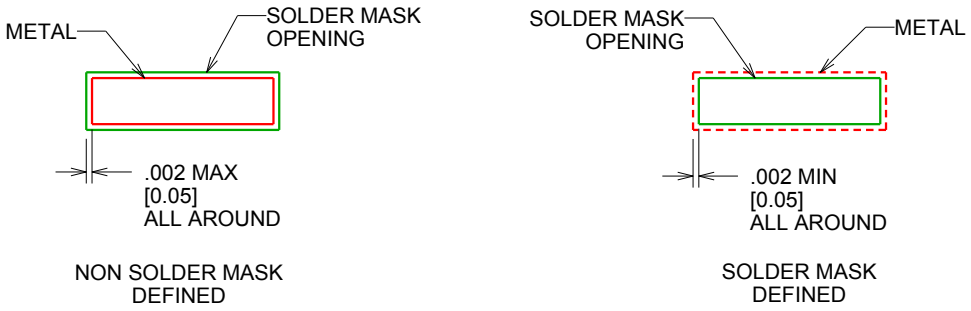


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

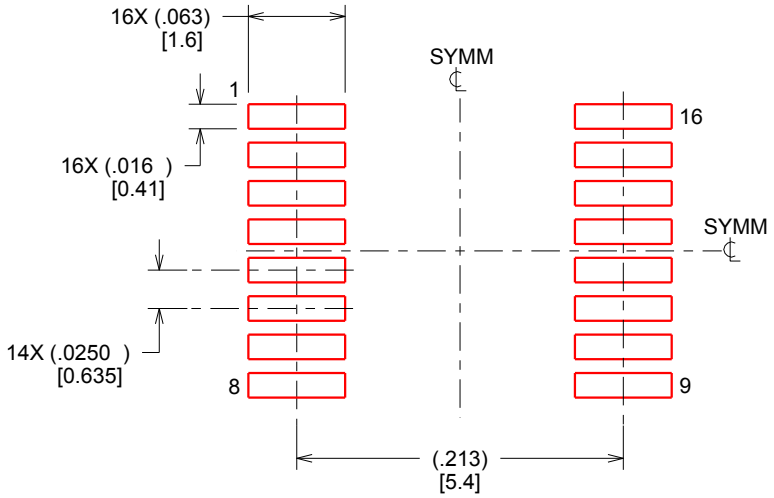
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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