



PCM1739

For most current data sheet and other product information, visit www.burr-brown.com

SoundPlus™ 24-Bit, 192kHz Sampling, Enhanced Multi-Level, Delta-Sigma, Audio DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 24-BIT RESOLUTION
- ANALOG PERFORMANCE ($V_{CC} = +5V$):
 - Dynamic Range: 106dB typ
 - SNR: 105dB typ
 - THD+N: 0.0015% typ
 - Full-Scale Output: 3.1Vp-p typ
- 4x/8x OVERSAMPLING DIGITAL FILTER:
 - Passband: $0.454f_s$
 - Stopband: $0.546f_s$
 - Stopband Attenuation: -82dB
 - Passband Ripple: ± 0.002 dB
- SAMPLING FREQUENCY: 10kHz to 192kHz
- SYSTEM CLOCK: $128f_s$, $192f_s$, $256f_s$, $384f_s$, $512f_s$, or $768f_s$ with Auto Detect
- ACCEPTS 24- or 16-BIT AUDIO DATA
- DATA FORMATS: Standard, I²S
- MODE CONTROLS
 - Digital De-Emphasis
 - Soft Mute
 - Zero Flags for Each Output
- DUAL SUPPLY OPERATION:
 - +5V Analog, +3.3V Digital
- 5V TOLERANT DIGITAL INPUTS
- SMALL SSOP-28 PACKAGE

APPLICATIONS

- A/V RECEIVERS
- DVD AUDIO AND MOVIE PLAYERS
- DVD ADD-ON CARDS FOR ENTERTAINMENT PCs
- HDTV RECEIVERS
- CAR AUDIO SYSTEMS
- OTHER APPLICATIONS REQUIRING 24-BIT AUDIO

DESCRIPTION

The PCM1739 is a CMOS, monolithic, integrated circuit which includes stereo 24-bit audio digital-to-analog converters and support circuitry in a small SSOP-28 package. The data converters utilize Burr-Brown's enhanced multi-level delta-sigma architecture, which employs 4th-order noise shaping and 8-level amplitude quantization to achieve excellent dynamic performance and improved tolerance to clock jitter. The PCM1739 accepts industry-standard audio data formats with 16- or 24-bit data, providing easy interfacing to audio DSP and decoder chips. Sampling rates up to 192kHz are supported.

SPECIFICATIONS

All specifications at $T_A = +25^\circ\text{C}$, $+V_{CC} = +5\text{V}$, $+V_{DD} = +3.3\text{V}$, system clock = $384f_s$ ($f_s = 44.1\text{kHz}$) and 24-bit data, unless otherwise noted.

		PCM1739E				
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
RESOLUTION			24		Bits	
DATA FORMAT						
Audio Data Interface Formats	User Selectable	Standard/I ² S				
Audio Data Bit Length	User Selectable	16 or 24 Bits				
Audio Data Format		MSB-First, Binary Two's Complement				
System Clock Frequency		128, 192, 256, 384, 512, 768f _S				
Sampling Frequency (f _S)		10		200	kHz	
DIGITAL INPUT/OUTPUT						
Logic Family		TTL-Compatible				
Input Logic Level		2.0	TTL-Compatible	0.8	VDC	
V _{IH}					VDC	
V _{IL}						
Input Logic Current						
I _{IH}	V _{IN} = V _{DD}				0.1	μA
I _{IL}	V _{IN} = 0V		−0.1	μA		
I _{IH} ⁽¹⁾	V _{IN} = V _{DD}	65		100	μA	
I _{IL} ⁽¹⁾	V _{IN} = 0V			−0.1	μA	
Output Logic Level		2.4		1.0	VDC	
V _{OH} ⁽²⁾	I _{OH} = −2mA				VDC	
V _{OL} ⁽²⁾	I _{OL} = +2mA				VDC	
V _{OH} ⁽³⁾	I _{OH} = −4mA	2.4		1.0	VDC	
V _{OL} ⁽³⁾	I _{OL} = +4mA				VDC	
DYNAMIC PERFORMANCE ⁽⁴⁾						
THD+N, V _{OUT} = 0dB	f _S = 44.1kHz, 384f _S		0.0015	0.0035	%	
	f _S = 96kHz, 256f _S		0.0020	0.0050	%	
	f _S = 192kHz, 128f _S		0.25	0.0060	%	
V _{OUT} = −60dB	f _S = 44.1kHz		0.6	0.8	%	
	f _S = 96kHz		0.7	1.0	%	
	f _S = 192kHz		0.8	1.2	%	
Dynamic Range	EIAJ, A-Weighted, f _S = 44.1kHz	102	106		dB	
	A-Weighted, f _S = 96kHz	100	105		dB	
	A-Weighted, f _S = 192kHz	98	104		dB	
Signal-to-Noise Ratio ⁽⁵⁾	EIAJ, A-Weighted, f _S = 44.1kHz	100	105		dB	
	A-Weighted, f _S = 96kHz	100	104		dB	
	A-Weighted, f _S = 192kHz	100	104		dB	
Channel Separation	f _S = 44.1kHz	100	104		dB	
	f _S = 96kHz	98	103		dB	
	f _S = 192kHz	96	102		dB	
DC ACCURACY						
Gain Error			±1.0	±3.0	% of FSR	
Gain Mismatch, Channel-to-Channel			±1.0	±3.0	% of FSR	
Bipolar Zero Error	V _{OUT} = 0.5V _{CC} at BPZ		±30	±60	mV	
ANALOG OUTPUT						
Output Voltage	Full Scale (−0dB)		62% of V _{CC}		Vp-p	
Center Voltage			50% of V _{CC}		VDC	
Load Impedance	AC Load	5			kΩ	
DIGITAL FILTER PERFORMANCE						
Filter Characteristics						
Passband	±0.002dB	0.546fs		0.454f _S	Hz	
	−3dB			0.490f _S	Hz	
Stopband						Hz
Passband Ripple					±0.002	dB
Stopband Attenuation	Stopband = 0.546f _S			−75		dB
	Stopband = 0.567f _S	−82		dB		
Delay Time			34/f _S		sec	
De-Emphasis Error			±0.1		dB	
ANALOG FILTER PERFORMANCE						
Frequency Response	At 20kHz		−0.03		dB	
	At 44kHz		−0.20		dB	
Cut-Off Frequency	−3dB		190		kHz	

SPECIFICATIONS (cont.)

All specifications at +25°C, +V_{CC} = +5V, +V_{DD} = +3.3V, system clock = 384f_S (f_S = 44.1kHz) and 24-bit data, unless otherwise noted.

PARAMETER	CONDITONS	PCM1739E			UNITS
		MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS					
Voltage Range					
V _{DD}		+3.0	+3.3	+3.6	VDC
V _{CC}		+4.5	+5.0	+5.5	VDC
Supply Current					
I _{DD} ⁽⁶⁾	V _{DD} = 3.3V f _S = 44.1 kHz		8.5	12.0	mA
	f _S = 96kHz, 256f _S		16.5		mA
	f _S = 192kHz, 128f _S		19.5		mA
I _{CC}	V _{CC} = 5.0V f _S = 44.1kHz		13.0	18.0	mA
	f _S = 96kHz, 256f _S		14.0		mA
	f _S = 192kHz, 128f _S		14.5		mA
Power Dissipation	V _{DD} = 3.3V, V _{CC} = 5.0V f _S = 44.1kHz		93	130	mW
	f _S = 96kHz, 256f _S		124		mW
	f _S = 192kHz, 128f _S		137		mW
TEMPERATURE RANGE					
Operation		0		70	°C
Storage		-55		+125	°C
Thermal Resistance θ_{JA}			100		°C/W

NOTES: (1) Pins 8, 9, 26, 27, 28 (TEST1, IBIT, DEM0 DEM1, FORM). (2) Pins 23, 24 (ZEROL, ZEROR). (3) Pin 4 (CLKO). (4) Analog performance specs are tested with Shibasoku #725 THD Meter 400Hz HPF, 30kHz LPF on, average mode with 20kHz bandwidth limiting. The load connected to the analog output is 5k Ω or larger, AC-coupled. (5) SNR is tested with Infinite Zero Detection off. (6) CLKO is disabled.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage, V _{DD}	+4.0V
V _{CC}	+6.5V
Input Current (except power supply pins)	±10mA
Supply Voltage Difference	±0.1V
GND Voltage Difference	±0.1V
Digital Input Voltage	-0.2V to +5.5V
Digital Output Voltage	-0.2V to (V _{DD} + 0.2V)
Power Dissipation	650mW
Operating Temperature Range	0°C to +70°C
Storage Temperature	-55°C to +125°C
Lead Temperature (soldering, 5s)	+260°C
Package Temperature (IR reflow, 10s)	+235°C



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

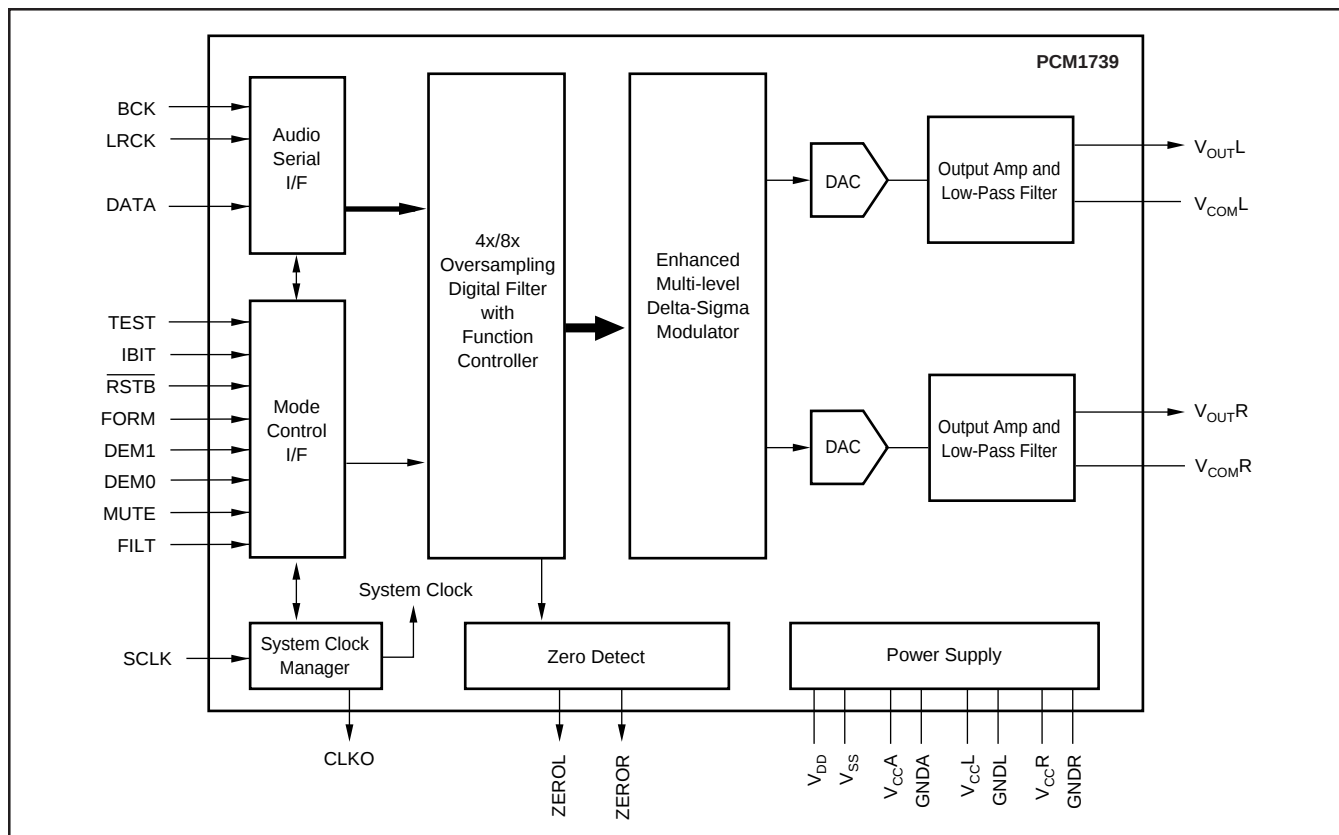
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PACKAGE	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER ⁽¹⁾	TRANSPORT MEDIA
PCM1739E	28-Lead SSOP	324	0°C to +70°C	PCM1739E	PCM1739E PCM1739E/2K	Rails Tape and Reel

NOTES: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of "PCM1739E/2K" will get a single 2000-piece Tape and Reel.

BLOCK DIAGRAM

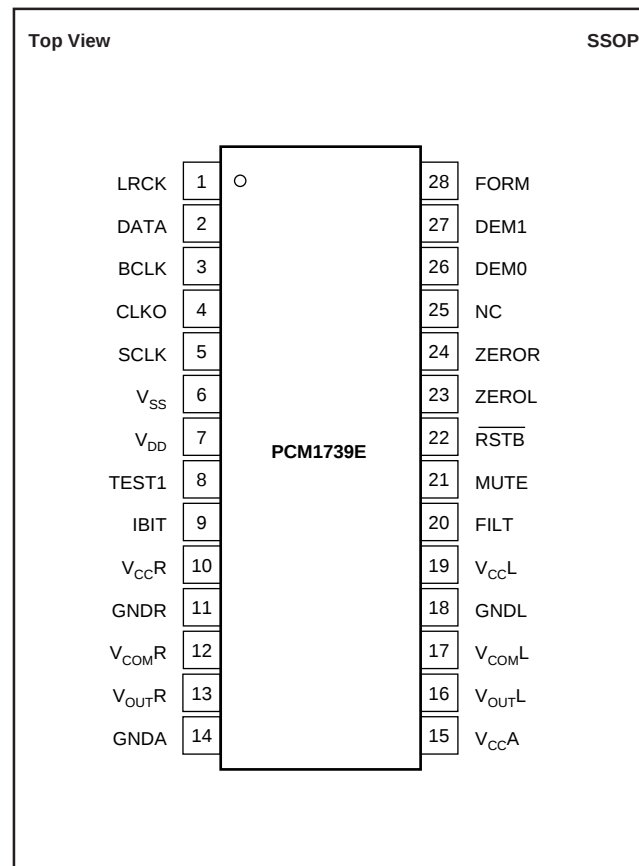


PIN ASSIGNMENTS

PIN	NAME	TYPE	DESCRIPTION
1	LRCK	IN	Left/Right Word Clock ⁽¹⁾
2	DATA	IN	Data In for Left and Right Channels ⁽¹⁾
3	BCLK	IN	Bit Clock ⁽¹⁾
4	CLKO	OUT	System Clock Output
5	SCLK	IN	System Clock Input ⁽¹⁾
6	V _{SS}	—	Digital Ground
7	V _{DD}	—	Digital Supply, +3.3V.
8	TEST1	IN	Test Pin. Must be connected to V _{DD} ⁽²⁾ .
9	IBIT	IN	Audio Data Word Length Select ⁽²⁾
10	V _{CCR}	—	Analog Supply for Right Channel, +5V.
11	GNDR	—	Analog Ground for Right Channel
12	V _{COMR}	—	Common for Right Channel
13	V _{OUTR}	OUT	Analog Output for Right Channel
14	GNDA	—	Analog Ground
15	V _{CCA}	—	Analog Supply, +5V.
16	V _{OUTL}	OUT	Analog Output for Left Channel
17	V _{COML}	—	Common for Left Channel
18	GNDL	—	Analog Ground for Left Channel
19	V _{CCL}	—	Analog Supply for Left Channel, +5V.
20	FILT	IN	4x/8x Interpolation Filter Select ⁽²⁾
21	MUTE	IN	Digital Mute for Left and Right Channels ⁽²⁾
22	RSTB	IN	Reset, Active Low ⁽¹⁾ .
23	ZEROL	OUT	Zero Flag for Left Channel
24	ZEROR	OUT	Zero Flag for Right Channel
25	NC	—	No Connect
26	DEM0	IN	De-Emphasis Filter Select 0 ⁽²⁾
27	DEM1	IN	De-Emphasis Filter Select 1 ⁽²⁾
28	FORM	IN	Audio Data Format Select ⁽²⁾

NOTES: (1) Schmitt-Trigger input with internal pull-down, 5V tolerant.
(2) Schmitt-Trigger input, 5V tolerant.

PIN CONFIGURATION

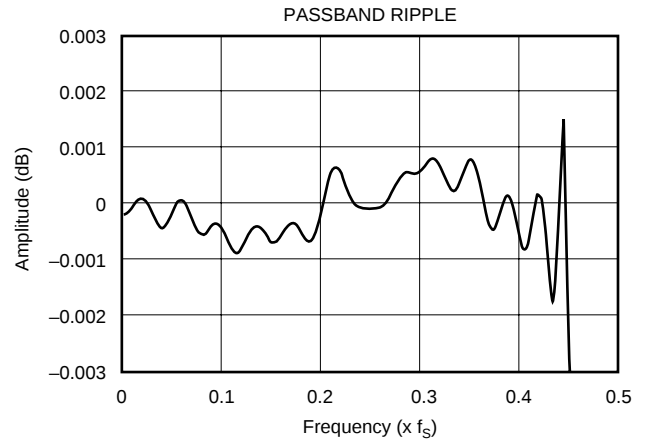
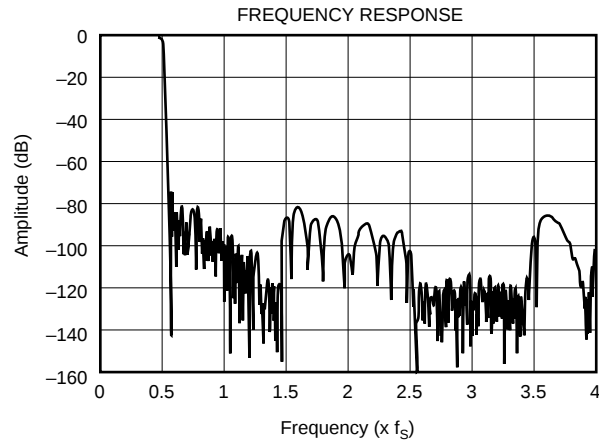


TYPICAL PERFORMANCE CURVES

All specifications at $T_A = +25^\circ\text{C}$, $V_{DD} = V_{CC} = 5\text{V}$, $\text{SYSCLK} = 384f_s$ ($f_s = 44.1\text{kHz}$), and 20-bit input data, unless otherwise noted.

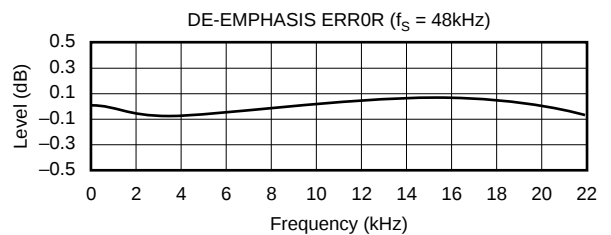
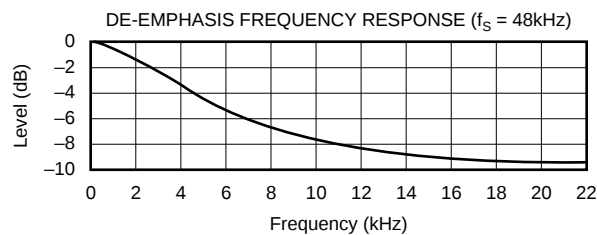
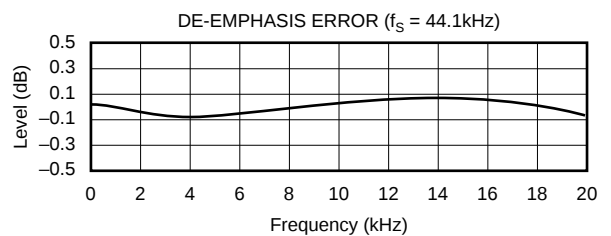
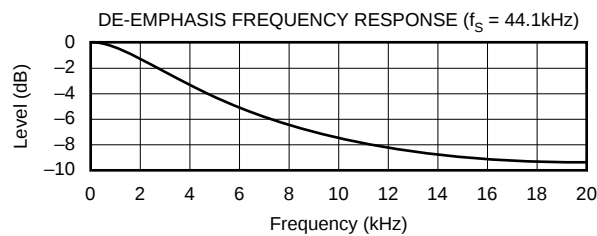
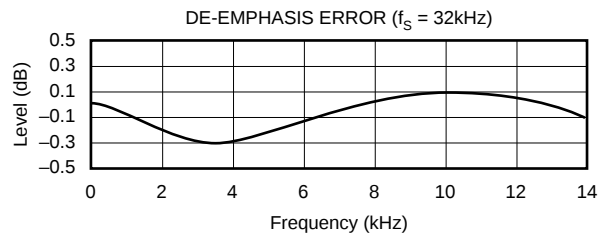
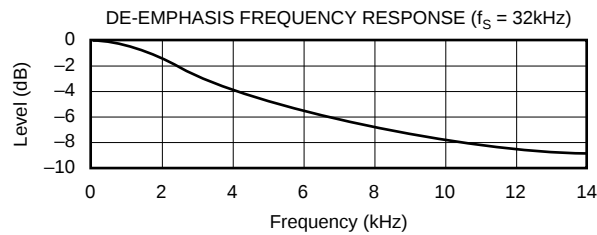
DIGITAL FILTER

Digital Filter (De-Emphasis Off, $f_s = 44.1\text{kHz}$)



DIGITAL FILTER

De-Emphasis Error

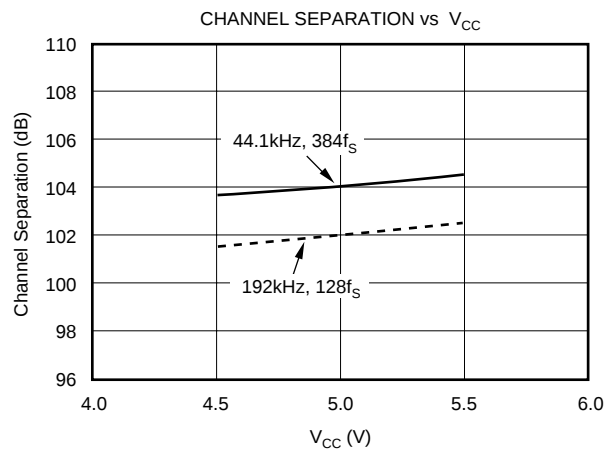
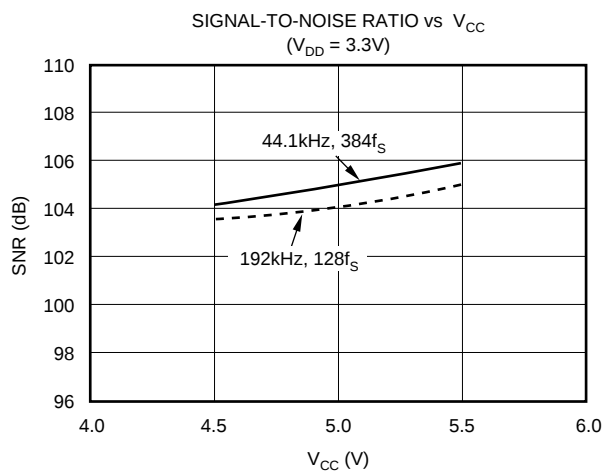
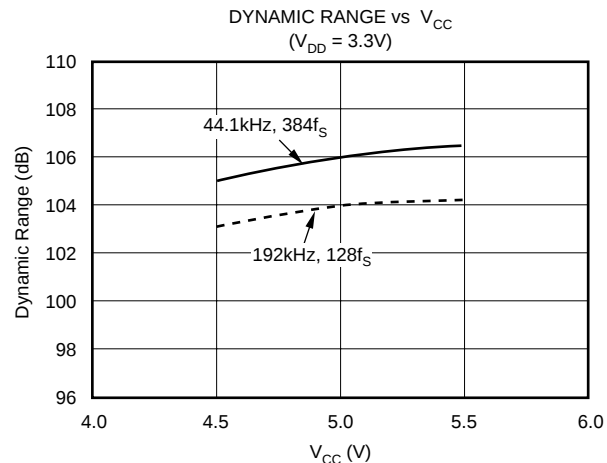
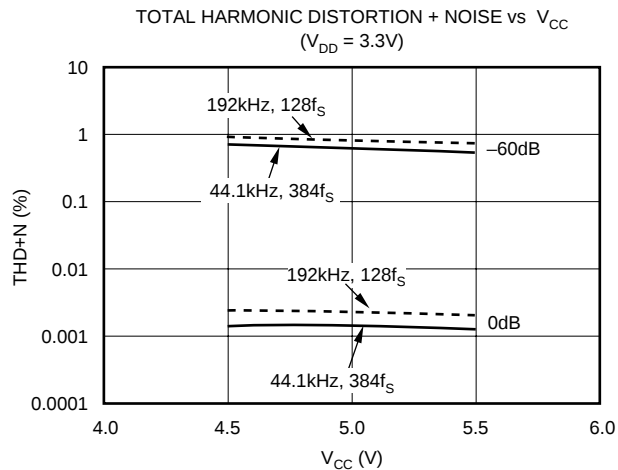


TYPICAL PERFORMANCE CURVES (cont.)

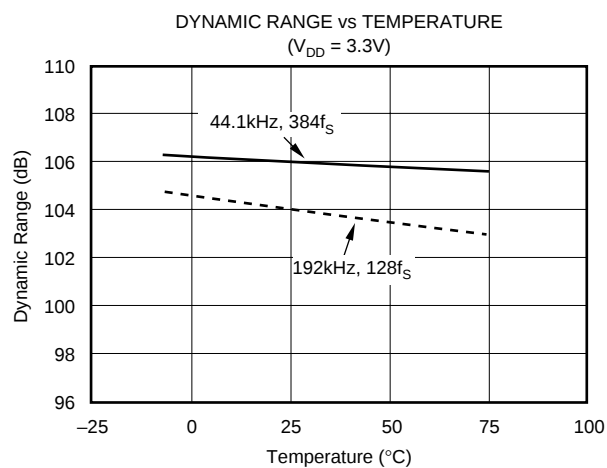
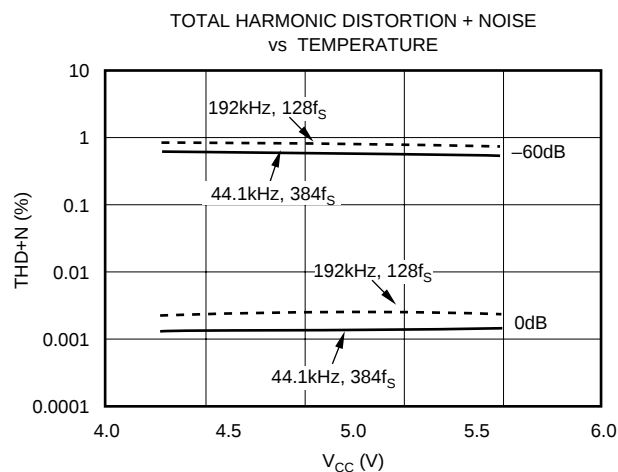
All specifications at $T_A = +25^\circ\text{C}$, $V_{DD} = V_{CC} = 5\text{V}$, $\text{SYSCLK} = 384f_S$ ($f_S = 44.1\text{kHz}$), and 20-bit input data, unless otherwise noted.

ANALOG DYNAMIC PERFORMANCE

Supply Voltage Characteristics



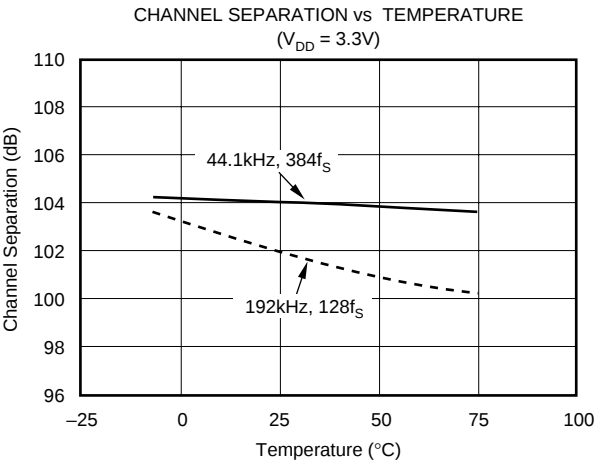
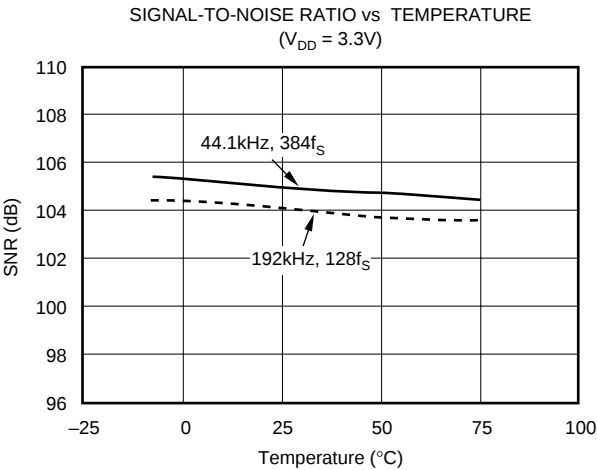
Temperature Characteristics



TYPICAL PERFORMANCE CURVES (cont.)

All specifications at $T_A = +25^{\circ}\text{C}$, $V_{DD} = V_{CC} = 5\text{V}$, $\text{SYSCLK} = 384f_S$ ($f_S = 44.1\text{kHz}$), and 20-bit input data, unless otherwise noted.

Temperature Characteristics (cont.)



SYSTEM CLOCK AND RESET FUNCTIONS

SYSTEM CLOCK INPUT

The PCM1739 requires a system clock for operating the digital interpolation filters and multi-level delta-sigma modulators. The system clock is applied at the SCLK input (pin 5). Table I shows examples of system clock frequencies for common audio sampling rates.

Figure 1 shows the timing requirements for the system clock input. For optimal performance, it is important to use a clock source with low phase jitter and noise. Burr-Brown's PLL1700 multi-clock generator is an excellent choice for providing the PCM1739 system clock.

SYSTEM CLOCK OUTPUT

A buffered version of the system clock input is available at the CLKO output (pin 4). CLKO operates at the same frequency as the system clock, SCLK.

POWER-ON AND EXTERNAL RESET FUNCTIONS

The PCM1739 includes a power-on reset function. Figure 2 shows the operation of this function. The system clock input at SCLK should be active for at least one clock period prior to $V_{DD} = 2.0V$. With the system clock active and $V_{DD} > 2.0V$, the power-on reset function will be enabled. The initialization sequence requires 1024 system clocks from the time $V_{DD} > 2.0V$. The PCM1739 also includes an external reset capability using the $\overline{RSTB}$ input (pin 22). This allows an external controller or master reset circuit to force the PCM1739 to initialize to its reset default state. For normal operation, $\overline{RSTB}$ should be set to a logic '1'.

Figure 3 shows the external reset operation and timing. The $\overline{RSTB}$ pin is set to logic '0' for a minimum of 20ns. The $\overline{RSTB}$ pin is then set to a logic '1' state, which starts the initialization sequence, which lasts for 1024 system clock periods.

The external reset is especially useful in applications where there is a delay between PCM1739 power up and system clock activation. In this case, the $\overline{RSTB}$ pin should be held at a logic '0' level until the system clock has been activated.

SAMPLING FREQUENCY (f_s)	SYSTEM CLOCK FREQUENCY, f_{SCLK} , (MHZ)					
	$128f_s$	$192f_s$	$256f_s$	$384f_s$	$512f_s$	$768f_s$
16kHz	—	—	4.0960	6.1440	8.1920	12.2880
32kHz	—	—	8.1920	12.2880	16.3840	24.5760
44.1kHz	—	—	11.2896	16.9344	22.5792	33.8688
48kHz	—	—	12.2880	18.4320	24.5760	36.8640
88.2kHz	—	—	22.5792	33.8688	45.1584	See Note 1
96kHz	12.2880	18.4320	24.5760	36.8640	49.1520	See Note 1
176.4kHz	24.5792	33.8688	See Note 2	See Note 2	See Note 2	See Note 2
192kHz	24.5760	36.8640	See Note 2	See Note 2	See Note 2	See Note 2

NOTES: (1) The $768f_s$ system clock rate is not supported for $f_s > 64kHz$. (2) This system clock rate is not supported for the given sampling frequencies.

TABLE I. System Clock Rates for Common Audio Sampling Frequencies.

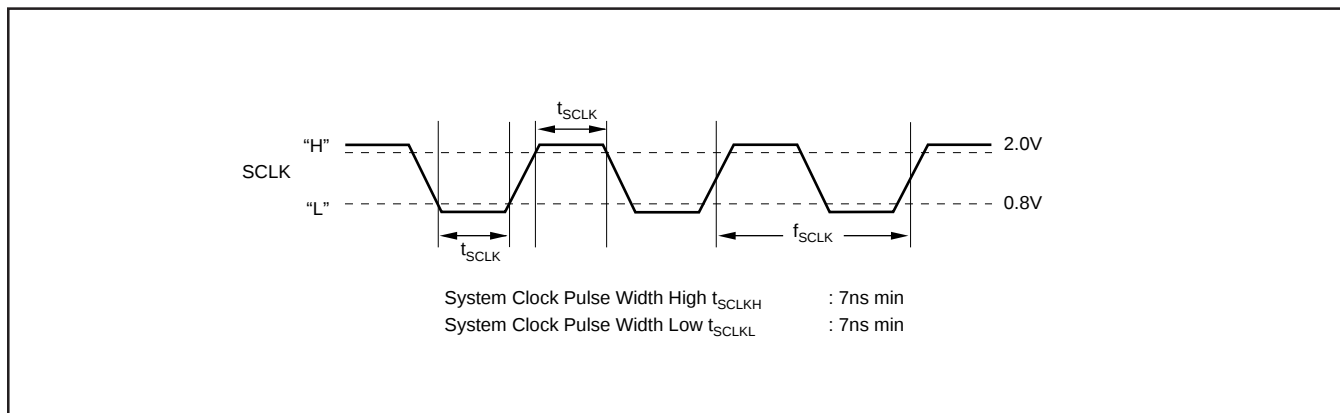


FIGURE 1. System Clock Input Timing.

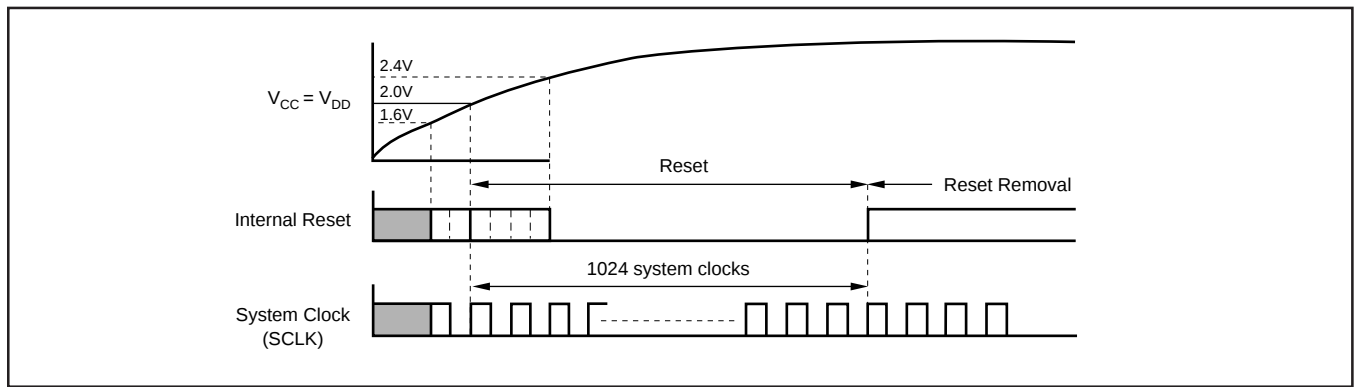


FIGURE 2. Power-On Reset Timing.

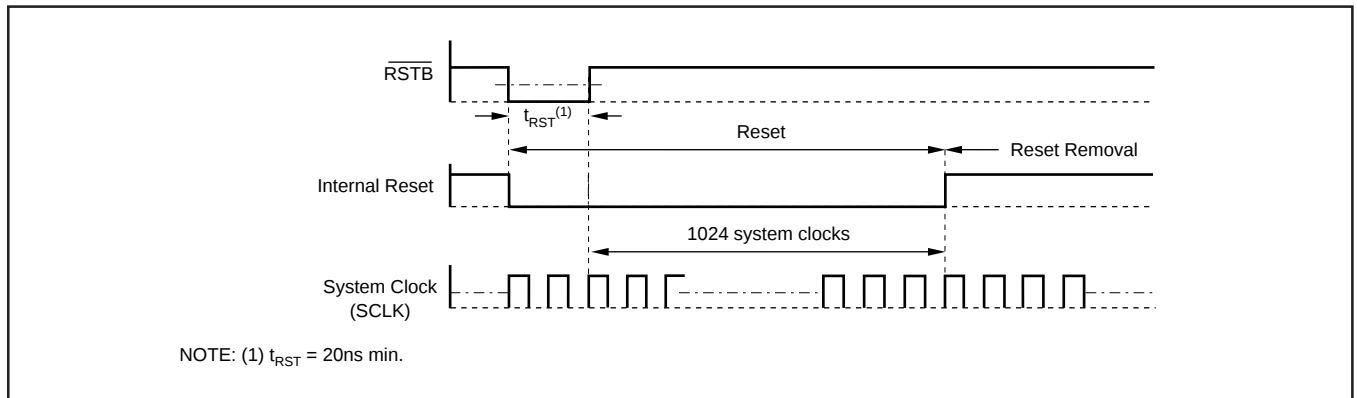


FIGURE 3. External Reset Timing.

AUDIO SERIAL INTERFACE

The audio serial interface for the PCM1739 is comprised of a 3-wire synchronous serial port. It includes LRCK (pin 1), BCLK (pin 3), and DATA (pin 2). BCLK is the serial audio bit clock, and is used to clock the serial data present on DATA into the audio interface's serial shift registers. Serial data is clocked into the PCM1739 on the rising edge of BCLK. LRCK is the serial audio left/right word clock. It is used to latch serial data into the serial audio interface's internal registers.

Both LRCK and BCLK must be synchronous to the system clock. Ideally, it is recommended that LRCK and BCLK be derived from the system clock input or output, SCLK or CLKO. The left/right clock, LRCK, is operated at the sampling frequency (f_s). The bit clock, BCK, may be operated at 48 or 64 times the sampling frequency.

AUDIO DATA FORMATS AND TIMING

The PCM1739 supports industry-standard audio data formats, including Standard and I²S. The audio data word length may be either 24 or 16 bits. Data format and word length are selected using the FORM and IBIT pins, as described in the Mode Controls section of this data sheet. All formats require Binary Two's Complement, MSB-first audio data. The data formats are shown in Figure 4, while Figure 5 shows a detailed timing diagram for the serial audio interface.

MODE CONTROLS

This section describes the mode control pins used to configure the operating mode of the PCM1739.

AUDIO DATA FORMAT

The data format used by the audio serial interface is selected using the FORM input (pin 28). The formats available include Standard and I²S. Table II shows the FORM pin configuration.

FORM	DATA FORMAT
L	Standard
H	I ² S

TABLE II. Audio Data Format Selection.

AUDIO DATA WORD LENGTH

The data word length used by the audio serial interface is selected using the IBIT input (pin 9). The word length may be either 24 or 16 bits. Table III shows the IBIT pin configuration.

IBIT	DATA WORD LENGTH
L	24 Bits
H	16 Bits

TABLE III. Audio Data Word Length Selection.

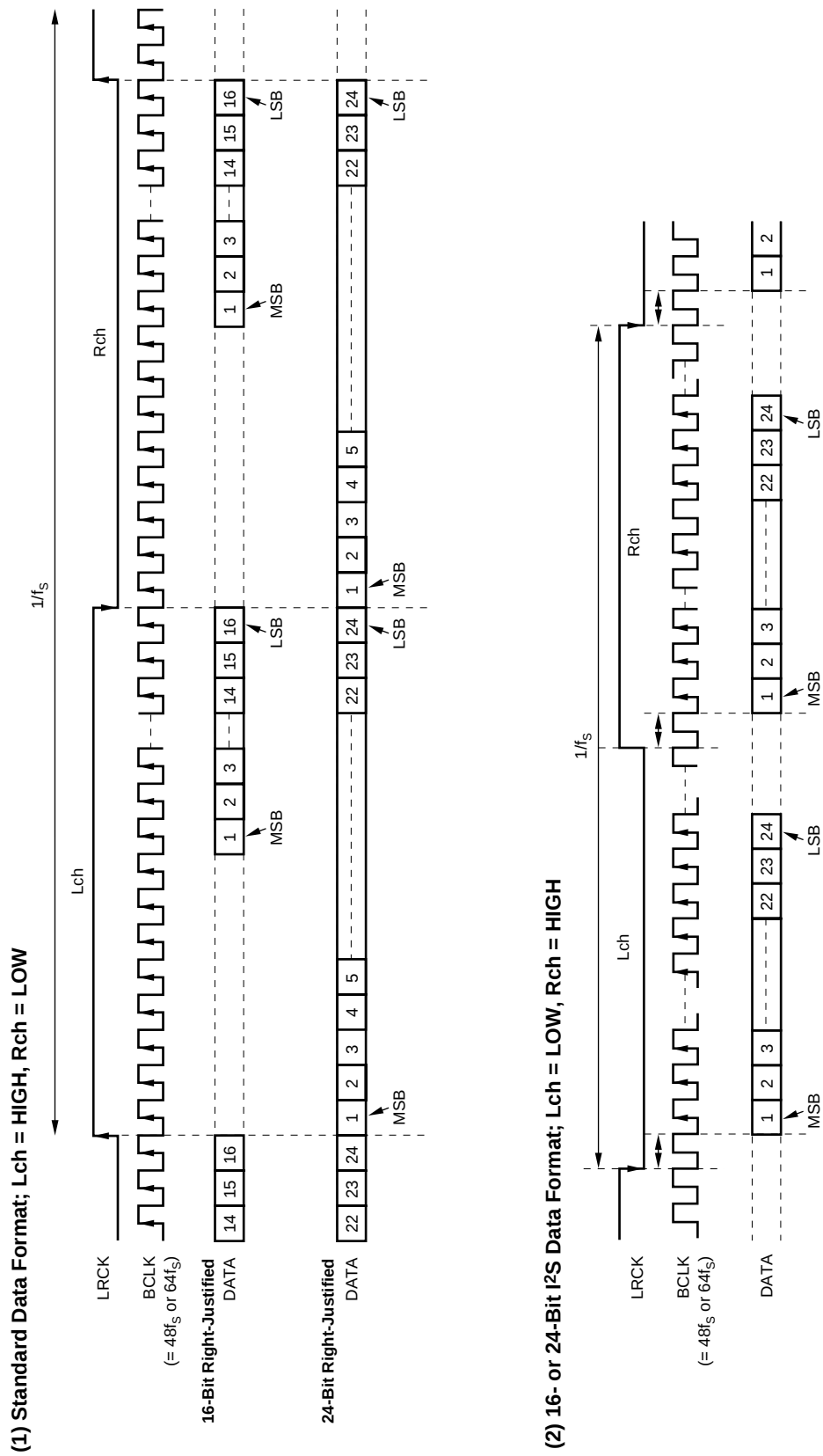


FIGURE 4. Audio Data Input Formats.

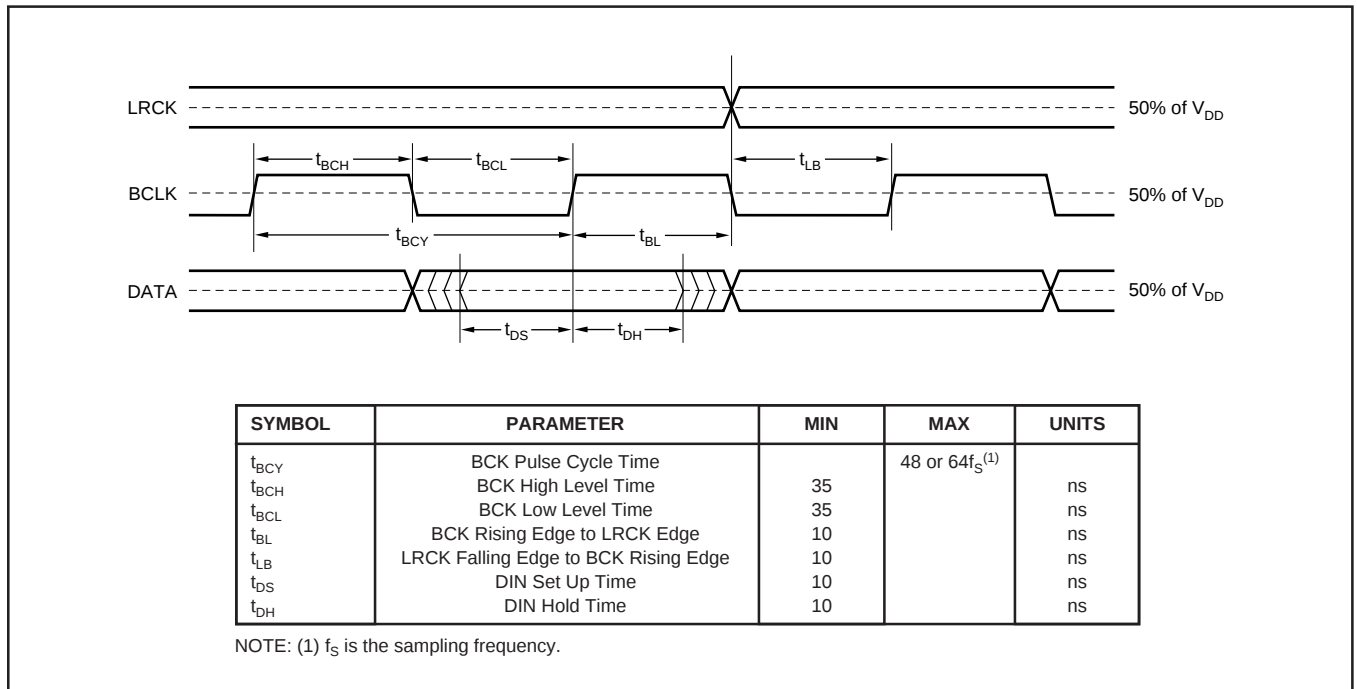


FIGURE 5. Audio Interface Timing.

4x/8x DIGITAL INTERPOLATION

The PCM1739's digital filter may be configured for either 4x or 8x oversampling. The 8x oversampling setting is utilized for sampling frequencies up to 96kHz, while 4x oversampling is utilized for 192kHz operation. The FILT input (pin 20) is used to select the oversampling rate of the digital filter. Table IV shows the FILT pin configuration.

FILT	OVERSAMPLING RATE
L	8x
H	4x (Required for 192kHz operation)

TABLE IV. Digital Filter Oversampling Rate Selection.

SOFT MUTE

The Soft Mute function provides for quiet muting of the DAC outputs, V_{OUTL} (pin 16) and V_{OUTR} (pin 13). This is done by ramping an internal digital attenuator from unity gain to digital mute (all 0's input to the digital filter). The MUTE input (pin 21) is used to enable and disable the Soft Mute function. Table V shows the MUTE pin configuration.

MUTE	SOFT MUTE STATUS
L	Disabled
H	Enabled

TABLE V. Soft Mute Selection.

DIGITAL DE-EMPHASIS

The PCM1739 provides a De-emphasis function for sampling rates equal to 32kHz, 44.1kHz or 48kHz. It is incorporated into the digital filter of the PCM1739. The De-empha-

sis function is required for proper playback of early audio compact disks (CDs), which were mastered with signal emphasis for higher frequencies in the audio band. This was done to improve the poor high frequency performance of early CD players. Plots of the de-emphasis filter and error functions for 32kHz, 44.1kHz, and 48kHz are shown in the Typical Performance Curves section of this data sheet.

The DEM0 (pin 26) and DEM1 (pin 27) inputs of the PCM1739 are used to enable and disable the digital de-emphasis function. Table VI shows the DEM0 and DEM1 pin configurations.

DEM1	DEM0	DE-EMPHASIS FUNCTION
L	L	OFF
L	H	32kHz De-Emphasis Filter
H	L	44.1kHz De-Emphasis Filter
H	H	48kHz De-Emphasis Filter

TABLE VI. Digital De-Emphasis.

ANALOG OUTPUTS

The PCM1739 includes two independent output channels; V_{OUTL} (pin 16) and V_{OUTR} (pin 13). These are unbalanced outputs, each capable of driving 3.1Vp-p typical into a 5k Ω , AC-coupled load ($V_{CC} = +5V$). The internal output amplifiers for V_{OUTL} and V_{OUTR} are DC biased to a DC common-mode (or bipolar zero) voltage, equal to $V_{CC}/2$.

The output amplifiers include an RC continuous time filter, which helps to reduce the out-of-band noise energy present at the DAC outputs due to the noise shaping characteristics of the PCM1739's delta-sigma D/A converters. The fre-

quency response of this filter is shown in Figure 6. By itself, this filter is not enough to attenuate the out-of-band noise to an acceptable level for most applications. An external low-pass filter is required to provide sufficient out-of-band noise rejection. Further discussion of DAC post filter circuits is provided in the Applications Information section of this data sheet.

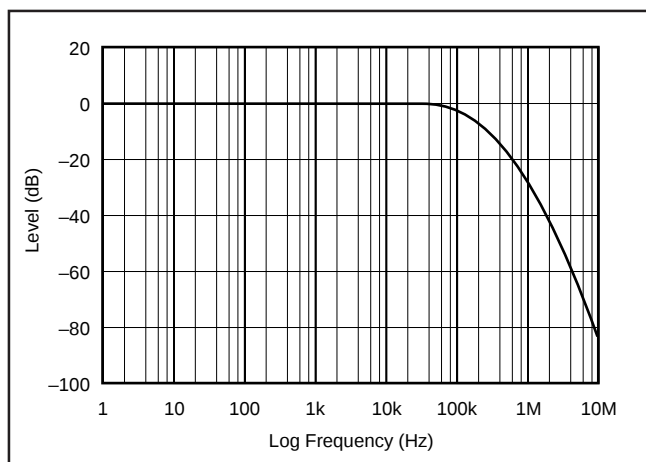


FIGURE 6. Output Filter Frequency Response.

V_{COML} AND V_{COMR} OUTPUTS

Two unbuffered, DC common-mode voltage output pins, V_{COML} (pin 17) and V_{COMR} (pin 12), are brought out for decoupling purposes. These pins are normally biased to a DC voltage level equal to $V_{CC}/2$. These pins may be used to bias external circuits, but they must be connected to high impedance nodes. Figure 7 shows examples of the proper use of the V_{COML} and V_{COMR} pins for external biasing applications.

ZERO FLAG OUTPUTS

The PCM1739 includes circuitry for detecting an all zero data condition for the data input pin, DATA. Zero detection for each output channel is independent from the other. If the data for a given channel remains at a '0' level for 1024 sample periods (or LRCK clock periods), a Zero Detect condition exists for the that channel. Given that a Zero Detect condition exists, the Zero Flag pin(s) for the corresponding channel(s) will be set to a logic '1' state. The zero flag outputs include ZEROL (pin 23) and ZEROR (pin 24). These pins can be used to operate external mute circuits, or used as status indicators for audio signal processor, microcontroller, or other digitally-controlled functions.

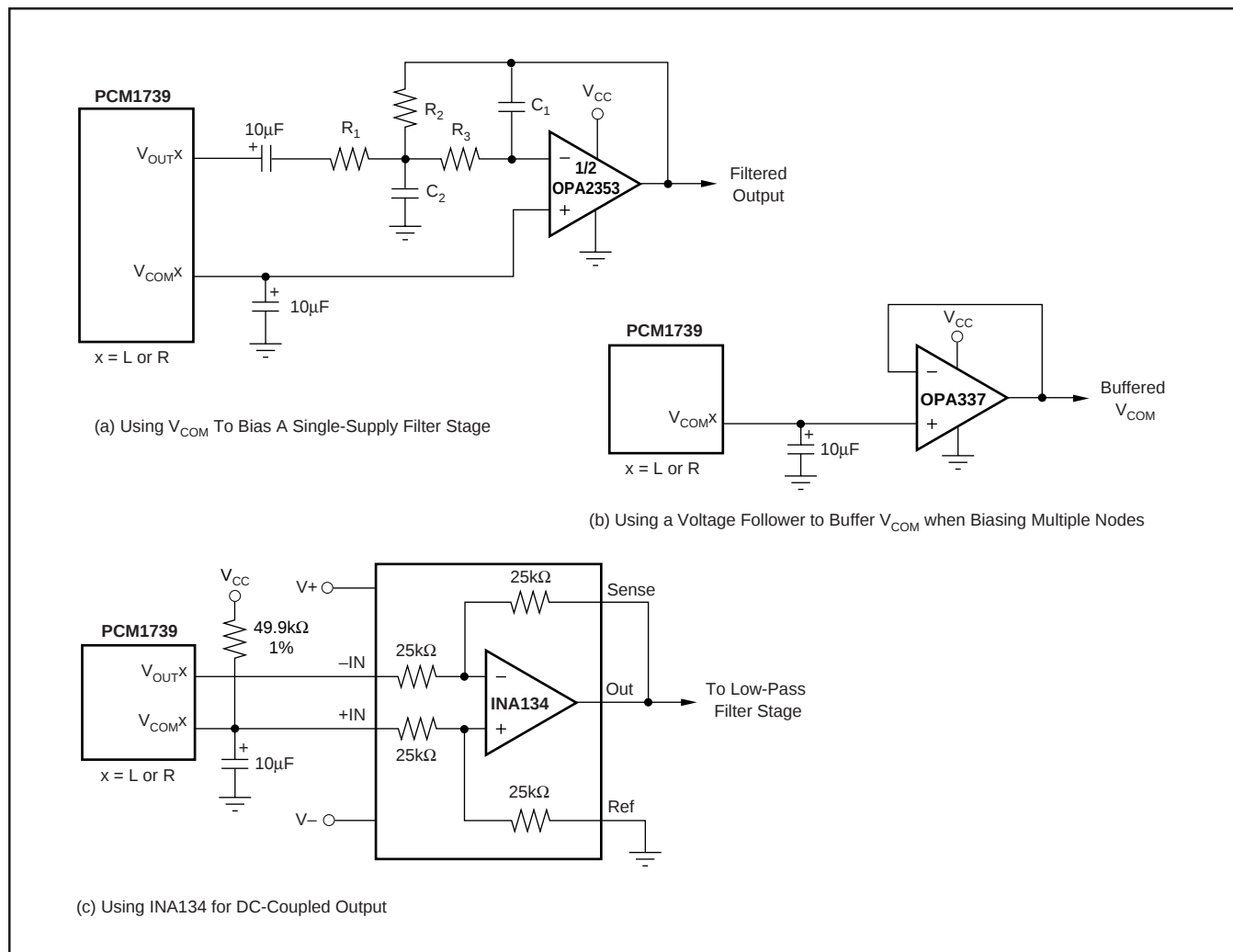


FIGURE 7. Biasing External Circuits Using the V_{COML} and V_{COMR} Pins.

APPLICATIONS INFORMATION

CONNECTION DIAGRAM

A basic connection diagram with the necessary power supply bypassing and decoupling components is shown in Figure 8. Burr-Brown recommends using the component values shown in Figure 8 for all designs.

The use of series resistors (22Ω to 100Ω) is recommended for the SCLK, LRCK, LRCK, BCLK, and DATA inputs. The series resistor combines with the stray PCB and device input capacitance to form a low-pass filter, which reduces high frequency noise emissions and helps to dampen glitches and ringing present on clock and data lines.

POWER SUPPLIES AND GROUNDING

The PCM1739 requires a +5V analog supply and a +3.3V digital supply. The +5V supply is used to power the DAC analog and output filter circuitry, while the +3.3V supply is used to power the digital filter and logic circuitry. For best performance, the +3.3V supply should be derived from the +5V supply using a linear regulator, shown in Figure 8. Burr-Brown's REG1117-3.3 is an ideal choice for this application.

Proper power supply bypassing is shown in Figure 8. The bypass capacitors should be located as close as possible to the PCM1739 package. The $1\mu\text{F}$ and $10\mu\text{F}$ capacitors should be tantalum or aluminum electrolytic, while the $0.1\mu\text{F}$ capacitors are ceramic (X7R type is recommended for surface mount applications).

D/A OUTPUT CIRCUITS

Delta-sigma D/A converters utilize noise-shaping techniques to improve in-band Signal-to-Noise (SNR) performance at the expense of generating increased out-of-band noise above the Nyquist Frequency, or $f_s/2$. The out-of-band noise must be low-pass filtered in order to provide optimal converter performance. This is accomplished by a combination of on-chip and external low pass filtering.

Figures 7a and 9 show the recommended external low pass active filter circuits for dual and single-supply applications. These circuits are 2nd-order filters using the Multiple Feed-back (MFB) circuit arrangement, which reduces sensitivity to passive component variations over frequency and temperature. For more information regarding MFB active filter design, please refer to Burr-Brown Applications Bulletin AB-034.

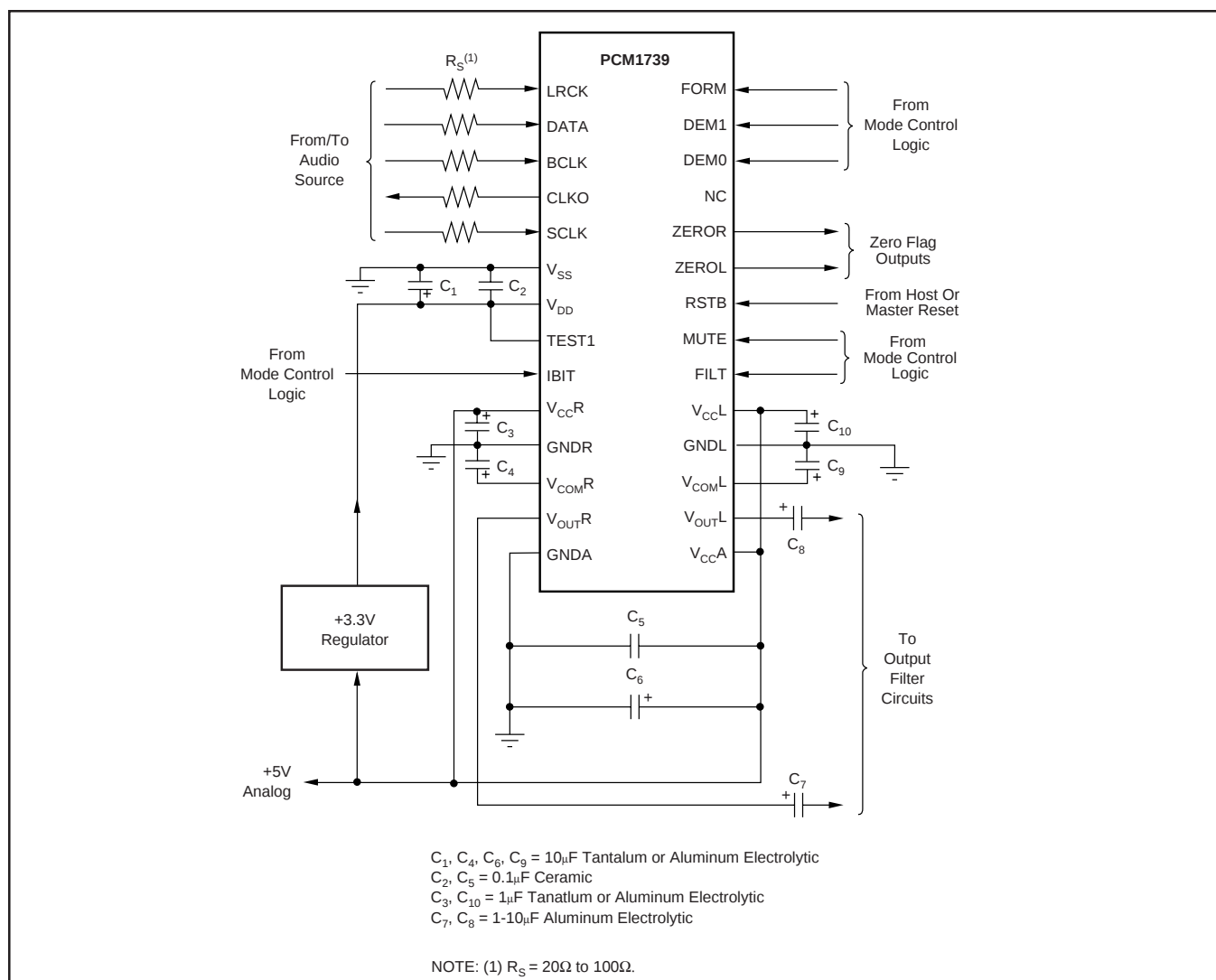


FIGURE 8. Basic Connection Diagram.

Since the overall system performance is defined by the quality of the D/A converters and their associated analog output circuitry, high quality audio op amps are recommended for the active filters. Burr-Brown's OPA2134 and OPA2353 dual op amps are shown in Figures 7a and 9, and are recommended for use with the PCM1739.

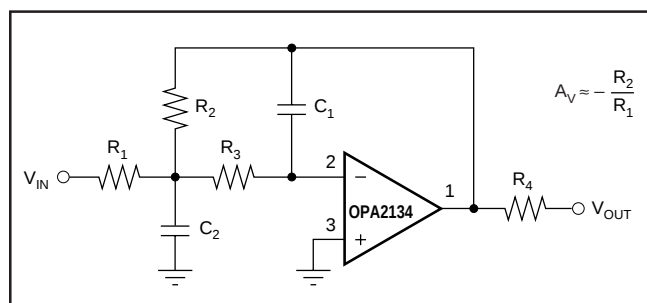


FIGURE 9. Dual Supply Filter Circuit.

PCB LAYOUT GUIDELINES

A typical PCB floor plan for the PCM1739 is shown in Figure 10. A ground plane is recommended, with the analog and digital sections being isolated from one another using a split or cut in the circuit board. The PCM1739 should be oriented with the digital I/O pins facing the ground plane split/cut, allowing for direct connection of the digital audio interface and control signals originating from the digital section of the board.

Separate power supplies are recommended for the digital and analog sections of the board. This prevents the switching noise present on the digital supply from contaminating the analog power supply and degrading the dynamic performance of the PCM1739. In cases where a common +5V supply must be used for the analog and digital sections, an

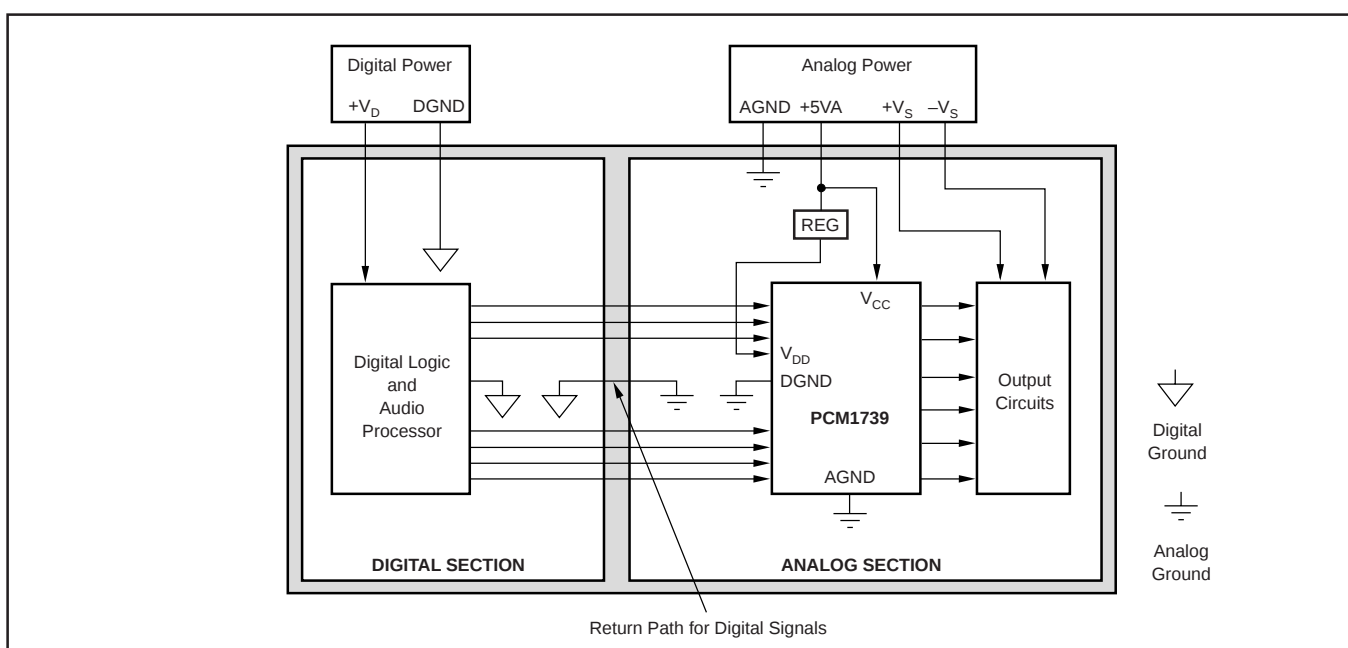


FIGURE 10. Recommended PCB Layout.

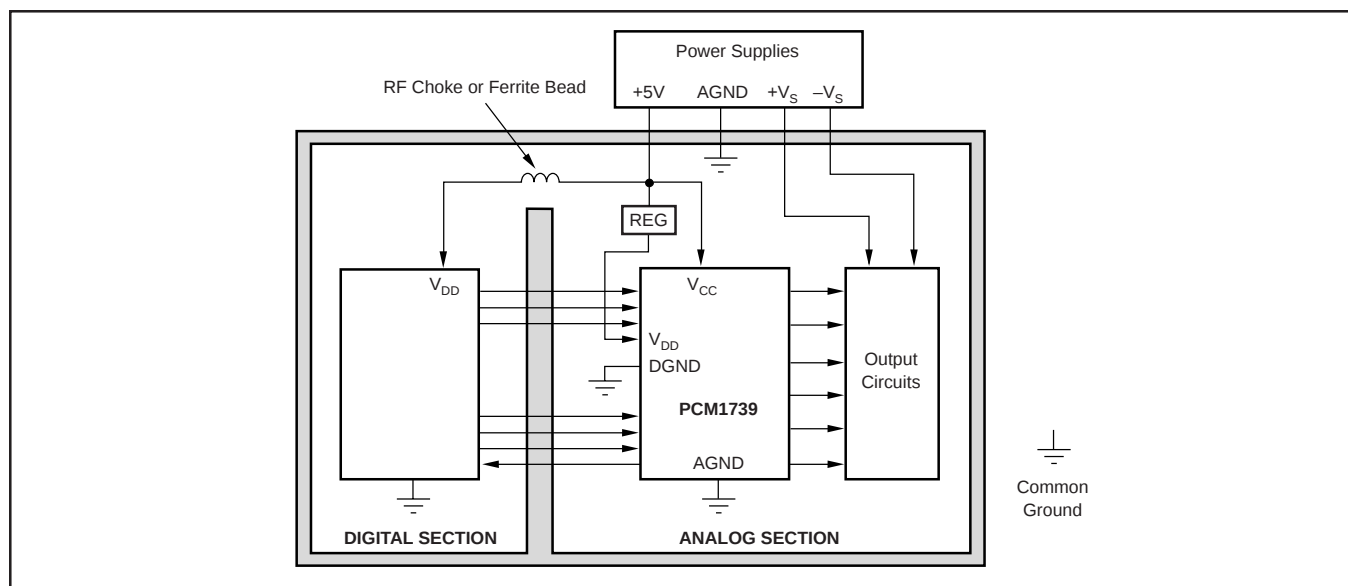


FIGURE 11. Single-Supply PCB Layout.

inductance (RF choke, ferrite bead) should be placed between the analog and digital +5V supply connections to avoid coupling of the digital switching noise into the analog circuitry. Figure 11 shows the recommended approach for single-supply applications

THEORY OF OPERATION

The delta-sigma section of PCM1739 is based on a 8-level amplitude quantizer and a 4th-order noise shaper. This section converts the oversampled input data to 8-level delta-sigma format.

A block diagram of the 8-level delta-sigma modulator is shown in Figure 12. This 8-level delta-sigma modulator has the advantage of stability and clock jitter sensitivity over the typical one-bit (2-level) delta-sigma modulator.

The combined oversampling rate of the delta-sigma modulator and the interpolation filter is $64f_s$ for all system clock combinations (128, 192, 256, 384, 512, 768 f_s).

The theoretical quantization noise performance of the 8-level delta-sigma modulator is shown in Figure 13. The

enhanced multi-level delta-sigma architecture also has advantages for input clock jitter sensitivity due to the multi-level quantizer, with the simulated jitter sensitivity shown in Figure 14.

KEY PERFORMANCE PARAMETERS AND MEASUREMENT

This section provides information on how to measure key dynamic performance parameters for the PCM1739. In all cases, an Audio Precision System Two Cascade or equivalent audio measurement system is utilized to perform the testing.

TOTAL HARMONIC DISTORTION + NOISE

Total Harmonic Distortion + Noise (THD+N) is a significant figure of merit for audio D/A converters since it takes into account both harmonic distortion and all noise sources within a specified measurement bandwidth. The true rms value of the distortion and noise is referred to as THD+N.

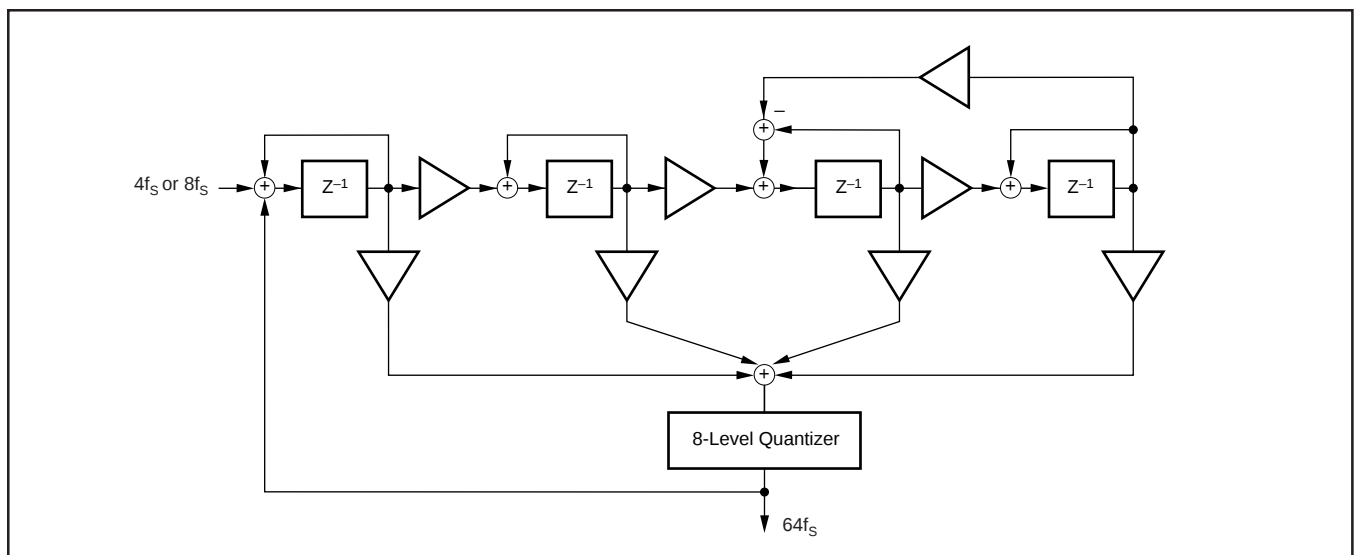


FIGURE 12. Eight-Level Delta-Sigma Modulator.

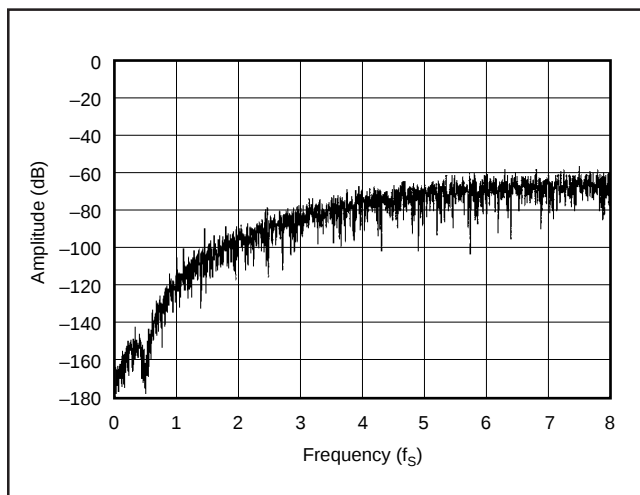


FIGURE 13. Quantization Noise Spectrum.

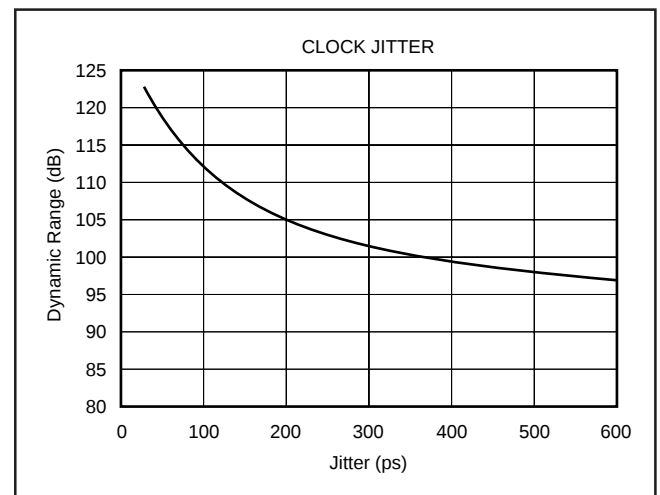


FIGURE 14. Jitter Sensitivity.

For the PCM1739, THD+N is measured with a full scale, 1kHz digital sine wave as the test stimulus at the input of the DAC. The digital generator is set to 24-bit audio word length and a sampling frequency of 44.1kHz, 96kHz, or 192kHz. The digital generator output is taken from the unbalanced S/PDIF connector of the measurement system. The S/PDIF data is transmitted via a coaxial cable to the digital audio receiver on the DEM-DAI1739 demo board. The receiver is then configured to output 24-bit data in either I²S or left-justified data format. The DAC audio interface format is programmed to match the receiver output format. The analog output is then taken from the DAC post filter and connected to the analog analyzer input of the measurement system. The analog input is band limited using filters resident in the analyzer. The resulting THD+N is measured by the analyzer and displayed by the measurement system.

DYNAMIC RANGE

Dynamic range is specified as A-Weighted, THD+N measured with a -60dBFS, 1kHz digital sine wave stimulus at the input of the D/A converter. This measurement is de-

signed to give a good indicator of how the DAC will perform given a low-level input signal.

The measurement setup for the dynamic range measurement is shown in Figure 15, and is similar to the THD+N test setup discussed previously. The differences include the bandlimit filter selection, the additional A-Weighting filter, and the -60dBFS input level.

IDLE CHANNEL SIGNAL-TO-NOISE RATIO

The SNR test provides a measure of the noise floor of the D/A converter. The input to the D/A is all 0's data, and the D/A converter's Infinite Zero Detect Mute function must be disabled (default condition at power up for the PCM1739). This ensures that the delta-sigma modulator output is connected to the output amplifier circuit so that idle tones (if present) can be observed and effect the SNR measurement. The dither function of the digital generator must also be disabled to ensure an all '0's data stream at the input of the D/A converter.

The measurement setup for SNR is identical to that used for dynamic range, with the exception of the input signal level. (see the notes provided in Figure 16).

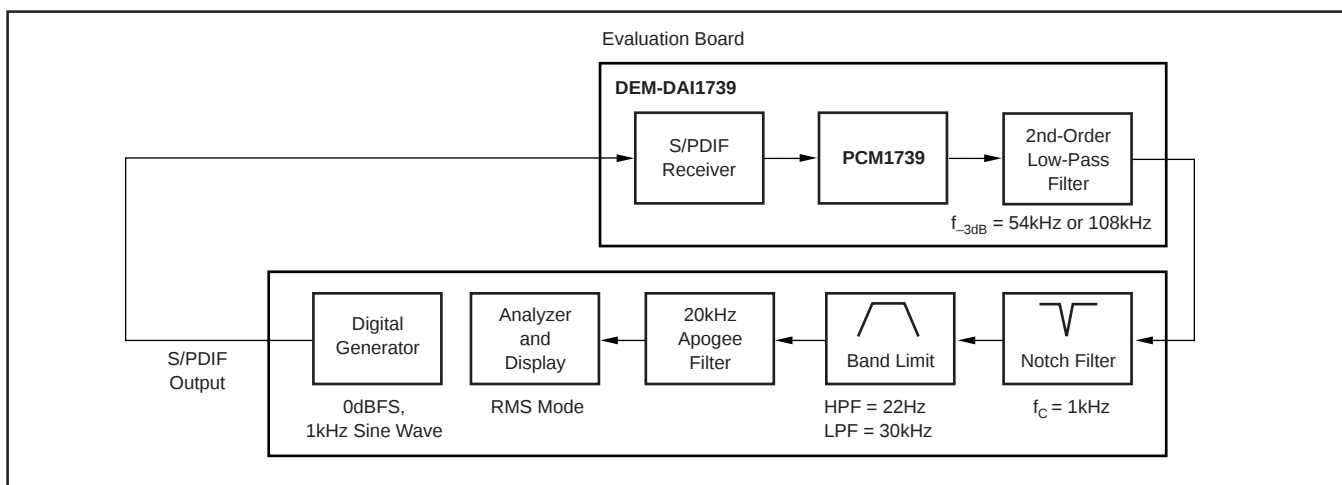


FIGURE 15. Test Setup for THD+N Measurement.

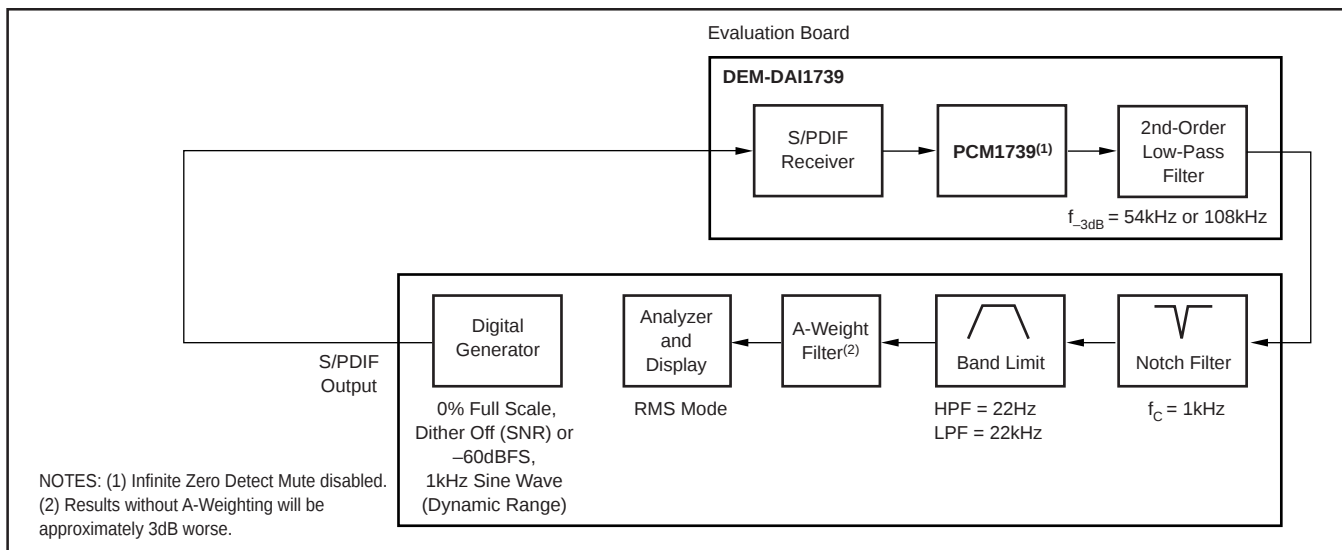


FIGURE 16. Test Set-Up for Dynamic Range and SNR Measurements.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
PCM1739E	ACTIVE	SSOP	DB	28	47	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCM1739E/2K	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCM1739E/2KG4	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCM1739EG4	ACTIVE	SSOP	DB	28	47	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

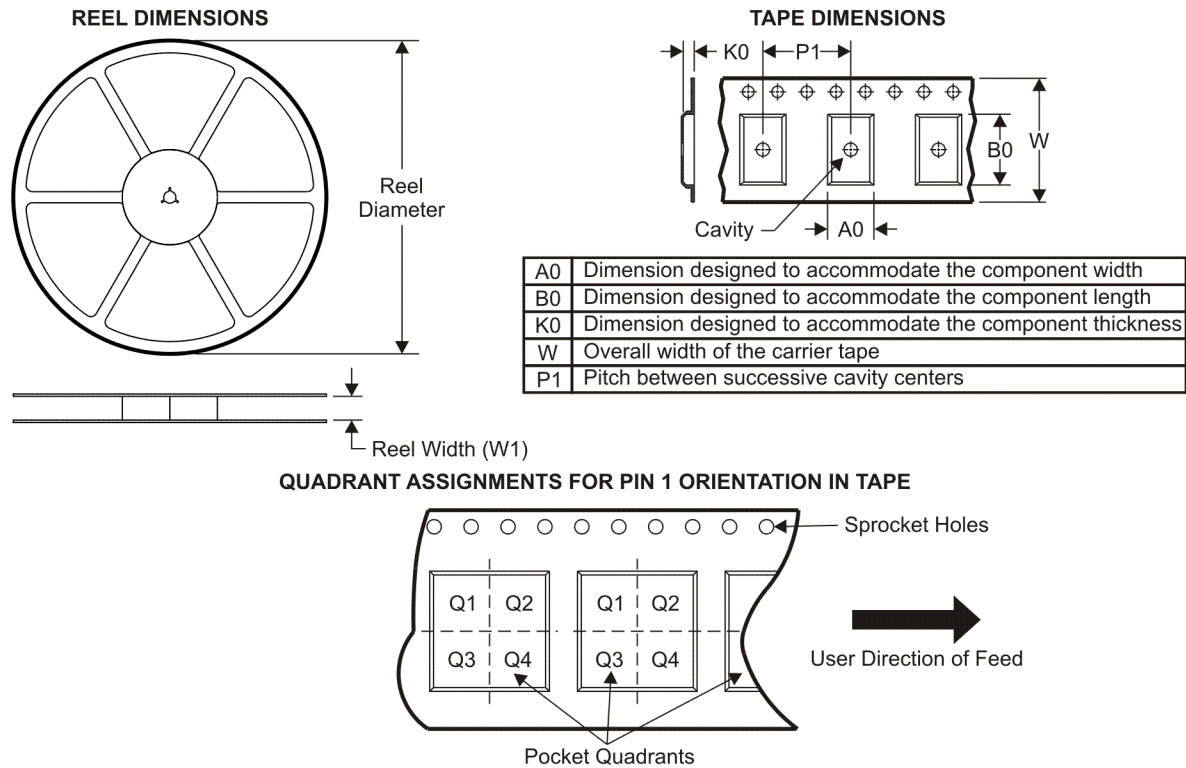
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

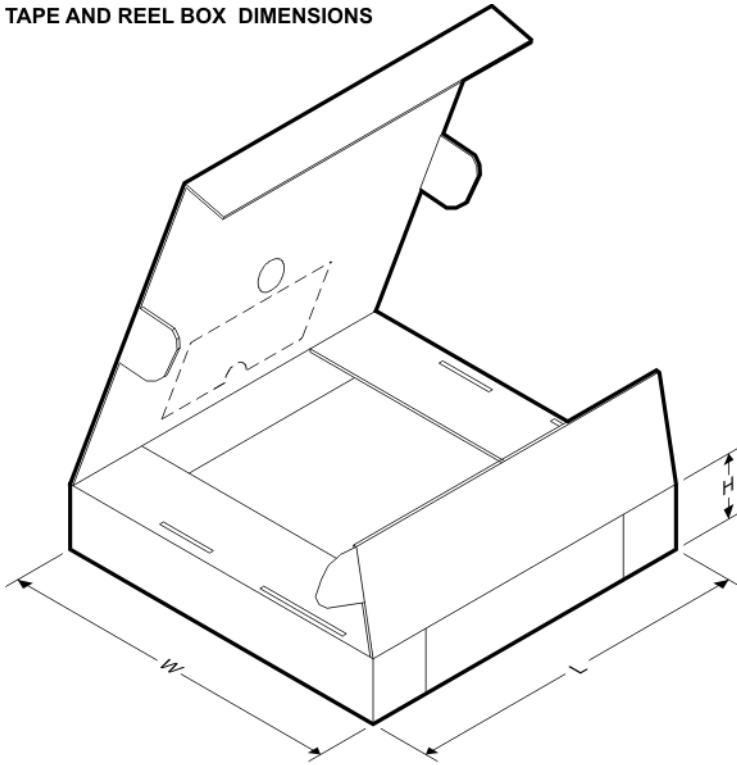
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM1739E/2K	SSOP	DB	28	2000	330.0	17.4	8.5	10.8	2.4	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM1739E/2K	SSOP	DB	28	2000	336.6	336.6	28.6

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2008, Texas Instruments Incorporated