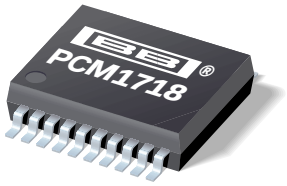
BURR-BROWN®



PCM1718E

SoundPLUS™ Stereo Audio DIGITAL-TO-ANALOG CONVERTER

FEATURES

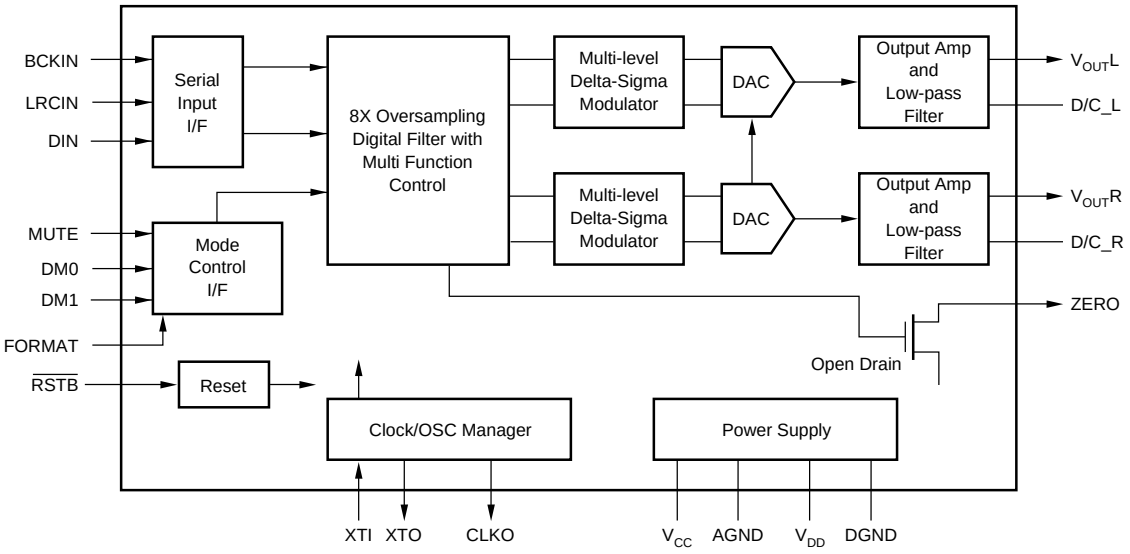
- **ACCEPTS 16- or 18-BIT I²S, OR 18-BIT NORMAL INPUT DATA**
- **COMPLETE STEREO DAC:**
  - **8X Oversampling Digital Filter**
  - **Multi-Level Delta-Sigma DAC**
  - **Analog Low Pass Filter**
  - **Output Amplifier**
- **HIGH PERFORMANCE:**
  - **–90dB THD+N**
  - **96dB Dynamic Range**
  - **100dB SNR**
- **SYSTEM CLOCK: 256fs or 384fs**
- **WIDE POWER SUPPLY: +2.7V to +5.5V**
- **SELECTABLE FUNCTIONS:**
  - **Soft Mute**
  - **Digital De-emphasis**
- **SMALL 20-PIN SSOP PACKAGE**

DESCRIPTION

The PCM1718 is a complete low cost stereo, audio digital-to-analog converter, including digital interpolation filter, 3rd-order delta-sigma DAC, and analog output amplifiers. PCM1718 is fabricated on a highly advanced 0.6µ CMOS process. PCM1718 accepts 18-bit normal input data format, or 16- or 18-bit I²S data format.

The digital filter performs an 8X interpolation function, as well as special functions such as soft mute and digital de-emphasis.

PCM1718 is suitable for a wide variety of cost-sensitive consumer applications where good performance is required. Its low cost, small size, and single power supply make it ideal for BS tuners, keyboards, MPEG audio, PCMCIA audio cards (ZV port), MIDI applications, and set-top boxes.



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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

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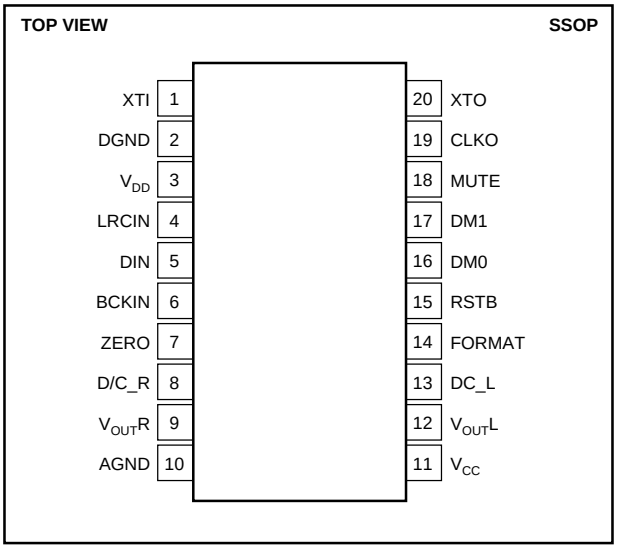
SPECIFICATIONS

All specifications at +25°C, $+V_{CC}$ = $+V_{DD}$ = +5V, fs = 44.1kHz, and 18-bit input data, SYSCLK = 384fs, unless otherwise noted. Measurement bandwidth is 20kHz.

PARAMETER	CONDITIONS	PCM1718E MIN	PCM1718E TYP	PCM1718E MAX	UNITS
RESOLUTION		16		18	Bits
DIGITAL INPUT/OUTPUT					
Logic Family			CMOS		
Input Logic Level:					
V_{IH}(2)		70% of V_{DD}			V
V_{IL}(2)				30% of V_{DD}	V
V_{IH}(3)		70% of V_{DD}			V
V_{IL}(3)				30% of V_{DD}	V
V_{IH}(4)		64% of V_{DD}			V
V_{IL}(4)				28% of V_{DD}	V
Input Logic Current:					
I_{IH}(5)				–6.0	µA
I_{IL}(5)				–120	µA
I_{IH}(6)				–2	µA
I_{IL}(6)				0.02	µA
I_{IH}(4)	V_{IN} = 3.2V			40	µA
I_{IL}(4)	V_{IN} = 1.4V			–40	µA
Output Logic Level: ($+V_{DD}$ = +5V)					
V_{OH}(7)	I_{OH} = –5mA	3.8			V
V_{OL}(7)	I_{OL} = +5mA			1.0	V
V_{OL}(8)	I_{OL} = +5mA			1.0	V
Interface Format			Selectable Normal, I^2S		
Data Format			16/18 Bits MSB First Binary Two's Complement		
Sampling Frequency		32	44.1	48	kHz
System Clock Frequency	256fs/384fs	8.192/12.288	11.2896/16.9344	12.288/18.432	MHz
DC ACCURACY					
Gain Error			±1.0	±5.0	% of FSR
Gain Mismatch Channel-to-Channel			±1.0	±5.0	% of FSR
Bipolar Zero Error	V_O = 1/2 V_{CC} at Bipolar Zero		±30		mV
DYNAMIC PERFORMANCE(1)	V_{CC} = +5V, f = 991Hz				
THD+N at FS (0dB)			–90	–80	dB
THD+N at –60dB			–34		dB
Dynamic Range	EIAJ, A-weighted	90	96		dB
Signal-To-Noise Ratio	EIAJ, A-weighted	92	100		dB
Channel Separation		90	97		dB
Level Linearity Error (–90dB)			±0.5		dB
DYNAMIC PERFORMANCE(1)	V_{CC} = +3V, f = 991Hz				
THD+N at FS (0dB)			–86		dB
Dynamic Range	EIAJ, A-weighted		91		dB
Signal-To-Noise Ratio	EIAJ, A-weighted		94		dB
DIGITAL FILTER PERFORMANCE					
Pass Band Ripple				±0.17	dB
Stop Band Attenuation		–35			dB
Pass Band				0.445	fs
Stop Band		0.555			fs
De-emphasis Error	(fs = 32kHz ~ 48kHz)	–0.2		+0.55	dB
Delay Time (Latency)			11.125/fs		sec
ANALOG OUTPUT					
Voltage Range	FS (0dB) OUT		62% of V_{CC}		Vp-p
Load Impedance		5			kΩ
Center Voltage			50% of V_{CC}		V
POWER SUPPLY REQUIREMENTS					
Voltage Range:	$+V_{CC}$	+2.7		+5.5	VDC
	$+V_{DD}$	+2.7		+5.5	VDC
Supply Current: $+I_{CC}$ $+I_{DD}$(9)	$+V_{CC}$ = $+V_{DD}$ = +5V		18.0	25.0	mA
	$+V_{CC}$ = $+V_{DD}$ = +3V		9.0	15.0	mA
Power Dissipation	$+V_{CC}$ = $+V_{DD}$ = +5V		90	125	mW
	$+V_{CC}$ = $+V_{DD}$ = +3V		27	45	mW
TEMPERATURE RANGE					
Operation		–25		+85	°C
Storage		–55		+100	°C

NOTES: (1) Tested with Shibasoku #725 THD. Meter 400Hz HPF, 30kHz LPF On, Average Mode with 20kHz bandwidth limiting. (2) Pins 4, 5, 6, 14: LRCIN, DIN, BCKIN, FORMAT. (3) Pins 15, 16, 17, 18: RSTB, DM0, DM1, MUTE (Schmitt trigger input). (4) Pin 1: XTI. (5) Pins 15, 16, 17, 18: RSTB, DM0, DM1, MUTE (if pull-up resistor is used). (6) Pins 4, 5, 6: LRCIN, DIN, BCKIN (if pull-up resistor is not used). (7) Pin 19: CLKO. (8) Pin 7: ZERO. (9) No load on pins 19 (CLKO) and 20 (XTO).

PIN CONFIGURATION



PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)
PCM1718E	20-Pin SSOP	334-1

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	+6.5V
$+V_{CC}$ to $+V_{DD}$ Difference	±0.1V
Input Logic Voltage	–0.3V to (V_{DD} + 0.3V)
Power Dissipation	200mW
Operating Temperature Range	–25°C to +85°C
Storge Temperature	–55°C to +125°C
Lead Temperature (soldering, 5s)	+260°C
Thermal Resistance, θ_{JA}	+70°C/W

PIN ASSIGNMENTS

PIN	NAME	FUNCTION
Data Input Interface Pins		
4	LRCIN	Sample Rate Clock Input. Controls the update rate (fs).
5	DIN	Serial Data Input. MSB first, right justified (Sony format, 18 bits) or I^2S (Philips format, 16 or 18 bits).
6	BCKIN	Bit Clock Input. Clocks in the data present on DIN input.
Mode Control and Clock Signals		
1	XTI	Oscillator Input (External Clock Input). For an internal clock, tie XTI to one side of the crystal oscillator. For an external clock, tie XTI to the output of the chosen external clock.
14(1)	FORMAT	A “HIGH” selects I^2S input data format, and a “LOW” selects Normal (Sony) input data format.
16(1)	DM0	De-emphasis selection.
17(1)	DM1	De-emphasis selection.
18(1)	MUTE	Soft Mute Control. When set “LOW”, the outputs are muted.
19	CLKO	Buffered Output of Oscillator. Equivalent to XTI.
20	XTO	Oscillator Output. When using the internal clock, tie to the opposite side (from pin 1) of the crystal oscillator. When using an external clock, leave XTO open.
Operational Controls and Flags		
7	ZERO	Infinite Zero Detection Flag, open drain output. When the input is continuously zero for 65,536 cycles of BCKIN, ZERO is “LOW”.
15(1)	RSTB	Resets DAC operation with an active “LOW” pulse.
Analog Output Functions		
8	D/C_R	Right Channel Output Amplifier Common. Bypass to ground with 10µF capacitor.
9	V_{OUT}R	Right Channel Analog Output. V_{OUT} max = 0.62 x V_{CC}.
12	V_{OUT}L	Left Channel Analog Output. V_{OUT} max = 0.62 x V_{CC}.
13	D/C_L	Left Channel Output Amplifier Common. Bypass to ground with 10µF capacitor.
Power Supply Connections		
2	DGND	Digital Ground.
3	V_{DD}	Digital Power Supply (+5V or +3V).
10	AGND	Analog Ground.
11	V_{CC}	Analog Power Supply (+5V or +3V).

NOTE: (1) With internal pull-up.

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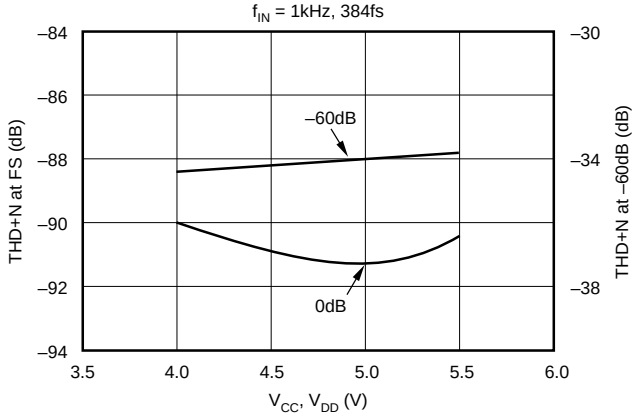
TYPICAL PERFORMANCE CURVES

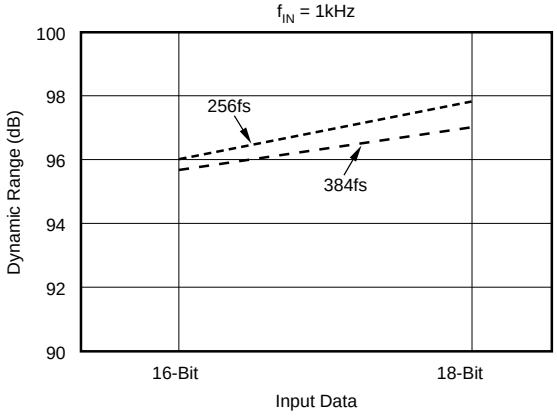
At T_A = +25°C, V_S = +5V, R_L = 100Ω, C_L = 2pF, and R_{FB} = 402Ω, unless otherwise noted.

DYNAMIC PERFORMANCE

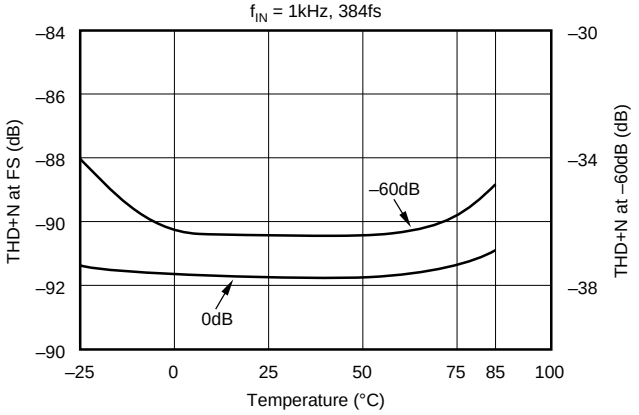
THD+N vs V_{CC}, V_{DD}
f_{IN} = 1kHz, 384fs



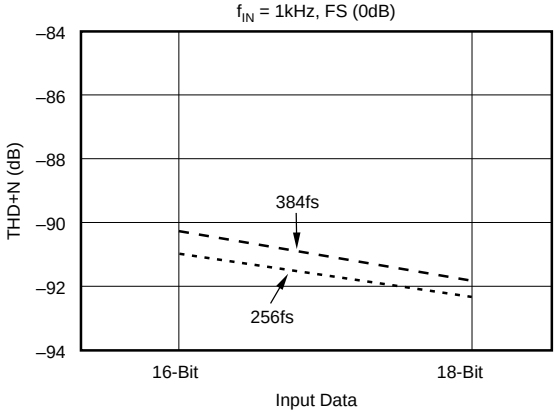
DYNAMIC RANGE vs INPUT DATA
f_{IN} = 1kHz



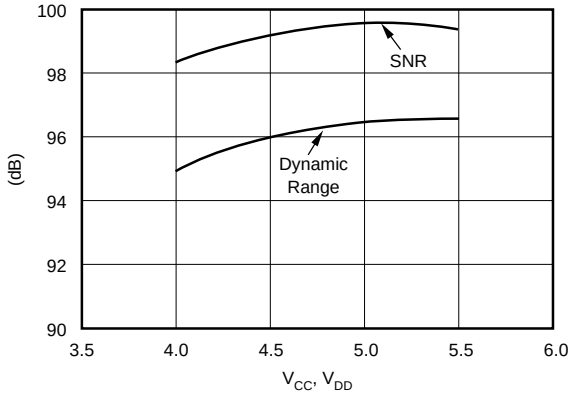
THD+N vs TEMPERATURE
f_{IN} = 1kHz, 384fs



THD+N vs INPUT DATA
f_{IN} = 1kHz, FS (0dB)



DYNAMIC RANGE AND SNR vs V_{CC}, V_{DD}
f_{IN} = 1kHz, 384fs

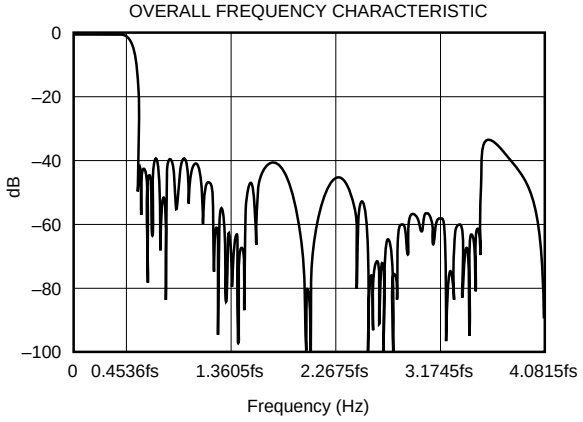


TYPICAL PERFORMANCE CURVES

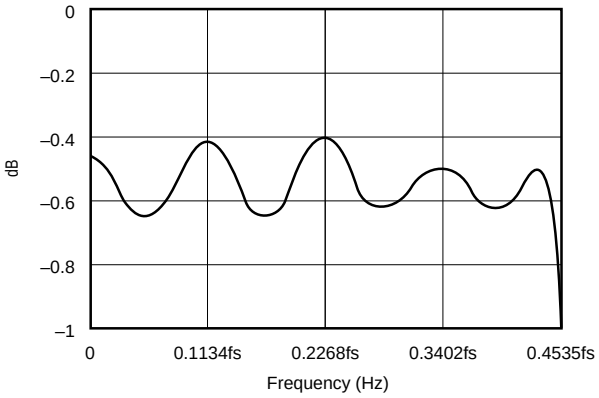
At T_A = +25°C, V_S = +5V, R_L = 44.1kHz, f_{SYS} = 384fs, and 18-bit input data, unless otherwise noted.

DIGITAL FILTER

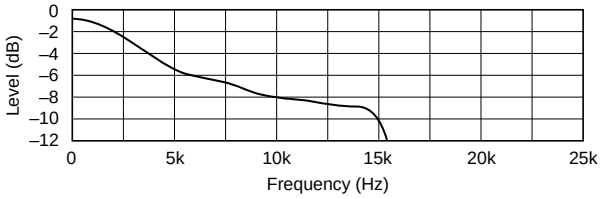
OVERALL FREQUENCY CHARACTERISTIC



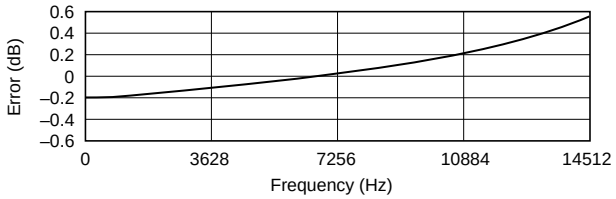
PASSBAND RIPPLE CHARACTERISTIC



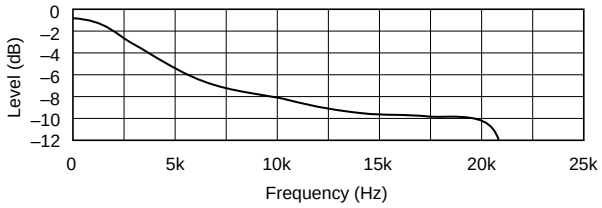
DE-EMPHASIS FREQUENCY RESPONSE (32kHz)



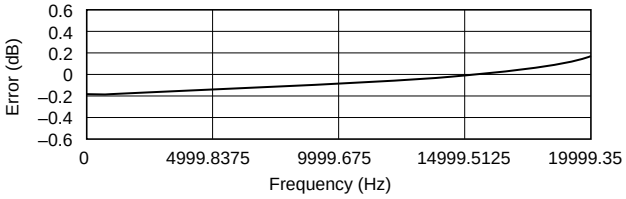
DE-EMPHASIS ERROR (32kHz)



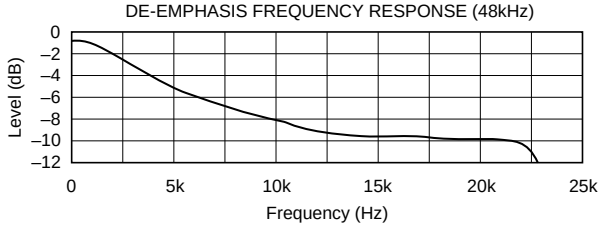
DE-EMPHASIS FREQUENCY RESPONSE (44.1kHz)



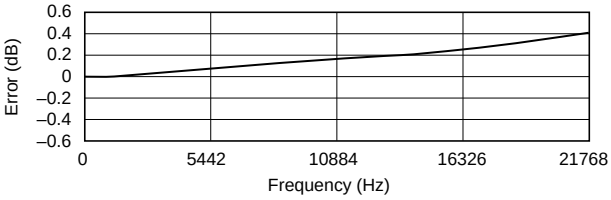
DE-EMPHASIS ERROR (44.1kHz)



DE-EMPHASIS FREQUENCY RESPONSE (48kHz)



DE-EMPHASIS ERROR (48kHz)



SYSTEM CLOCK

The system clock for PCM1718 must be either 256fs or 384fs, where fs is the audio sampling frequency (typically 32kHz, 44.1kHz, or 48kHz). The system clock is used to operate the digital filter and the modulator.

The system clock can be either a crystal oscillator placed between XTI (pin 1) and XTO (pin 20), or an external clock input to XTI. If an external system clock is used, XTO is open (floating). Figure 1 illustrates the typical system clock connections.

PCM1718 has a system clock detection circuit which automatically senses if the system clock is operating at 256fs or 384fs. The system clock should be synchronized with LRCIN (pin 4) clock. LRCIN (left-right clock) operates at the sampling frequency fs. In the event these clocks are not synchronized, PCM1718 can compensate for the phase difference internally. If the phase difference between left-right and system clocks is greater than 6 bit clocks (BCKIN), the synchronization is performed internally. While the synchronization is processing, the analog output is forced to a DC level at bipolar zero. The synchronization typically occurs in less than 1 cycle of LRCIN.

DATA INTERFACE FORMATS

Digital audio data is interfaced to PCM1718 on pins 4, 5, and 6—LRCIN (left-right clock), DIN (data input) and BCKIN (bit clock). PCM1718 can accept both normal and I^2S data formats. Normal data format is MSB first, two's complement, right-justified. I^2S data is compatible with Philips serial data protocol. Figures 3 and 4 illustrate the input data formats.

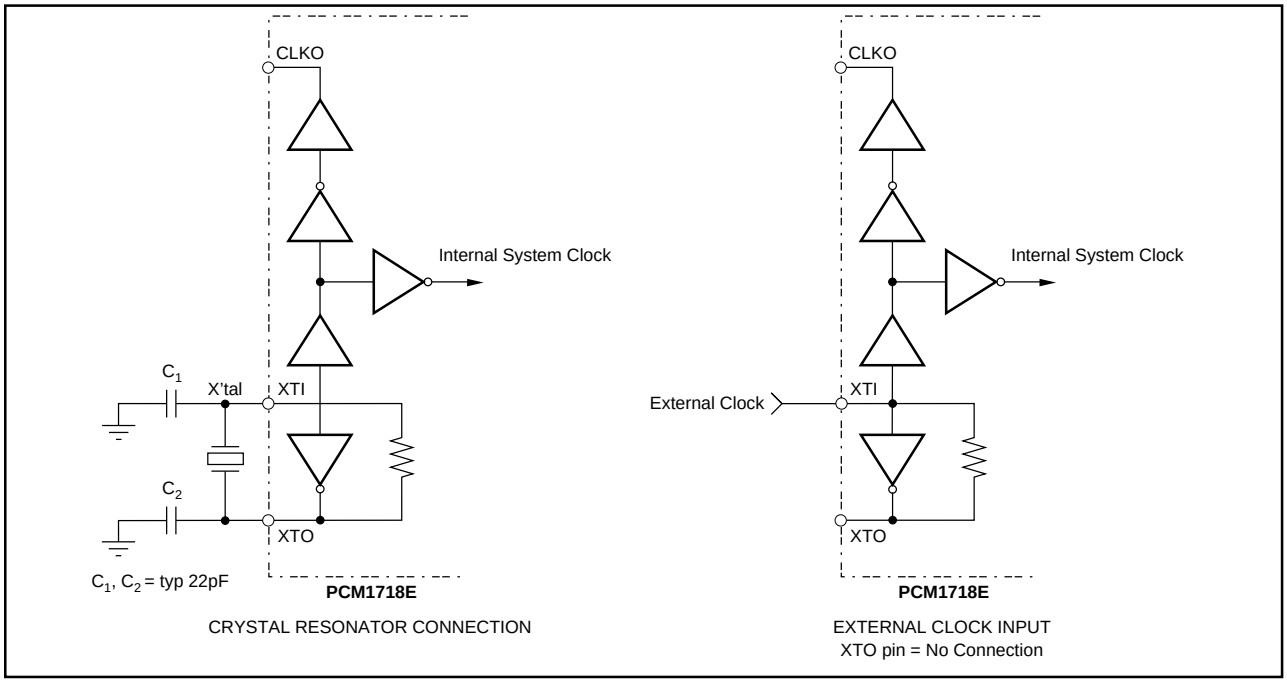
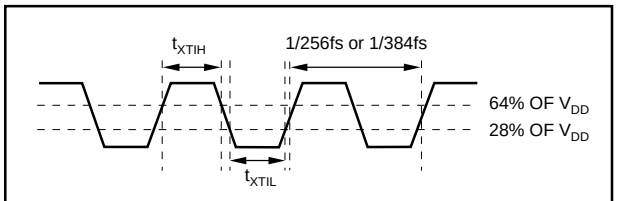


FIGURE 1. Internal Clock Circuit Diagram and Oscillator Connection.



External System Clock High	t_{XTIH}	10ns (min)
External System Clock Low	t_{XTIL}	10ns (min)

FIGURE 2. External Clock Timing Requirements.

FUNCTIONAL CONTROLS

PCM1718 allows the user to control the input data format, soft mute, and digital de-emphasis frequency. Table I illustrates the selectable functions:

FUNCTION	CONTROL PIN
Data Input Format Normal I^2S	FORMAT (Pin 14)
De-emphasis 32kHz 44.1kHz 48kHz	DM0, DM1 (Pins 16, 17)
Soft Mute	MUTE (Pin 18)
Reset	RSTB (Pin 15)

TABLE I. Selectable Functions.

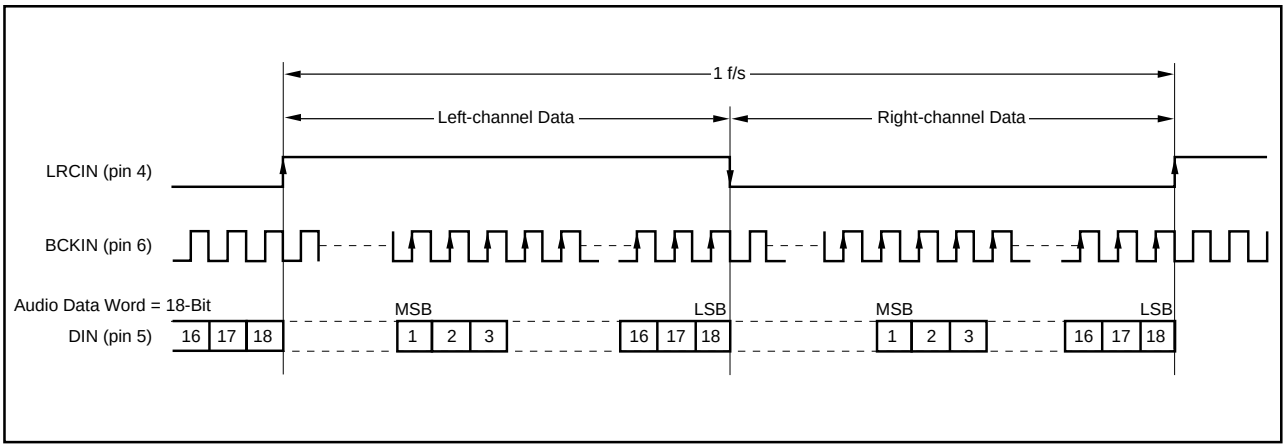


FIGURE 3. "Normal" Data Input Timing.

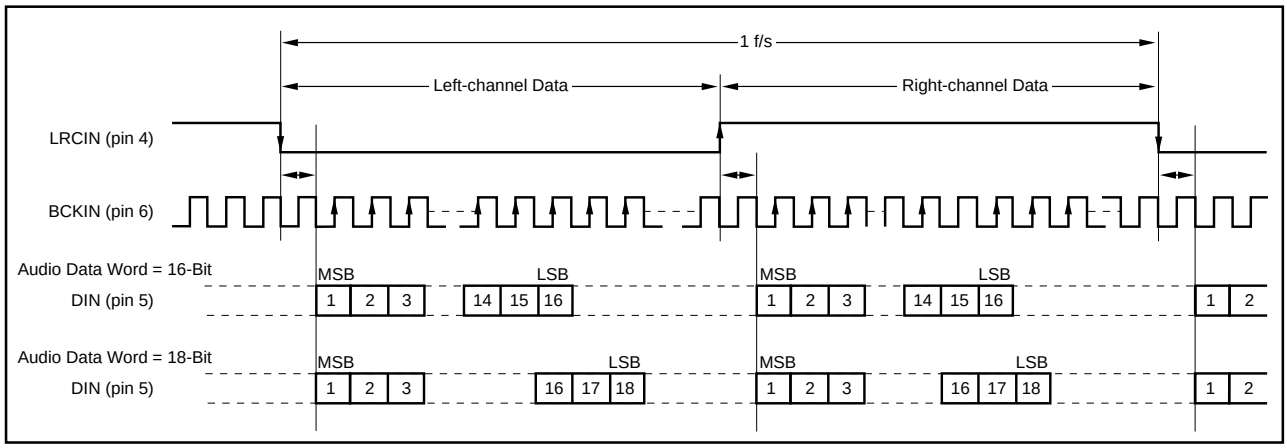
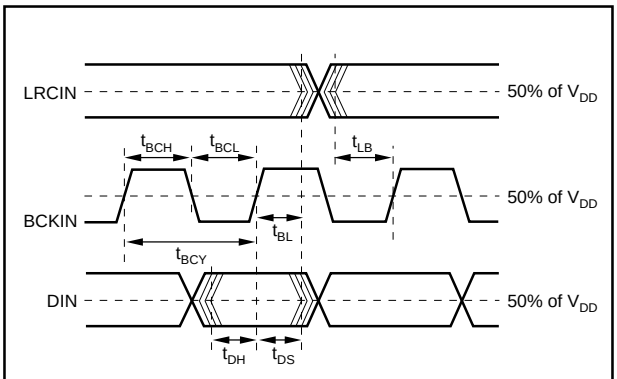


FIGURE 4. "I²S" Data Input Timing.



BCKIN Pulsewidth (High Level)	t_{BCH}	50ns (min)
BCKIN Pulsewidth (Low Level)	t_{BCL}	50ns (min)
BCKIN Pulse Cycle Time	t_{BCY}	100ns (min)
BCKIN Rising Edge → LRCIN Edge	t_{BL}	30ns (min)
LRCIN Edge → BCKIN Rising Edge	t_{LB}	30ns (min)
DIN Setup Time	t_{DS}	30ns (min)
DIN Hold Time	t_{DH}	30ns (min)

FIGURE 5. Data Input Timing.

Data Format

A "HIGH" on pin 14 (FORMAT) sets the input format to I²S, and a "LOW" sets the format to Normal (MSB-first, right-justified Sony format).

Soft Mute

A "LOW" on pin 18 (MUTE) causes both outputs to be muted. This muting is done in the digital domain so there is no audible "click" when the soft mute is enacted.

De-Emphasis

PCM1718 allows for digital de-emphasis for all three standard sampling frequencies:

DM1 (Pin 17)	DM0 (Pin 16)	De-Emphasis Mode
0	0	OFF
0	1	48kHz
1	0	44.1kHz
1	1	32kHz

Reset

PCM1718 has both internal power on reset circuit and the RSTB-pin (pin 15) which accepts external forced reset by RSTB = LOW. For internal power on reset, initialize (reset) is done automatically at power on V_{DD} >2.2V (typ). During internal reset = LOW, the output of the DAC is invalid and the analog outputs are forced to $V_{CC}/2$. Figure 6 illustrates the timing of internal power on reset.

For the RSTB-pin, PSTB-pin accepts external forced reset by RSTB = L. During RSTB = L, the output of the DAC is invalid and the analog outputs are forced to $V_{CC}/2$ after internal initialize (1024 system clocks count after RSTB = H.) Figure 7 illustrates the timing of RSTB-pin reset.

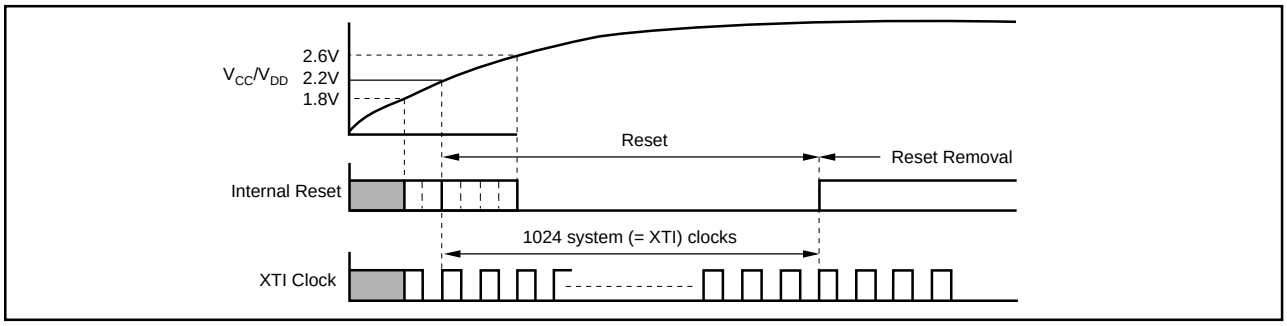


FIGURE 6. Internal Power-On Reset Timing.

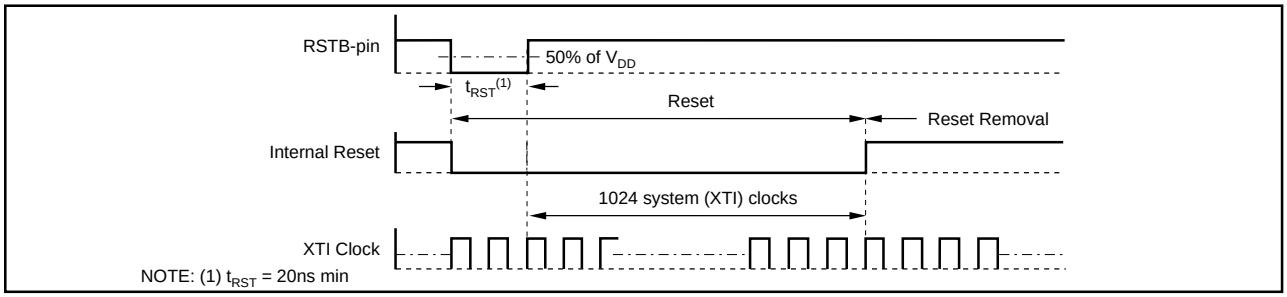


FIGURE 7. RSTB-Pin Reset Timing.

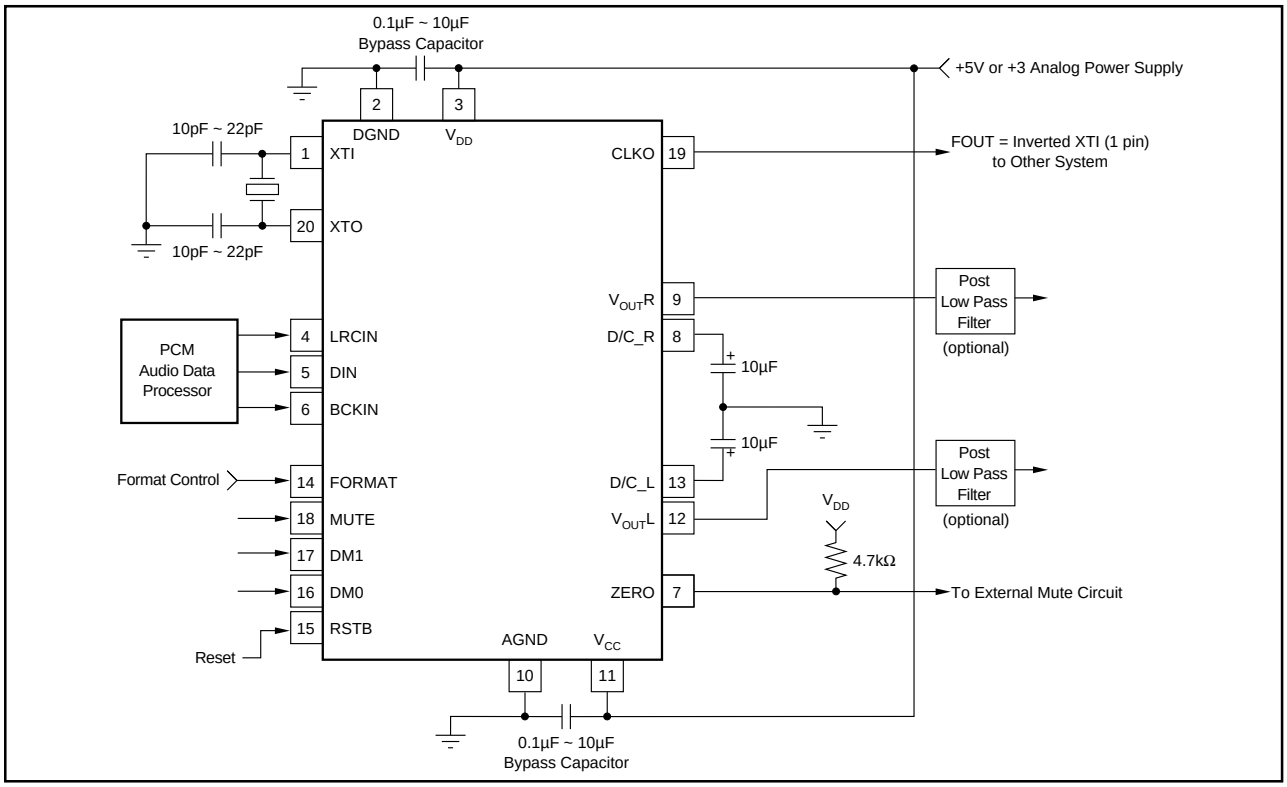


FIGURE 8. Typical Connection Diagram of PCM1718.

POWER SUPPLY CONNECTIONS

PCM1718 has two power supply connections: digital (V_{DD}) and analog (V_{CC}). Each connection also has a separate ground. If the power supplies turn on at different times, there is a possibility of a latch-up condition. To avoid this condition, it is recommended to have a common connection between the digital and analog power supplies. If separate supplies are used without a common connection, the delta between the two supplies during ramp-up time must be less than 0.6V.

An application circuit to avoid a latch-up condition is shown in Figure 9.

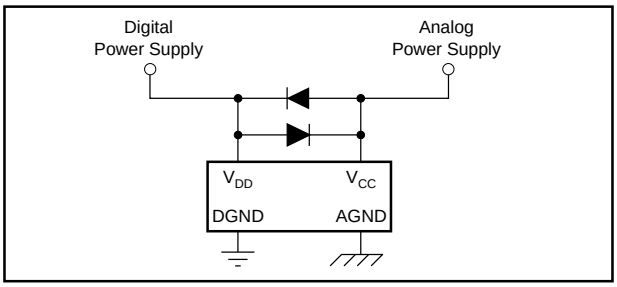


FIGURE 9. Latch-up Prevention Circuit.

BYPASSING POWER SUPPLIES

The power supplies should be bypassed as close as possible to the unit. Refer to Figure 8 for optimal values of bypass capacitors.

THEORY OF OPERATION

The delta-sigma section of PCM1718 is based on a 5-level amplitude quantizer and a 3rd-order noise shaper. This section converts the oversampled input data to 5-level delta-sigma format.

A block diagram of the 5-level delta-sigma modulator is shown in Figure 10. This 5-level delta-sigma modulator has the advantage of stability and clock jitter sensitivity over the typical one-bit (2 level) delta-sigma modulator.

The combined oversampling rate of the delta-sigma modulator and the internal 8-times interpolation filter is 48fs for a 384fs system clock, and 64fs for a 256fs system clock. The theoretical quantization noise performance of the 5-level delta-sigma modulator is shown in Figure 11.

Multi Level
Delta Sigma

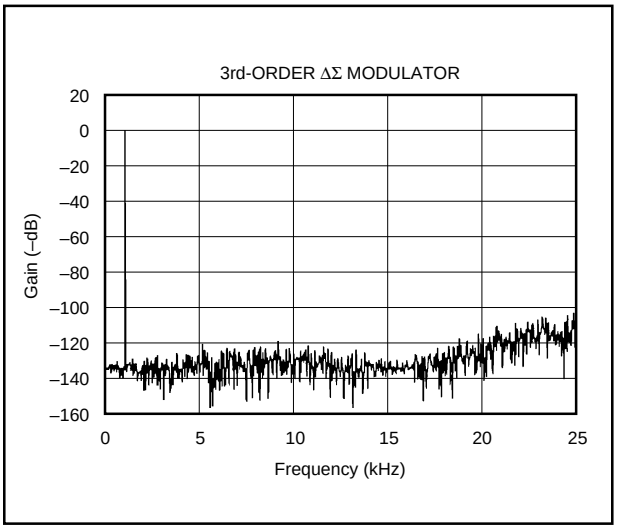


FIGURE 11. Quantization Noise Spectrum.

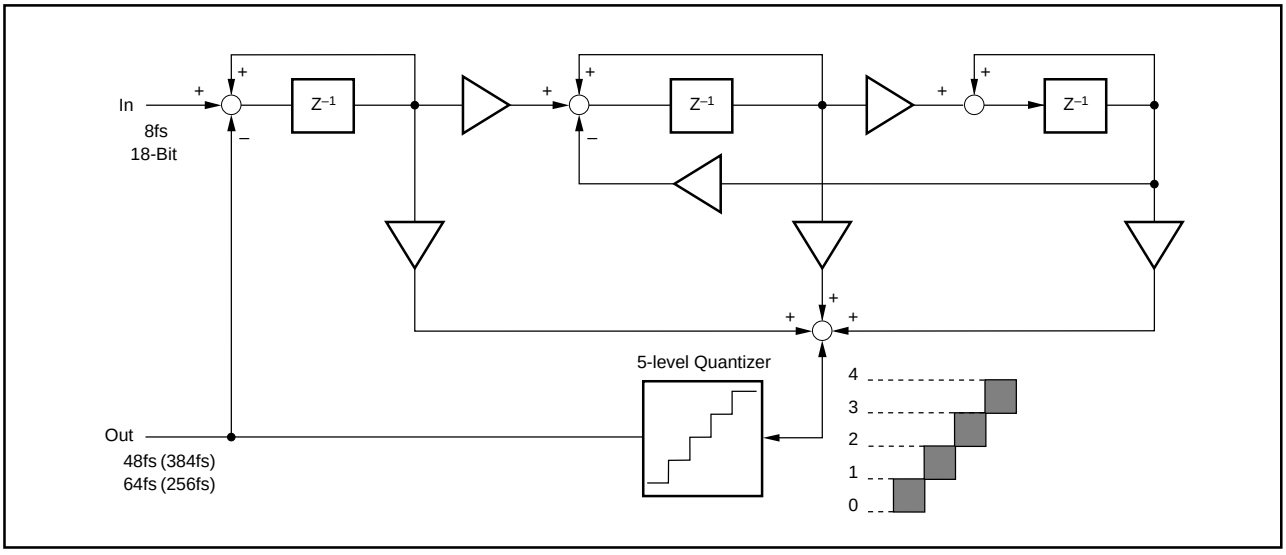


FIGURE 10. 5-Level ΔΣ Modulator Block Diagram.

APPLICATION CONSIDERATIONS

DELAY TIME

There is a finite delay time in delta-sigma converters. In A/D converters, this is commonly referred to as latency. For a delta-sigma D/A converter, delay time is determined by the order number of the FIR filter stage, and the chosen sampling rate. The following equation expresses the delay time of PCM1718:

$$T_D = 11.125 \times 1/fs$$

For fs = 44.1kHz, T_D = 11.125/44.1kHz = 251.4µs

Applications using data from a disc or tape source, such as CD audio, CD-Interactive, Video CD, DAT, Minidisc, etc., generally are not affected by delay time. For some professional applications such as broadcast audio for studios, it is important for total delay time to be less than 2ms.

OUTPUT FILTERING

For testing purposes all dynamic tests are done on the PCM1718 using a 20kHz low pass filter. This filter limits the measured bandwidth for THD+N, etc. to 20kHz. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the specifications. The low pass filter removes out of band noise. Although it is not audible, it may affect dynamic specification numbers.

The performance of the internal low pass filter from DC to 24kHz is shown in Figure 12. The higher frequency rolloff of the filter is shown in Figure 13. If the user's application has the PCM1718 driving a wideband amplifier, it is recommended to use an external low pass filter. A simple 3rd-order filter is shown in Figure 14. For some applications, a passive RC filter or 2nd-order filter may be adequate.

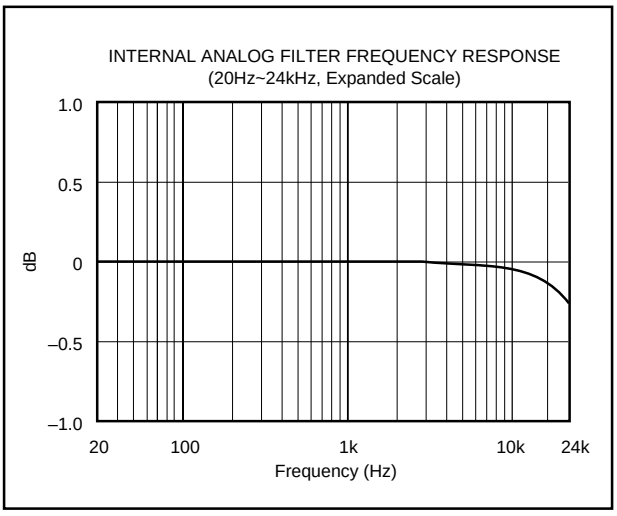


FIGURE 12. Low Pass Filter Frequency Response.

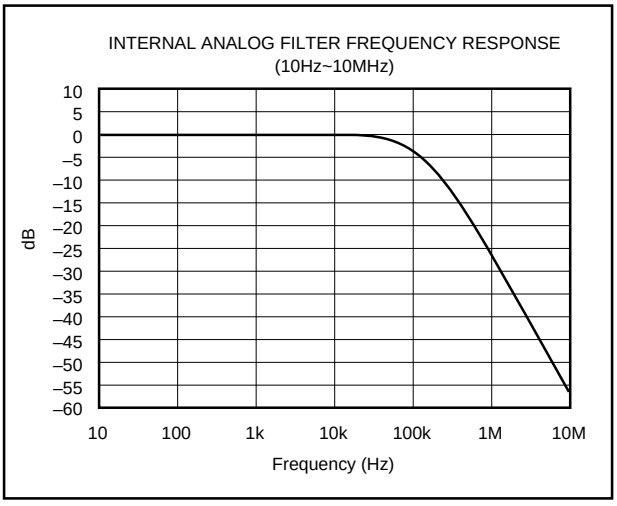


FIGURE 13. Low Pass Filter Frequency Response.

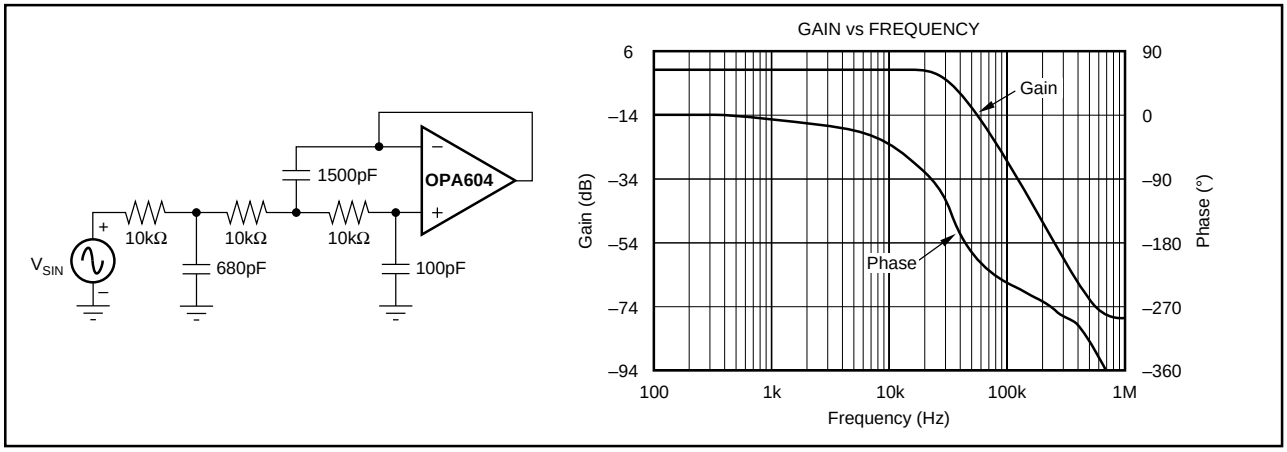


FIGURE 14. 3rd-Order LPF.

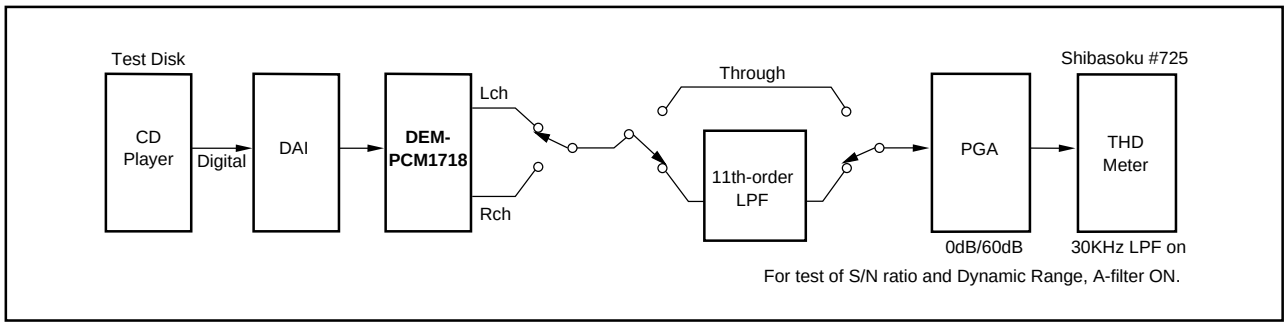


FIGURE 15. Test Block Diagram.

TEST CONDITIONS

Figure 15 illustrates the actual test conditions applied to PCM1718 in production. The 11th-order filter is necessary in the production environment for the removal of noise resulting from the relatively long physical distance between the unit and the test analyzer. In most actual applications, the 3rd-order filter shown in Figure 14 is adequate. Under normal conditions, THD+N typical performance is –70dB with a 30kHz low pass filter (shown here on the THD meter), improving to –89dB when the external 20kHz 11th-order filter is used. For cost-sensitive applications, a single RC filter, as shown in Figure 18, may be adequate.

EVALUATION FIXTURES

DEM-PCM1718

This evaluation fixture is primarily intended for quick evaluation of the PCM1718's performance. DEM-PCM1718 can accept either an external clock or a user-installed crystal oscillator. All of the functions can be controlled by on-board switches. DEM-PCM1718 does not contain a receiver chip or an external low pass filter. DEM-PCM1718 requires a single +2.7V to +5V power supply.

OUT-OF-BAND NOISE CONSIDERATIONS

Delta-sigma DACs are by nature very sensitive to jitter on the master clock. Phase noise on the clock will result in an increase in noise, ultimately degrading dynamic range. It is difficult to quantify the effect of jitter due to problems in synthesizing low levels of jitter. One of the reasons delta-sigma DACs are prone to jitter sensitivity is the large quantization noise when the modulator can only achieve two discrete output levels (0 or 1). The multi-level delta-sigma DAC has improved theoretical SNR because of multiple output states. This reduces sensitivity to jitter. Figure 16 contrasts jitter sensitivity between a one-bit PWM type DAC and multi-level delta-sigma DAC. The data was derived using a simulator, where clock jitter could be completely synthesized.

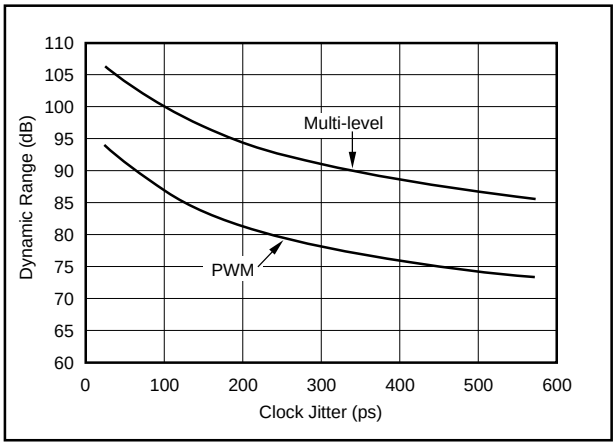


FIGURE 16. Simulation Results of Clock Jitter Sensitivity.

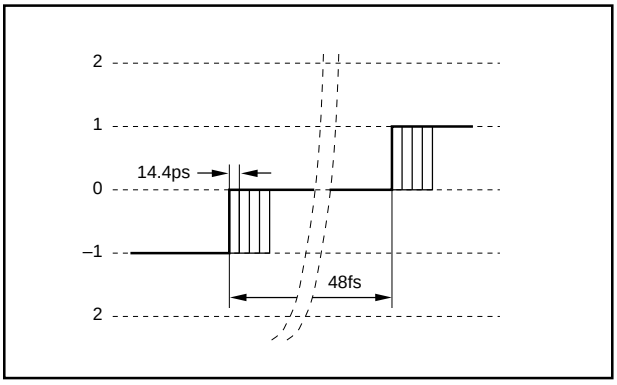


FIGURE 17. Simulation Method for Clock Jitter.

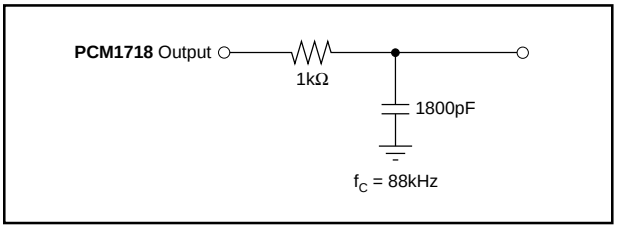


FIGURE 18. RC Output Filter.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCM1718E	ACTIVE	SSOP	DB	20	65	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM		PCM1718E	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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