# PCM1690 24-Bit, 192-kHz Sampling, Enhanced Multi-Level ΔΣ, Eight-Channel Audio Digital-to-Analog Converter

## 1 Features

- 24-Bit Delta-Sigma DAC
- 8-Channel DAC:
  - High Performance: Differential, $f_S$ = 48 kHz
  - THD+N: –94 dB
  - SNR: 113 dB
  - Dynamic Range: 113 dB
  - Sampling Rate: 8 kHz to 192 kHz
  - System Clock: 128 $f_S$, 192 $f_S$, 256 $f_S$, 384 $f_S$, 512 $f_S$, 768 $f_S$, 1152 $f_S$
  - Differential Voltage Output: 8 $V_{PP}$
  - Analog Lowpass Filter Included
  - 4x/8x Oversampling Digital Filter:
    - Passband Ripple: ±0.0018 dB
    - Stop Band Attenuation: –75 dB
  - Zero Flag
- Flexible Audio Interface:
  - I/F Format: I²S™, Left-/Right-Justified, DSP, TDM
  - Data Length: 16, 20, 24, 32 Bits
- Flexible Mode Control:
  - 3-Wire SPI, 2-Wire I²C-Compatible Serial Control Interface, or Hardware Control
- Multiple Functions Through SPI or I²C I/F:
  - Audio I/F Format Select: I²S, Left-Justified, Right-Justified, DSP, TDM
  - Digital Attenuation and Soft Mute
  - Digital De-Emphasis: 32 kHz, 44.1 kHz, 48 kHz
  - Data Polarity Control
  - Power Down
- Multiple Functions Through H/W Control:
  - Audio I/F Format Select: I²S, TDM
  - Digital De-Emphasis Filter: 44.1 kHz
- Analog Mute by Clock Halt Detection
- External RESET Pin
- Power Supplies:
  - 5 V for Analog and 3.3 V for Digital
- Package: HTSSOP-48
- Operating Temperature Range:
  - –40°C to +85°C

## 2 Applications

- Blu-ray™ DVD Players
- HD DVD Players
- AV Receivers
- Home Theaters
- Car Audio External Amplifiers
- Car Audio AVN Applications

## 3 Description

The PCM1690 device is a high-performance, single-chip, 24-bit, eight-channel, audio digital-to-analog converter (DAC) with differential outputs. The eight-channel, 24-bit DAC employs an enhanced, multi-level delta-sigma (ΔΣ) modulator and supports 8-kHz to 192-kHz sampling rates and a 16-/20-/24-/32-bit width digital audio input word on the audio interface. The audio interface of the PCM1690 supports the time-division-multiplexed (TDM) format in addition to the standard I²S, left-justified, right-justified, and DSP formats.

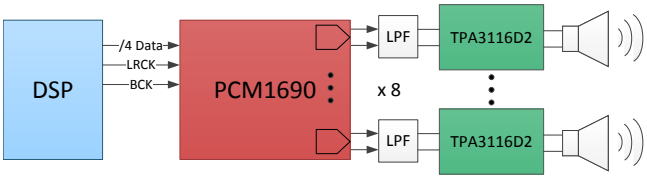
The PCM1690 can be controlled through a three-wire, SPI-compatible interface, or two-wire, I²C-compatible serial interface in software, which provides access to all functions including digital attenuation, soft mute, de-emphasis, and so forth. Also, hardware control mode provides a subset of user-programmable functions through two control pins. The PCM1690 is available in a 12-mm × 8-mm (12-mm × 6-mm body) HTSSOP-48 package.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| PCM1690 | HTSSOP (48) | 12.50 mm × 6.10 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Simplified Application Diagram**




An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision A (January 2009) to Revision B** — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

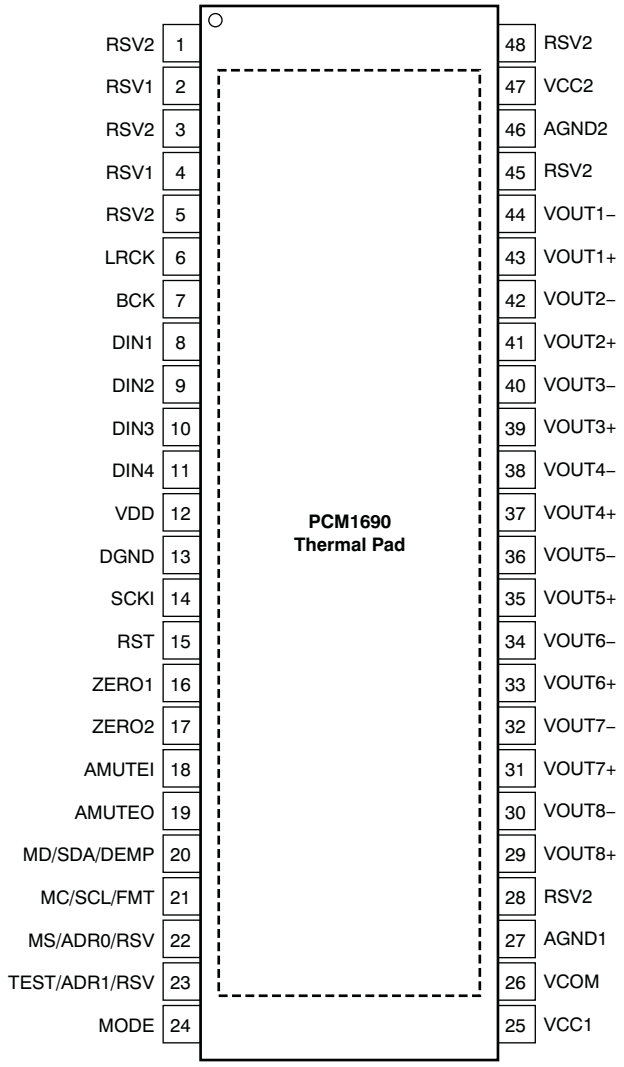
**Changes from Original (October 2008) to Revision A** — **Page**

- Changed Figure 41 ... 37


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# 5 Pin Configuration and Functions

**DCA Package**
**48-Pin HTSSOP With PowerPAD**
**Top View**




**Pin Functions**

| PIN | | I/O | PULLDOWN | 5-V TOLERANT | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | PIN | | | | |
| RSV2 | 1 | — | — | — | Reserved, tied to analog ground |
| RSV1 | 2 | — | — | — | Reserved, left open |
| RSV2 | 3 | — | — | — | Reserved, tied to analog ground |
| RSV1 | 4 | — | — | — | Reserved, left open |
| RSV2 | 5 | — | — | — | Reserved, tied to analog ground |
| LRCK | 6 | I | Yes | No | Audio data word clock input |
| BCK | 7 | I | Yes | No | Audio data bit clock input |
| DIN1 | 8 | I | No | No | Audio data input for DAC1 and DAC2 |
| DIN2 | 9 | I | No | No | Audio data input for DAC3 and DAC4 |
| DIN3 | 10 | I | No | No | Audio data input for DAC5 and DAC6 |

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## Pin Functions (continued)

| PIN | | I/O | PULLDOWN | 5-V TOLERANT | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | PIN | | | | |
| DIN4 | 11 | I | No | No | Audio data input for DAC7 and DAC8 |
| VDD | 12 | — | — | — | Digital power supply, +3.3 V |
| DGND | 13 | — | — | — | Digital ground |
| SCKI | 14 | I | No | Yes | System clock input |
| RST | 15 | I | Yes | Yes | Reset and power-down control input with active low |
| ZERO1 | 16 | O | No | No | Zero detect flag output 1 |
| ZERO2 | 17 | O | No | No | Zero detect flag output 2 |
| AMUTEI | 18 | I | No | Yes | Analog mute control input with active low |
| AMUTEO | 19 | O | No | Yes | Analog mute status output(1) with active low |
| MD/SDA/DEMP | 20 | I/O | No | Yes | Input data for SPI, data for $I^2C$(1), de-emphasis control for hardware control mode |
| MC/SCL/FMT | 21 | I | No | Yes | Clock for SPI, clock for $I^2C$, format select for hardware control mode |
| MS/ADR0/RSV | 22 | I | Yes | Yes | Chip Select for SPI, address select 0 for $I^2C$, reserve (set low) for hardware control mode |
| TEST/ADR1/RSV | 23 | I/O | No | Yes | Test (factory use, left open) for SPI, address select 1 for $I^2C$, reserve (set low) for hardware control mode |
| MODE | 24 | I | No | No | Control port mode selection. Tied to VDD: SPI, left open: H/W mode, tied to DGND: $I^2C$ |
| VCC1 | 25 | — | — | — | Analog power supply 1, +5 V |
| VCOM | 26 | — | — | — | Voltage common decoupling |
| AGND1 | 27 | — | — | — | Analog ground 1 |
| RSV2 | 28 | — | — | — | Reserved, tied to analog ground |
| VOUT8+ | 29 | O | No | No | Positive analog output from DAC8 |
| VOUT8- | 30 | O | No | No | Negative analog output from DAC8 |
| VOUT7+ | 31 | O | No | No | Positive analog output from DAC7 |
| VOUT7- | 32 | O | No | No | Negative analog output from DAC7 |
| VOUT6+ | 33 | O | No | No | Positive analog output from DAC6 |
| VOUT6- | 34 | O | No | No | Negative analog output from DAC6 |
| VOUT5+ | 35 | O | No | No | Positive analog output from DAC5 |
| VOUT5- | 36 | O | No | No | Negative analog output from DAC5 |
| VOUT4+ | 37 | O | No | No | Positive analog output from DAC4 |
| VOUT4- | 38 | O | No | No | Negative analog output from DAC4 |
| VOUT3+ | 39 | O | No | No | Positive analog output from DAC3 |
| VOUT3- | 40 | O | No | No | Negative analog output from DAC3 |
| VOUT2+ | 41 | O | No | No | Positive analog output from DAC2 |
| VOUT2- | 42 | O | No | No | Negative analog output from DAC2 |
| VOUT1+ | 43 | O | No | No | Positive analog output from DAC1 |
| VOUT1- | 44 | O | No | No | Negative analog output from DAC1 |
| RSV2 | 45 | — | — | — | Reserved, tied to analog ground |
| AGND2 | 46 | — | — | — | Analog ground 2 |
| VCC2 | 47 | — | — | — | Analog power supply 2, +5 V |
| RSV2 | 48 | — | — | — | Reserved, tied to analog ground |

(1) Open-drain configuration in out mode.


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# 6 Specifications

## 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted).(1)

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage | VCC1, VCC2 | –0.3 | 6.5 | V |
| | VDD | –0.3 | 4 | V |
| Ground voltage differences | AGND1, AGND2, DGND | –0.1 | 0.1 | V |
| Supply voltage differences | VCC1, VCC2 | –0.1 | 0.1 | V |
| Digital input voltage | RST, TEST, MS, MC, MD, SCKI, AMUTEI, AMUTEO | –0.3 | 6.5 | V |
| | BCK, LRCK, DIN1/2/3/4, MODE, ZERO1, ZERO2 | –0.3 | (VDD + 0.3) < 4 | V |
| Analog input voltage | VCOM, VOUT1–8± | –0.3 | (VCC + 0.3) < 6.5 | V |
| Input current | (all pins except supplies) | –10 | 10 | mA |
| Ambient temperature under bias | | –40 | 125 | °C |
| Junction temperature | | | 150 | °C |
| Lead temperature | (soldering, 5s) | | 260 | °C |
| Package temperature | (IR reflow, peak) | | 260 | °C |
| Storage temperature | $T_{stg}$ | –55 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

| | | VALUE | UNIT |
|---|---|---|---|
| $V_{(ESD)}$ Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±1000 | V |
| | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±250 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Analog supply voltage, VCC | | 4.5 | 5 | 5.5 | V |
| Digital supply voltage, VDD | | 3 | 3.3 | 3.6 | V |
| Digital Interface | | | LVTTL compatible | | |
| Digital input clock frequency | Sampling frequency, LRCK | 8 | | 192 | kHz |
| | System clock frequency, SCKI | 2.048 | | 36.864 | MHz |
| Analog output voltage | Differential | | 8 | | $V_{PP}$ |
| Analog output load resistance | To AC-coupled GND | 5 | | | kΩ |
| | To DC-coupled GND | 15 | | | kΩ |
| Analog output load capacitance | | | | 50 | pF |
| Digital output load capacitance | | | | 20 | pF |
| Operating free-air temperature | PCM1690 consumer grade | –40 | 25 | 85 | °C |

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## 6.4 Thermal Information

| THERMAL METRIC(1) | | PCM1690 DCA (HTSSOP) 48 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 29.2 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 10.2 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 10.3 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.3 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 10.2 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 0.4 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Electrical Characteristics: Digital Input/Output

All specifications at $T_A$ = 25°C, VCC1 = VCC2 = 5 V, VDD = 3.3 V, $f_S$ = 48 kHz, SCKI = 512 $f_S$, 24-bit data, and Sampling Mode = Auto, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DATA FORMAT** | | | | | | |
| $f_S$ | Sampling frequency | | 8 | 48 | 192 | kHz |
| | System clock frequency | 128 $f_S$, 192 $f_S$, 256 $f_S$, 384 $f_S$, 512 $f_S$, 768 $f_S$, 1152 $f_S$ | 2.048 | | 36.864 | MHz |
| **INPUT LOGIC** | | | | | | |
| $V_{IH}$ | Input logic level, high (BCK, LRCK, and DIN (1) (2)) | | 2 | | VDD | VDC |
| $V_{IL}$ | Input logic level, low (BCK, LRCK, and DIN ((1) (2)) | | | | 0.8 | VDC |
| $V_{IH}$ | Input logic current, high (SCKI, ADR5/ADR1/RSV, MC/SCL/FMT, MD/SDA/DEMP, and AMUTEI (3)(4)) | | 2 | | 5.5 | VDC |
| $V_{IL}$ | Input logic current, low (SCKI, ADR5/ADR1/RSV, MC/SCL/FMT, MD/SDA/DEMP, and AMUTEI (3)(4)) | | | | 0.8 | VDC |
| $I_{IH}$ | Input logic current, high (SCKI, TEST/ADR1/RSV, MC/SCL/FMT, MD/SDA/DEMP, and AMUTEI (2)(3)) | $V_{IN}$ = VDD | | | ±10 | µA |
| $I_{IL}$ | Input logic current, low (SCKI, TEST/ADR1/RSV, MC/SCL/FMT, MD/SDA/DEMP, and AMUTEI (2) (3)) | $V_{IN}$ = 0 V | | | ±10 | µA |
| $I_{IH}$ | Input logic current, high (BCK, LRCK, REST, MSI/ADR0/RSV (1)(4)) | $V_{IN}$ = VDD | | 65 | 100 | µA |
| $I_{IL}$ | Input logic current, high (BCK, LRCK, REST, MSI/ADR0/RSV (1) (4)) | $V_{IN}$ = 0 V | | | ±10 | µA |
| **OUTPUT LOGIC** | | | | | | |
| $V_{OH}$ | Output logic level, high (ZERO1 and ZERO2(5)) | $I_{OUT}$ = –4 mA | 2.4 | | | VDC |
| $V_{OL}$ | Output logic level, low (ZERO1 and ZERO2(5) (6) ) | $I_{OUT}$ = +4 mA | | | 0.4 | VDC |
| **REFERENCE OUTPUT** | | | | | | |
| | VCOM output voltage | | | 0.5 × VCC1 | | V |
| | VCOM output impedance | | | 7.5 | | kΩ |
| | Allowable VCOM output source/sink current | | | | 1 | µA |

(1) BCK and LRCK (Schmitt trigger input with 50-kΩ typical internal pull-down resistor).
(2) DIN1/2/3/4 (Schmitt trigger input).
(3) SCKI, TEST/ADR1/RSV, MC/SCL/FMT, MD/SDA/DEMP, and AMUTEI (Schmitt trigger input, 5-V tolerant).
(4) RST and MS/ADR0/RSV (Schmitt trigger input with 50-kΩ typical internal pull-down resistor, 5-V tolerant).
(5) ZERO1 and ZERO2.
(6) SDA ($I^2C$ mode, open-drain low output) and AMUTEO (open-drain low output).


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## 6.6 Electrical Characteristics: DAC

All specifications at $T_A$ = 25°C, VCC1 = VCC2 = 5 V, VDD = 3.3 V, $f_S$ = 48 kHz, SCKI = 512 $f_S$, 24-bit data, and Sampling Mode = Auto, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **RESOLUTION** | | | 16 | 24 | | Bits |
| **DC ACCURACY** | | | | | | |
| | Gain mismatch channel-to-channel | | | ±2 | ±6 | % of FSR |
| | Gain error | | | ±2 | ±6 | % of FSR |
| | Bipolar zero error | | | ±1 | | % of FSR |
| **DYNAMIC PERFORMANCE**(1) (2) | | | | | | |
| THD+N | Total harmonic distortion + noise | $f_S$ = 48 kHz, $V_{OUT}$ = 0 dB | | –94 | –88 | dB |
| | | $f_S$ = 96 kHz, $V_{OUT}$ = 0 dB | | –94 | | dB |
| | | $f_S$ = 192 kHz, $V_{OUT}$ = 0 dB | | –94 | | dB |
| | Dynamic range | $f_S$ = 48 kHz, EIAJ, A-weighted | 106 | 113 | | dB |
| | | $f_S$ = 96 kHz, EIAJ, A-weighted | | 113 | | dB |
| | | $f_S$ = 192 kHz, EIAJ, A-weighted | | 113 | | dB |
| SNR | Sighnal-to-noise ratio | $f_S$ = 48 kHz, EIAJ, A-weighted | 106 | 113 | | dB |
| | | $f_S$ = 96 kHz, EIAJ, A-weighted | | 113 | | dB |
| | | $f_S$ = 192 kHz, EIAJ, A-weighted | | 113 | | dB |
| | Channel separation (between one channel and others) | $f_S$ = 48 kHz | 103 | 109 | | dB |
| | | $f_S$ = 96 kHz | | 109 | | dB |
| | | $f_S$ = 192 kHz | | 108 | | dB |
| **ANALOG OUTPUT** | | | | | | |
| | Output voltage | Differential | | 1.6 × VCC1 | | $V_{PP}$ |
| | Center voltage | | | 0.5 × VCC1 | | V |
| | Load impedance | To AC-coupled GND(3) | 5 | | | kΩ |
| | | To DC-coupled GND(3) | 15 | | | kΩ |
| | LPF frequency response | f = 20 kHz | | –0.04 | | dB |
| | | f = 44 kHz | | –0.18 | | dB |
| **DIGITAL FILTER PERFORMANCE WITH SHARP ROLL-OFF** | | | | | | |
| | Passband (single, dual) | Except SCKI = 128 $f_S$ and 192 $f_S$ | | | 0.454 × $f_S$ | Hz |
| | | SCKI = 128 $f_S$ and 192 $f_S$ | | | 0.432 × $f_S$ | Hz |
| | Passband (quad) | | | | 0.432 × $f_S$ | Hz |
| | Stop band (single, dual) | Except SCKI = 128 $f_S$ and 192 $f_S$ | 0.546 × $f_S$ | | | Hz |
| | | SCKI = 128 $f_S$ and 192 $f_S$ | 0.569 × $f_S$ | | | Hz |
| | Stop band (quad) | | 0.569 × $f_S$ | | | Hz |
| | Passband ripple | < 0.454 × $f_S$, 0.432 × $f_S$ | | | ±0.0018 | dB |
| | Stop band attenuation | > 0.546 × $f_S$, 0.569 × $f_S$ | –75 | | | dB |

(1) In differential mode at VOUTx± pin, $f_{OUT}$ = 1 kHz, using Audio Precision System II, Average mode with 20-kHz LPF and 400-Hz HPF.
(2) $f_S$ = 48 kHz: SCKI = 512 $f_S$ (single), $f_S$ = 96 kHz : SCKI = 256 $f_S$ (dual), $f_S$ = 192 kHz : SCKI = 128 $f_S$ (quad).
(3) Allowable minimum input resistance of differential to single-ended converter with D to S Gain = G is calculated as (1 + 2G)/(1 + G) × 5k for AC-coupled and (1+ 0.9G)/(1 + G) × 15k for DC-coupled connection; refer to Figure 39 and Figure 40 of the *Application Information* section.

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## Electrical Characteristics: DAC (continued)

All specifications at $T_A$ = 25°C, VCC1 = VCC2 = 5 V, VDD = 3.3 V, $f_S$ = 48 kHz, SCKI = 512 $f_S$, 24-bit data, and Sampling Mode = Auto, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **DIGITAL FILTER PERFORMANCE WITH SLOW ROLL-OFF** | | | | | |
| Passband | | | | 0.328 × $f_S$ | Hz |
| Stop band | | 0.673 × $f_S$ | | | Hz |
| Passband ripple | < 0.328 × $f_S$ | | | ±0.0013 | dB |
| Stop band attenuation | > 0.673 × $f_S$ | –75 | | | dB |
| **DIGITAL FILTER PERFORMANCE** | | | | | |
| Group delay time (single, dual) | Except SCKI = 128 $f_S$ and 192 $f_S$ | | 28/$f_S$ | | s |
| | SCKI = 128 $f_S$ and 192 $f_S$ | | 19/$f_S$ | | s |
| Group delay time (quad) | | | 19/$f_S$ | | s |
| De-emphasis error | | | ±0.1 | | dB |

## 6.7 Electrical Characteristics: Power-Supply Requirements

All specifications at $T_A$ = 25°C, VCC1 = VCC2 = 5 V, VDD = 3.3 V, $f_S$ = 48 kHz, SCKI = 512 $f_S$, 24-bit data, and Sampling Mode = Auto, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER-SUPPLY REQUIREMENTS** | | | | | | |
| VCC1/2 | Voltage range | | 4.5 | 5 | 5.5 | VDC |
| VDD | | | 3 | 3.3 | 3.6 | VDC |
| $I_{CC}$ | Supply current | $f_S$ = 48 kHz | | 74 | 110 | mA |
| | | $f_S$ = 192 kHz | | 74 | | mA |
| | | Full power-down (1) | | 170 | | µA |
| $I_{DD}$ | | $f_S$ = 48 kHz | | 57 | 90 | mA |
| | | $f_S$ = 192 kHz | | 76 | | mA |
| | | Full power-down (1) | | 60 | | µA |
| Power dissipation | | $f_S$ = 48 kHz $f_S$ = 192 kHz Full power-down (1) | | 558 | 847 | mW |
| | | | | 621 | | mW |
| | | | | 1.05 | | mW |
| **TEMPERATURE RANGE** | | | | | | |
| Operating temperature | | PCM1690 Consumer grade | –40 | | 85 | °C |

(1) SCKI, BCK, and LRCK stopped.

## 6.8 System Clock Timing Requirements

(see Figure 1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{SCY}$ | System clock cycle time | 27 | | ns |
| $t_{SCH}$ | System clock width high | 10 | | ns |
| $t_{SCL}$ | System clock width low | 10 | | ns |
| — | System clock duty cycle | 40% | 60% | |


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## 6.9 Audio Interface Timing Requirements for Left-Justified, Right-Justified, and I2S Data Formats

(see Figure 2)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{BCY}$ | BCK cycle time | 75 | | ns |
| $t_{BCH}$ | BCK pulse width high | 35 | | ns |
| $t_{BCL}$ | BCK pulse width low | 35 | | ns |
| $t_{LRS}$ | LRCK set-up time to BCK rising edge | 10 | | ns |
| $t_{LRH}$ | LRCK hold time to BCK rising edge | 10 | | ns |
| $t_{DIS}$ | DIN1/2/3/4 set-up time to BCK rising edge | 10 | | ns |
| $t_{DIH}$ | DIN1/2/3/4 hold time to BCK rising edge | 10 | | ns |

## 6.10 Audio Interface Timing Requirements for DSP and TDM Data Formats

(see Figure 3)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{BCY}$ | BCK cycle time | 40 | | ns |
| $t_{BCH}$ | BCK pulse width high | 15 | | ns |
| $t_{BCL}$ | BCK pulse width low | 15 | | ns |
| $t_{LRW}$ | LRCK pulse width high (DSP format) | $t_{BCY}$ | $t_{BCY}$ | |
| | LRCK pulse width high (TDM format) | $t_{BCY}$ | $1/f_S - t_{BCY}$ | |
| $t_{LRS}$ | LRCK set-up time to BCK rising edge | 10 | | ns |
| $t_{LRH}$ | LRCK hold time to BCK rising edge | 10 | | ns |
| $t_{DIS}$ | DIN1/2/3/4 set-up time to BCK rising edge | 10 | | ns |
| $t_{DIH}$ | DIN1/2/3/4 hold time to BCK rising edge | 10 | | ns |

## 6.11 Three-Wire Serial Control Interface Timing Requirements

(see Figure 4)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{MCY}$ | MC pulse cycle time | 100 | | ns |
| $t_{MCL}$ | MC low-level time | 40 | | ns |
| $t_{MCH}$ | MC high-level time | 40 | | ns |
| $t_{MHH}$ | MS high-level time | $t_{MCY}$ | | ns |
| $t_{MSS}$ | MS falling edge to MC rising edge | 30 | | ns |
| $t_{MSH}$ | MS rising edge from MC rising edge for LSB | 15 | | ns |
| $t_{MDH}$ | MD hold time | 15 | | ns |
| $t_{MDS}$ | MD set-up time | 15 | | ns |

## 6.12 SCL and SDA Control Interface Timing Requirements

(see Figure 5)

| | | STANDARD MODE | | FAST MODE | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $f_{SCL}$ | SCL clock frequency | | 100 | | 400 | kHz |
| $t_{BUF}$ | Bus free time between STOP and START condition | 4.7 | | 1.3 | | µs |
| $t_{LOW}$ | Low period of the SCL clock | 4.7 | | 1.3 | | µs |
| $t_{HI}$ | High period of the SCL clock | 4 | | 0.6 | | µs |
| $t_{S-SU}$ | Set-up time for START/Repeated START condition | 4.7 | | 0.6 | | µs |
| $t_{S-HD}$ | Hold time for START/Repeated START condition | 4.0 | | 0.6 | | µs |
| $t_{D-SU}$ | Data set-up time | 250 | | 100 | | ns |
| $t_{D-HD}$ | Data hold time | 0 | 3450 | 0 | 900 | ns |
| $t_{SCL-R}$ | Rise time of SCL signal | | 1000 | 20 + 0.1 $C_B$ | 300 | ns |

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## SCL and SDA Control Interface Timing Requirements (continued)

(see Figure 5)

| | | STANDARD MODE | | FAST MODE | | |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | UNIT |
| $t_{SCL-F}$ | Fall time of SCL signal | | 1000 | 20 + 0.1 $C_B$ | 300 | ns |
| $t_{SDA-R}$ | Rise time of SDA signal | | 1000 | 20 + 0.1 $C_B$ | 300 | ns |
| $t_{SDA-F}$ | Fall time of SDA signal | | 1000 | 20 + 0.1 $C_B$ | 300 | ns |
| $t_{P-SU}$ | Set-up time for STOP condition | 4 | | 0.6 | | µs |
| $t_{GW}$ | Allowable glitch width | | N/A | | 50 | |
| $C_B$ | Capacitive load for SDA and SCL line | | 400 | | 100 | pF |
| $V_{NH}$ | Noise margin at high level for each connected device (including hysteresis) | 0.2 × VDD | | 0.2 × VDD | | V |
| $V_{NL}$ | Noise margin at low level for each connected device (including hysteresis) | 0.1 × VDD | | 0.1 × VDD | | V |
| $V_{HYS}$ | Hysteresis of Schmitt trigger input | N/A | | 0.05 × VDD | | V |

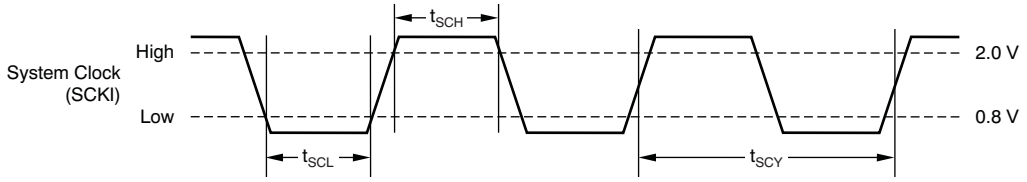



**Figure 1. System Clock Timing Requirements**

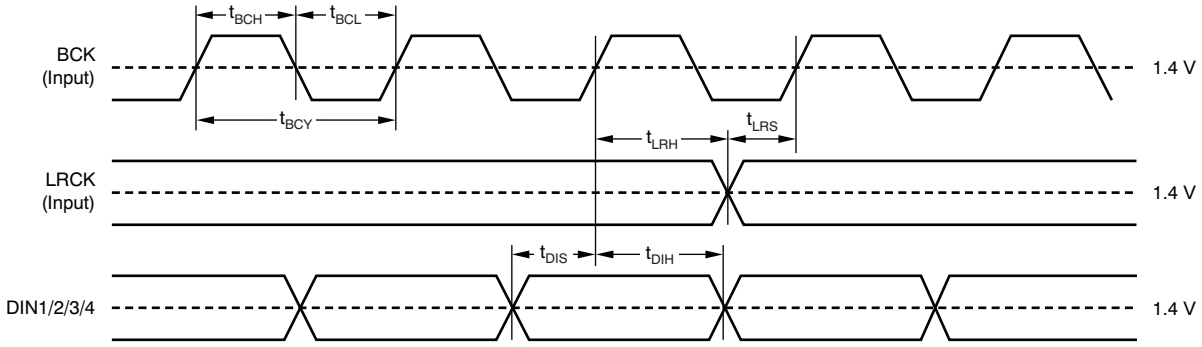



**Figure 2. Audio Interface Timing Requirements for Left-Justified, Right-Justified, and I²S Data Formats**

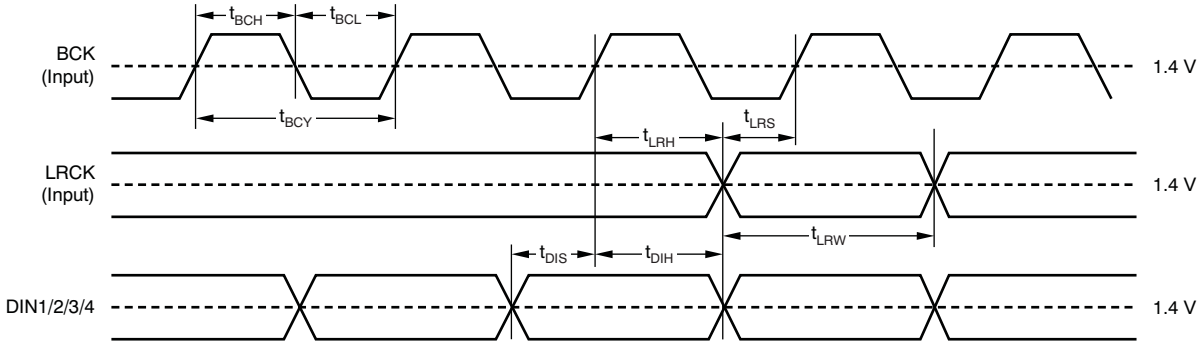



**Figure 3. Audio Interface Timing Requirements for DSP and TDM Data Formats**


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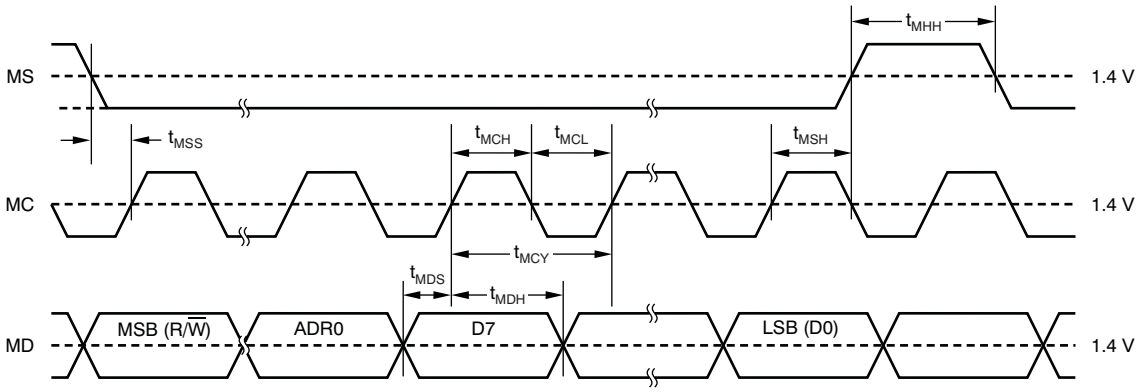



**Figure 4. Three-Wire Serial Control Interface Timing**

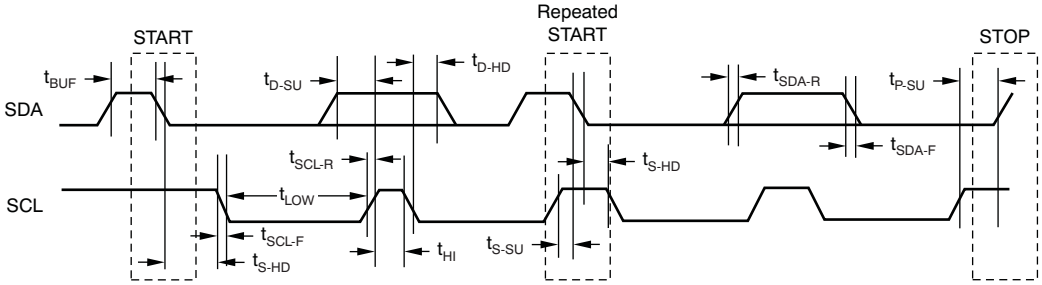



**Figure 5. SCL and SDA Control Interface Timing**

## 6.13 Typical Characteristics

### 6.13.1 Digital Filter

All specifications at $T_A$ = 25°C, VCC1 = VCC2 = 5 V, VDD = 3.3 V, $f_S$ = 48 kHz, SCKI = 512 $f_S$, 24-bit data, and Sampling Mode = Auto, unless otherwise noted.

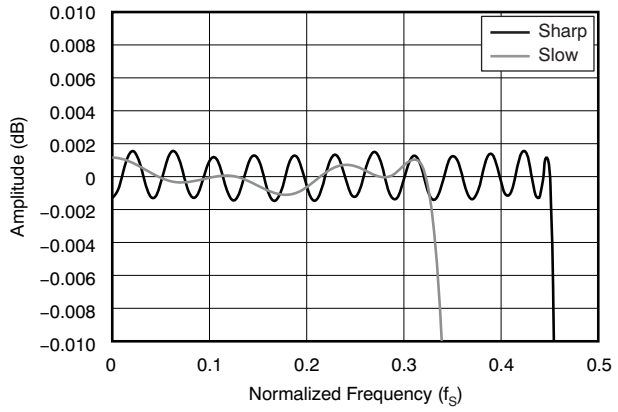



**Figure 6. Frequency Response Passband (Single Rate)**

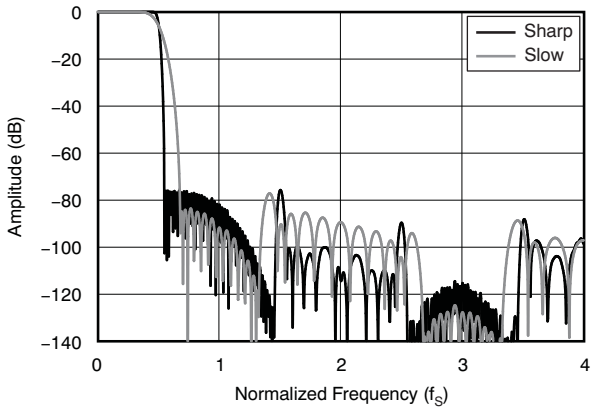



**Figure 7. Frequency Response (Dual Rate)**

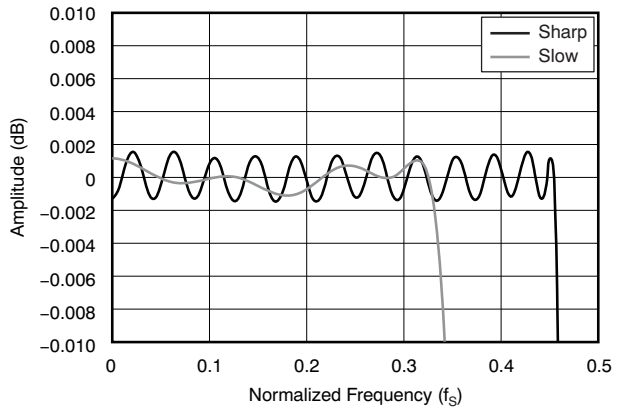



**Figure 8. Frequency Response Passband (Dual Rate)**

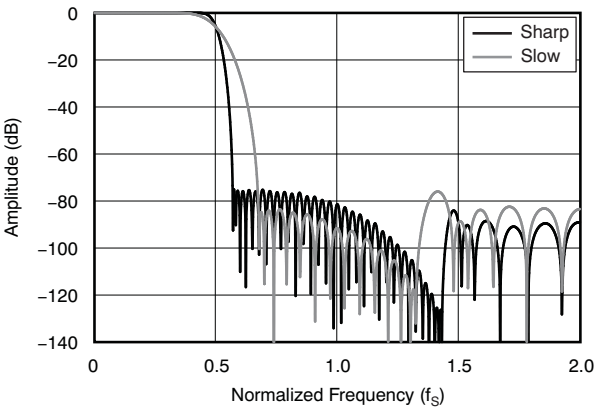



**Figure 9. Frequency Response (Quad Rate)**


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## Digital Filter (continued)

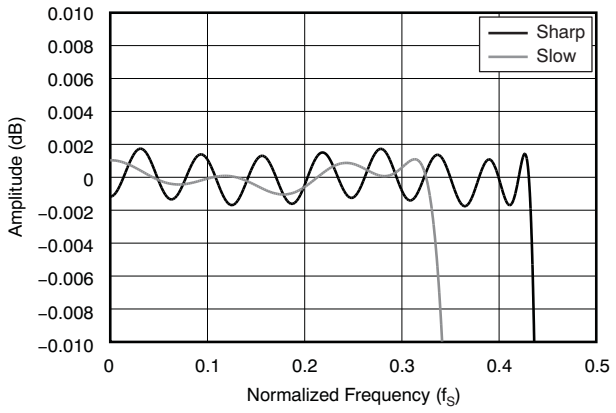
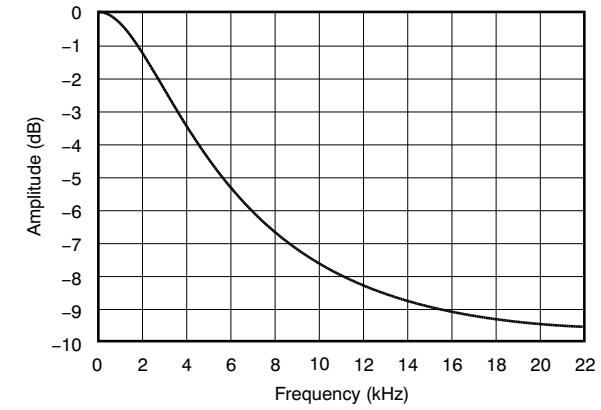



**Figure 10. Frequency Response Passband (Quad Rate)**

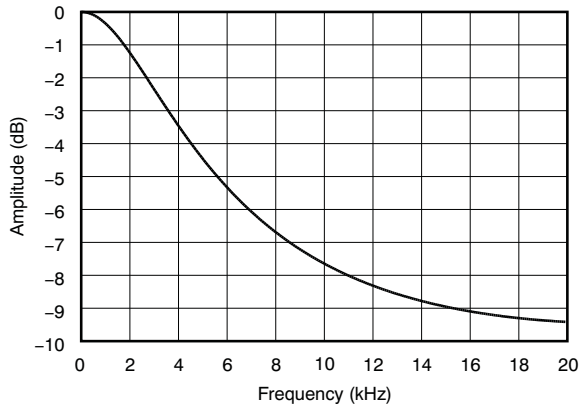
### 6.13.2 Digital De-Emphasis Filter

All specifications at $T_A$ = 25°C, VCC1 = VCC2 = 5 V, VDD = 3.3 V, $f_S$ = 48 kHz, SCKI = 512 $f_S$, 24-bit data, and Sampling Mode = Auto, unless otherwise noted.




$f_S$ = 48 kHz

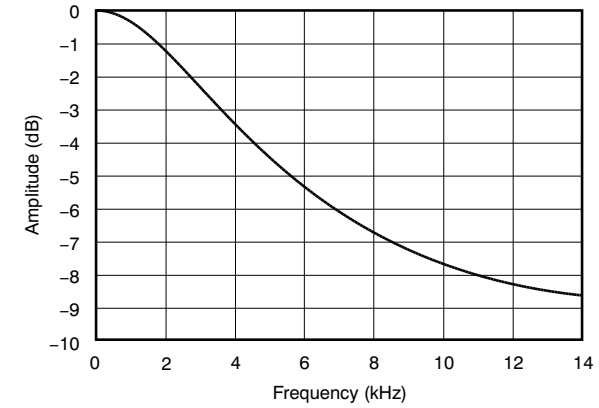
**Figure 11. De-emphasis Characteristic**




$f_S$ = 44.1 kHz

**Figure 12. De-emphasis Characteristic**

## Digital De-Emphasis Filter (continued)




$f_S$ = 32 kHz

**Figure 13. De-emphasis Characteristic**

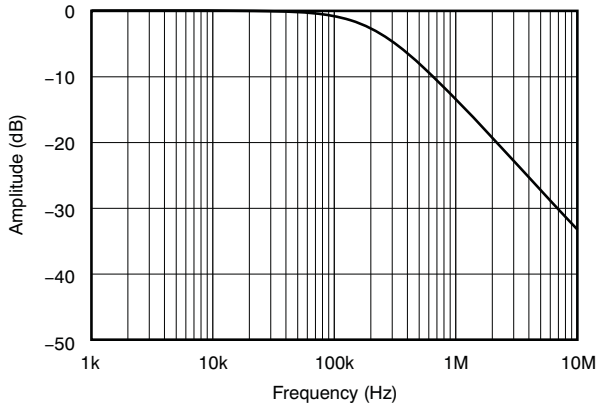



**Figure 14. Analog Filter Characteristic**


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### 6.13.3 Dynamic Performance

All specifications at $T_A$ = 25°C, VCC1 = VCC2 = 5 V, VDD = 3.3 V, $f_S$ = 48 kHz, SCKI = 512 $f_S$, 24-bit data, and Sampling Mode = Auto, unless otherwise noted.

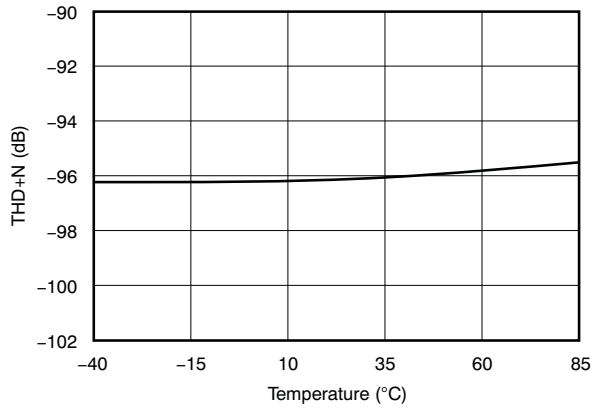



**Figure 15. THD+N vs Temperature**

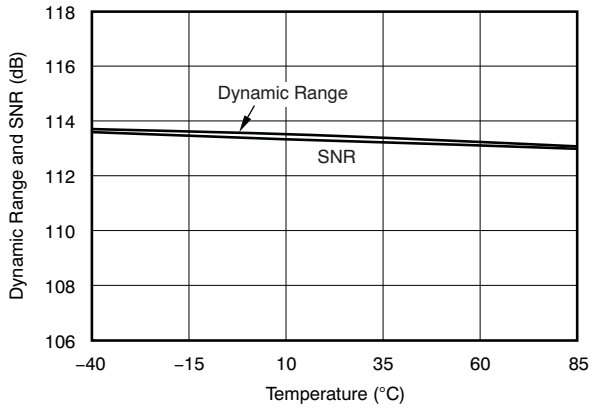



**Figure 16. Dynamic Range and SNR vs Temperature**

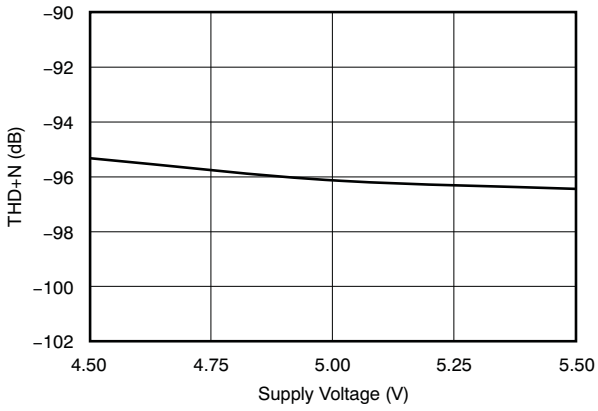



**Figure 17. THD+N vs Supply Voltage**

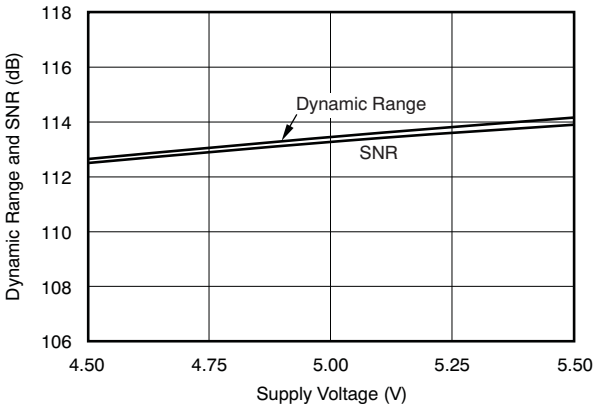
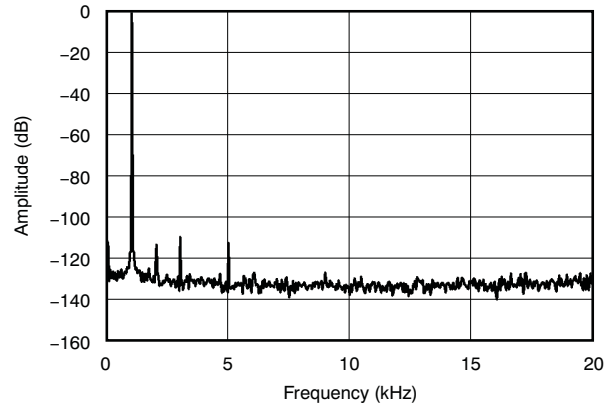



**Figure 18. Dynamic Range and SNR vs Supply Voltage**

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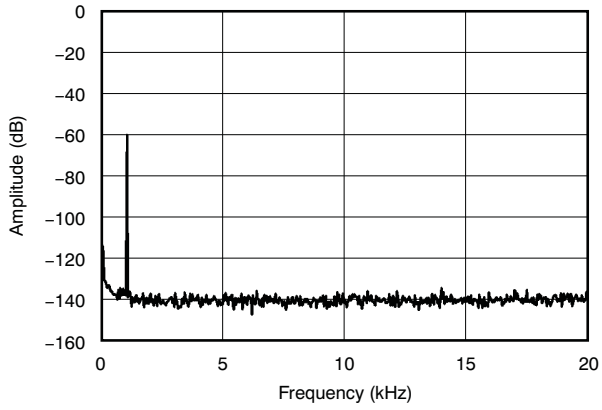
### 6.13.4 Output Spectrum

All specifications at $T_A$ = 25°C, VCC1 = VCC2 = 5 V, VDD = 3.3 V, $f_S$ = 48 kHz, SCKI = 512 $f_S$, 24-bit data, and Sampling Mode = Auto, unless otherwise noted.



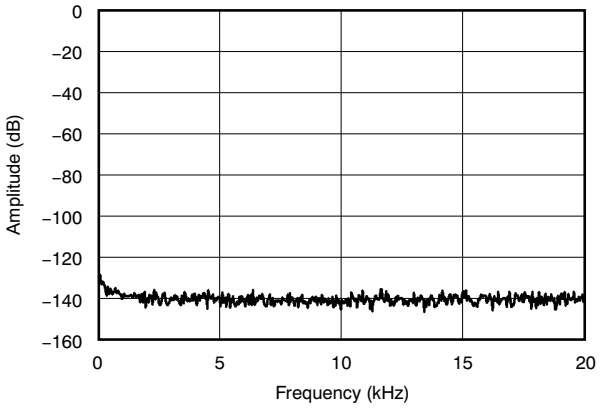

0 dB, N = 32768

**Figure 19. Output Spectrum**




–60 dB, N = 32768

**Figure 20. Output Spectrum**




BPZ, N = 32768

**Figure 21. Output Spectrum**


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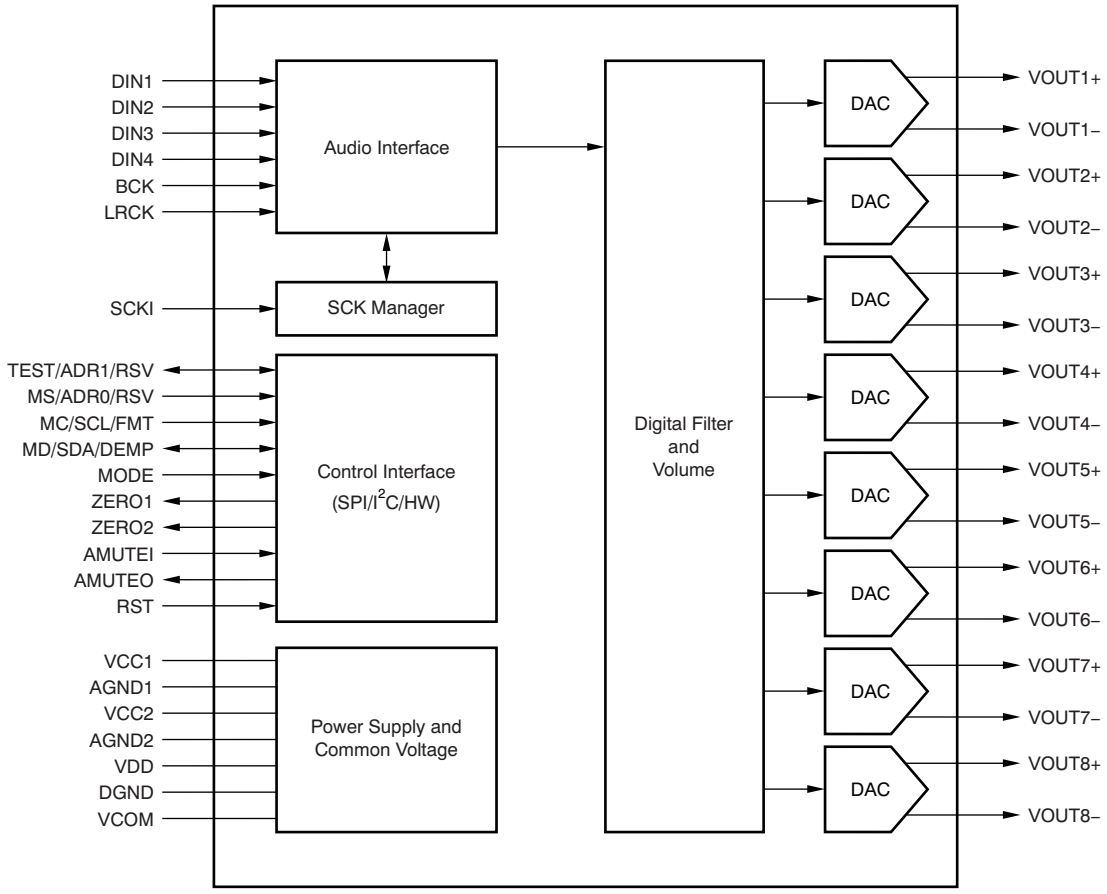
# 7 Detailed Description

## 7.1 Overview

The PCM1690 is a high-performance, multi-channel DAC targeted for consumer audio applications such as Blu-ray DVD players and HD DVD players, as well as home multi-channel audio applications (such as home theaters and A/V receivers). The PCM1690 consists of an eight-channel DAC. The DAC output type is fixed with a differential configuration. The PCM1690 supports 16-/20-/24-/32-bit linear PCM input data in $I^2S$- and left-justified audio formats, and 24-bit linear PCM input data in right-justified, DSP, and TDM formats for various sampling frequencies from 8 kHz to 192 kHz. The TDM format is useful for saving bus line interface numbers for multi-channel audio data communication between the DAC and a digital audio processor. The PCM1690 offers three modes for device control: two-wire $I^2C$ software, three-wire SPI software, and hardware modes.

- **Audio data interface formats:** $I^2S$, LJ, RJ, DSP, TDM
- **Audio data word length:** 16, 20, 24, 32 Bits
- **Audio data format:** MSB first, twos complement

## 7.2 Functional Block Diagram




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## 7.3 Feature Description

### 7.3.1 Analog Outputs

The PCM1690 includes eight DACs, each with individual pairs of differential voltage outputs pins. The full-scale output voltage is (1.6 × VCC1) $V_{PP}$ at the differential output mode. A DC-coupled load is allowed in addition to an AC-coupled load if the load resistance conforms to the specification. These balanced outputs are each capable of driving 0.8 VCC1 (4 $V_{PP}$) typical into a 5-kΩ, AC-coupled or 15-kΩ, DC-coupled load with VCC1 = +5 V. The internal output amplifiers for VOUT1 through VOUT8 are biased to the DC common voltage, equal to (0.5 × VCC1).

The output amplifiers include an RC continuous-time filter that helps to reduce the out-of-band noise energy present at the DAC outputs as a result of the noise shaping characteristics of the PCM1690 delta-sigma (ΔΣ) DACs. The frequency response of this filter is shown in the *Analog Filter Characteristic* (Figure 14). By itself, this filter is not enough to attenuate the out-of-band noise to an acceptable level for most applications. An external lowpass filter is required to provide sufficient out-of-band noise rejection. Further discussion of DAC post-filter circuits is provided in the *Application Information* section.

**Table 1. Pin Assignments in Differential Output Mode**

| DIGITAL INPUT | CHANNEL | DIFFERENTIAL OUTPUT |
|---|---|---|
| DIN1 | 1 (DAC1) | VOUT1+, VOUT1– |
| | 2 (DAC2) | VOUT2+, VOUT2– |
| DIN2 | 3 (DAC3) | VOUT3+, VOUT3– |
| | 4 (DAC4) | VOUT4+, VOUT4– |
| DIN3 | 5 (DAC5) | VOUT5+, VOUT5– |
| | 6 (DAC6) | VOUT6+, VOUT6– |
| DIN4 | 7 (DAC7) | VOUT7+, VOUT7– |
| | 8 (DAC8) | VOUT8+, VOUT8– |

### 7.3.2 Voltage Reference VCOM

The PCM1690 includes a pin for the common-mode voltage output, VCOM. This pin must be connected to the analog ground through a decoupling capacitor. This pin can also be used to bias external high-impedance circuits, if they are required.

### 7.3.3 System Clock Input

The PCM1690 requires an external system clock input applied at the SCKI input for DAC operation. The system clock operates at an integer multiple of the sampling frequency, or $f_S$. The multiples supported in DAC operation include 128 $f_S$, 192 $f_S$, 256 $f_S$, 384 $f_S$, 512 $f_S$, 768 $f_S$, and 1152 $f_S$. Details for these system clock multiples are shown in Table 2. Figure 1 and *System Clock Timing Requirements* show the SCKI timing requirements.

**Table 2. System Clock Frequencies for Common Audio Sampling Rates**

| DEFAULT SAMPLING MODE | SAMPLING FREQUENCY | SYSTEM CLOCK FREQUENCY (MHz) | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | $f_S$ (kHz) | 128 $f_S$ | 192 $f_S$ | 256 $f_S$ | 384 $f_S$ | 512 $f_S$ | 768 $f_S$ | 1152 $f_S$ |
| Single rate | 8 | N/A | N/A | 2.0480 | 3.0720 | 4.0960 | 6.1440 | 9.2160 |
| | 16 | 2.0480 | 3.0720 | 4.0960 | 6.1440 | 8.1920 | 12.2880 | 18.4320 |
| | 32 | 4.0960 | 6.1440 | 8.1920 | 12.2880 | 16.3840 | 24.5760 | 36.8640 |
| | 44.1 | 5.6448 | 8.4672 | 11.2896 | 16.9344 | 22.5792 | 33.8688 | N/A |
| | 48 | 6.1440 | 9.2160 | 12.2880 | 18.4320 | 24.5760 | 36.8640 | N/A |
| Dual rate | 88.2 | 11.2896 | 16.9344 | 22.5792 | 33.8688 | N/A | N/A | N/A |
| | 96 | 12.2880 | 18.4320 | 24.5760 | 36.8640 | N/A | N/A | N/A |
| Quad rate | 176.4 | 22.5792 | 33.8688 | N/A | N/A | N/A | N/A | N/A |
| | 192 | 24.5760 | 36.8640 | N/A | N/A | N/A | N/A | N/A |


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### 7.3.4 Sampling Mode

The PCM1690 supports three sampling modes (single rate, dual rate, and quad rate) in DAC operation. In single rate mode, the DAC operates at an oversampling frequency of x128 (except when SCKI = 128 $f_S$ and 192 $f_S$). This mode is supported for sampling frequencies less than 50 kHz. In dual rate mode, the DAC operates at an oversampling frequency of x64; this mode is supported for sampling frequencies less than 100 kHz. In quad rate mode, the DAC operates at an oversampling frequency of x32. The sampling mode is automatically selected according to the ratio of system clock frequency and sampling frequency by default (that is, single rate for 512 $f_S$, 768 $f_S$, and 1152 $f_S$; dual rate for 256 $f_S$ and 384 $f_S$; and quad rate for 128 $f_S$ and 192 $f_S$), but manual selection is also possible for specified combinations through the serial mode control register.

Table 3 and Figure 22 show the relation among the oversampling rate (OSR) of the digital filter and ΔΣ modulator, the noise-free shaped bandwidth, and each sampling mode setting.

**Table 3. DAC Filter OSR, Modulator OSR, and Noise-Free Shaped Bandwidth for Each Sampling Mode**

| SAMPLING MODE REGISTER SETTING | SYSTEM CLOCK FREQUENCY ($xf_S$) | NOISE-FREE SHAPED BANDWIDTH (kHz)(1) | | | DIGITAL FILTER OSR | MODULATOR OSR |
|---|---|---|---|---|---|---|
| | | $f_S$ = 48 kHz | $f_S$ = 96 kHz | $f_S$ = 192 kHz | | |
| Auto | 512, 768, 1152 | 40 | N/A | N/A | ×8 | x128 |
| | 256, 384 | 20 | 40 | N/A | x8 | x64 |
| | 128, 192(2) | 10 | 20 | 40 | x4 | x32 |
| Single | 512, 768, 1152 | 40 | N/A | N/A | x8 | x128 |
| | 256, 384 | 40 | N/A | N/A | x8 | x128 |
| | 128, 192(2) | 20 | N/A | N/A | x4 | x64 |
| Dual | 256, 384 | 20 | 40 | N/A | x8 | x64 |
| | 128, 192(2) | 20 | 40 | N/A | x4 | x64 |
| Quad | 128, 192(2) | 10 | 20 | 40 | x4 | x32 |

(1) Bandwidth in which noise is shaped out.
(2) Quad mode filter characteristic is applied.

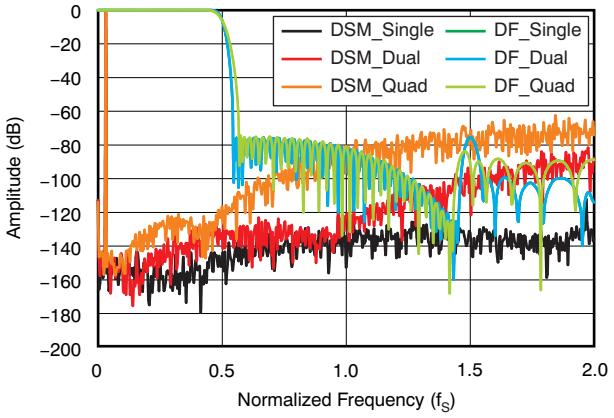



**Figure 22. ΔΣ Modulator and Digital Filter Characteristic**

### 7.3.5 Reset Operation

The PCM1690 has both an internal power-on reset circuit and an external reset circuit. The sequences for both reset circuits are shown in Figure 23 and Figure 24. Figure 23 describes the timing at the internal power-on reset. Initialization is triggered automatically at the point where VDD exceeds 2.2 V typical, and the internal reset is released after 3846 SCKI clock cycles from power-on if RST is held high and SCKI is provided. VOUT from the DACs are forced to the VCOM level initially (that is, 0.5 × VCC1) and settle at a specified level according to the rising VCC. If synchronization among SCKI, BCK, and LRCK is maintained, VOUT provides an output that corresponds to DIN after 3846 SCKI clocks from power-on. If the synchronization is not held, the internal reset is not released, and both operating modes are maintained at reset and power-down states; after synchronization forms again, the DAC returns to normal operation with the previous sequences.

Figure 24 shows a timing diagram at the external reset. RST accepts an externally-forced reset with RST low, and provides a device reset and power-down state that achieves the lowest power dissipation state available in the PCM1690. If RST goes from high to low under synchronization among SCKI, BCK, and LRCK, the internal reset is asserted, all registers and memory are reset, and finally the PCM1690 enters into all power-down states. At the same time, VOUT is immediately forced into the AGND1 level. To begin normal operation again, toggle RST high; the same power-up sequence is performed as the power-on reset shown in Figure 23.

The PCM1690 does not require particular power-on sequences for VCC and VDD; it allows VDD on and then VCC on, or VCC on and then VDD on. From the viewpoint of the *Absolute Maximum Ratings* , however, simultaneous power-on is recommended for avoiding unexpected responses on VOUTx. Figure 23 shows the response for VCC on with VDD on.

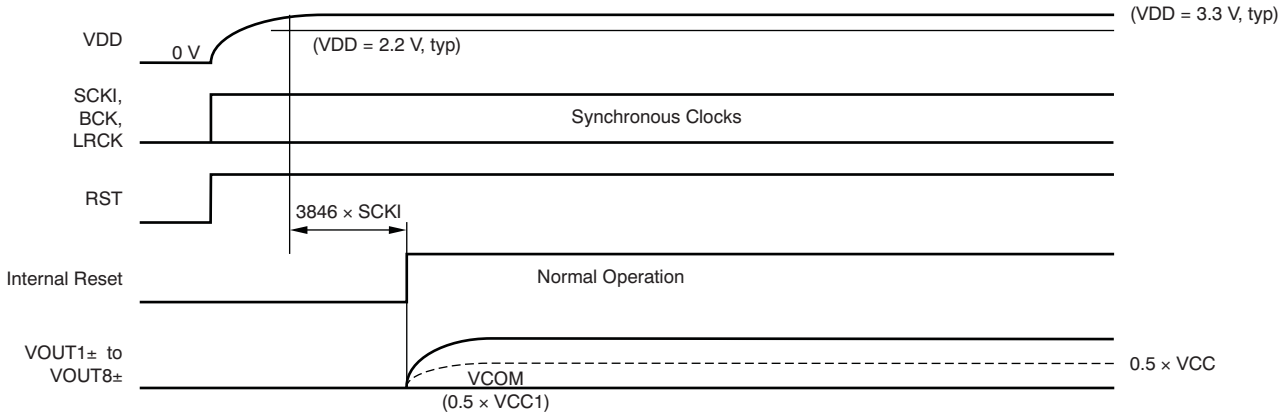



**Figure 23. Power-On-Reset Timing Requirements**

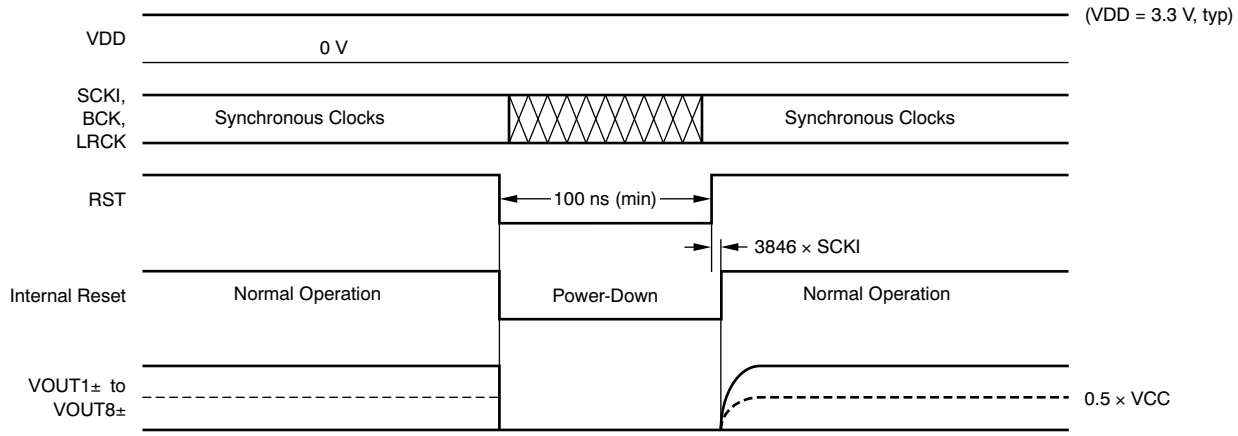



**Figure 24. External Reset Timing Requirements**


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### 7.3.6 Zero Flag

The PCM1690 has two ZERO flag pins (ZERO1 and ZERO2) that can be assigned to the combinations shown in Table 4. Zero flag combinations are selected through control register settings. If the input data of the left and right channel of all assigned channels remain at '0' for 1024 sampling periods (LRCK clock periods), the ZERO1/2 bits are set to a high level, logic '1' state. Furthermore, if the input data of any channels of assigned channels read '1', the ZERO1/2 are set to a low level, logic '0' state, immediately. Zero data detection is supported for 16-/20-/24-bit data width, but is not supported for 32-bit data width.

The active polarity of the zero flag output can be inverted through control register settings. The reset default is active high for zero detection. In parallel hardware control mode, ZERO1 and ZERO2 are fixed with combination *A* shown in Table 4.

**Table 4. Zero Flag Outputs Combination**

| ZERO FLAG COMBINATION | ZERO1 | ZERO2 |
|---|---|---|
| A | DATA1, left channel | DATA1, right channel |
| B | DATA1–4 | DATA1–4 |
| C | DATA4 | DATA1–3 |
| D | DATA1 | DATA2–4 |

### 7.3.7 AMUTE Control

The PCM1690 has an AMUTE control input, status output pins, and functionality. AMUTEI is the input control pin of the internal analog mute circuit. An AMUTEI low input causes the DAC output to cut-off from the digital input and forces it to the center level (0.5 VCC1). AMUTEO is the status output pin of the internal analog mute circuit. AMUTEO low indicates the analog mute control circuit is active because of a programmed condition (such as an SCKI halt, asynchronous detect, zero detect, or issue with the DAC disable command) that forces the DAC outputs to a center level. Because AMUTEI is not terminated internally and AMUTEO is an open-drain output, pull-ups by the appropriate resistors are required for proper operation.

Additionally, because the AMUTEI pin control and power-down control in register (OPEDA when high, PSMDA when low) do not function together, AMUTEI takes priority over power-down control. Therefore, power-down control is ignored during AMUTEI low, and AMUTEI low forces the DAC output to a center level (0.5 VCC1) even if the power-down control is asserted.

### 7.3.8 Three-Wire (SPI) Serial Control

The PCM1690 includes an SPI-compatible serial port that operates asynchronously with the audio serial interface. The control interface consists of MD/SDA/DEMP, MC/SCL/FMT, and MS/ADR0/RSV. MD is the serial data input to program the mode control registers. MC is the serial bit clock that shifts the data into the control port. MS is the select input to enable the mode control port.

### 7.3.9 Control Data Word Format

All single write operations via the serial control port use 16-bit data words. Figure 25 shows the control data word format. The first bit (fixed at '0') is for write controls; after the first bit are seven other bits, labeled ADR[6:0] that set the register address for the write operation. The eight least significant bits (LSBs), D[7:0] on MD, contain the data to be written to the register specified by ADR[6:0].

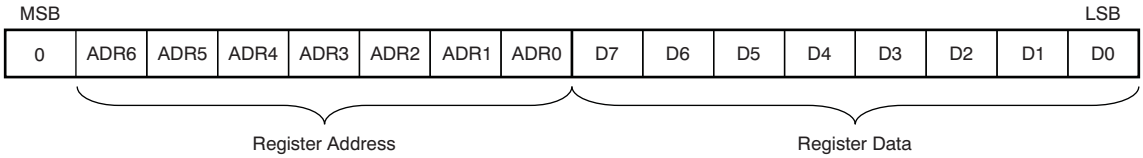
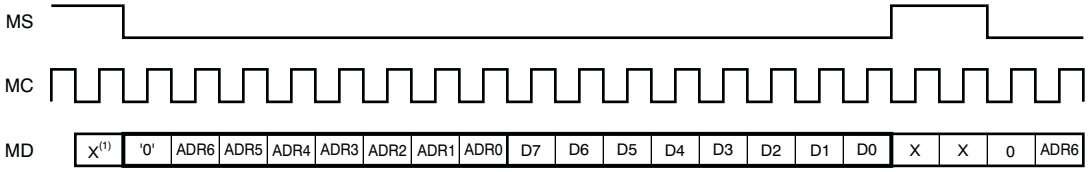



**Figure 25. Control Data Word Format for MD**

### 7.3.10 Register Write Operation

Figure 26 shows the functional timing diagram for single write operations on the serial control port. MS is held at a high state until a register is to be written. To start the register write cycle, MS is set to a low state. 16 clocks are then provided on MC, corresponding to the 16 bits of the control data word on MD. After the 16th clock cycle has been completed, MS is set high to latch the data into the indexed mode control register.

Also, the PCM1690 supports multiple write operations in addition to single write operations, which can be performed by sending the following N-times of the 8-bit register data after the first 16-bit register address and register data while keeping the MC clocks and MS at a low state. Closing a multiple write operation can be accomplished by setting MS to a high state.




(1) X = don't care.

**Figure 26. Register Write Operation**

### 7.3.11 Two-Wire ($I^2C$) Serial Control

The PCM1690 supports an $I^2C$-compatible serial bus and data transmission protocol for fast mode configured as a slave device. This protocol is explained in the $I^2C$ specification 2.0.

The PCM1690 has a 7-bit slave address, as shown in Figure 27. The first five bits are the most significant bits (MSB) of the slave address and are factory-preset to 10011. The next two bits of the address byte are selectable bits that can be set by MS/ADR0/RSV and TEST/ADR1/RSV. A maximum of four PCM1690s can be connected on the same bus at any one time. Each PCM1690 responds when it receives its own slave address.

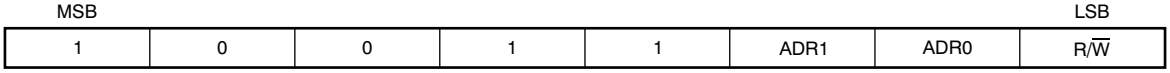
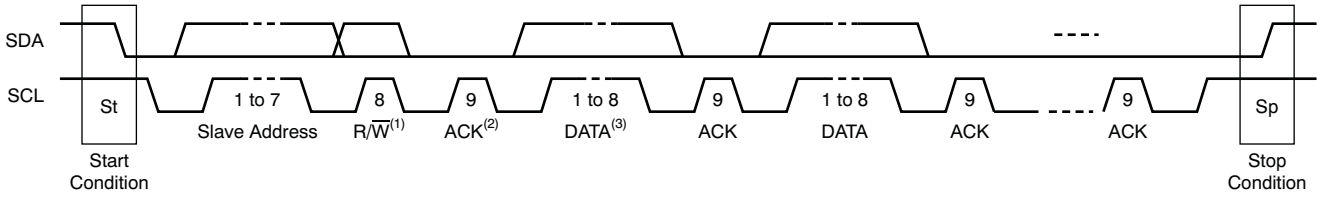



**Figure 27. Slave Address**


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### 7.3.12 Packet Protocol

A master device must control the packet protocol, which consists of a start condition, slave address with the read/write bit, data if a write operation is required, acknowledgment if a read operation is required, and stop condition. The PCM1690 supports both slave receiver and transmitter functions. Details about DATA for both write and read operations are described in Figure 28.




(1) R/$\overline{W}$: Read operation if '1'; write operation otherwise.

(2) ACK: Acknowledgment of a byte if '0', not Acknowledgment of a byte if '1'.

(3) DATA: Eight bits (byte); details are described in the *Write Operation* and *Read Operation* sections.

**Figure 28. $I^2C$ Packet Control Protocol**

### 7.3.13 Write Operation

The PCM1690 supports a receiver function. A master device can write to any PCM1690 register using single or multiple accesses. The master sends a PCM1690 slave address with a write bit, a register address, and the data. If multiple access is required, the address is that of the starting register, followed by the data to be transferred. When valid data are received, the index register automatically increments by one. When the register address reaches &h4F, the next value is &h40. When undefined registers are accessed, the PCM1690 does not send an acknowledgment. Figure 29 shows a diagram of the write operation. The register address and write data are in 8-bit, MSB-first format.

| Transmitter | M | M | M | S | M | S | M | S | M | S | | S | M |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Data Type | St | Slave Address | $\overline{W}$ | ACK | Reg Address | ACK | Write Data 1 | ACK | Write Data 2 | ACK | | ACK | Sp |

NOTE: M = Master device, S = Slave device, St = Start condition, $\overline{W}$ = Write, ACK = Acknowledge, and Sp = Stop condition.

**Figure 29. Framework for Write Operation**

### 7.3.14 Read Operation

A master device can read the registers of the PCM1690. The value of the register address is stored in an indirect index register in advance. The master sends the PCM1690 slave address with a read bit after storing the register address. Then the PCM1690 transfers the data that the index register points to. Figure 30 shows a diagram of the read operation.

| Transmitter | M | M | M | S | M | S | M | M | M | S | S | M | M |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Data Type | St | Slave Address | $\overline{W}$ | ACK | Reg Address | ACK | Sr | Slave Address | R | ACK | Read Data | NACK | Sp |

NOTE: M = Master device, S = Slave device, St = Start condition, Sr = Repeated start condition, $\overline{W}$ = Write, R = Read, ACK = Acknowledge, NACK = Not acknowledge, and Sp = Stop condition.

NOTE: The slave address after the repeated start condition must be the same as the previous slave address.

**Figure 30. Framework for Read Operation**

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### 7.3.15 Timing Requirements: SCL and SDA

A detailed timing diagram for SCL and SDA is shown in Figure 5.

## 7.4 Device Functional Modes

### 7.4.1 Audio Serial Port Operation

The PCM1690 audio serial port consists of six signals: BCK, LRCK, DIN1, DIN2, DIN3, and DIN4. BCK is a bit clock input. LRCK is a left/right word clock input or frame synchronization clock input. DIN1/2/3/4 are the audio data inputs for VOUT1–8.

### 7.4.2 Audio Data Interface Formats and Timing

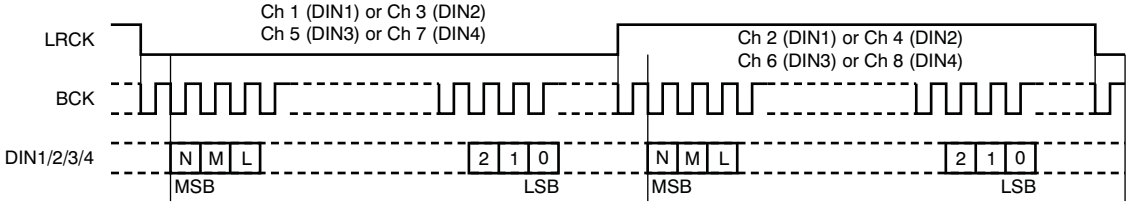
The PCM1690 supports 10 audio data interface formats: 16-/20-/24-/32-bit $I^2S$, 16-/20-/24-/32-bit left-justified, 24-bit right-justified, 16-bit right-justified, 24-bit left-justified mode DSP, 24-bit $I^2S$ mode DSP, 24-bit left-justified mode TDM, 24-bit $I^2S$ mode TDM, 24-bit left-justified mode high-speed TDM, and 24-bit $I^2S$ mode high-speed TDM. In the case of $I^2S$, left-justified, and right-justified data formats, 64 BCKs, 48 BCKs, and 32 BCKs per LRCK period are supported; but 48 BCKs are limited in 192/384/768 $f_S$ SCKI, and 32 BCKs are limited in 16-bit right-justified only. In the case of TDM data format in single rate, BCK, LRCK, and DIN1 are used. In the case of TDM data format in dual rate, BCK, LRCK, and DIN1/2 are used. In the case of high-speed TDM format in dual rate, BCK, LRCK, and DIN1 are used. In the case of high-speed TDM format in quad rate, BCK, LRCK, and DIN1/2 are used. TDM format and high-speed TDM format are supported only at SCKI = 512 $f_S$, 256 $f_S$, 128 $f_S$, and $f_{BCK} \le f_{SCKI}$. The audio data formats are selected by MC/SCL/FMT in hardware control mode and by control register settings in software control mode. All data must be in binary twos complement and MSB first.

Table 5 summarizes the applicable formats and describes the relationships among them and the respective restrictions with mode control. Figure 31 through Figure 37 show 10 audio interface data formats.

**Table 5. Audio Data Interface Formats and Sampling Rate, Bit Clock, and System Clock Restrictions**

| CONTROL MODE | FORMAT | DATA BITS | MAX LRCK FREQUENCY ($f_S$) | SCKI RATE ($xf_S$) | BCK RATE ($xf_S$) | APPLICABLE PINS |
|---|---|---|---|---|---|---|
| Software control | $I^2S$/Left-Justified | 16/20/24/32(1) | 192 kHz | 128 to 1152(2) | 64, 48 | DIN1/2/3/4 |
| | Right-Justified | 24, 16 | 192 kHz | 128 to 1152(2) | 64, 48, 32 (16 bit)(3) | DIN1/2/3/4 |
| | $I^2S$/Left-Justified DSP | 24 | 192 kHz | 128 to 768 | 64 | DIN1/2/3/4 |
| | $I^2S$/ Left-Justified TDM | 24 | 48 kHz | 256, 512 | 256 | DIN1 |
| | | 24 | 96 kHz | 128, 256 | 128 | DIN1/2 |
| | High-Speed $I^2S$/Left-Justified TDM | 24 | 96 kHz | 256 | 256 | DIN1 |
| | | 24 | 192 kHz | 128 | 128 | DIN1/2 |
| Hardware control | $I^2S$ | 16/20/24/32(1) | 192 kHz | 128 to 1152(2) | 64, 48 | DIN1/2/3/4 |
| | $I^2S$ TDM | 24 | 48 kHz | 512 | 256 | DIN1 |
| | | 24 | 96 kHz | 256 | 128 | DIN1/2 |

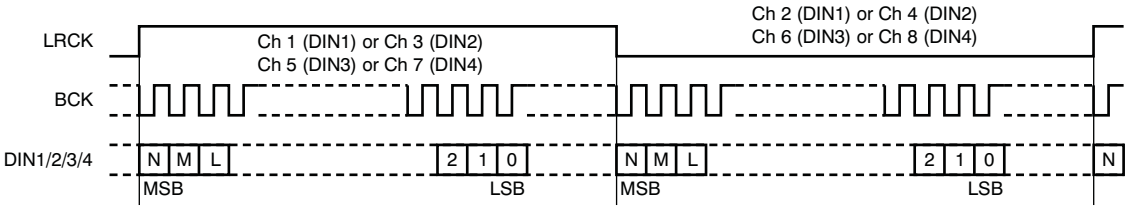
(1) 32-bit data length is acceptable only for BCK = 64 $f_S$ and when using $I^2S$ and Left-Justified format.
(2) 1152 $f_S$ is acceptable only for $f_S$ = 32 kHz, BCK = 64 $f_S$, and when using $I^2S$, Left-Justified, and 24-bit Right-Justified format.
(3) BCK = 32 $f_S$ is supported only for 16-bit data length.




N = 15/19/23/31, M = 14/18/22/30, and L = 13/17/21/29

**Figure 31. Audio Data Format: 16-/20-/24-/32-Bit $I^2S$**


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N = 15/19/23/31, M = 14/18/22/30, and L = 13/17/21/29

**Figure 32. Audio Data Format: 16-/20-/24-/32-Bit Left-Justified**

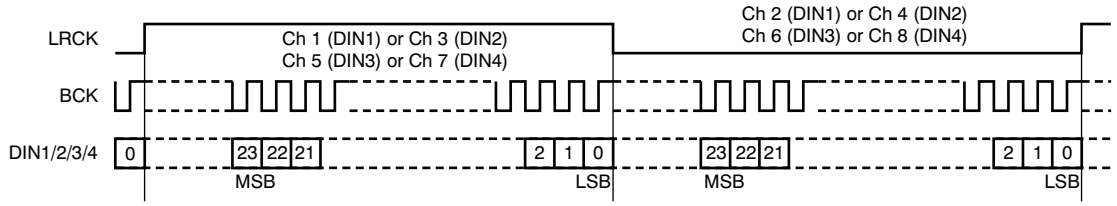



**Figure 33. Audio Data Format: 24-Bit Right-Justified**

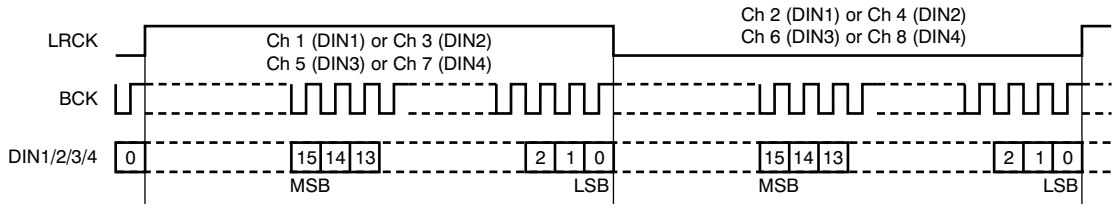



**Figure 34. Audio Data Format: 16-Bit Right-Justified**

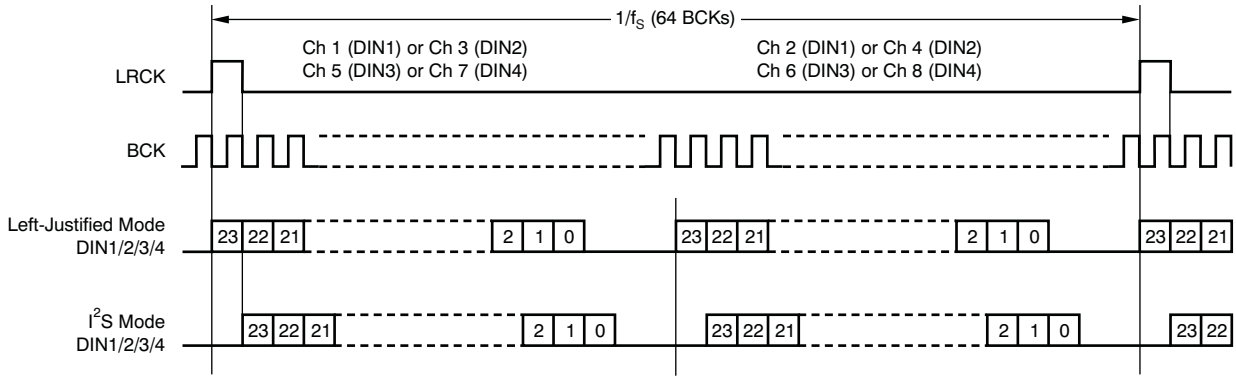
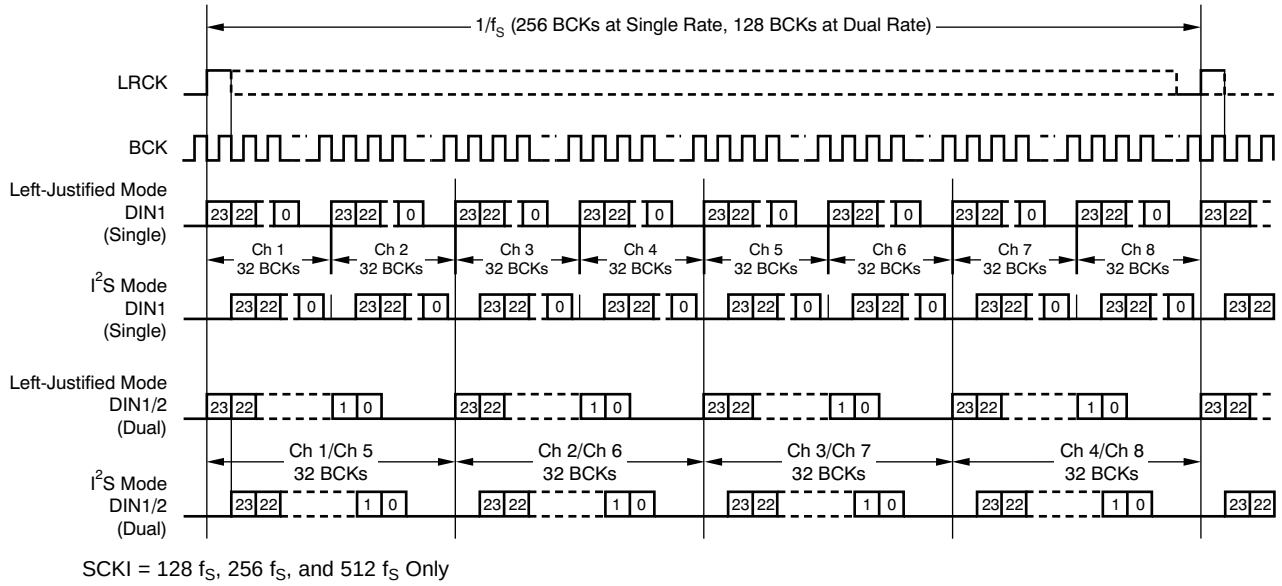
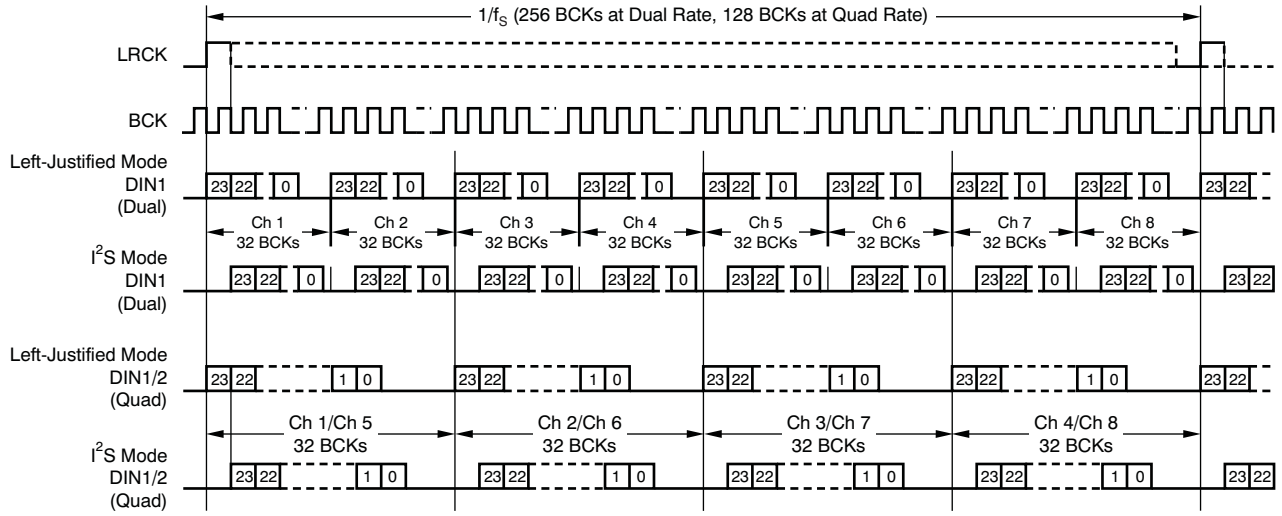



**Figure 35. Audio Data Format: 24-Bit DSP Format**




SCKI = 128 $f_S$, 256 $f_S$, and 512 $f_S$ Only

**Figure 36. Audio Data Format: 24-Bit TDM Format**




SCKI = 128 $f_S$ and 256 $f_S$ Only

**Figure 37. Audio Data Format: 24-Bit High-Speed TDM Format**

### 7.4.3 Synchronization With the Digital Audio System

The PCM1690 operates under the system clock (SCKI) and the audio sampling rate (LRCK). Therefore, SCKI and LRCK must have a specific relationship. The PCM1690 does not need a specific phase relationship between the audio interface clocks (LRCK, BCK) and the system clock (SCKI), but does require a specific frequency relationship (ratiometric) between LRCK, BCK, and SCKI.

If the relationship between SCKI and LRCK changes more than ±2 BCK clocks because of jitter, sampling frequency change, etc., the DAC internal operation stops within $1/f_S$, and the analog output is forced into VCOM (0.5 VCC1) until re-synchronization between SCKI, LRCK, and BCK completes and then $38/f_S$ (single, dual rate) or $29/f_S$ (quad rate) passes. In the event the change is less than ±2 BCKs, re-synchronization does not occur, and this analog output control and discontinuity does not occur.


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Figure 38 shows the DAC analog output during loss of synchronization. During undefined data periods, some noise may be generated in the audio signal. Also, the transition of normal to undefined data and undefined (or zero) data to normal data creates a discontinuity of data on the analog outputs, which then may generate some noise in the audio signal.

DAC outputs (VOUTx) hold the previous state if the system clock halts, but the asynchronous and re-synchronization processes will occur after the system clock resumes.

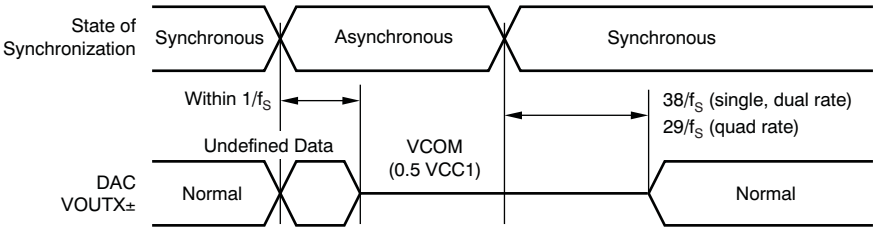



**Figure 38. DAC Outputs During Loss of Synchronization**

### 7.4.4 Mode Control

The PCM1690 includes three mode control interfaces with two oversampling configurations, depending on the input state of the MODE pin, as shown in Table 6. The pull-up and pull-down resistors must each be less than 10 kΩ.

**Table 6. Mode Control Selection**

| MODE | MODE CONTROL INTERFACE |
|---|---|
| Tied to DGND, low | Two-wire ($I^2C$) serial control, selectable oversampling configuration |
| Left open | Two-wire parallel control, auto mode oversampling configuration |
| Tied to VDD, high | Three-wire (SPI) serial control, selectable oversampling configuration |

The input state of the MODE pin is sampled at the moment of power-on, or during a low-to-high transition of the RST pin, with the system clock input. Therefore, input changes after reset are ignored until the next power-on or reset. From the mode control selection described in Table 6, the functions of four pins are changed, as shown in Table 7.

**Table 7. Pin Functions for Interface Mode**

| PIN | PIN ASSIGNMENTS | | |
|---|---|---|---|
| | SPI | $I^2C$ | H/W |
| 20 | MD (input) | SDA (input/output) | DEMP (input) |
| 21 | MC (input) | SCL (input) | FMT (input) |
| 22 | MS (input) | ADR0 (input) | RSV (input, low) |
| 23 | Test (output, open) | ADR1 (input) | RSV (input, low) |

In serial mode control, the actual mode control is performed by register writes (and reads) through the SPI- or $I^2C$-compatible serial control port. In parallel mode control, two specific functions are controlled directly through the high/low control of two specific pins, as described in the following section.

### 7.4.5 Parallel Hardware Control

The functions shown in Table 8 and Table 9 are controlled by two pins, DEMP and FMT, in parallel hardware control mode. The DEMP pin controls the 44.1-kHz digital de-emphasis function of all eight channels. The FMT pin controls the audio interface format for all eight channels.

**Table 8. DEMP Functionality**

| DEMP | DESCRIPTION |
|---|---|
| Low | De-emphasis off |
| High | 44.1 kHz de-emphasis on |

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**Table 9. FMT Functionality**

| FMT | DESCRIPTION |
|---|---|
| Low | 16-/20-/24-/32-bit $I^2S$ format |
| High | 24-bit $I^2S$ mode TDM format |

## 7.5 Register Maps

### 7.5.1 Control Register Definitions (Software Mode Only)

The PCM1690 has many user-programmable functions that are accessed via control registers, and are programmed through the SPI or $I^2C$ serial control port. Table 10 shows the available mode control functions along with reset default conditions and associated register address. Table 11 lists the register map.

**Table 10. User-Programmable Mode Control Functions**

| FUNCTION | RESET DEFAULT | REGISTER | LABEL |
|---|---|---|---|
| Mode control register reset | Normal operation | 64 | MRST |
| System reset | Normal operation | 64 | SRST |
| Analog mute function control | Mute disabled | 64 | AMUTE[3:0] |
| Sampling mode selection | Auto | 64 | SRDA[1:0] |
| Power-save mode selection | Power save | 65 | PSMDA |
| Audio interface format selection | $I^2S$ | 65 | FMTDA[3:0] |
| Operation control | Normal operation | 66 | OPEDA[3:0] |
| Digital filter roll-off control | Sharp roll-off | 66 | FLT[3:0] |
| Output phase selection | Normal | 67 | REVDA[8:1] |
| Soft mute control | Mute disabled | 68 | MUTDA[8:1] |
| Zero flag | Not detected | 69 | ZERO[8:1] |
| Digital attenuation mode | 0 dB to –63 dB, 0.5 dB step | 70 | DAMS |
| Digital de-emphasis function control | Disabled | 70 | DEMP[1:0] |
| Zero flag function selection | ZERO1: DIN1, left-channel<br>ZERO2: DIN1, right-channel | 70 | AZRO[1:0] |
| Zero flag polarity selection | High for detection | 70 | ZREV |
| Digital attenuation level setting | 0 dB, no attenuation | 71–79 | ATDAx[7:0] |

**Table 11. Register Map**

| ADR[6:0] | | DATA[7:0] | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| DEC | HEX | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| 64 | 40 | MRST | SRST | AMUTE3 | AMUTE2 | AMUTE1 | AMUTE0 | SRDA1 | SRDA0 |
| 65 | 41 | PSMDA | RSV(1) | RSV(1) | RSV(1) | FMTDA3 | FMTDA2 | FMTDA1 | FMTDA0 |
| 66 | 42 | OPEDA3 | OPEDA2 | OPEDA1 | OPEDA0 | FLT3 | FLT2 | FLT1 | FLT0 |
| 67 | 43 | REVDA8 | REVDA7 | REVDA6 | REVDA5 | REVDA4 | REVDA3 | REVDA2 | REVDA1 |
| 68 | 44 | MUTDA8 | MUTDA7 | MUTDA6 | MUTDA5 | MUTDA4 | MUTDA3 | MUTDA2 | MUTDA1 |
| 69 | 45 | ZERO8 | ZERO7 | ZERO6 | ZERO5 | ZERO4 | ZERO3 | ZERO2 | ZERO1 |
| 70 | 46 | DAMS | RSV(1) | DEMP1 | DEMP0 | RSV(1) | AZRO1 | AZRO0 | ZREV |
| 71 | 47 | RSV(1) | RSV(1) | RSV(1) | RSV(1) | RSV(1) | RSV(1) | RSV(1) | RSV(1) |
| 72 | 48 | ATDA17 | ATDA16 | ATDA15 | ATDA14 | ATDA13 | ATDA12 | ATDA11 | ATDA10 |
| 73 | 49 | ATDA27 | ATDA26 | ATDA25 | ATDA24 | ATDA23 | ATDA22 | ATDA21 | ATDA20 |
| 74 | 4A | ATDA37 | ATDA36 | ATDA35 | ATDA34 | ATDA33 | ATDA32 | ATDA31 | ATDA30 |
| 75 | 4B | ATDA47 | ATDA46 | ATDA45 | ATDA44 | ATDA43 | ATDA42 | ATDA41 | ATDA40 |
| 76 | 4C | ATDA57 | ATDA56 | ATDA55 | ATDA54 | ATDA53 | ATDA52 | ATDA51 | ATDA50 |
| 77 | 4D | ATDA67 | ATDA66 | ATDA65 | ATDA64 | ATDA63 | ATDA62 | ATDA61 | ATDA60 |

(1) RSV must be set to '0'.


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**Table 11. Register Map (continued)**

| ADR[6:0] | | DATA[7:0] | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| DEC | HEX | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| 78 | 4E | ATDA77 | ATDA76 | ATDA75 | ATDA74 | ATDA73 | ATDA72 | ATDA71 | ATDA70 |
| 79 | 4F | ATDA87 | ATDA86 | ATDA85 | ATDA84 | ATDA83 | ATDA82 | ATDA81 | ATDA80 |

### 7.5.2 Register Definitions

**Table 12. Register 64 (Hex 40)**

| DEC | HEX | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|
| 64 | 40 | MRST | SRST | AMUTE3 | AMUTE2 | AMUTE1 | AMUTE0 | SRDA1 | SRDA0 |

| | | |
|---|---|---|
| **MRST** | **Mode control register reset**<br>This bit sets the mode control register reset to the default value. Pop noise may be generated. Returning the MRST bit to '1' is unnecessary because it is automatically set to '1' after the mode control register is reset. | |
| | Default value = 1. | |
| | **MRST** | **Mode control register reset** |
| | 0 | Set default value |
| | 1 | Normal operation (default) |
| **SRST** | **System reset**<br>This bit controls the system reset, which includes the resynchronization between the system clock and sampling clock, and DAC operation restart. The mode control register is not reset and the PCM1789 does not go into a power-down state. Returning the SRST bit to '1' is unnecessary; it is automatically set to '1' after triggering a system reset.<br>Default value = 1. | |
| | **SRST** | **System reset** |
| | 0 | Resynchronization |
| | 1 | Normal operation (default) |
| **AMUTE[3:0]** | **Analog mute function control**<br>These bits control the enabling/disabling of each source event that triggers the analog mute control circuit.<br>Default value = 0000. | |
| | **AMUTE** | **Analog mute function control** |
| | xxx0 | Disable analog mute control by SCKI halt |
| | xxx1 | Enable analog mute control by SCKI halt |
| | xx0x | Disable analog mute control by asynchronous detect |
| | xx1x | Enable analog mute control by asynchronous detect |
| | x0xx | Disable analog mute control by ZERO1 and ZERO2 detect |
| | x1xx | Enable analog mute control by ZERO1 and ZERO2 detect |
| | 0xxx | Disable analog mute control by DAC disable command |
| | 1xxx | Enable analog mute control by DAC disable command |
| **SRDA[1:0]** | **Sampling mode selection**<br>These bits control the sampling mode of DAC operation. In Auto mode, the sampling mode is automatically set according to multiples between the system clock and sampling clock: single rate for 512 $f_S$, 768 $f_S$, and 1152 $f_S$, dual rate for 256 $f_S$ or 384 $f_S$, and quad rate for 128 $f_S$ and 192 $f_S$.<br>Default value = 00. | |
| | **SRDA** | **Sampling mode selection** |
| | 00 | Auto (default) |
| | 01 | Single rate |
| | 10 | Dual rate |
| | 11 | Quad rate |

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**Table 13. Register 65 (Hex 41)**

| DEC | HEX | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|
| 65 | 41 | PSMDA | RSV | RSV | RSV | FMTDA3 | FMTDA2 | FMTDA1 | FMTDA0 |

| | |
|---|---|
| **PSMDA** | **Power-save mode selection**<br>This bit selects the power-save mode for the OPEDA[3:0] function. When PSMDA = 0, OPEDA[3:0] controls the power-save mode and normal operation. When PSMDA = 1, OPEDA functions controls the DAC disable (not power-save mode) and normal operation.<br>Default value: 0. |

| PSMDA | Power-save mode selection |
|---|---|
| 0 | Power-save enable mode (default) |
| 1 | Power-save disable mode |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved; do not use. |
| **FMTDA[3:0]** | **Audio interface format selection**<br>These bits control the audio interface format for DAC operation. Details of the format, and any related restrictions with the system clock are described in the *Audio Data Interface Formats and Timing* section.<br>Default value: 0000 (16-/20-/24-/32-bit $I^2S$ format). |

| FMTDA | Audio interface format selection |
|---|---|
| 0000 | 16-/20-/24-/32-bit $I^2S$ format (default) |
| 0001 | 16-/20-/24-/32-bit left-justified format |
| 0010 | 24-bit right-justified format |
| 0011 | 16-bit right-justified format |
| 0100 | 24-bit $I^2S$ mode DSP format |
| 0101 | 24-bit left-justified mode DSP format |
| 0110 | 24-bit $I^2S$ mode TDM format |
| 0111 | 24-bit left-justified mode TDM format |
| 1000 | 24-bit high-speed $I^2S$ mode TDM format |
| 1001 | 24-bit high-speed left-justified mode TDM format |
| 101x | Reserved |
| 11xx | Reserved |
| 1 | Slow roll-off |

**Table 14. Register 66 (Hex 42)**

| DEC | HEX | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|
| 66 | 42 | OPEDA3 | OPEDA2 | OPEDA1 | OPEDA0 | FLT3 | FLT2 | FLT1 | FLT0 |

| | |
|---|---|
| **OPEDA[3:0]** | **Operation control**<br>These bits control the DAC operation mode. In operation disable mode, the DAC output is cut off from DIN and the internal DAC data are reset. If PSMDA = 1, the DAC output is forced into VCOM. IF PSMDA = 0, the DAC output is forced into AGND and the DAC goes into a power-down state. For normal operating mode, these bits must be '0'. The serial mode control is effective during operation disable mode.<br>Default value: 0000. |

| OPEDA | Operation control |
|---|---|
| xxx0 | DAC1/2 normal operation |
| xxx1 | DAC1/2 operation disable with or without power save |
| xx0x | DAC3/4 normal operation |
| xx1x | DAC3/4 operation disable with or without power save |
| x0xx | DAC5/6 normal operation |
| x1xx | DAC5/6 operation disable with or without power save |
| 0xxx | DAC7/8 normal operation |
| 1xxx | DAC7/8 operation disable with or without power save |


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| | |
|---|---|
| **FLT[3:0]** | **Digital filter roll-off control**<br>These bits allow users to select the digital filter roll-off that is best suited to their applications. Sharp and slow filter roll-off selections are available. The filter responses for these selections are shown in the *Typical Characteristics* section of this data sheet.<br>Default value: 0000. |

| FLT | Digital filter roll-off control |
|---|---|
| xxx0 | DAC1/2 sharp roll-off |
| xxx1 | DAC1/2 slow roll-off |
| xx0x | DAC3/4 sharp roll-off |
| xx1x | DAC3/4 slow roll-off |
| x0xx | DAC5/6 sharp roll-off |
| x1xx | DAC5/6 slow roll-off |
| 0xxx | DAC7/8 sharp roll-off |
| 1xxx | DAC7/8 slow roll-off |

**Table 15. Register 67 (Hex 43)**

| DEC | HEX | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|
| 67 | 43 | REVDA8 | REVDA7 | REVDA6 | REVDA5 | REVDA4 | REVDA3 | REVDA2 | REVDA1 |

| | |
|---|---|
| **REVDA[8:1]** | **Output phase selection**<br>These bits are used to control the phase of DAC analog signal outputs.<br>Default value: 0000 0000. |

| REVDA | Output phase selection |
|---|---|
| xxxx xxx0 | DAC1 normal output |
| xxxx xxx1 | DAC1 inverted output |
| xxxx xx0x | DAC2 normal output |
| xxxx xx1x | DAC2 inverted output |
| xxxx x0xx | DAC3 normal output |
| xxxx x1xx | DAC3 inverted output |
| xxxx 0xxx | DAC4 normal output |
| xxxx 1xxx | DAC4 inverted output |
| xxx0 xxxx | DAC5 normal output |
| xxx1 xxxx | DAC5 inverted output |
| xx0x xxxx | DAC6 normal output |
| xx1x xxxx | DAC6 inverted output |
| x0xx xxxx | DAC7 normal output |
| x1xx xxxx | DAC7 inverted output |
| 0xxx xxxx | DAC8 normal output |
| 1xxx xxxx | DAC8 inverted output |

**Table 16. Register 68 (Hex 44)**

| DEC | HEX | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|
| 68 | 44 | MUTDA8 | MUTDA7 | MUTDA6 | MUTDA5 | MUTDA4 | MUTDA3 | MUTDA2 | MUTDA1 |

| | |
|---|---|
| **MUTDA[8:1]** | **Soft Mute control**<br>These bits are used to enable or disable the Soft Mute function for the corresponding DAC outputs, VOUT. The Soft Mute function is incorporated into the digital attenuators. When mute is disabled (MUTDA[8:1] = 0), the attenuator and DAC operate normally. When mute is enabled by setting MUTDA[8:1] = 1, the digital attenuator for the corresponding output is decreased from the current setting to infinite attenuation. By setting MUTDA[8:1] = 0, the attenuator is increased to the last attenuation level in the same manner as it is for decreasing levels. This configuration reduces *pop and zipper noise* during muting of the DAC output. This Soft Mute control uses the same resource of digital attenuation level setting. Mute control has priority over the digital attenuation level setting.<br>Default value: 0000 0000. |

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| | MUTDA | Soft Mute control |
|---|---|---|
| | xxxx xxx0 | DAC1 Mute disabled |
| | xxxx xxx1 | DAC1 Mute enabled |
| | xxxx xx0x | DAC2 Mute disabled |
| | xxxx xx1x | DAC2 Mute enabled |
| | xxxx x0xx | DAC3 Mute disabled |
| | xxxx x1xx | DAC3 Mute enabled |
| | xxxx 0xxx | DAC4 Mute disabled |
| | xxxx 1xxx | DAC4 Mute enabled |
| | xxx0 xxxx | DAC5 Mute disabled |
| | xxx1 xxxx | DAC5 Mute enabled |
| | xx0x xxxx | DAC6 Mute disabled |
| | xx1x xxxx | DAC6 Mute enabled |
| | x0xx xxxx | DAC7 Mute disabled |
| | x1xx xxxx | DAC7 Mute enabled |
| | 0xxx xxxx | DAC8 Mute disabled |
| | 1xxx xxxx | DAC8 Mute enabled |

**Table 17. Register 69 (Hex 45)**

| DEC | HEX | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|
| 69 | 45 | ZERO8 | ZERO7 | ZERO6 | ZERO5 | ZERO4 | ZERO3 | ZERO2 | ZERO1 |

| | | |
|---|---|---|
| **ZERO[8:1]** | **Zero flag (read-only)**<br>These bits indicate the present status of the zero detect circuit for each DAC channel; these bits are read-only. | |
| | **ZERO** | **Zero flag** |
| | xxxx xxx0 | DAC1 zero input not detected |
| | xxxx xxx1 | DAC1 zero input detected |
| | xxxx xx0x | DAC2 zero input not detected |
| | xxxx xx1x | DAC2 zero input detected |
| | xxxx x0xx | DAC3 zero input not detected |
| | xxxx x1xx | DAC3 zero input detected |
| | xxxx 0xxx | DAC4 zero input not detected |
| | xxxx 1xxx | DAC4 zero input detected |
| | xxx0 xxxx | DAC5 zero input not detected |
| | xxx1 xxxx | DAC5 zero input detected |
| | xx0x xxxx | DAC6 zero input not detected |
| | xx1x xxxx | DAC6 zero input detected |
| | x0xx xxxx | DAC7 zero input not detected |
| | x1xx xxxx | DAC7 zero input detected |
| | 0xxx xxxx | DAC8 zero input not detected |
| | 1xxx xxxx | DAC8 zero input detected |


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**Table 18. Register 70 (Hex 46)**

| DEC | HEX | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|
| 70 | 46 | DAMS | RSV | DEMP1 | DEMP0 | RSV | AZRO1 | AZRO0 | ZREV |

| | | |
|---|---|---|
| **DAMS** | **Digital attenuation mode**<br>This bit selects the attenuation mode.<br>Default value: 0. | |
| | **DAMS** | **Digital attenuation mode** |
| | 0 | Fine step: 0.5-dB step for 0 dB to –63 dB range (default) |
| | 1 | Wide range: 1-dB step for 0 dB to –100 dB range |
| **RSV** | **Reserved** | |
| | Reserved; do not use. | |
| **DEMP[1:0]** | **Digital de-emphasis function/sampling rate control**<br>These bits are used to disable or enable the various sampling frequencies of the digital de-emphasis function.<br>Default value: 00. | |
| | **DEMP** | **Digital de-emphasis function/sampling rate control** |
| | 00 | Disable (default) |
| | 01 | 48 kHz enable |
| | 10 | 44.1 kHz enable |
| | 11 | 32 kHz enable |
| **AZRO[1:0]** | **Zero flag channel combination selection**<br>The AZRO[1:0] bits are used to select the zero flag channel combination for ZERO1 and ZERO2.<br>If the analog mute function control by ZERO flags is used, AZRO[1:0] must not be set '00'; otherwise, analog mute works even if the data of DATA2–4 are not zero.<br>Default value: $00_B$. | |
| | **AZRO** | **Zero flag combination selection** |
| | 00 | Combination A: ZERO1 = DATA1 left channel, ZERO2 = DATA1 right channel (default) |
| | 01 | Combination B: ZERO1 = DATA1–4, ZERO2 = DATA1–4 |
| | 10 | Combination C: ZERO1 = DATA4, ZERO2 = DATA1–3 |
| | 11 | Combination D: ZERO1 = DATA1, ZERO2 = DATA2–4 |
| **ZREV** | **Zero flag polarity selection**<br>This bit controls the polarity of the zero flag pin.<br>Default value: 0. | |
| | **ZREV** | **Zero flag polarity selection** |
| | 0 | High for zero detect (default) |
| | 1 | Low for zero detect |

**Table 19. Registers 71-79 (Hex 47-49, 4A-4F)**

| DEC | HEX | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|
| 71 | 47 | RSV | RSV | RSV | RSV | RSV | RSV | RSV | RSV |
| 72 | 48 | ATDA17 | ATDA16 | ATDA15 | ATDA14 | ATDA13 | ATDA12 | ATDA11 | ATDA10 |
| 73 | 49 | ATDA27 | ATDA26 | ATDA25 | ATDA24 | ATDA23 | ATDA22 | ATDA21 | ATDA20 |
| 74 | 4A | ATDA37 | ATDA36 | ATDA35 | ATDA34 | ATDA33 | ATDA32 | ATDA31 | ATDA30 |
| 75 | 4B | ATDA47 | ATDA46 | ATDA45 | ATDA44 | ATDA43 | ATDA42 | ATDA41 | ATDA40 |
| 76 | 4C | ATDA57 | ATDA56 | ATDA55 | ATDA54 | ATDA53 | ATDA52 | ATDA51 | ATDA50 |
| 77 | 4D | ATDA67 | ATDA66 | ATDA65 | ATDA64 | ATDA63 | ATDA62 | ATDA61 | ATDA60 |
| 78 | 4E | ATDA77 | ATDA76 | ATDA75 | ATDA74 | ATDA73 | ATDA72 | ATDA71 | ATDA70 |
| 79 | 4F | ATDA87 | ATDA86 | ATDA85 | ATDA84 | ATDA83 | ATDA82 | ATDA81 | ATDA80 |

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| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved; do not use. |
| **ATDAx[7:0]** | **Digital attenuation level setting**<br>Where *x* = 1 to 8, corresponding to the DAC output ($V_{OUT}$x).<br>Each DAC output ($V_{OUT}$1 through $V_{OUT}$8) has a digital attenuation function. The attenuation level can be set from 0 dB to R dB, in S-dB steps. Changes in attenuator levels are made by incrementing or decrementing one step (S dB) for every 8/$f_S$ time interval until the programmed attenuator setting is reached. Alternatively, the attenuation level can be set to infinite attenuation (or mute). R (Range) and S (Step) is –63 and 0.5 for DAMS = 0 and –100 and 1.0 for DAMS = 1, respectively. The DAMS bit is defined in Register 70 (46h). Table 20 shows attenuation levels for various settings.<br>The attenuation level for each channel can be set individually using the following formula:<br>Attenuation level (dB) = S × (ATDAx[7:0]$_{DEC}$ – 255)<br>where ATDAx[7:0]$_{DEC}$ = 0 through 255.<br>For ATDAx[7:0]$_{DEC}$ = 0 through 128 with DAMS = 0 or 0 through 154 with DAMS = 1, attenuation is set to infinite attenuation (mute).<br>Default value: 1111 1111. |

**Table 20. Attenuation Levels for Various Settings**

| ATDAx[7:0] | | ATTENUATION LEVEL SETTING | |
|---|---|---|---|
| BINARY | DECIMAL | DAMS = 0 | DAMS = 1 |
| 1111 1111 | 255 | 0 dB, no attenuation (default) | 0 dB, no attenuation (default) |
| 1111 1110 | 254 | –0.5 dB | –1 dB |
| 1111 1101 | 253 | –1.0 dB | –2 dB |
| ... | ... | ... | ... |
| 1001 1100 | 156 | –45.9 dB | –99 dB |
| 1001 1011 | 155 | –50.0 dB | –100 dB |
| 1001 1010 | 154 | –50.5 dB | Mute |
| ... | ... | ... | ... |
| 1000 0010 | 130 | –62.5 dB | Mute |
| 1000 0001 | 129 | –63.0 dB | Mute |
| 0000 0000 | 128 | Mute | Mute |
| ... | ... | ... | ... |
| 0000 0000 | 0 | Mute | Mute |


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# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

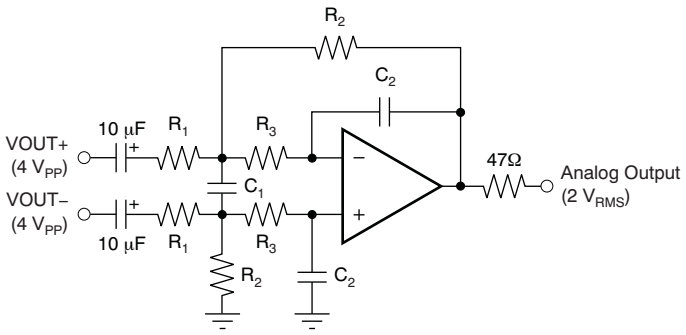
## 8.1 Application Information

### 8.1.1 Lowpass Filter and Differential-to-Single-Ended Converter for DAC Outputs

ΔΣ DACs use noise-shaping techniques to improve in-band signal-to-noise ratio (SNR) performance at the expense of generating increased out-of-band noise above the Nyquist frequency, or $f_S/2$. The out-of-band noise must be lowpass filtered in order to provide optimal converter performance. This filtering is accomplished by a combination of on-chip and external lowpass filters.

Figure 39 and Figure 40 show the recommended external differential-to-single-ended converter with lowpass active filter circuits for AC-coupled and DC-coupled applications. These circuits are second-order Butterworth filters using a multiple feedback (MFB) circuit arrangement that reduces sensitivity to passive component variations over frequency and temperature. For more information regarding MFB active filter designs, please refer to Applications Bulletin SBAA055, *Dynamic Performance Testing of Digital Audio D/A Converters*, available from the TI web site (www.ti.com) or the local Texas Instruments' sales office.

Because the overall system performance is defined by the quality of the DACs and the associated analog output circuitry, high-quality audio op amps are recommended for the active filters. Texas Instruments' OPA2134, OPA2353, and NE5532A dual op amps are shown in Figure 39 and Figure 40, and are recommended for use with the PCM1690.

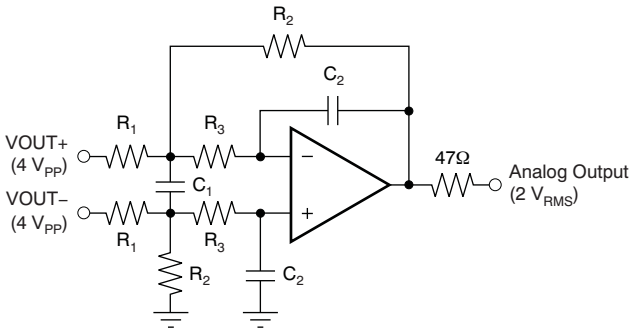



NOTE: Amplifier is an NE5532A x1/2 or OPA2134 x1/2; $R_1$ = 7.5-kΩ; $R_2$ = 5.6-kΩ; $R_3$ = 360-Ω; $C_1$ = 3300-pF; $C_2$ = 680-pF; Gain = 0.747; $f_{-3\ dB}$ = 53 kHz.

**Figure 39. AC-Coupled, Post-LPF and Differential to Single-Ended Buffer**

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## Application Information (continued)




NOTE: Amplifier is an NE5532A x1/2 or OPA2134 x1/2; $R_1$ = 15-kΩ; $R_2$ = 11-kΩ; $R_3$ = 820-Ω; $C_1$ = 1500-pF; $C_2$ = 330-pF; Gain = 0.733; $f_{-3\ dB}$ = 54 kHz.

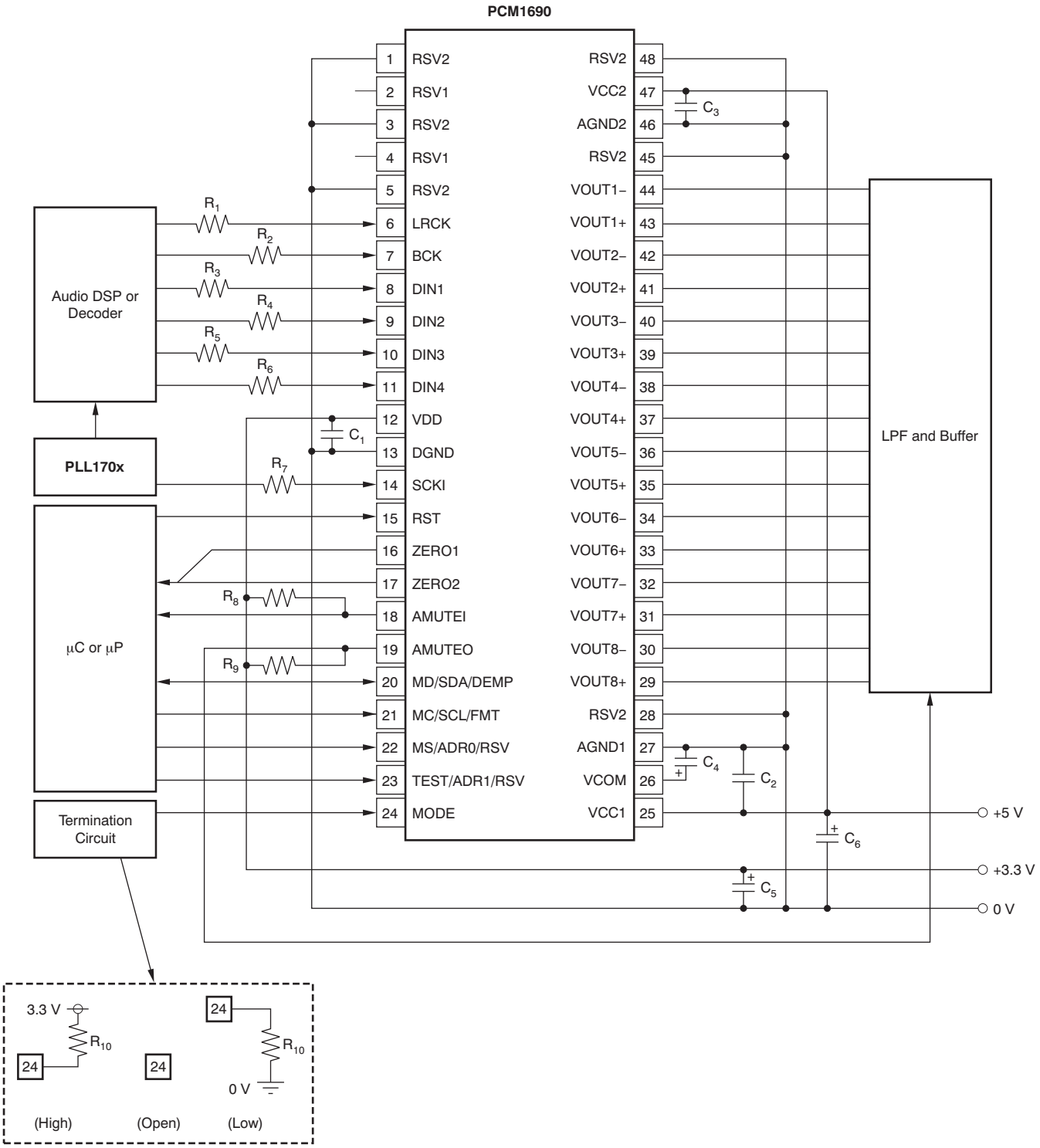
**Figure 40. DC-Coupled, Post-LPF and Differential to Single-Ended Buffer**

## 8.2 Typical Application

A basic connection diagram is shown in Figure 41, with the necessary power-supply bypassing and decoupling components. Texas Instruments' PLL170X is used to generate the system clock input at SCKI, as well as to generate the clock for the audio signal processor. The use of series resistors (22 Ω to 100 Ω) are recommended for SCKI, LRCK, BCK, DIN1, DIN2, DIN3, and DIN4 for electromagnetic interference (EMI) reduction.


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## Typical Application (continued)




NOTE: $C_1$ through $C_3$ are 1-µF ceramic capacitors. $C_4$ through $C_6$ are 10-µF electrolytic capacitors. $R_1$ through $R_7$ are 22-Ω to 100-Ω resistors. $R_8$ and $R_9$ are resistors appropriate for pull-up. $R_{10}$ is less than 10 kΩ.

**Figure 41. Basic Connection Diagram**

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## Typical Application (continued)

### 8.2.1 Design Requirements

- Control: Hardware, $I^2C$, or SPI
- Audio Input: PCM Serial data, TDM, or DSP
- Audio Output: (1.6 × VCC1) Vpp analog audio biased to (0.5 × VCC1) V
- Master Clock: PLL170X IC

### 8.2.2 Detailed Design Procedure

#### *8.2.2.1 Hardware Control Method*

There are 3 ways to control the PCM1690, hardware control, SPI, or I2C. Hardware control will provide a limited access to control features available in the PCM1690 but can be implemented with pull up and pull downs, or with GPIO of a microcontroller. Control via SPI or I2C will provide access to all control registers and features but will require a digital device that can implement SPI or I2C.

#### *8.2.2.2 Audio Input*

For Audio Input there are 3 options, PCM serial data, TDM, or DSP. All three will support the same quality of audio data, but having these 3 options to match the audio sources available outputs allows for greater flexibility. This selection is made by configuring the MODE pin which is detailed in Table 6 and shown in Pin Functions.

#### *8.2.2.3 Audio Output*

The output of the PCM1690 will produce a differential (1.6 × VCC1) Vpp signal at full scale into a 5-kΩ load, that must be filtered before being sent to an amplifier. Outputs Vout1 through Vout 8 will be biased at (0.5 × VCC1) V.

#### *8.2.2.4 Master Clock*

The master clock can come from wither a dedicated IC such as the PLL170X series, a crystal or the audio source IC. What is important is that the audio source and the PCM1690 are driven from the same source so that the audio clocks will be synchronous.

### 8.2.3 Application Curve

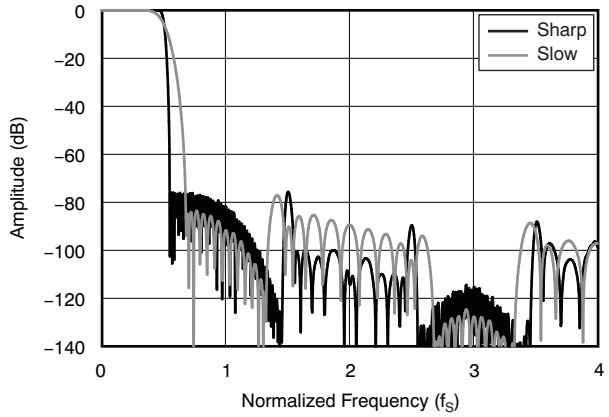



**Figure 42. Frequency Response (Single Rate)**


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# 9 Power Supply Recommendations

The PCM1690 requires 5 V for the analog supply and 3.3 V for the digital supply. The 5-V supply is used to power the DAC analog and output filter circuitry, and the 3.3-V supply is used to power the digital filter and serial interface circuitry. For best performance, it is recommended to use a linear regulator with the 5-V and 3.3-V supplies.

Five capacitors are required for supply bypassing (see Figure 41). These capacitors must be located as close as possible to the PCM1690 package. The 10-µF capacitors are aluminum electrolytic, while the three 1-µF capacitors are ceramic.

# 10 Layout

## 10.1 Layout Guidelines

A typical printed-circuit-board (PCB) layout for the PCM1690 is shown in Figure 43. A ground plane is recommended, with the analog and digital sections being isolated from one another using a split or cut in the circuit board. The PCM1690 must be oriented with the digital I/O pins facing the ground plane split/cut to allow for short, direct connections to the digital audio interface and control signals originating from the digital section of the board.

Separate power supplies are recommended for the digital and analog sections of the board. This configuration prevents the switching noise present on the digital supply from contaminating the analog power supply and degrading the dynamic performance of the PCM1690.

## 10.2 Layout Example

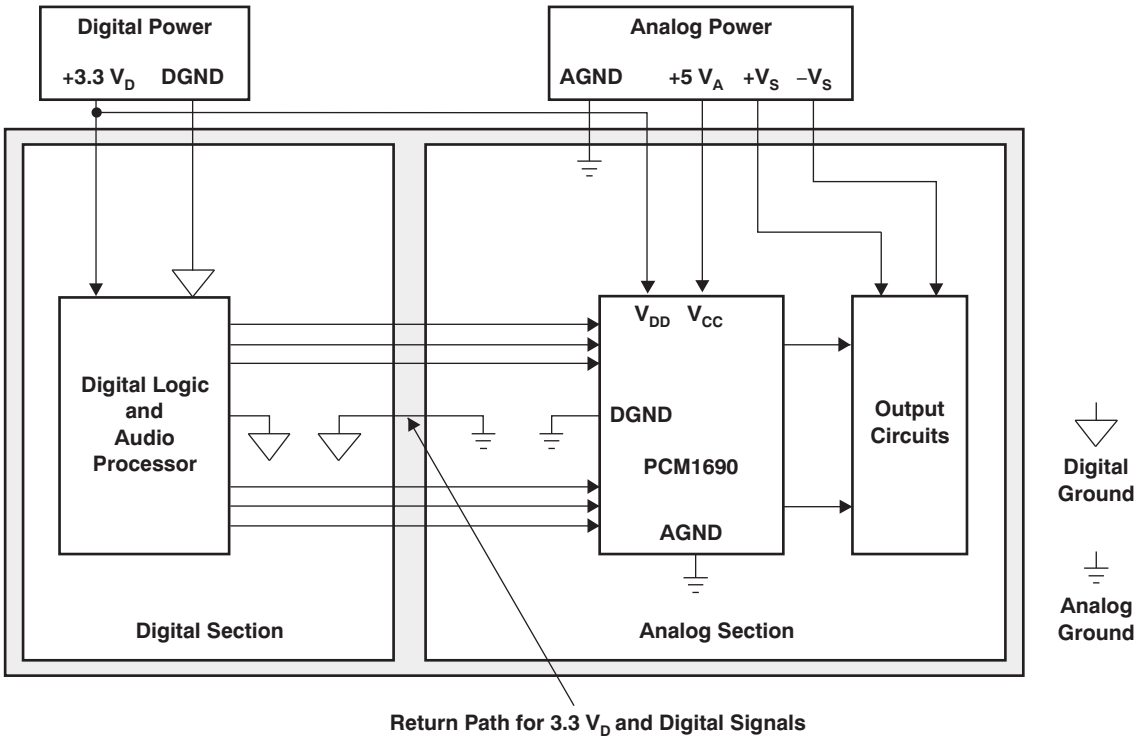



**Figure 43. Recommended PCB Layout**

# 11 Device and Documentation Support

## 11.1 Device Support

### 11.1.1 Development Support

For the PMC1690 application support, see the following:

- SoundPlus(TM) High Performance Audio Operational Amplifiers, OPA2134
- 3.3 V Dual PLL Multi-Clock Generator, PLL170X
- Dual Low-Noise Operational Amplifier, NE5532A
- High-Speed, Single-Supply, Rail-to-Rail Operational Amplifiers MicroAmplifier(TM) Series, OPA2353

## 11.2 Documentation Support

### 11.2.1 Related Documentation

For related documentation, see the following:

*Dynamic Performance Testing of Digital Audio D/A Converters*, SBAA055

## 11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.4 Trademarks

E2E is a trademark of Texas Instruments.
Blu-ray is a trademark of Blu-ray Disk Association.
$I^2S$ is a trademark of NXP Semiconductors.
All other trademarks are the property of their respective owners.

## 11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PCM1690DCA | ACTIVE | HTSSOP | DCA | 48 | 40 | Green (RoHS & no Sb/Br) | NIPDAU | Level-3-260C-168 HR | -40 to 85 | PCM1690 | Samples |
| PCM1690DCAR | ACTIVE | HTSSOP | DCA | 48 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-3-260C-168 HR | -40 to 85 | PCM1690 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF PCM1690 :**

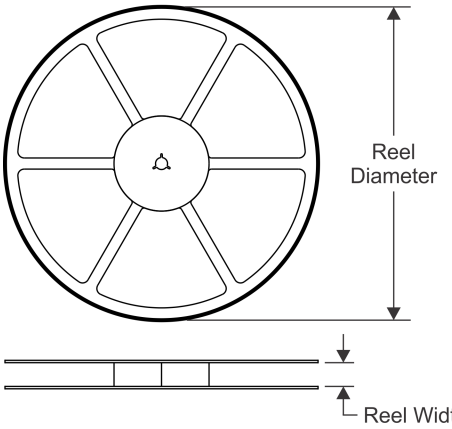
- Automotive: PCM1690-Q1

NOTE: Qualified Version Definitions:

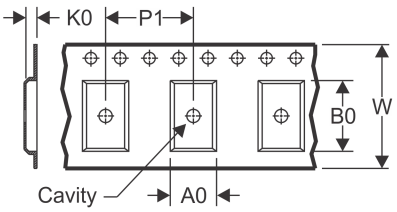
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

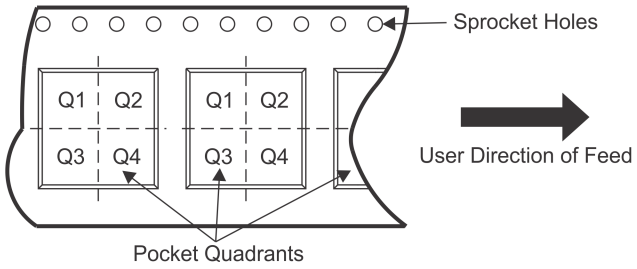



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

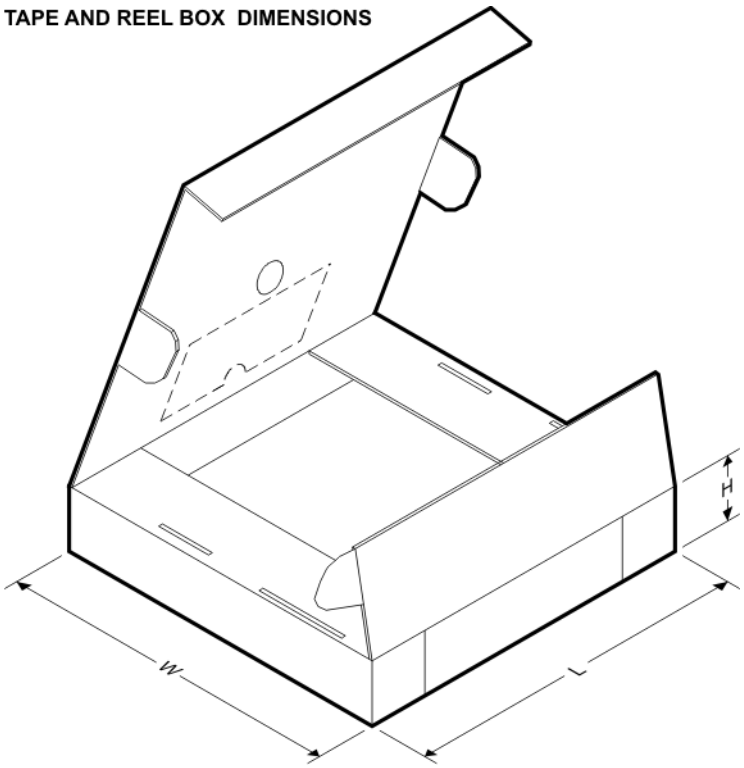
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PCM1690DCAR | HTSSOP | DCA | 48 | 2000 | 330.0 | 24.4 | 8.6 | 13.0 | 1.8 | 12.0 | 24.0 | Q1 |

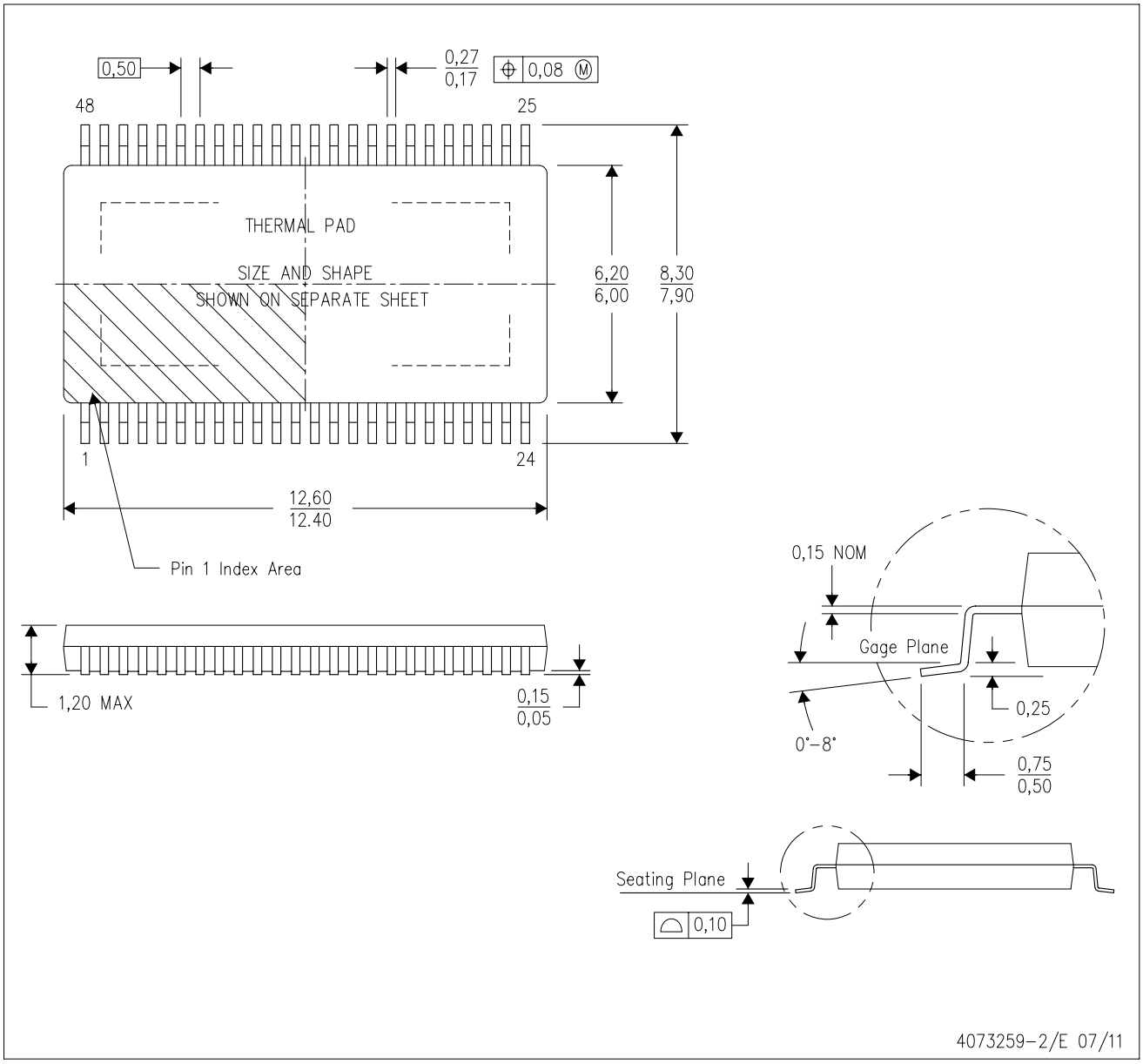
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| PCM1690DCAR | HTSSOP | DCA | 48 | 2000 | 350.0 | 350.0 | 43.0 |

DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL–OUTLINE




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–153

**PowerPAD is a trademark of Texas Instruments.**

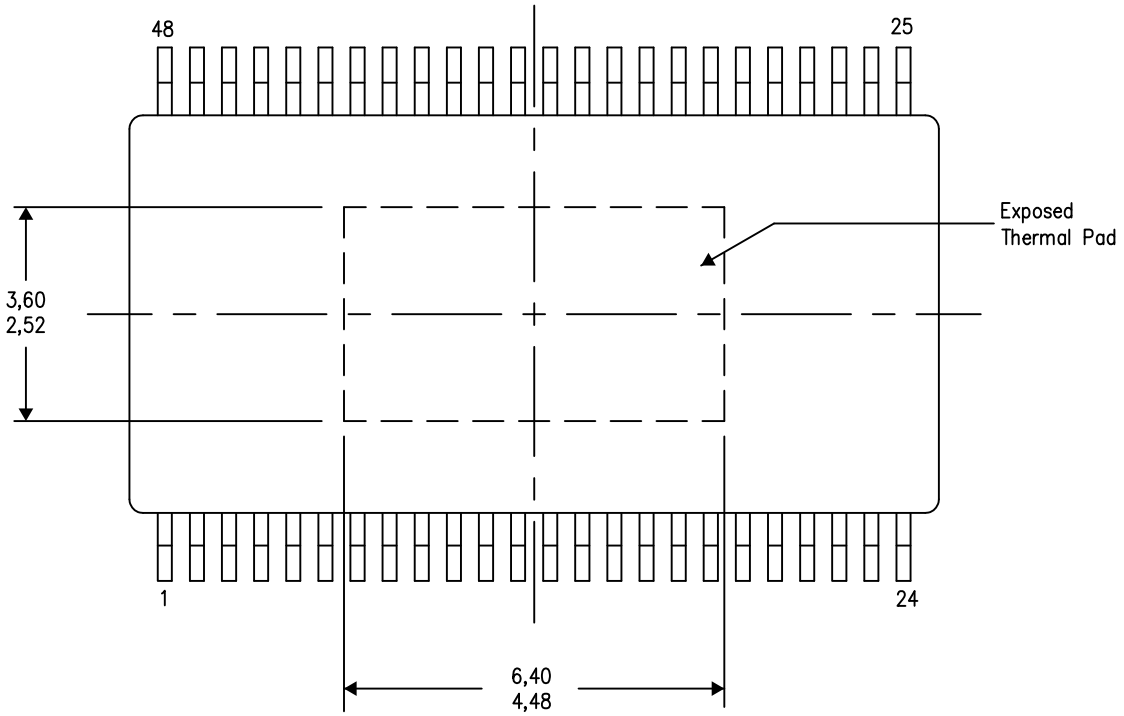
DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Top View

Exposed Thermal Pad Dimensions

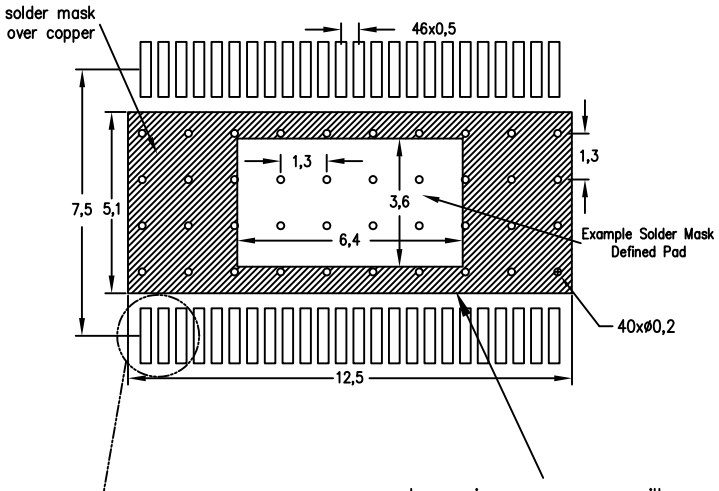
4206320–4/S 11/14

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments.

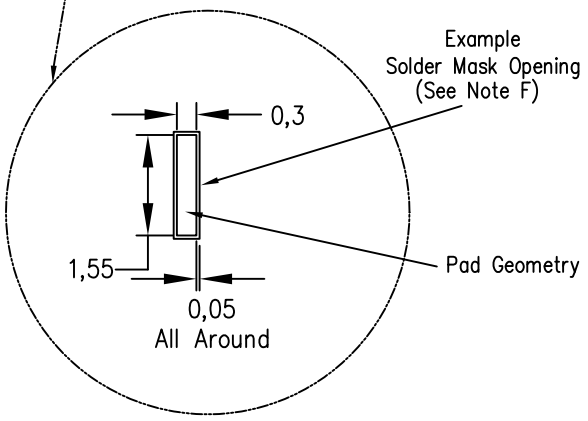
DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE

Example Board Layout
Via pattern and copper pad size
may vary depending on layout constraints

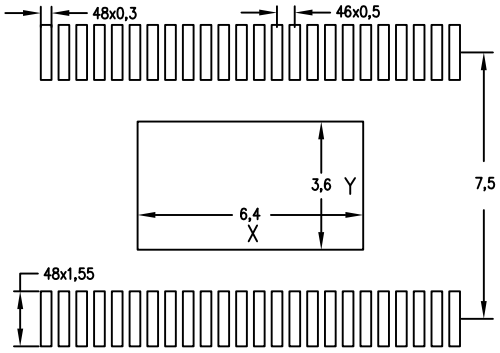



Increasing copper area will
enhance thermal performance
(See Note D)

Example
Non Soldermask Defined Pad




Stencil openings based
on a stencil thickness of .127mm
Reference table below for other
solder stencil thicknesses




(See Note E)

| Center PowerPAD Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 7.21 | 4.06 |
| 0.127mm | 6.40 | 3.60 |
| 0.152mm | 5.85 | 3.29 |
| 0.178mm | 5.41 | 3.04 |

4208546–3/H 11/14

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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