PCK351

1 : 10 clock distribution device with 3-state outputs

Rev. 02 — 16 December 2005 Product data sheet

1. General description

The PCK351 is a high-performance 3.3 V LVTTL clock distribution device. The PCK351 enables a single clock input to be distributed to ten outputs with minimum output skew and pulse skew. The use of distributed V_{CC} and GND pins in the PCK351 ensures reduced switching noise.

The PCK351 is characterized for operation over the supply range 3.0 V to 3.6 V, and over the industrial temperature range –40 °C to +85 °C.

2. Features

- 1 : 10 LVTTL clock distribution
- Low output-to-output skew
- Low output pulse skew
- Overvoltage tolerant inputs and outputs
- LVTTL-compatible inputs and outputs
- Distributed V_{CC} and ground pins reduce switching noise
- Balanced high-drive outputs (–32 mA I_{OH}, 32 mA I_{OL})
- Reduced power dissipation due to the state-of-the-art QUBiC-LP process
- Supply range of +3.0 V to +3.6 V
- Package options include plastic small-outline (D) and shrink small-outline (DB) packages
- Industrial temperature range –40 °C to +85 °C

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3. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 3.0$ ns.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PLH}	LOW-to-HIGH propagation delay	A input to Yn outputs; C_L = 50 pF; V_{CC} = 3.3 V	3.1	3.6	4.1	ns
t_{PHL}	HIGH-to-LOW propagation delay	A input to Yn outputs; C_L = 50 pF; V_{CC} = 3.3 V	3.1	3.6	4.1	ns
C_i	input capacitance	V_{CC} = 3.3 V; V_I = V_{CC} or GND; f = 10 MHz	-	4	-	pF
C_o	output capacitance	V_{CC} = 3.3 V; V_O = V_{CC} or GND; f = 10 MHz	-	6	-	pF
C_{PD}	power dissipation capacitance [1]	C_L = 50 pF; f = 1 MHz	-	48	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P in μW).
$P = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in volts.

4. Ordering information

Table 2: Ordering information

T_{amb} = −40 °C to +85 °C

Type number	Package		
	Name	Description	Version
PCK351D	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
PCK351DB	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1

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5. Functional diagram

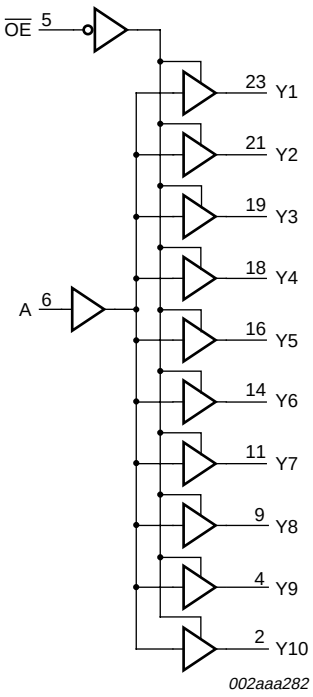

Fig 1. Logic diagram of PCK351

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6. Pinning information

6.1 Pinning

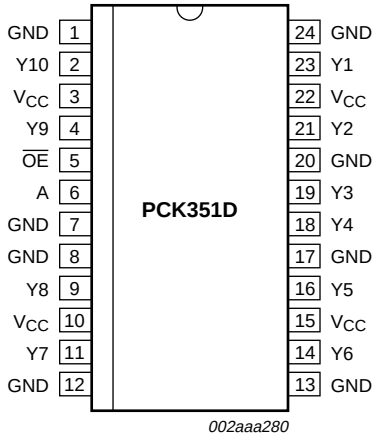

Fig 2. Pin configuration for SO24

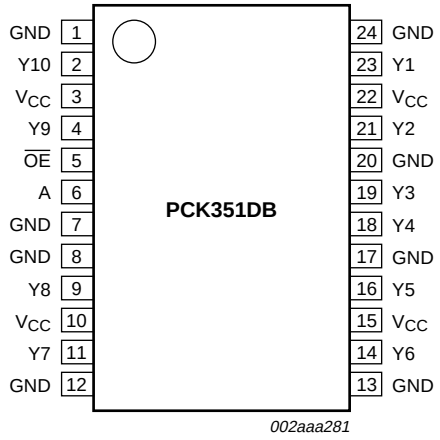

Fig 3. Pin configuration for SSOP24

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
GND	1, 7, 8, 12, 13, 17, 20, 24	ground (0 V)
Y10	2	outputs
Y9	4	
Y8	9	
Y7	11	
Y6	14	
Y5	16	
Y4	18	
Y3	19	
Y2	21	
Y1	23	
V_{CC}	3, 10, 15, 22	supply voltage
$\overline{OE}$	5	output enable input (active LOW)
A	6	data input

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7. Functional description

Refer to Figure 1 “Logic diagram of PCK351”.

7.1 Function table

Table 4: Function table

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state

Inputs		Outputs
A	**$\overline{OE}$**	**Yn**
L	H	Z
H	H	Z
L	L	L
H	L	H

7.2 Logic symbol

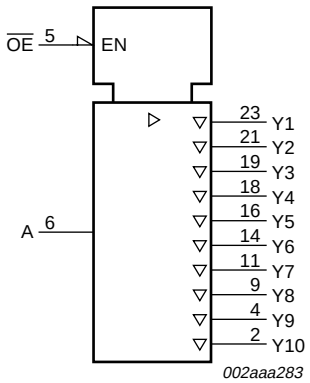

Fig 4. Logic symbol

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8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). [1]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	+4.6	V
V_I	input voltage		–0.5 [2]	+7.0	V
V_O	output voltage		–0.5 [2]	+3.6	V
I_{IK}	input clamping current	$V_I < 0$ V	-	–18	mA
I_{OK}	output clamping current	$V_I < 0$ V	-	–50	mA
$I_{O(sink)}$	output sink current		-	64	mA
I_{CC}	quiescent supply current		-	±75	mA
I_{GND}	ground current		-	±75	mA
T_{stg}	storage temperature		–65	+150	°C
P	power dissipation	T_{amb} = +55 °C			
		SO package	-	0.65	W
		SSOP package	-	1.7	W

[1] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

[2] The input and output negative voltage ratings may be exceeded if the input and output clamping currents are observed.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Unused pins (input or I/O) must be held HIGH or LOW.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		3.0	3.6	V
V_{IH}	HIGH-state input voltage		2.0	5.5	V
V_I	input voltage		0	0.8	V
T_{amb}	ambient temperature	see Table 7 and Table 8 per device	–40	+85	°C
t_r	rise time	input; V_{CC} = 3.3 ± 0.3 V	-	100	ns/V
t_f	fall time	input; V_{CC} = 3.3 ± 0.3 V	-	100	ns/V

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10. Characteristics

Table 7: Static characteristics

Over recommended operating conditions; voltages are referenced to GND (ground = 0 V). T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	input clamping voltage	V_{CC} = 3.0 V; I_I = –18 mA		-	-	–1.2	V
V_{OH}	HIGH-state output voltage	V_{CC} = 3.0 V; I_{OH} = –32 mA		2.0	-	-	V
V_{OL}	LOW-state output voltage	V_{CC} = 3.0 V; I_{OL} = 32 mA		-	-	0.5	V
I_{LI}	input leakage current	V_{CC} = 3.6 V; V_I = GND or 5.5 V		-	-	±1.0	µA
I_{LO}	output leakage current	V_{CC} = 3.6 V; V_O = 2.5 V		–15	-	–150	mA
I_{OZ}	OFF-state output current	3-state; V_{CC} = 3.6 V; V_O = 3 V	[1]	-	-	±10	µA
I_{CC}	quiescent supply current	V_{CC} = 3.6 V; V_I = V_{CC} or GND; I_O = 0 A					
		outputs HIGH		-	-	0.3	mA
		outputs LOW		-	-	25	mA
		outputs disabled		-	-	0.3	mA
C_i	input capacitance	V_{CC} = 3.3 V; V_I = V_{CC} or GND; f = 10 MHz		-	4	-	pF
C_o	output capacitance	V_{CC} = 3.3 V; V_O = V_{CC} or GND; f = 10 MHz		-	6	-	pF

[1] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

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Table 8: Dynamic characteristics

GND = 0 V; $t_r = t_f \leq 2.5$ ns.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC} = 3.3 V; T_{amb} = 25 °C; C_L = 50 pF						
t_{PLH}	LOW-to-HIGH propagation delay	A to Yn; see Figure 5 and Figure 8	3.1	3.8	4.1	ns
t_{PHL}	HIGH-to-LOW propagation delay	A to Yn; see Figure 5 and Figure 8	3.1	3.8	4.1	ns
t_{PZH}	OFF-state to HIGH propagation delay	$\overline{OE}$ to Yn; see Figure 6 and Figure 8	1.8	3.8	5.5	ns
t_{PZL}	OFF-state to LOW propagation delay	$\overline{OE}$ to Yn; see Figure 6 and Figure 8	1.8	3.8	5.5	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$\overline{OE}$ to Yn; see Figure 6 and Figure 8	1.8	3.8	5.9	ns
t_{PLZ}	LOW to OFF-state propagation delay	$\overline{OE}$ to Yn; see Figure 6 and Figure 8	1.8	3.8	5.9	ns
$t_{sk(o)}$	output skew time	A to Yn; output-to-output; see Figure 7 and Figure 8	-	0.3	0.5	ns
$t_{sk(p)}$	pulse skew time	A to Yn; see Figure 7 and Figure 8	-	0.2	0.8	ns
$t_{sk(pr)}$	process skew time	A to Yn; part-to-part; see Figure 7 and Figure 8	-	-	1	ns
t_r	rise time	A to Yn; see Figure 5 and Figure 8	0.3	-	2.0	ns
t_f	fall time	A to Yn; see Figure 5 and Figure 8	0.3	-	2.0	ns
V_{CC} = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C; C_L = 50 pF						
t_{PLH}	LOW-to-HIGH propagation delay	A to Yn; see Figure 5 and Figure 8	2.5	3.3	5.9	ns
t_{PHL}	HIGH-to-LOW propagation delay	A to Yn; see Figure 5 and Figure 8	2.5	3.3	5.9	ns
t_{PZH}	OFF-state to HIGH propagation delay	$\overline{OE}$ to Yn; see Figure 6 and Figure 8	1.3	-	5.9	ns
t_{PZL}	OFF-state to LOW propagation delay	$\overline{OE}$ to Yn; see Figure 6 and Figure 8	1.3	-	5.9	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$\overline{OE}$ to Yn; see Figure 6 and Figure 8	1.7	-	6.3	ns
t_{PLZ}	LOW to OFF-state propagation delay	$\overline{OE}$ to Yn; see Figure 6 and Figure 8	1.7	-	6.3	ns
$t_{sk(o)}$	output skew time	A to Yn; output-to-output; see Figure 7 and Figure 8	-	-	0.5	ns
$t_{sk(p)}$	pulse skew time	A to Yn; see Figure 7 and Figure 8	-	-	0.8	ns
$t_{sk(pr)}$	process skew time	A to Yn; part-to-part; see Figure 7 and Figure 8	-	-	1	ns
t_r	rise time	A to Yn; see Figure 5 and Figure 8	0.3	-	2.0	ns
t_f	fall time	A to Yn; see Figure 5 and Figure 8	0.3	-	2.0	ns

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Table 9: Switching characteristics

Temperature and V_{CC} coefficients over recommended operating free-air temperature and V_{CC} range. [1]

Symbol	Parameter	Conditions		Min	Max	Unit
$\Delta t_{PLH(T)}$	temperature coefficient of LOW-to-HIGH propagation delay A to Yn (average value)		[2]	-	65	ps/10 °C
$\Delta t_{PHL(T)}$	temperature coefficient of HIGH-to-LOW propagation delay A to Yn (average value)		[2]	-	45	ps/10 °C
$\Delta t_{PLH(V)}$	V_{CC} coefficient of LOW-to-HIGH propagation delay A to Yn (average value)		[3]	-	–140	ps/100 mV
$\Delta t_{PHL(V)}$	V_{CC} coefficient of HIGH-to-LOW propagation delay A to Yn (average value)		[3]	-	–120	ps/100 mV

[1] These data were extracted from characterization material and are not tested at the factory.

[2] $\Delta t_{PLH(T)}$ and $\Delta t_{PHL(T)}$ are virtually independent of V_{CC}.

[3] $\Delta t_{PLH(V)}$ and $\Delta t_{PHL(V)}$ are virtually independent of temperature.

10.1 AC waveforms

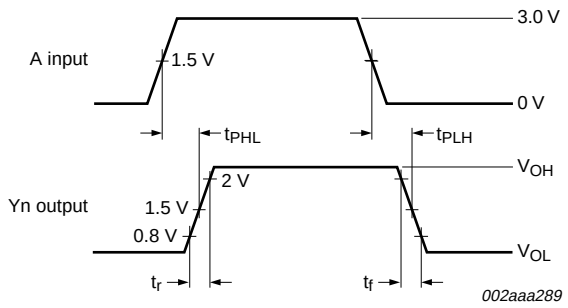

Fig 5. The input (A) to outputs (Yn) propagation delays and rise and fall times

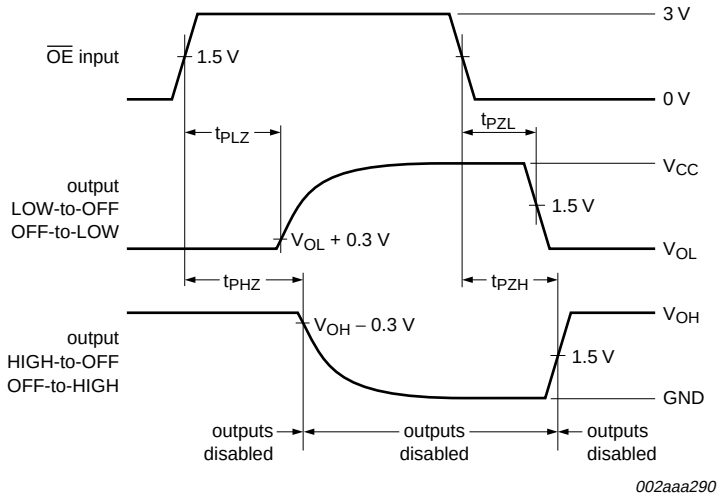

Fig 6. 3-state enable and disable times

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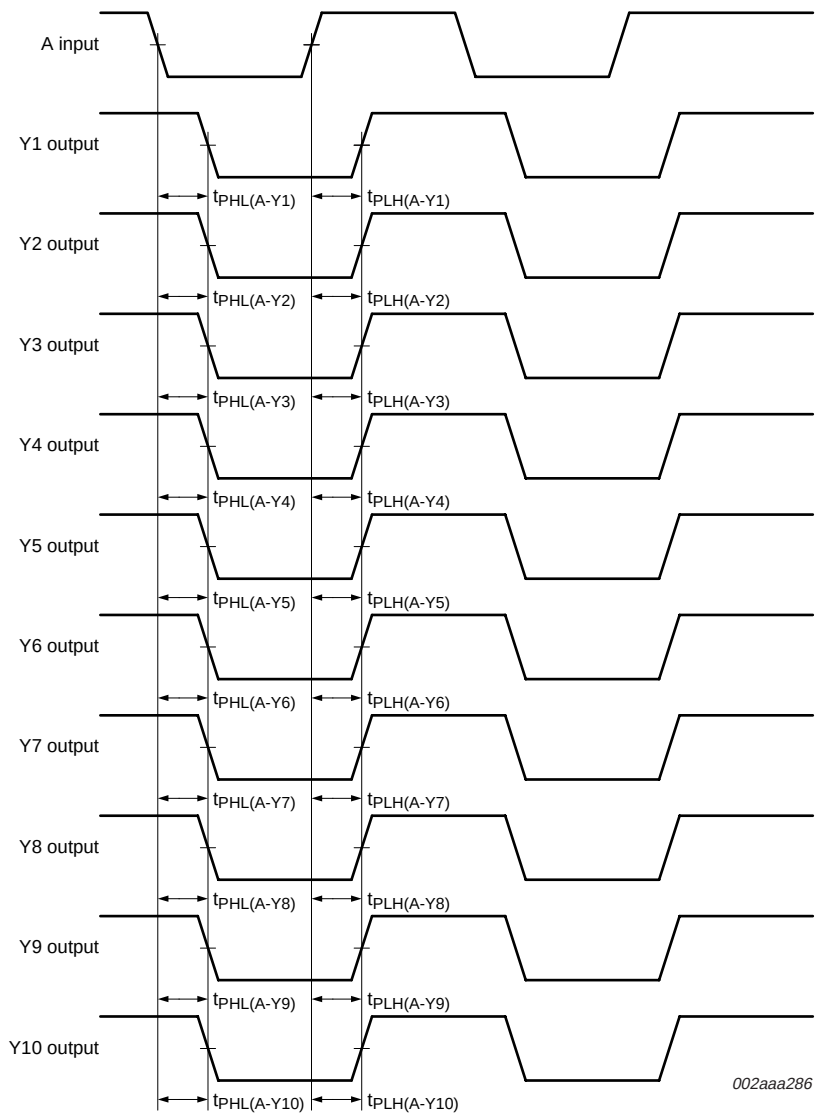

Output-to-output skew is the highest values of positive and negative edge skew: $t_{sk(o)} = t_{PLH(A\text{-}Yn)(max)} - t_{PLH(A\text{-}Yn)(min)}$ and $t_{sk(o)} = t_{PHL(A\text{-}Yn)(max)} - t_{PHL(A\text{-}Yn)(min)}$.

Output pulse skew is the highest value of: $t_{sk(p)} = |t_{PLH(A\text{-}Yn)} - t_{PHL(A\text{-}Yn)}|$.

Part-to-part skew $t_{sk(pr)}$ represents the positive and negative edge skew between outputs of several devices operating under identical conditions.

Fig 7. Calculation of $t_{sk(o)}$, $t_{sk(p)}$, and $t_{sk(pr)}$

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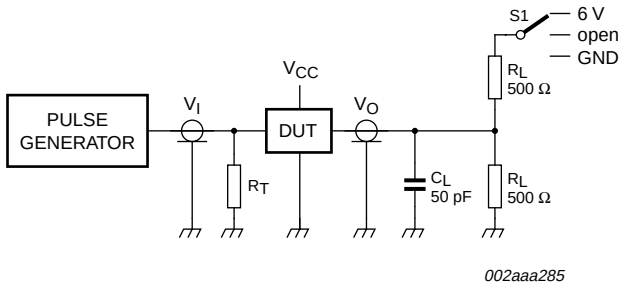
11. Test information



Test data are given in Table 10.

C_L = load capacitance includes jig and probe capacitance.

R_L = load resistance.

R_T = termination resistance.

Fig 8. Load circuitry for switching times

Table 10: Test data

Test	Load		Switch
	C_L	R_L	
t_{PLH}, t_{PHL}	50 pF	500 Ω	open
t_{PLZ}, t_{PZL}	50 pF	500 Ω	6 V
t_{PHZ}, t_{PZH}	50 pF	500 Ω	GND

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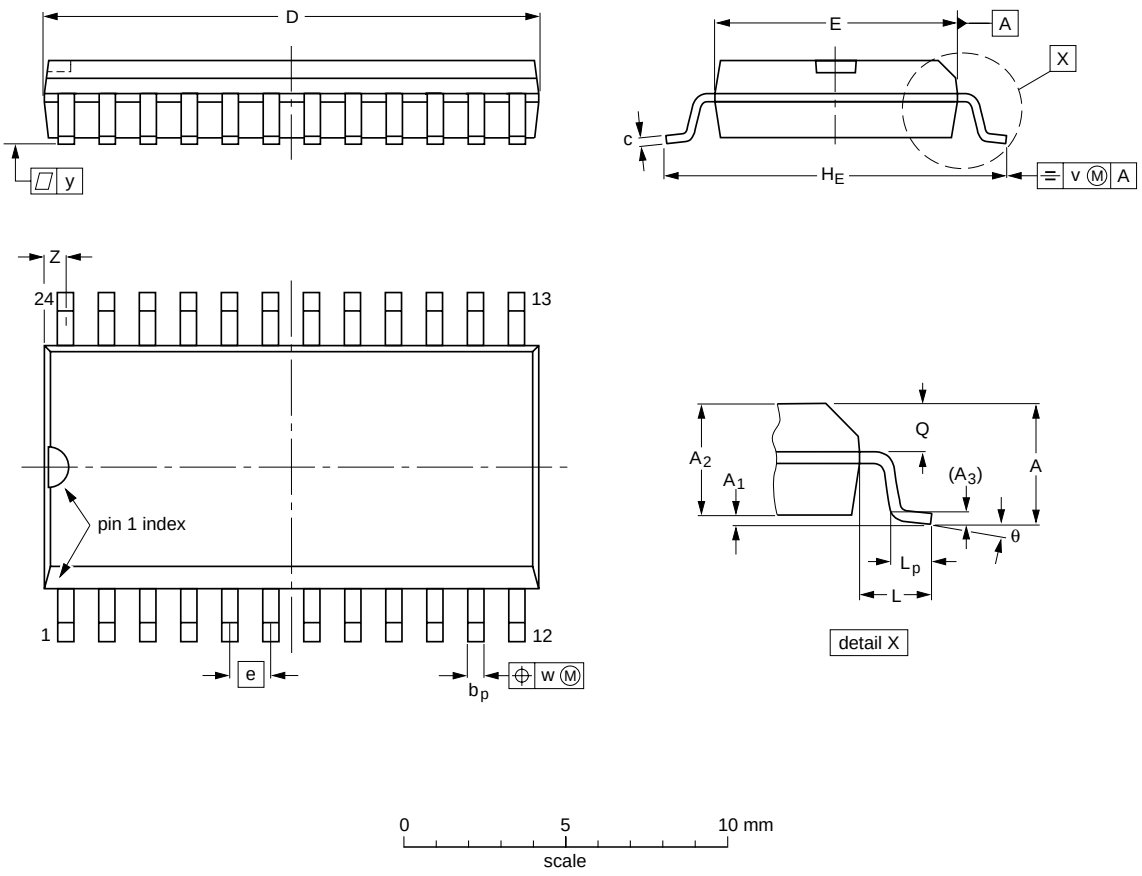
12. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

Fig 9. Package outline SOT137-1 (SO24)

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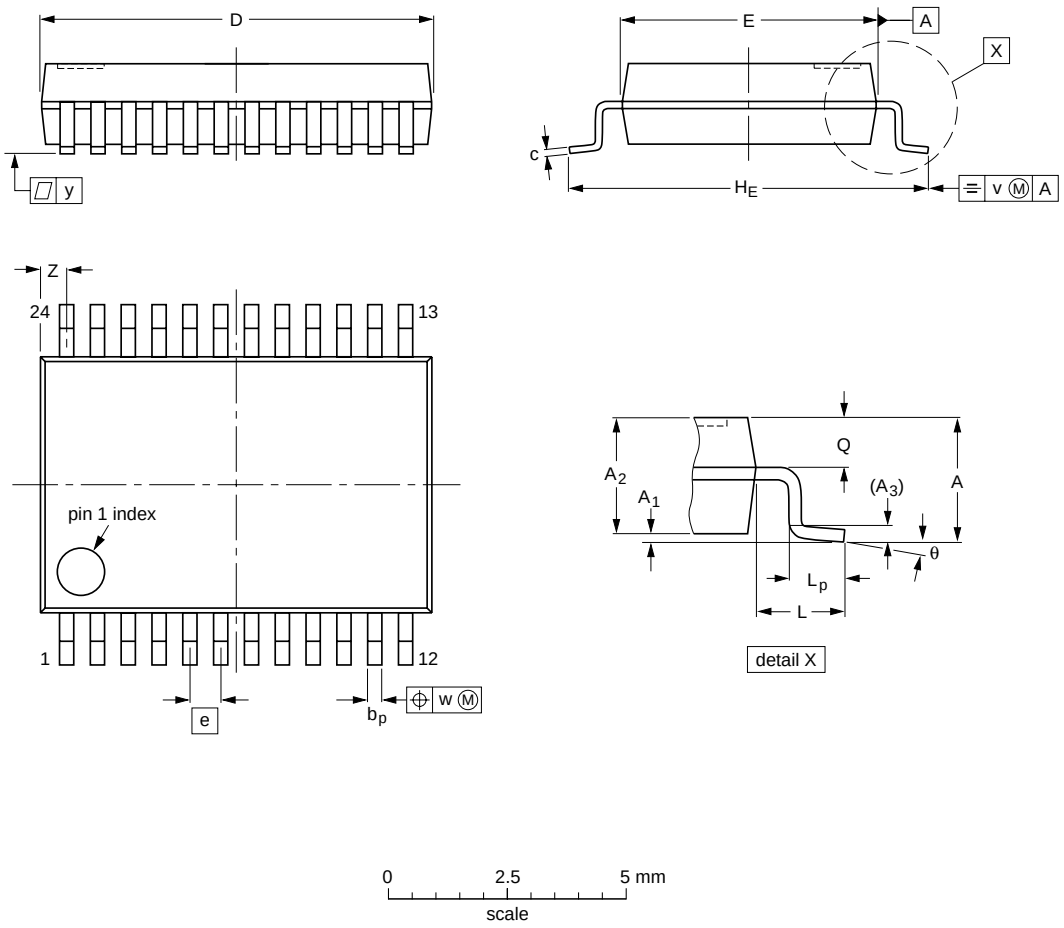
SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT340-1		MO-150				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT340-1 (SSOP24)

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13. Soldering

13.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

13.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

13.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

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– smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

13.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

13.5 Package related soldering information

Table 11: Suitability of surface mount IC packages for wave and reflow soldering methods

Package [1]	Soldering method	
	Wave	Reflow [2]
BGA, HTSSON..T [3], LBGA, LFBGA, SQFP, SSOP..T [3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [4]	suitable
PLCC [5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [5] [6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended [7]	suitable
CWQCCN..L [8], PMFP [9], WQCCN..L [8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

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[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

14. Revision history

Table 12: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PCK351_2	20051216	Product data sheet	-	-	PCK351-01
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • Section 2 “Features”: deleted (old) 12th bullet • Table 2 “Ordering information”: changed “Temperature range = –65 °C to +150 °C” to “T_{amb} = –40 °C to +85 °C” • Table 5 “Limiting values”: – removed (old) Table note [1]; this is now presented in the Definitions section – symbol “I_O” changed to “$I_{O(sink)}$” – row “I_{CC}, I_{GND}” split to 2 rows, and parameter for each revised • Table 6 “Recommended operating conditions”: – moved (old) Table note [1] to description below table title – split row “t_r, t_f” • Table 7 “Static characteristics”: changed parameter description of V_{IK} from “input diode voltage” to “input clamping voltage” • Table 8 “Dynamic characteristics”: – in descriptive line below table title: changed “$t_r = t_f = \leq 3.0$ ns” to “$t_r = t_f = \leq 2.5$ ns” – (V_{CC} = 3.3 V) typical value for t_{PLH} and t_{PHL} (A to Yn) changed from 3.6 ns to 3.8 ns – (V_{CC} = 3.3 V) typical value for t_{PHZ} and t_{PZH} ($\overline{OE}$ to Yn) changed from 4.0 ns to 3.8 ns – (V_{CC} = 3.3 V) t_r and t_f minimum values changed from “-” to “0.3 ns”; maximum values changed from “-” to “2.0 ns” – subheading “V_{CC} = 3.3 to 3.6 V; T_{amb} = 0 °C to +70 °C” changed to “V_{CC} = 3.0 V to 3.6 V; T_{amb} = –40 °C to +85 °C” – (V_{CC} = 3.0 V to 3.6 V) values for t_{PLH} and t_{PHL} (A to Yn) changed from “-” to “2.5 ns” (min), “3.3 ns” (typ), “5.9 ns” (max) – (V_{CC} = 3.0 V to 3.6 V) t_r and t_f minimum values changed from “-” to “0.3 ns”; maximum values changed from “-” to “2.0 ns”			
PCK351-01	20020514	Product data	853-2344 28198	9397 750 09791	-

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Level	Data sheet status [1]	Product status [2] [3]	Definition
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20. Contents

1	**General description**	**1**
2	**Features**	**1**
3	**Quick reference data**	**2**
4	**Ordering information**	**2**
5	**Functional diagram**	**3**
6	**Pinning information**	**4**
6.1	Pinning	4
6.2	Pin description	4
7	**Functional description**	**5**
7.1	Function table	5
7.2	Logic symbol	5
8	**Limiting values**	**6**
9	**Recommended operating conditions**	**6**
10	**Characteristics**	**7**
10.1	AC waveforms	9
11	**Test information**	**11**
12	**Package outline**	**12**
13	**Soldering**	**14**
13.1	Introduction to soldering surface mount packages	14
13.2	Reflow soldering	14
13.3	Wave soldering	14
13.4	Manual soldering	15
13.5	Package related soldering information	15
14	**Revision history**	**16**
15	**Data sheet status**	**17**
16	**Definitions**	**17**
17	**Disclaimers**	**17**
18	**Trademarks**	**17**
19	**Contact information**	**17**

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