PCF8536

Universal LCD driver for low multiplex rates including a 6 channel PWM generator

Rev. 2 — 21 February 2012 Product data sheet

1. General description

The PCF8536 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD)[1] with low multiplex rates. It generates the drive signals for any multiplexed LCD containing up to eight backplanes, up to 44 segments, and up to 320 elements. The PCF8536 is compatible with most microcontrollers and communicates via the two-line bidirectional I^2C-bus (PCF8536AT) or a three line unidirectional SPI-bus (PCF8536BT). Communication overheads are minimized using a display RAM with auto-incremented addressing.

The PCF8536 features an on-chip PWM controller for LED illumination. Up to six independent channels can be configured. Each channel has 128 levels allowing the possibility for two RGB controllers. Each of them provides over 2 million colors. Each channel can also be used for static drive.

2. Features and benefits

- Single-chip 320 segment LCD controller and driver with 6 channel PWM generator
- 6 channel PWM generator for backlight LED illumination
- Selectable display bias configuration
- Wide range for digital power supply: from 1.8 V to 5.5 V
- Wide LCD supply range: from 2.5 V for low threshold LCDs and up to 9.0 V for high threshold twisted nematic LCDs
- Low power consumption
- Selectable backplane drive configuration: 4, 6, or 8 backplane multiplexing
- LCD and logic supplies may be separated
- 320-bit RAM for display data storage
- 6 PWM outputs with a 7-bit resolution (128 steps) and drivers for external transistors
- Programmable PWM frame frequency to avoid LCD backlight flickering
- 400 kHz I^2C-bus interface (PCF8536AT)
- 5 MHz SPI-bus interface (PCF8536BT)
- Programmable frame frequency in the range of 60 Hz to 300 Hz in steps of 10 Hz; factory calibrated

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 19.

- 320 segments driven allowing:
  - up to 40 7-segment alphanumeric characters
  - up to 20 14-segment alphanumeric characters
  - any graphics of up to 320 elements
- Manufactured in silicon gate CMOS process

3. Applications

- White goods and consumer products

4. Ordering information

Table 1. Ordering information

Type number	Interface type	Package		
		Name	Description	Version
PCF8536AT/1	I^2C-bus	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1
PCF8536BT/1	SPI-bus	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1

5. Marking

Table 2. Marking codes

Type number	Marking code
PCF8536AT/1	PCF8536AT
PCF8536BT/1	PCF8536BT

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6. Block diagram

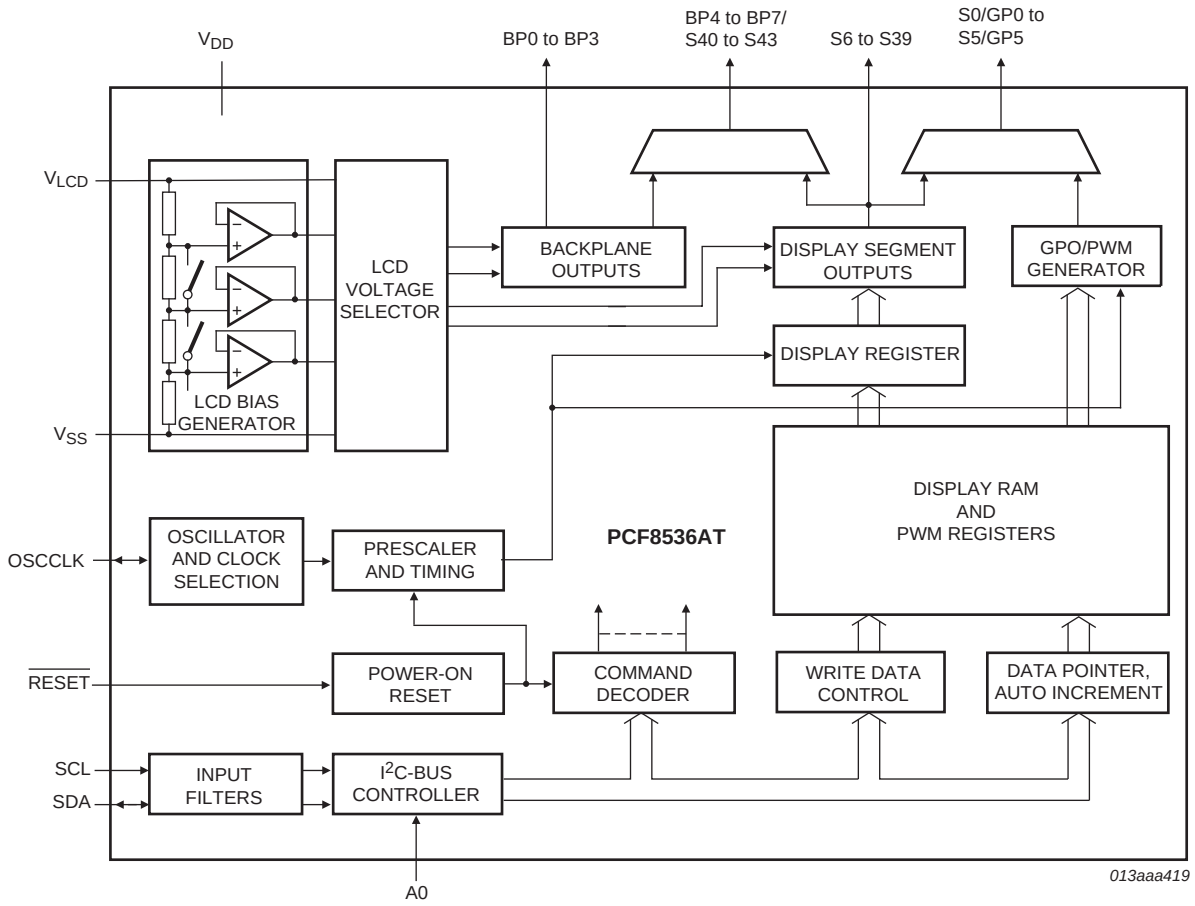


Fig 1. Block diagram of PCF8536AT

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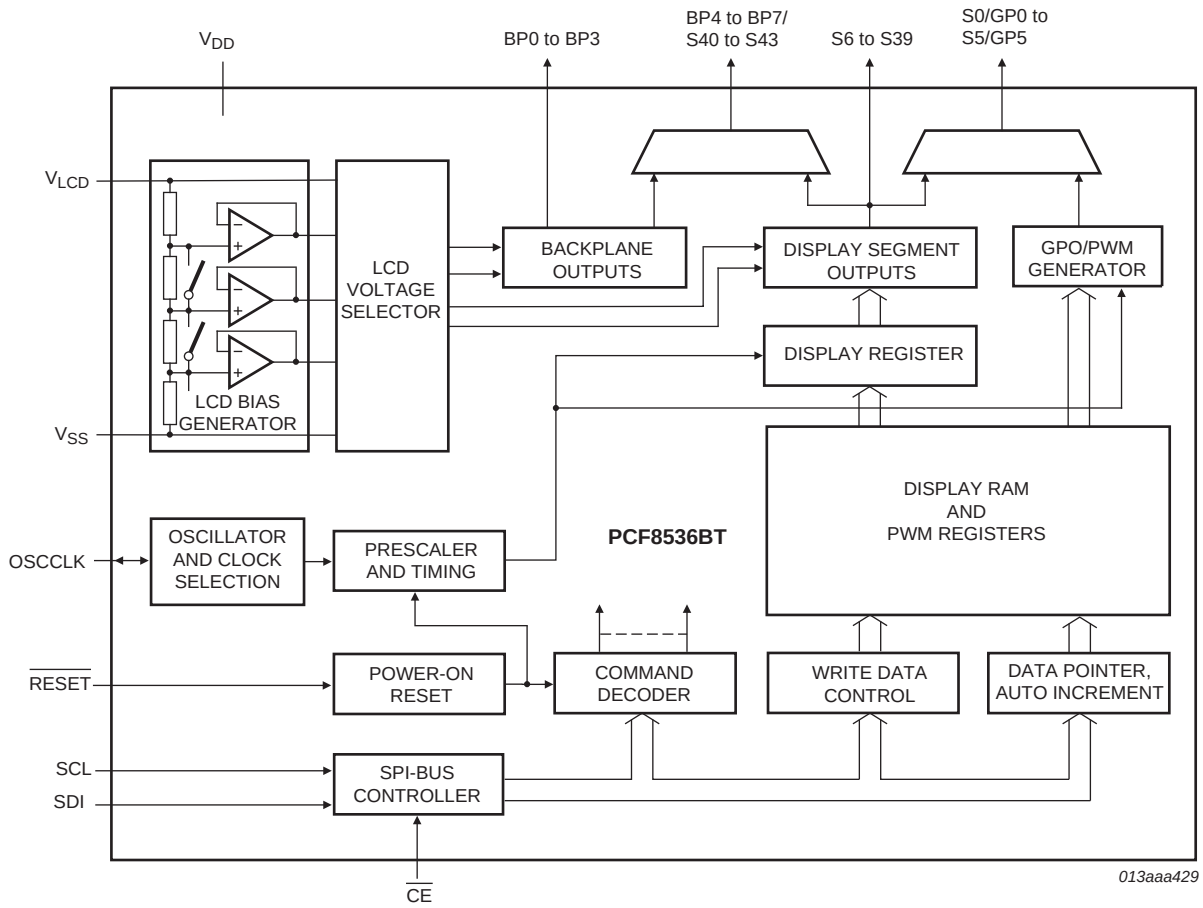


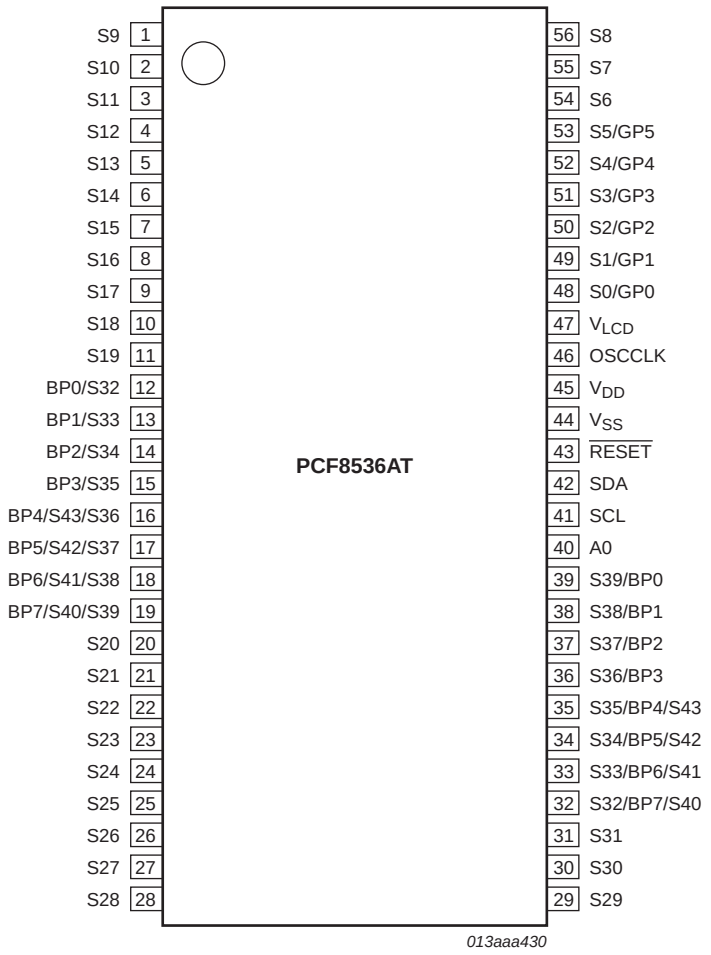
Fig 2. Block diagram of PCF8536BT

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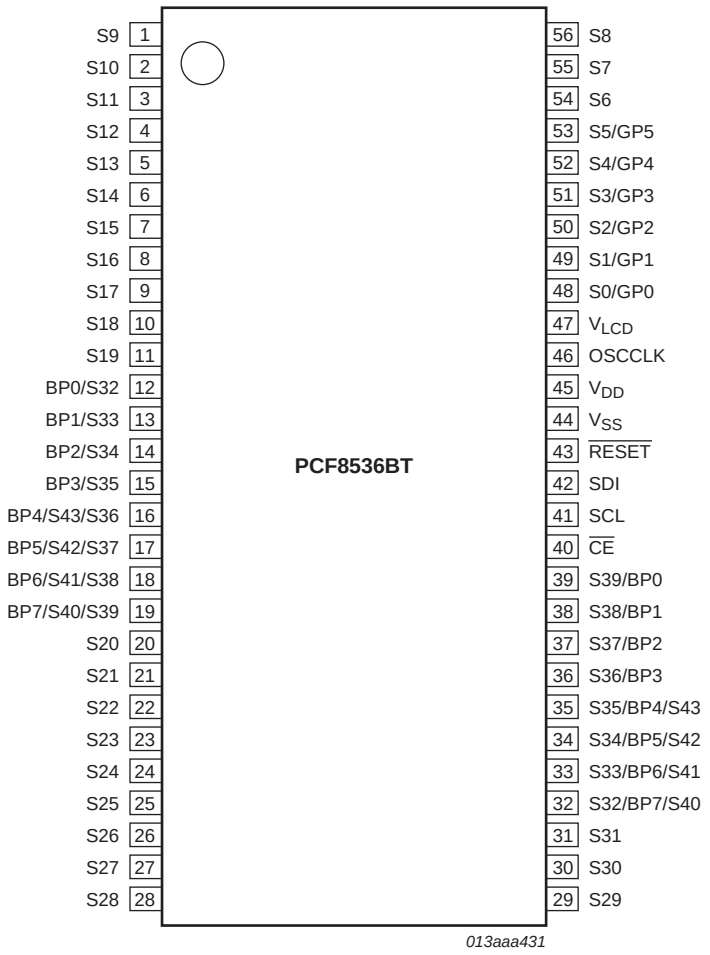
7. Pinning information

7.1 Pinning



Top view. For mechanical details, see Figure 51.

Fig 3. Pin configuration for TSSOP56 (PCF8536AT)



Top view. For mechanical details, see Figure 51.

Fig 4. Pin configuration for TSSOP56 (PCF8536BT)

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7.2 Pin description

Table 3. Pin description of PCF8536AT and PCF8536BT

Pin	Symbol		Type	Description
1 to 11	S9 to S19		output	LCD segment
20 to 31	S20 to S31		output	LCD segment
43	$\overline{\text{RESET}}$		input	active LOW reset input
44	V_{SS}		supply	ground supply voltage
45	V_{DD}		supply	supply voltage
46	OSCCLK		input/output	external clock input/internal oscillator output
47	V_{LCD}[1]		supply	LCD supply voltage
48 to 53	S0/GP0 to S5/GP5		output	LCD segment/GPO (PWM) output
54 to 56	S6 to S8		output	LCD segment
Pin layout depending on backplane swap configuration[2]				
	BPS = 0	**BPS = 1**[3]		
12	BP0	S32	output	LCD backplane/LCD segment
13	BP1	S33		
14	BP2	S34		
15	BP3	S35		
16	BP4/S43	S36		
17	BP5/S42	S37		
18	BP6/S41	S38		
19	BP7/S40	S39		
32	S32	BP7/S40		
33	S33	BP6/S41		
34	S34	BP5/S42		
35	S35	BP4/S43		
36	S36	BP3		
37	S37	BP2		
38	S38	BP1		
39	S39	BP0		
Pin layout depending on product and bus type				
	PCF8536AT	**PCF8536BT**		
40	A0		input	I²C-bus slave address selection
		$\overline{\text{CE}}$	input	SPI-bus chip enable - active LOW
41	SCL		input	I²C-bus serial clock
		SCL	input	SPI-bus serial clock
42	SDA		input/output	I²C-bus serial data
		SDI	input	SPI-bus data input

[1] V_{LCD} must be equal to or greater than V_{DD}.

[2] Effect of backplane swapping is illustrated in Figure 5 on page 10.

[3] Bit BPS is explained in Section 8.1.4 on page 9.

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8. Functional description

The PCF8536 is a versatile peripheral device designed to interface any microcontroller to a wide variety of LCDs and 6 backlight LEDs. It can directly drive any multiplexed LCD containing up to eight backplanes and up to 44 segments.

8.1 Commands of PCF8536

The PCF8536 is controlled by 15 commands, which are defined in Table 4. Any other combinations of operation code bits that are not mentioned in this document may lead to undesired operation modes of PCF8536.

Table 4. Commands of PCF8536

Command name	Register selection RS[1:0][1]		Bits								Reference
			7	6	5	4	3	2	1	0	
initialize	0	0	0	0	0	1	0	1	1	0	Section 8.1.1
OTP-refresh	0	0	1	1	1	1	0	0	0	0	Section 8.1.2
PWM-inversion	0	0	0	0	0	1	0	1	0	PWMI	Section 8.1.3
mode-settings	0	0	0	1	0	1	BPS	INV	PD	E	Section 8.1.4
oscillator-control	0	0	0	0	0	1	1	EFR	COE	OSC	Section 8.1.5
GPO-output-config	0	0	1	1	0	0	GPM1[1:0]		GPM0[1:0]		Section 8.1.6
	0	0	1	1	0	1	GPM3[1:0]		GPM2[1:0]		
	0	0	1	1	1	0	GPM5[1:0]		GPM4[1:0]		
set-MUX-mode	0	0	0	0	0	0	0	0	M[1:0]		Section 8.1.7
set-bias-mode	0	0	0	0	0	0	0	1	B[1:0]		Section 8.1.8
frame-frequency-LCD	0	0	0	0	1	FD[4:0]					Section 8.1.9
frame-frequency-PWM	0	0	0	1	0	0	FP[3:0]				Section 8.1.10
GPO-static-data	0	0	0	1	1	0	0	GPO2	GPO1	GPO0	Section 8.1.11
	0	0	0	1	1	0	1	GPO5	GPO4	GPO3	
load-data-pointer-LCD	0	0	1	0	DP[5:0]						Section 8.1.12
load-data-pointer-PWM	0	0	0	1	1	1	0	PP[2:0]			Section 8.1.13
write-RAM-data	0	1	D[7:0]								Section 8.1.14
write-PWM-data	1	0	0	P[6:0]							Section 8.1.15

[1] Information about control byte and register selection see Section 9.1 on page 46.

8.1.1 Command: initialize

This command generates a chip-wide reset. It has the same function as the $\overline{\text{RESET}}$ pin. Reset takes 1 ms to complete.

Table 5. Initialize - initialize command bit description

Bit	Symbol	Value	Description
7 to 0	-	00010110	fixed value

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8.1.2 Command: OTP-refresh

During production and testing of the device, each IC is calibrated to achieve the specified accuracy of the frame frequency. This calibration is performed on EPROM cells called One Time Programmable (OTP) cells. The device reads these cells every time the OTP-refresh command is sent. This instruction has to be sent after a reset has been made and before the display is enabled.

This command will be completed after a maximum of 30 ms and requires either the internal or external clock to run. If the internal oscillator is not used, then a clock must be supplied to the OSCCLK pin. If the OTP-refresh instruction is sent and no clock is present, then the request is stored until a clock is available.

Remark: It is recommended not to enter power-down mode during the OTP refresh cycle.

Table 6. OTP-refresh - OTP-refresh command bit description

Bit	Symbol	Value	Description
7 to 0	-	11110000	fixed value

8.1.3 Command: PWM-inversion

It is possible to invert the output of the PWM generators. This function may be useful for counteracting EMC issues. The description of this mode can be found in Section 8.11.2 on page 45.

Table 7. PWM-inversion - PWM inversion command bit description

Bit	Symbol	Value	Description
7 to 1	-	0001010	fixed value
0	PWMI		**PWM inversion mode**
		1	PWM inversion mode on
		0[1]	PWM inversion mode off

[1] Default value.

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8.1.4 Command: mode-settings

Table 8. Mode-settings - mode settings command bit description

Bit	Symbol	Value	Description
7 to 4	-	0101	fixed value
3	BPS		**backplane swapping**
		0[1]	backplane configuration 0
		1	backplane configuration 1
2	INV		**set inversion mode**
		0[1][2]	Driving scheme A: LCD line inversion mode
		1	Driving scheme B: LCD frame inversion mode
1	PD		**set power mode**
		1	power-down mode; backplane and segment outputs are connected to V_{SS} and the internal oscillator is switched off
		0[1]	power-up mode
0	E		**display switch**
		0[1]	display disabled; backplane and segment outputs are connected to V_{SS}
		1	display enabled

[1] Default value.

[2] See Section 8.1.4.2.

8.1.4.1 Backplane swapping

Backplane swapping can be configured with the BPS bit (see Table 8). It moves the location of the backplane and the associated segment outputs from one side of the PCF8536 to the other. Backplane swapping is sometimes desirable to aid with the routing of PCBs that do not use multiple layers.

The BPS bit has to be set to the required value before enabling the display. Failure to do so does not damage the PCF8536 or the display, however unexpected display content may appear.

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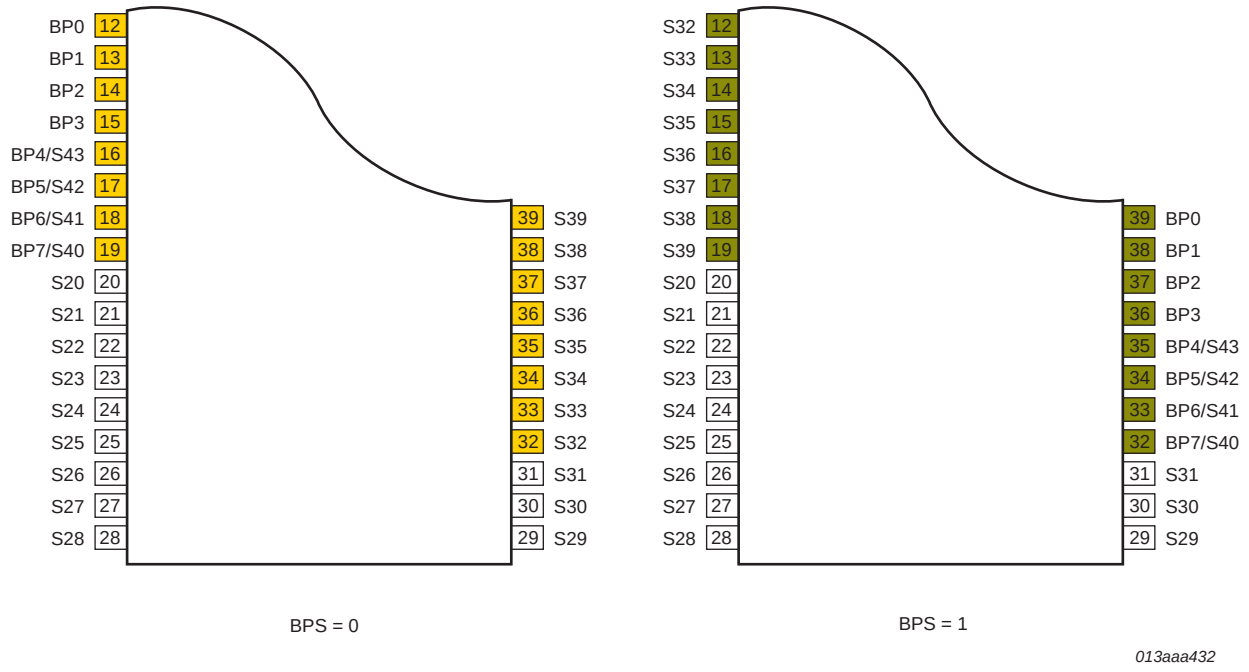


Fig 5. Effect of backplane swapping

8.1.4.2 Line inversion (driving scheme A) and frame inversion (driving scheme B)

The DC offset of the voltage across the LCD is compensated over a certain period: line-wise in line inversion mode (driving scheme A) or frame-wise in frame inversion mode (driving scheme B). With the INV bit (see Table 8), the compensation mode can be switched.

In frame inversion mode, the DC value is compensated across two frames and not within one frame. Changing the inversion mode to frame inversion reduces the power consumption; therefore it is useful when power consumption is a key point in the application.

Frame inversion may not be suitable for all applications. The RMS voltage across a segment is better defined; however, since the switching frequency is reduced, there is possibility for flicker to occur.

The waveforms of Figure 15 on page 29 to Figure 18 on page 32 are showing line inversion mode. Figure 19 on page 33 shows an example of frame inversion.

8.1.4.3 Power-down mode

The power-down bit (PD) allows the PCF8536 to be put in a minimum power configuration. In order to avoid display artefacts, it is recommended to enter power-down only after the display has been switched off by setting bit E to logic 0.

During power-down, the internal oscillator is switched off and any selected PWM output is revert to the static value stored in bits GPO0 to GPO5. These bits may be programmed to give a static logic 0 or static logic 1 on selected GP0 to GP5 pins.

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Table 9. Effect of the power-down bit (PD)

Effect on function	Mode settings	Effect of setting PD	
		0	1
backplane output	E = 1	normal function	V_{SS}
segment output	E = 1	normal function	V_{SS}
internal oscillator	OSC = 0, COE = 1	on	off
OSCCLK pin	OSC = 0, COE = 1	output of internal oscillator frequency	V_{DD}
OSCCLK pin	OSC = 1	input clock	clock input, can be logic 0, logic 1, or left floating
GPO	static drive	static drive	static drive
GPO	PWM drive	PWM drive	static drive

With the following sequence, the PCF8536 can be set to a state of minimum power consumption, called power-down mode.

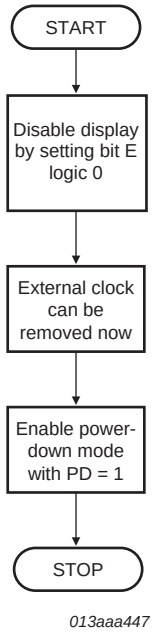


Fig 6. Recommended power-down sequence

Remarks:

- It is necessary to run the power-down sequence before removing the supplies. Depending on the application, care must be taken that no other signals are present at the chip input or output pins when removing the supplies (see Section 10). Otherwise it may cause unwanted display artifacts. In case of an uncontrolled removal of supply voltages, the PCF8536 will not be damaged.
- Static voltages across the liquid crystal display can build up when the external LCD supply voltage (V_{LCD}) is on while the IC supply voltage is off, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts, V_{LCD} and V_{DD} must be applied or removed together.

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- A clock signal must always be supplied to the device when the display is active. Removing the clock may freeze the LCD in a DC state, which is not suitable for the liquid crystal. It is recommended to disable the display first and afterwards to remove the clock signal.

8.1.4.4 Display enable

The display enable bit (E) is used to enable and disable the display. When the display is disabled, all LCD outputs go to V_{SS}. This function is implemented to ensure that no voltage can be induced on the LCD outputs as it may lead to unwanted displays of segments.

Recommended start-up sequences are found in Section 8.2.3

Remarks:

- The state of display enable has no effect on the GPO outputs.
- Display enable is not synchronized to an LCD frame boundary. Therefore using this function to flash a display for prolonged periods is not recommended due to the possible build-up of DC voltages on the display.

8.1.5 Command: oscillator-control

The oscillator-control command switches between internal and external oscillator and enables or disables the pin OSCCLK. It is also used to define what the external frequency will be.

Table 10. Oscillator-control - oscillator control command bit description

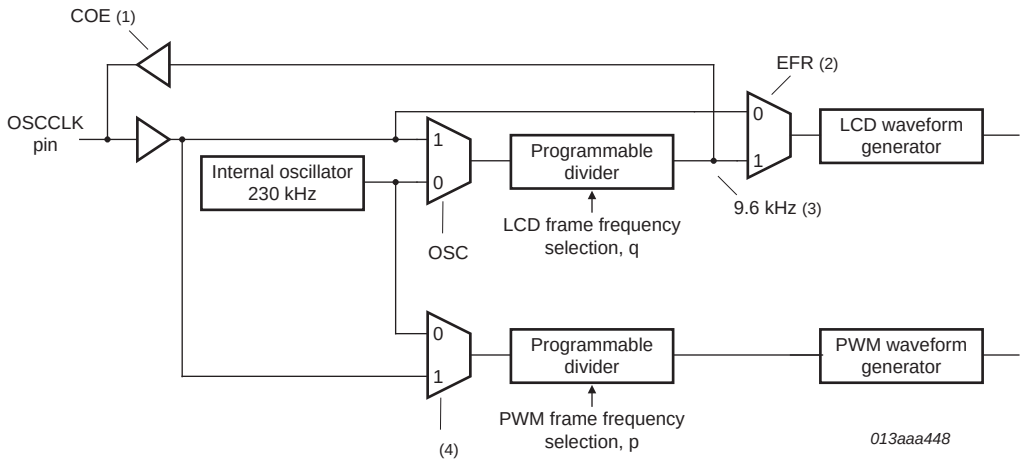
Bit	Symbol	Value	Description
7 to 3	-	00011	fixed value
2	EFR		**external clock frequency** applied on pin OSCCLK
		0[1]	9.6 kHz
		1	230 kHz
1	COE		**clock output enable for pin OSCCLK**
		0[1]	clock signal not available on pin OSCCLK; pin OSCCLK is in 3-state
		1	clock signal available on pin OSCCLK
0	OSC		**oscillator source**
		0[1]	internal oscillator running
		1	external oscillator used; pin OSCCLK becomes an input; used in combination with EFR to determine input frequency

[1] Default value.

The bits OSC, COE, and EFR control the source and frequency of the clock used to generate the LCD and PWM signals (see Figure 7). Valid combinations are shown in Table 11.

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(1) Can only be used with the internal oscillator (OSC = 0).

(2) Can only be used with an external oscillator (OSC = 1).

(3) Nominal value for divide factor q is 24; source clock is 230 kHz (see Section 8.1.9).

(4) PWM requires an external or internal 230 kHz clock.

Fig 7. Oscillator selection

Table 11. Valid combinations of bits OSC, EFR, and COE

OSC	COE	EFR	OSCCLK pin	Clock source
0	0	not used	inactive; may be left floating	internal oscillator used
0	1	not used	output of internal oscillator frequency (prescaler)	internal oscillator used
1	not used	0	9.6 kHz input	OSCCLK pin
1	not used	1	230 kHz input	OSCCLK pin

Table 12. Typical use of bits OSC, EFR, and COE

Usage	OSC	CDE	EFR
LCD and/or PWM with internal oscillator	0	0	not used
LCD and PWM with external oscillator	1	not used	1
LCD with external oscillator	1	not used	0

8.1.5.1 Oscillator

The internal logic and LCD drive signals of the PCF8536 are timed either by the built-in oscillator or from an external clock.

Internal clock: When the internal oscillator is used, all LCD and PWM signals are generated from it. The oscillator runs at nominal 230 kHz. The relationship between this frequency and the LCD frame frequency is detailed in Section 8.1.9. The relationship between this frequency and the PWM frame frequency is detailed in Section 8.1.10.

Control over the internal oscillator is made with the OSC bit (see Section 8.1.5). The internal oscillator is also switched on or off under certain combinations of modes which are described in Table 13.

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Table 13. Internal oscillator on/off table

PD	OSC	PWM	EFR	Internal oscillator state[1]
power-down	n.a.	n.a.	n.a.	off
power-up	internal oscillator	n.a.	n.a.	on
	external oscillator	off	n.a.	off
		on	9.6 kHz	on[2]
		on	230 kHz	off

[1] When $\overline{\text{RESET}}$ is active, the internal oscillator is off.

[2] Special case. The PWM generator needs 230 kHz and must be enabled when PWM is enabled.

It is possible to make the internal oscillator signal available on pin OSCCLK by using the oscillator-control command (see Table 10) and configuring the clock output enable (COE) bit. If not required, the pin OSCCLK should be left open or connected to V_{SS}. At power-on the signal at pin OSCCLK is disabled and pin OSCCLK is in 3-state.

Clock output is only valid when using the internal oscillator. The signal will appear on the OSCCLK pin.

An intermediate clock frequency is available at the OSCCLK pin. The duty cycle of this clock varies with the chosen divide ratio.

Table 14. OSCCLK table

PD	OSC	COE	EFR	OSCCLK pin[1]
power-down	n.a.	off	n.a.	3-state[2]
power-down	n.a.	on	n.a.	V_{DD}
power-up	internal oscillator	off	n.a.	3-state
		on	n.a.	9.6 kHz output[3]
	external oscillator	n.a.	9.6 kHz	9.6 kHz input
			230 kHz	230 kHz input

[1] When $\overline{\text{RESET}}$ is active, the pin OSCCLK is in 3-state.

[2] In this state, an external clock may be applied, but it is not a requirement.

[3] 9.6 kHz is the nominal frequency with q = 24, see Table 15.

External clock: In applications where an external clock must be applied to the PCF8536, bit OSC (see Table 10) has to be set logic 1. In this case pin OSCCLK becomes an input.

The OSCCLK signal must switch between the V_{SS} and the V_{DD} voltage supplied to the chip.

The system is designed for a 230 kHz clock or alternatively for using a 9.6 kHz clock. The EFR bit determines the external clock frequency. The clock frequency ($f_{clk(ext)}$) in turn determines the LCD frame frequency, see Table 15.

The PWM generator requires a 230 kHz clock to operate. If PWM is enabled and an external clock of 9.6 kHz is selected, then the internal oscillator will automatically start and be used for the PWM signal generation.

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Remark: If an external clock is used, then this clock signal must always be supplied to the device when the display is on. Removing the clock may freeze the LCD in a DC state which will damage the LCD material.

8.1.5.2 Timing and frame frequency

The timing of the PCF8536 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. The timing also generates the LCD frame frequency which it derives as an integer division of the clock frequency (see Table 15). The frame frequency is a fixed division of the internal clock or of the frequency applied to pin OSCCLK when an external clock is used.

Table 15. LCD frame frequencies

Frame frequency	Typical external frequency (Hz)	Nominal frame frequency (Hz)	EFR bit	Value of q[1]
$f_{fr(LCD)} = \frac{f_{clk(ext)}}{48}$	9600	200	0	-
$f_{fr(LCD)} = \frac{f_{clk(ext)}}{48 \cdot q}$	230000	200	1	24

[1] Other values of the frame frequency prescaler see Table 21.

When the internal clock is used, or an external clock with EFR = 1, the LCD frame frequency can be programmed by software in steps of approximately 10 Hz in the range of 60 Hz to 300 Hz (see Table 21). Furthermore the internal oscillator is factory calibrated, see Table 44 on page 59.

8.1.6 Command: GPO-output-config

The behavior of the combined LCD and GPO outputs S5/GP5 to S0/GP0 is configured with the bits described in Table 16.

Table 16. GPO-output-config - output mode config command for S5/GP5 to S0/GP0

Bit	Symbol	Value	Description
GPM0 and GPM1			
7 to 4	-	1100	fixed value
3 to 2	GPM1[1:0]	see Table 17	output mode for S1/GP1
1 to 0	GPM0[1:0]	see Table 17	output mode for S0/GP0
GPM2 and GPM3			
7 to 4	-	1101	fixed value
3 to 2	GPM3[1:0]	see Table 17	output mode for S3/GP3
1 to 0	GPM2[1:0]	see Table 17	output mode for S2/GP2
GPM4 and GPM5			
7 to 4	-	1110	fixed value
3 to 2	GPM5[1:0]	see Table 17	output mode for S5/GP5
1 to 0	GPM4[1:0]	see Table 17	output mode for S4/GP4

Each output can be individually configured to be either an LCD segment output, a PWM output or a static general-purpose output (GPO), see Table 17.

Remark: Even if using GPO only, V_{LCD} must still be applied to the device.

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Table 17. GPMO mode definition

GPM0[1:0] to GPM5[1:0]	Mode	Description
00[1], 01	LCD	output is an LCD segment
10	static	output is static GPO
11	PWM	output is PWM GPO

[1] Default value.

8.1.7 Command: set-MUX-mode

The multiplex drive mode is configured with the bits described in Table 18.

Table 18. Set-MUX-mode - set multiplex drive mode command bit description

Bit	Symbol	Value	Description
7 to 2	-	000000	fixed value
1 to 0	M[1:0]	00[1], 01	1:8 multiplex drive mode; eight backplanes
		10	1:6 multiplex drive mode; 6 backplanes
		11	1:4 multiplex drive mode; 4 backplanes

[1] Default value.

8.1.8 Command: set-bias-mode

The set-bias-mode command allows setting the bias level.

Table 19. Set-bias-mode - set bias mode command bit description

Bit	Symbol	Value	Description
7 to 2	-	000001	fixed value
1 to 0	B[1:0]	00[1], 01	$\frac{1}{4}$ bias
		11	$\frac{1}{3}$ bias
		10	$\frac{1}{2}$ bias

[1] Default value.

8.1.9 Command: frame-frequency-LCD

With the frame-frequency-LCD command, the frame frequency for the display can be configured. The clock frequency determines the frame frequency.

Table 20. Frame-frequency-LCD - frame frequency and output clock frequency command bit description

Bit	Symbol	Value	Description
7 to 5	-	001	fixed value
4 to 0	FD[4:0]	see Table 21	frequency prescaler

The system is designed for a 230 kHz clock. It is either internally generated or externally provided. Alternatively a 9.6 kHz clock signal can be provided as well. The EFR bit (see Table 10) has to be set according to the external clock frequency.

When EFR is set to 9.6 kHz, then the LCD frame frequency is calculated with Equation 1:

$$f_{fr(LCD)} = \frac{f_{clk(ext)}}{48} \quad (1)$$

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When EFR is set to 230 kHz, then the LCD frame frequency is calculated with Equation 2:

$$f_{fr(LCD)} = \frac{f_{clk(ext)}}{48 \cdot q} \quad (2)$$

where q is the frequency divide factor (see Table 21).

Remark: $f_{clk(ext)}$ is the external input clock frequency to pin OSCCLK.

When the internal oscillator is used, the intermediate frequency may be output on the OSCCLK pin. Its frequency is given in Table 21.

Table 21. Frame frequency prescaler values for 230 kHz clock operation

FD[4:0]	Nominal LCD frame frequency (Hz)[1]	Divide factor, q	Intermediate clock frequency (Hz)
00000	59.9	80	2875
00001	70.5	68	3382
00010	79.9	60	3833
00011	90.4	53	4340
00100	99.8	48	4792
00101	108.9	44	5227
00110	119.8	40	5750
00111	129.5	37	6216
01000	140.9	34	6765
01001	149.7	32	7188
01010	159.7	30	7667
01011	171.1	28	8214
01100	177.5	27	8519
01101	191.7	25	9200
01110[2]	199.7	24	9583
01111	208.3	23	10000
10000	217.8	22	10455
10001	228.3	21	10952
10010	239.6	20	11500
10011	252.2	19	12105
10100	266.2	18	12778
10101	281.9	17	13529
10110	299.5	16	14375
10111 to 11111	not used		

[1] Nominal frame frequency calculated for the default clock frequency of 230 kHz.

[2] Default value.

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8.1.10 Command: frame-frequency-PWM

With the frame-frequency-PWM command, the frame frequency for the PWM signal can be set.

The PWM system requires a clock of 230 kHz either internally generated or externally supplied. Using a slower clock may result in visible flickering of LEDs driven with the PWM signal.

When EFR is set to 230 kHz, then the PWM frame frequency will be calculated with Equation 3:

$$f_{PWM} = \frac{f_{clk(ext)}}{128 \cdot p} \quad (3)$$

where p is the frequency divide factor (see Table 23).

Table 22. Frame-frequency-PWM - PWM frame frequency command bit description

Bit	Symbol	Value	Description
7 to 4	-	0100	fixed value
3 to 0	FP[3:0]	see Table 23	frequency prescaler

Table 23. PWM frame frequency prescaler values for 230 kHz clock operation

FP[3:0]	Nominal PWM frame frequency (Hz)[1]	Divide factor, p
0000	59.9	30
0001	69.1	26
0010	81.7	22
0011	89.8	20
0100	99.8	18
0101	112.3	16
0110	119.8	15
0111[2]	128.3	14
1000	138.2	13
1001	149.7	12
1010	163.4	11
1011	179.7	10
1100	199.7	9
1101	224.6	8
1110	256.7	7
1111	299.5	6

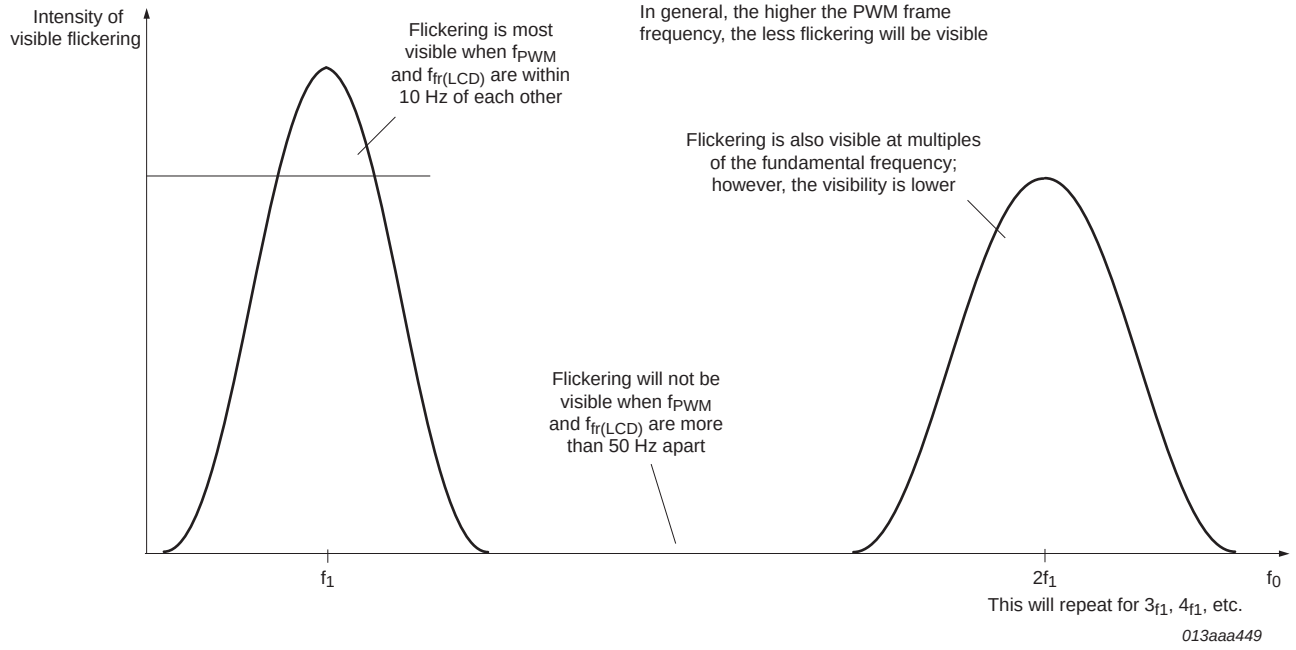
[1] Nominal frame frequency calculated for the default clock frequency of 230 kHz.

[2] Default value.

In order to avoid flickering caused by the interaction of the backlight LED and the LCD frame frequency, the PWM frame frequency should be programmed to be more than 50 Hz different from LCD frame frequency or multiples of the LCD frame frequency (see Figure 8 and Table 49 on page 68).

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Where $f_0 = f_{PWM}$ and $f_1 = f_{fr(LCD)}$ or $f_1 = f_{PWM}$ and $f_0 = f_{fr(LCD)}$.

Fig 8. Flicker avoidance for LED backlighting

8.1.11 Command: GPO-static-data

When static GPOs are selected instead of PWM, then the value for the output is taken from these register bits. The output is a static level.

Table 24. GPO-static-data - write GPO data for GP0 to GP5 command bit description

Bit	Symbol	Value	Description
GPO0 to GPO2			
7 to 3	-	01100	fixed value
2	GPO2	0[1]	0 level output on pin GP2
		1	1 level output on pin GP2
1	GPO1	0[1]	0 level output on pin GP1
		1	1 level output on pin GP1
0	GPO0	0[1]	0 level output on pin GP0
		1	1 level output on pin GP0
GPO3 to GPO5			
7 to 3	-	01101	fixed value
2	GPO5	0[1]	0 level output on pin GP5
		1	1 level output on pin GP5
1	GPO4	0[1]	0 level output on pin GP4
		1	1 level output on pin GP4
0	GPO3	0[1]	0 level output on pin GP3
		1	1 level output on pin GP3

[1] Default value.

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8.1.12 Command: load-data-pointer-LCD

The load-data-pointer-LCD command defines the start address of the display RAM. The data pointer is auto incremented after each RAM write. The size of the display RAM is dependent on the current multiplex drive mode setting, see Table 25.

Table 25. Load-data-pointer-LCD - load data pointer command bit description

Bit	Symbol	Value	Description
7 to 6	-	10	fixed value
Multiplex drive mode 1:8			
5 to 0	DP[5:0]	000000[1] to 100111	6-bit binary value of 0 to 39
Multiplex drive mode 1:6			
5 to 0	DP[5:0]	000000[1] to 101001	6-bit binary value of 0 to 41
Multiplex drive mode 1:4			
5 to 0	DP[5:0]	000000[1] to 101011	6-bit binary value of 0 to 43

[1] Default value.

Remark: Data pointer values outside of the valid range will be ignored and no RAM content will be transferred until a valid data pointer value is set.

Filling of the display RAM is described in Section 8.9.

8.1.13 Command: load-data-pointer-PWM

The load-data-pointer-PWM command defines one of the 6 PWM addresses.

Table 26. Load-data-pointer-PWM - load data pointer command bit description

Bit	Symbol	Value	Description
7 to 3	-	01110	fixed value
2 to 0	PP[2:0]	000[1] to 101	3-bit binary value of 0 to 5

[1] Default value.

Remark: Data pointer values outside of the valid range will be ignored and no PWM content will be transferred until a valid data pointer value is set.

8.1.14 Command: write-RAM-data

This command will initiate the transfer of data to the display RAM. Data will be written into the address defined by the load-data-pointer-LCD command. RAM filling is described in Section 8.9.

Table 27. Write-RAM-data - write RAM data command bit description[1]

Bit	Symbol	Value	Description
7 to 0	D[7:0]	00000000 to 11111111[2]	writing data byte-wise to RAM

[1] For this command to be effective bit RS[1:0] of the control byte has to be set logic 01, see Table 36 on page 46.

[2] After Power-On Reset (POR), the RAM content is random and should be brought to a defined status by writing meaningful content otherwise unexpected display content may appear.

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8.1.15 Command: write-PWM-data

This command will initiate the transfer of data to the PWM registers. Data will be written into the address defined by the load-data-pointer-PWM command. PWM register filling is described in Section 8.10

Table 28. Write-PWM-data - write PWM data command bit description[1]

Bit	Symbol	Value	Description
7	-	0	fixed value
6 to 0	P[6:0]	0000000[2] to 1111111	writing data byte-wise to PWM registers

[1] For this command to be effective bit RS[1:0] of the control byte has to be set logic 10, see Table 36 on page 46.

[2] Default value. After Power-On Reset (POR) the PWM content is set to 0.

8.2 Start-up and shut-down

8.2.1 Reset and Power-On Reset (POR)

After a reset and at power-on the PCF8536 resets to starting conditions as follows:

1. The display is disabled.
2. All backplane outputs are set to V_{SS}.
3. All segment outputs are set to V_{SS}.
4. All GPO outputs are disabled.
5. Selected drive mode is: 1:8 with $\frac{1}{4}$ bias.
6. The data pointers are cleared (set logic 0).
7. PWM values are all reset to zero.
8. RAM data is not initialized. Its content can be considered to be random.
9. The internal oscillator is running; no clock signal is available on pin OSCCLK; pin OSCCLK is in 3-state.

The reset state is as shown in Table 29.

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Table 29. Reset state

Reset state of configurable bits shown in the command table format for clarity.

Associated command	Bits							
	7	6	5	4	3	2	1	0
PWM-inversion								PWMI = 0
mode-settings	-	-	-	-	BPS = 0	INV = 0	PD = 0	E = 0
oscillator-control	-	-	-	-	-	EFR = 0	COE = 0	OSC = 0
GPO-output-config	-	-	-	-	GPM1[1:0] = 00		GPM0[1:0] = 00	
	-	-	-	-	GPM3[1:0] = 00		GPM2[1:0] = 00	
	-	-	-	-	GPM5[1:0] = 00		GPM4[1:0] = 00	
set-MUX-mode	-	-	-	-	-	-	M[1:0] = 00	
set-bias-mode	-	-	-	-	-	-	B[1:0] = 00	
frame-frequency-LCD	-	-	-	FD[4:0] = 01110				
frame-frequency-PWM	-	-	-	-	FP[3:0] = 0111			
GPO-static-data	-	-	-	-	-	GPO2 = 0	GPO1 = 0	GPO0 = 0
	-	-	-	-	-	GPO5 = 0	GPO4 = 0	GPO3 = 0
load-data-pointer-LCD	-	-	DP[5:0] = 00 0000					
load-data-pointer-PWM	-	-	-	-	-	PP[2:0] = 000		

The first command sent to the device after the power-on event must be the initialize command (see Section 8.1.1).

After Power-On Reset (POR) and before enabling the display, the RAM content should be brought to a defined state by writing meaningful content (e.g. a graphic) otherwise unwanted display artifacts may appear on the display.

8.2.2 $\overline{\text{RESET}}$ pin function

The $\overline{\text{RESET}}$ pin of the PCF8536 will reset all the registers to their default state. The reset state is given in Table 29. The RAM contents will remain unchanged. After the reset signal is removed, the PCF8536 will behave in the same manner as after Power-On Reset (POR). See Section 8.2.1 for details.

8.2.3 Recommended start-up sequences

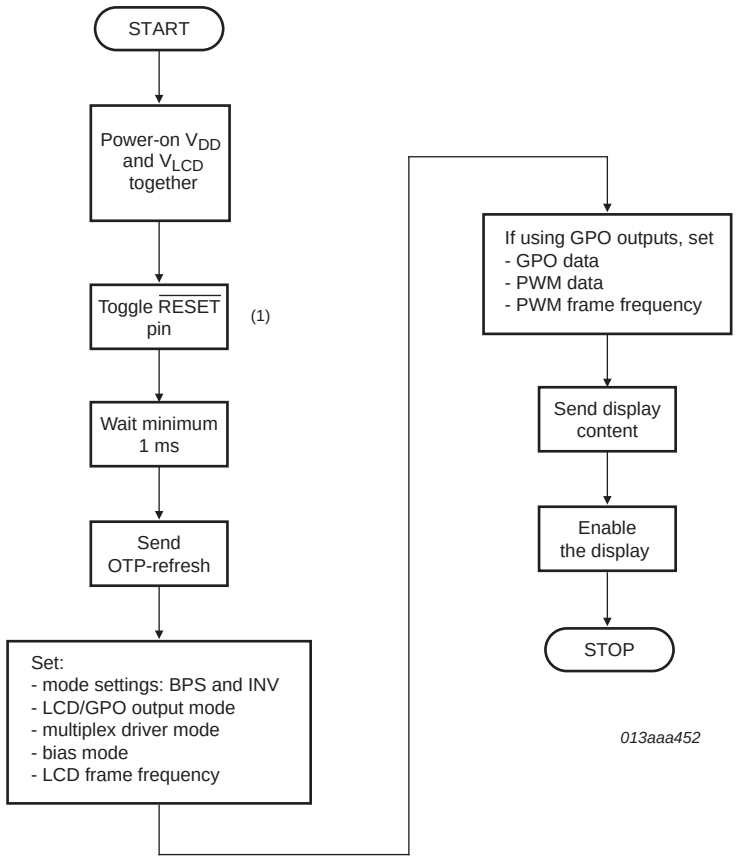
This chapter describes how to proceed with the initialization of the chip in different application modes.

In general, the sequence should always be:

1. Power-on the device,
2. set the display and functional modes,
3. fill the display memory and then
4. turn on the display.

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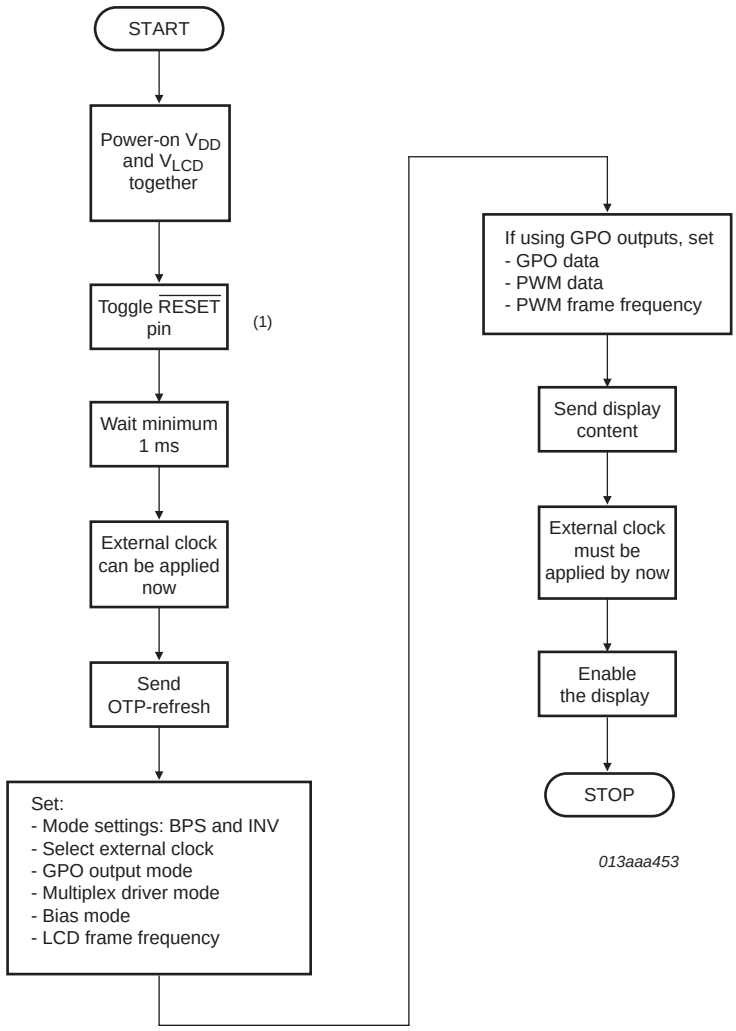


(1) Alternatively, it is possible to send the initialize command.

Fig 9. Recommended start-up sequence when using the internal oscillator

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(1) Alternatively, it is possible to send the initialize command.

Fig 10. Recommended start-up sequence when using an external clock signal

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8.3 Possible display configurations

The PCF8536 is a versatile peripheral device designed to interface between any microcontroller to a wide variety of LCD segment or dot matrix displays (see Figure 11). It can drive multiplexed LCD with 4, 6, or 8 backplanes and up to 44 segments.

The display configurations possible with the PCF8536 depend on the number of active backplane outputs required. A selection of possible display configurations is given in Table 30.

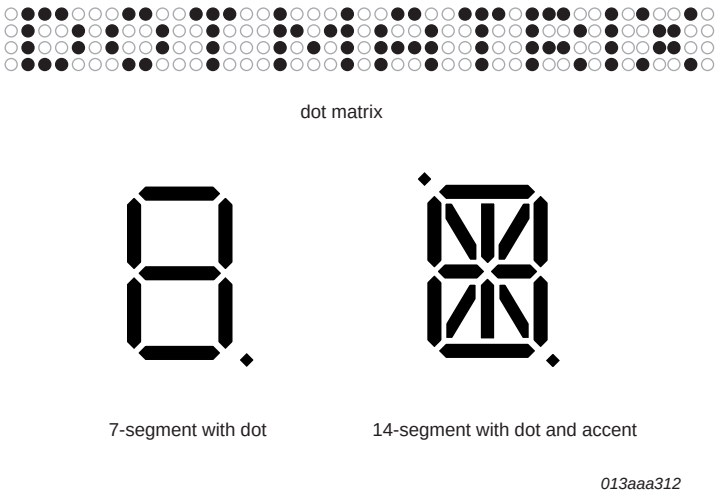


Fig 11. Example of displays suitable for PCF8536

Table 30. Selection of display configurations

Number of			Digits/Characters		Dot matrix/ Elements
Backplanes	Segments	Icons	7 segment[1]	14 segment[2]	
No GPO or PWM outputs enabled					
8	40	320	40	20	320
6	42	252	31	15	252
4	44	176	22	11	176
With 6 GPO or PWM outputs enabled					
8	34	272	34	17	272
6	36	216	27	13	216
4	38	152	19	9	152

[1] 7 segment display has 8 elements including the decimal point.

[2] 14 segment display has 16 elements including decimal point and accent dot.

All of the display configurations in Table 30 can be implemented in the typical systems shown in Figure 12 and Figure 13.

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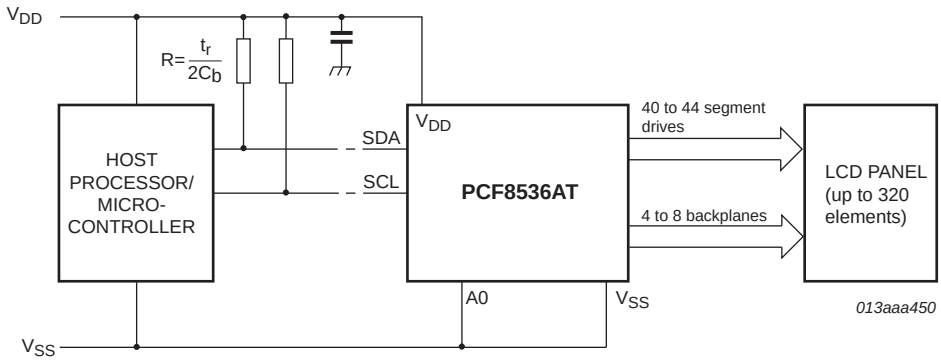


Fig 12. Typical system configuration for the I²C-bus

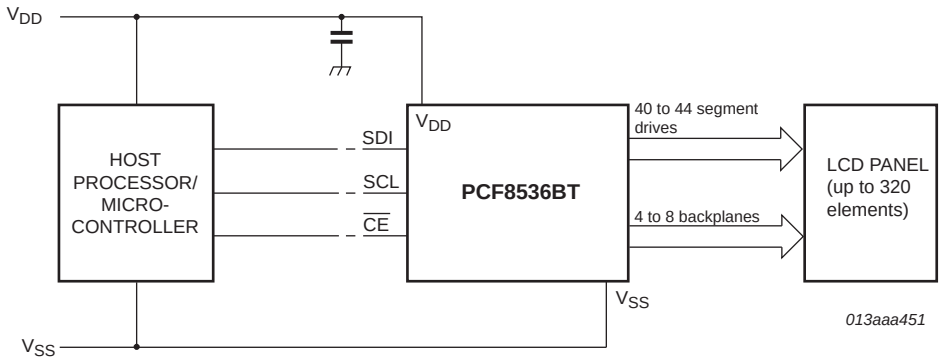


Fig 13. Typical system configuration for the SPI-bus

The host microcontroller maintains the two line I²C-bus or a three line SPI-bus communication channel with the PCF8536. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are the power supplies (V_{DD}, V_{SS}, V_{LCD}) and the LCD panel selected for the application.

The minimum recommended values for external capacitors on V_{DD} and V_{LCD} are 100 nF respectively. Decoupling of V_{LCD} will help to reduce display artifacts. The decoupling capacitors should be placed close to the IC with short connections to the respective supply pin and V_{SS}.

8.4 LCD voltage selector

The LCD voltage selector co-ordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by the set-bias-mode command (see Table 19) and the set-MUX-mode command (see Table 18).

Fractional LCD biasing voltages are obtained from an internal voltage divider. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of V_{LCD} and the resulting discrimination ratios (D), are given in Table 31.

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Discrimination is a term which is defined as the ratio of the on and off RMS voltage across a segment. It can be thought of as a measurement of contrast.

Table 31. Preferred LCD drive modes: summary of characteristics

LCD multiplex drive mode	Number of:		LCD bias configuration	$\frac{V_{off(RMS)}}{V_{LCD}}$	$\frac{V_{on(RMS)}}{V_{LCD}}$	$D = \frac{V_{on(RMS)}}{V_{off(RMS)}}$ [1]	V_{LCD}[2]
	Backplanes	Levels					
1:4 [3]	4	3	½	0.433	0.661	1.527	$2.309V_{off(RMS)}$
1:4	4	4	⅓	0.333	0.577	1.732	$3.0V_{off(RMS)}$
1:4 [3]	4	5	¼	0.331	0.545	1.646	$3.024V_{off(RMS)}$
1:6 [3]	6	3	½	0.456	0.612	1.341	$2.191V_{off(RMS)}$
1:6	6	4	⅓	0.333	0.509	1.527	$3.0V_{off(RMS)}$
1:6	6	5	¼	0.306	0.467	1.527	$3.266V_{off(RMS)}$
1:8 [3]	8	3	½	0.467	0.586	1.254	$2.138V_{off(RMS)}$
1:8 [3]	8	4	⅓	0.333	0.471	1.414	$3.0V_{off(RMS)}$
1:8	8	5	¼	0.293	0.424	1.447	$3.411V_{off(RMS)}$

[1] Determined from Equation 6.

[2] Determined from Equation 5.

[3] In these examples, the discrimination factor and hence the contrast ratios are smaller. The advantage of these LCD drive modes is a reduction of the LCD voltage V_{LCD}.

A practical value for V_{LCD} is determined by equating $V_{off(RMS)}$ with a defined LCD threshold voltage ($V_{th(off)}$), typically when the LCD exhibits approximately 10 % contrast.

Bias is calculated by $\frac{1}{1+a}$, where the values for a are

a = 1 for ½ bias

a = 2 for ⅓ bias

a = 3 for ¼ bias

The RMS on-state voltage ($V_{on(RMS)}$) for the LCD is calculated with Equation 4

$$V_{on(RMS)} = V_{LCD}\sqrt{\frac{a^2 + 2a + n}{n \times (1+a)^2}} \quad (4)$$

where V_{LCD} is the resultant voltage at the LCD segment and where the values for n are

n = 4 for 1:4 multiplex drive

n = 6 for 1:6 multiplex drive

n = 8 for 1:8 multiplex drive

The RMS off-state voltage ($V_{off(RMS)}$) for the LCD is calculated with Equation 5:

$$V_{off(RMS)} = V_{LCD}\sqrt{\frac{a^2 - 2a + n}{n \times (1+a)^2}} \quad (5)$$

Discrimination is the ratio of $V_{on(RMS)}$ to $V_{off(RMS)}$ and is determined from Equation 6:

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$$D = \frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{a^2 + 2a + n}{a^2 - 2a + n}} \quad (6)$$

It should be noted that V_{LCD} is sometimes referred to as the LCD operating voltage.

8.4.1 Electro-optical performance

Suitable values for $V_{on(RMS)}$ and $V_{off(RMS)}$ are dependent on the LCD liquid used. The RMS voltage, at which a pixel will be switched on or off, determine the transmissibility of the pixel.

For any given liquid, there are two threshold values defined. One point is at 10 % relative transmission (at $V_{th(off)}$) and the other at 90 % relative transmission (at $V_{th(on)}$), see Figure 14. For a good contrast performance, the following rules should be followed:

$$V_{on(RMS)} \geq V_{th(on)} \quad (7)$$

$$V_{off(RMS)} \leq V_{th(off)} \quad (8)$$

$V_{on(RMS)}$ and $V_{off(RMS)}$ are properties of the display driver and are affected by the selection of a, n (see Equation 4 to Equation 6) and the V_{LCD} voltage.

$V_{th(off)}$ and $V_{th(on)}$ are properties of the LCD liquid and can be provided by the module manufacturer. $V_{th(off)}$ is sometimes just named V_{th}. $V_{th(on)}$ is sometimes named saturation voltage V_{sat}.

It is important to match the module properties to those of the driver in order to achieve optimum performance.

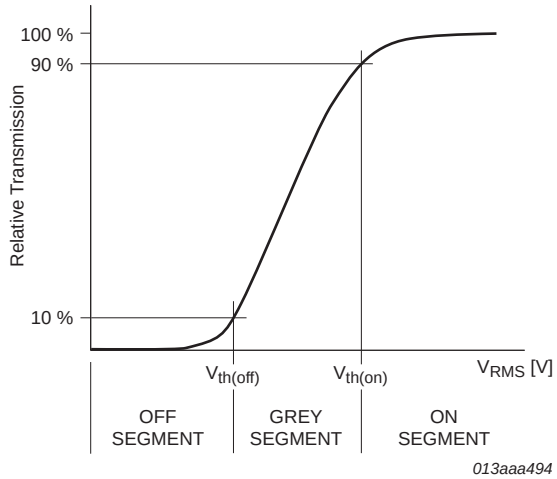


Fig 14. Electro-optical characteristic: relative transmission curve of the liquid

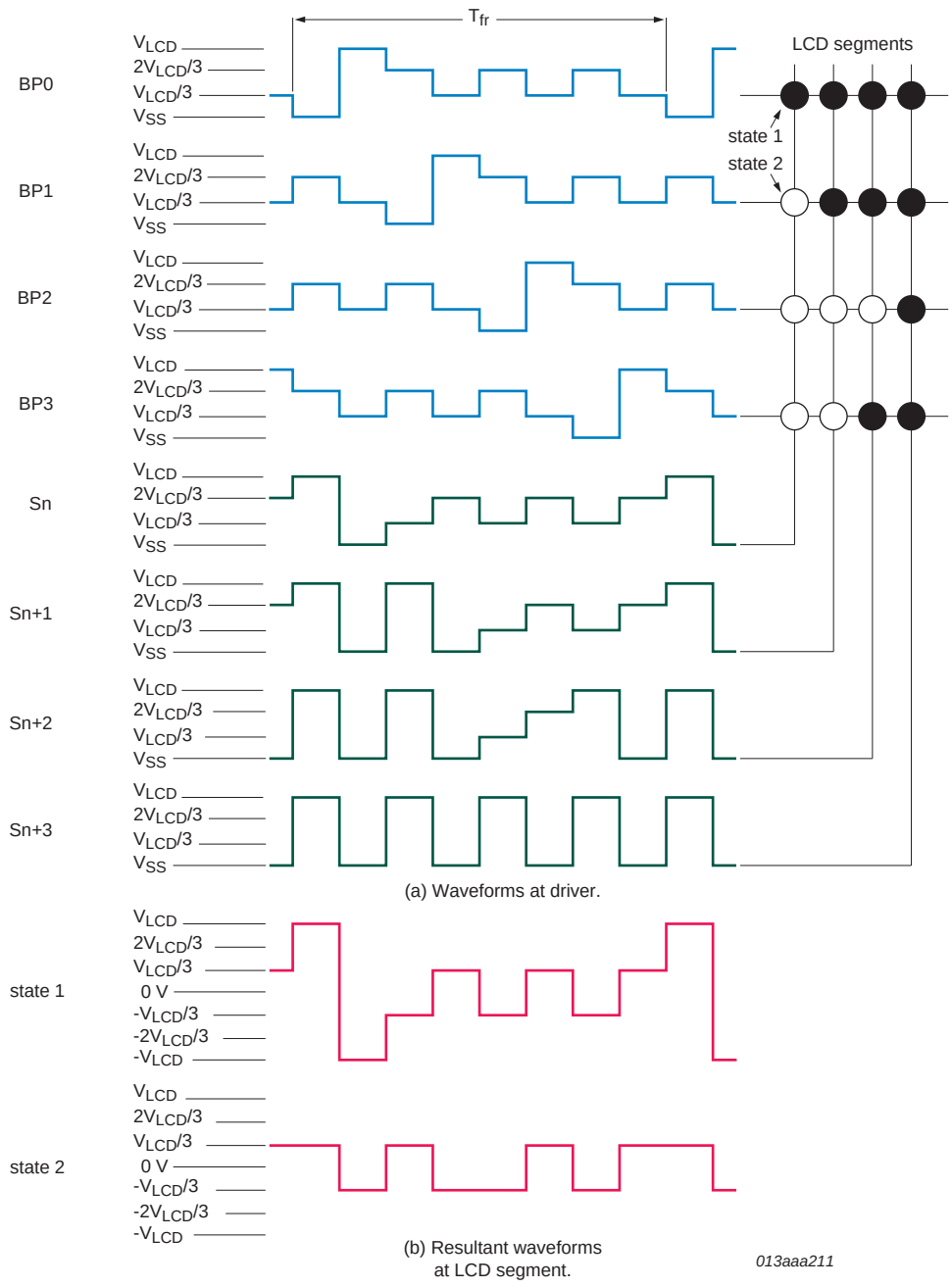
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8.5 LCD drive mode waveforms

8.5.1 1:4 Multiplex drive mode

When four backplanes are provided in the LCD, the 1:4 multiplex drive mode applies, as shown in Figure 15. This drawing is also showing the case of line inversion (see Section 8.1.4.2).



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$. $V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{on(RMS)}(t) = 0.577V_{LCD}$. $V_{off(RMS)}(t) = 0.333V_{LCD}$.

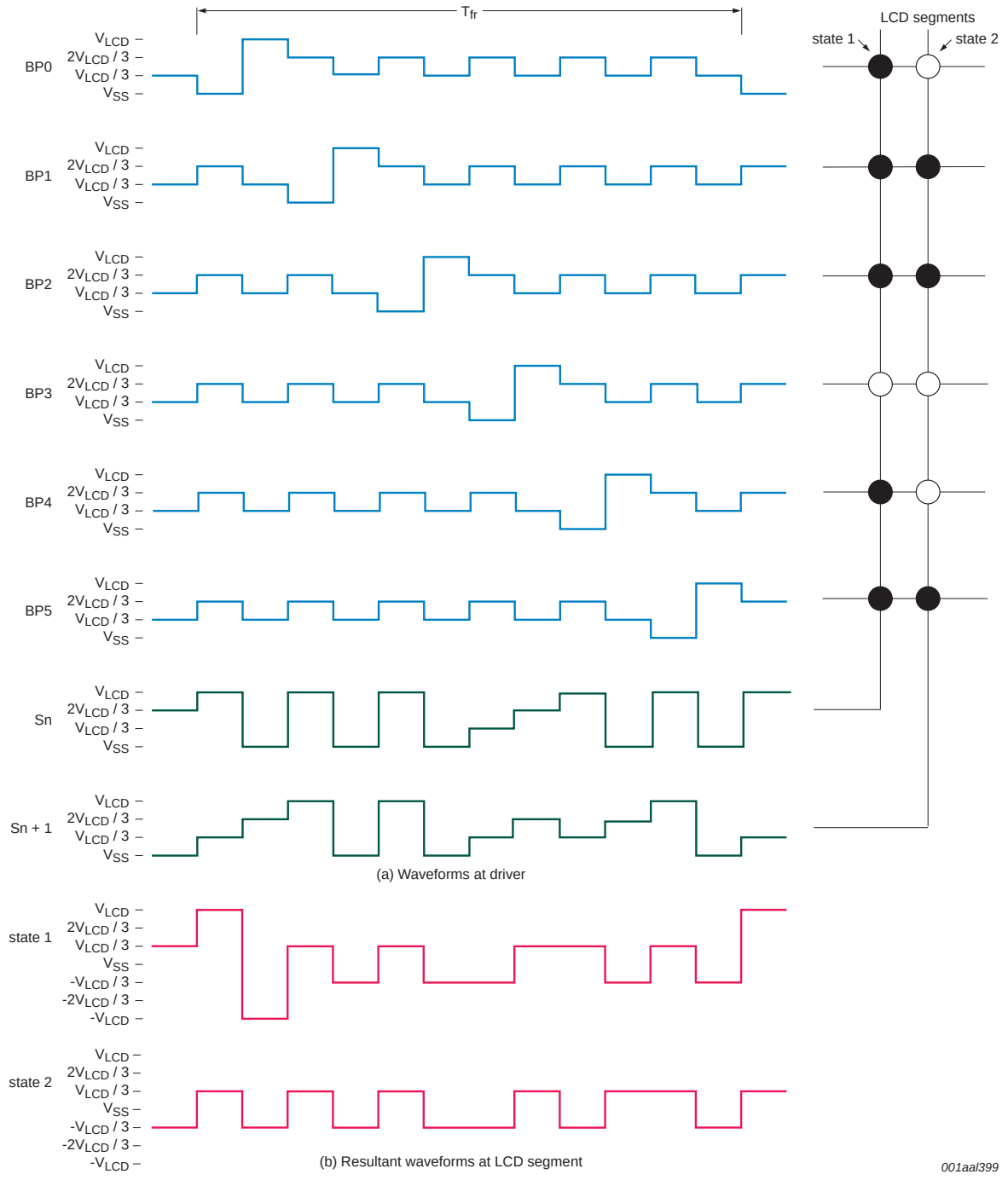
Fig 15. Waveforms for the 1:4 multiplex drive mode with ⅓ bias and line inversion

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8.5.2 1:6 Multiplex drive mode

When six backplanes are provided in the LCD, the 1:6 multiplex drive mode applies. The PCF8536 allows use of ⅓ bias or ¼ bias in this mode as shown in Figure 16 and Figure 17. These waveforms are drawn for the case of line inversion (see Section 8.1.4.2).

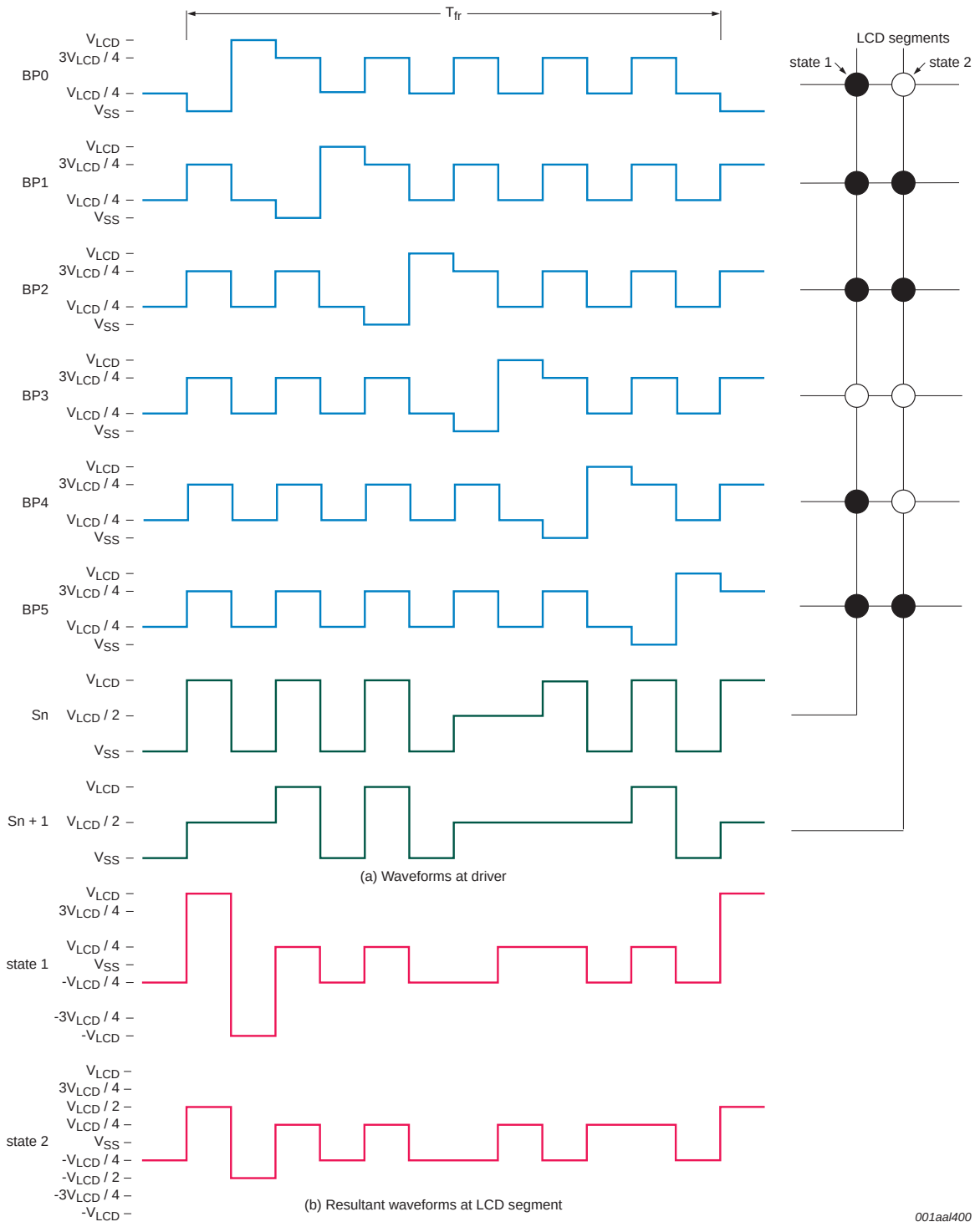


$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$. $V_{state2}(t) = V_{Sn+1}(t) - V_{BP0}(t)$. $V_{on(RMS)}(t) = 0.509V_{LCD}$. $V_{off(RMS)}(t) = 0.333V_{LCD}$.

Fig 16. Waveforms for 1:6 multiplex drive mode with bias ⅓ and line inversion

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$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$. $V_{state2}(t) = V_{Sn+1}(t) - V_{BP0}(t)$.

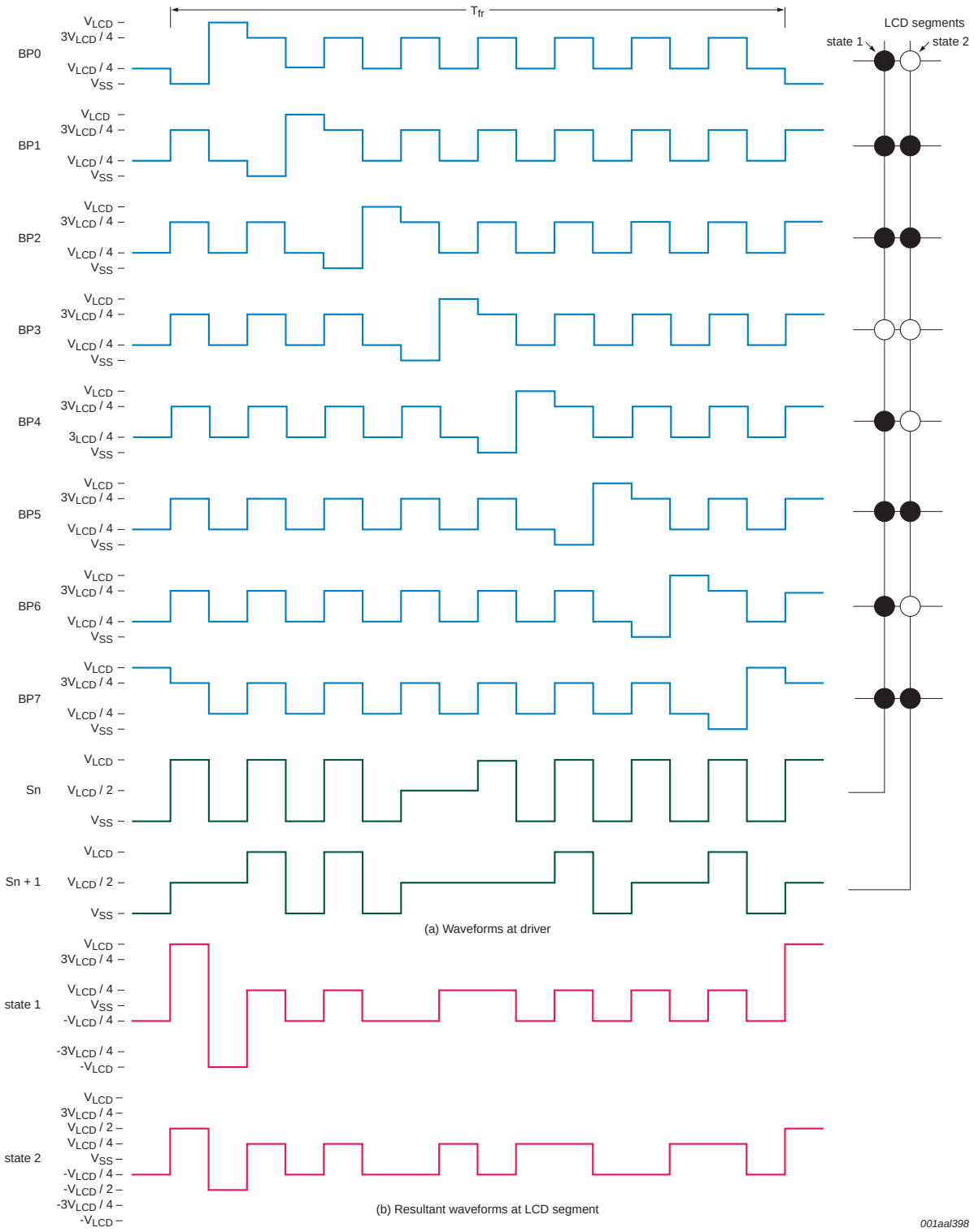
$V_{on(RMS)}(t) = 0.467V_{LCD}$. $V_{off(RMS)}(t) = 0.306V_{LCD}$.

Fig 17. Waveforms for 1:6 multiplex drive mode with bias ¼ and line inversion

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8.5.3 1:8 Multiplex drive mode

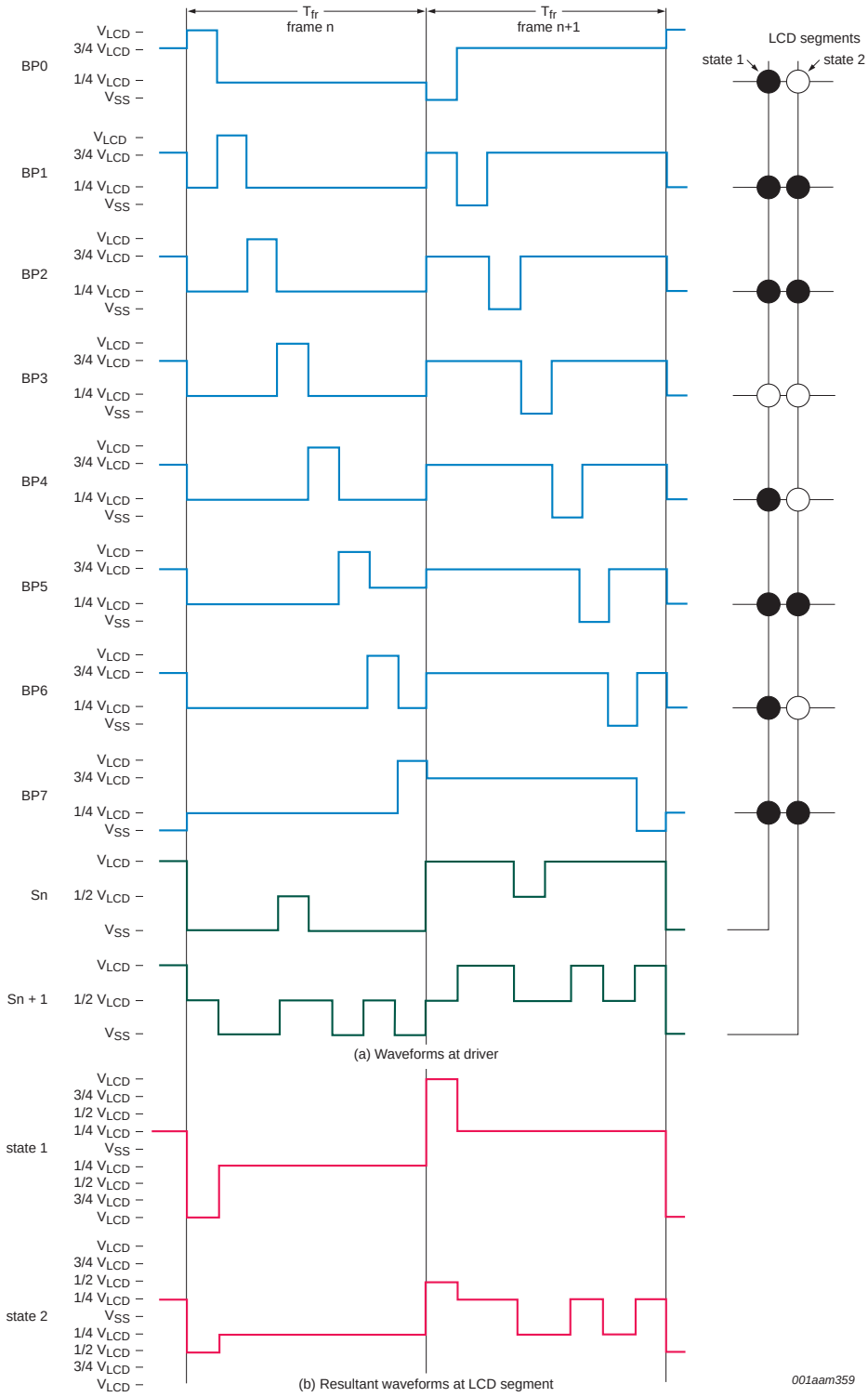


$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$. $V_{state2}(t) = V_{Sn+1}(t) - V_{BP0}(t)$. $V_{on(RMS)}(t) = 0.424V_{LCD}$. $V_{off(RMS)}(t) = 0.293V_{LCD}$.

Fig 18. Waveforms for 1:8 multiplex drive mode with bias ¼ and line inversion

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$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$. $V_{state2}(t) = V_{Sn+1}(t) - V_{BP0}(t)$. $V_{on(RMS)}(t) = 0.424V_{LCD}$. $V_{off(RMS)}(t) = 0.293V_{LCD}$.

Fig 19. Waveforms for 1:8 multiplex drive mode with bias ¼ and frame inversion

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8.6 Display register

The display register holds the display data while the corresponding multiplex signals are generated.

8.7 Backplane outputs

The LCD drive section includes eight backplane outputs: BP0 to BP7. The backplane output signals are generated based on the selected LCD multiplex drive mode.

- In 1:8 multiplex drive mode: BP0 to BP7 must be connected directly to the LCD.
- In 1:6 multiplex drive mode: BP0 to BP5 must be connected directly to the LCD.
- In 1:4 multiplex drive mode: BP0 to BP3 must be connected directly to the LCD.

8.8 Segment outputs

The LCD drive section includes up to 44 segment outputs (S0 to S43) which must be connected directly to the LCD. The segment output signals are generated based on the multiplexed backplane signals and with data resident in the display register. When less segment outputs are required, the unused segment outputs must be left open-circuit.

The number of available segments depends on the multiplex drive mode selected and the number of GPOs used. The table shows consecutive GPOs selected, but this is just for simplicity of explanation. Any combination of GPOs may be used.

Table 32. Backplane and active segment combinations

Basic examples. GPO pins may be configured in any combination. Other LCD segment and GPO combinations are possible.

Multiplex drive mode	Active BPs	Active GPOs						
		None	GP0 only	GP0 to GP1	GP0 to GP2	GP0 to GP3	GP0 to GP4	GP0 to GP5
1:8	BP0 to BP7	S0 to S39	S1 to S39	S2 to S39	S3 to S39	S4 to S39	S5 to S39	S6 to S39
1:6	BP0 to BP5	S0 to S41	S1 to S41	S2 to S41	S3 to S41	S4 to S41	S5 to S41	S6 to S41
1:4	BP0 to BP3	S0 to S43	S1 to S43	S2 to S43	S3 to S43	S4 to S43	S5 to S43	S6 to S43

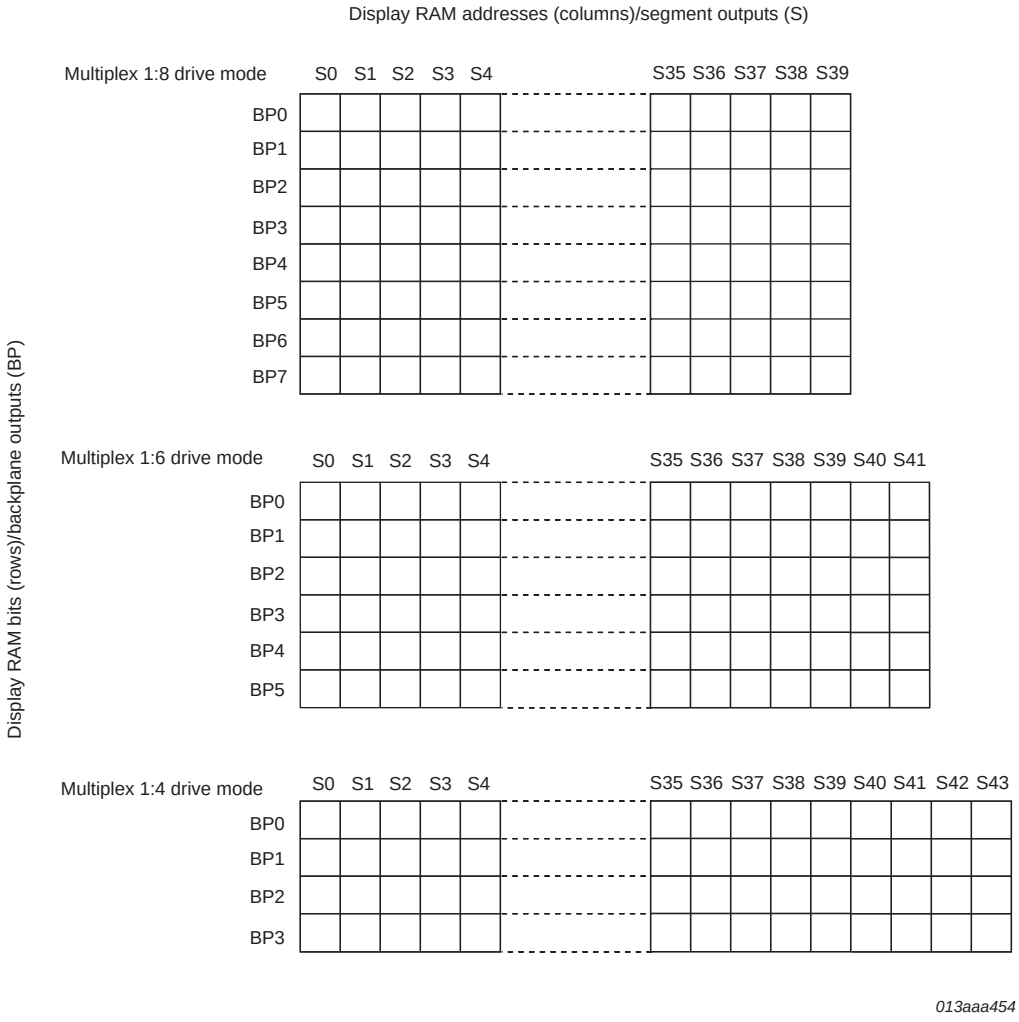
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8.9 Display RAM

The display RAM stores the LCD data. Depending on the multiplex drive mode, the arrangement of the RAM is changed.

- multiplex drive 1:8: RAM is 40 × 8 bit
- multiplex drive 1:6: RAM is 42 × 6 bit
- multiplex drive 1:4: RAM is 44 × 4 bit



The display RAM bitmap shows the direct relationship between the display RAM column and the segment outputs and between the bits in a RAM row and the backplane outputs.

Fig 20. Display RAM bitmap

Logic 1 in the RAM bit map indicates the on-state ($V_{on(RMS)}$) of the corresponding LCD element; similarly, logic 0 indicates the off-state ($V_{off(RMS)}$). For more information on $V_{on(RMS)}$ and $V_{off(RMS)}$, see Section 8.4.

There is a one-to-one correspondence between

- the bits in the RAM bitmap and the LCD elements,

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- the RAM columns and the segment outputs,
- the RAM rows and the backplane outputs.

The display RAM bit map, Figure 20, shows row 0 to row 7 which correspond with the backplane outputs BP0 to BP7, and column 0 to column 43 which correspond with the segment outputs S0 to S43. In multiplexed LCD applications, the data of each row of the display RAM is time-multiplexed with the corresponding backplane (row 0 with BP0, row 1 with BP1, and so on).

When display data is transmitted to the PCF8536, the display bytes received are stored in the display RAM in accordance with the selected LCD multiplex drive mode. The data is stored as it arrives and depending on the current multiplex drive mode, data is stored in quadruples, sextuples or bytes.

8.9.1 Data pointer (LCD part)

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the load-data-pointer-LCD command (see Table 25).

Following this command, an arriving data byte is stored starting at the display RAM address indicated by the data pointer.

The data pointer is automatically incremented in accordance with the chosen LCD multiplex drive mode configuration. That is, after each byte is stored, the contents of the data pointer are incremented

- by two (1:4 multiplex drive mode),
- by one or two (1:6 multiplex drive mode),
- by one (1:8 multiplex drive mode).

Multiplex drive 1:6 is a special case and is described later on.

When the address counter reaches the end of the RAM, it stops incrementing after the last byte is transmitted. Redundant bits of the last byte and subsequent bytes transmitted are discarded until the pointer is reset. To send new RAM data, the data pointer must be reset.

If an I^2C-bus or SPI-bus data access is terminated early then the state of the data pointer is unknown. The data pointer must then be re-written prior to further RAM accesses.

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8.9.2 RAM filling in 1:4 multiplex drive mode

In the 1:4 multiplex drive mode the RAM is organized in four rows and 44 columns. The eight transmitted data bits are placed in two successive display RAM columns of four rows (see Figure 21). In order to fill the whole four RAM rows, 22 bytes need to be sent to the PCF8536. After the last byte sent, the data pointer must be reset before the next RAM content update. Additional data bytes sent and any data bits that spill over the RAM will be discarded.

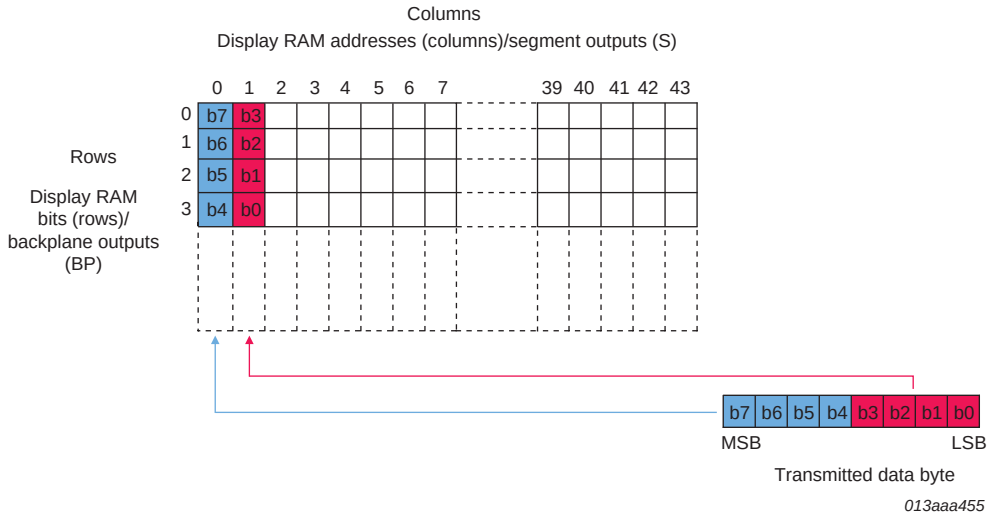


Fig 21. Display RAM filling order in 1:4 multiplex drive mode

Depending on the start address of the data pointer, there is the possibility for a boundary condition. This will occur when more data bits are sent than fit into the remaining RAM. The additional data bits are discarded. See Figure 22.

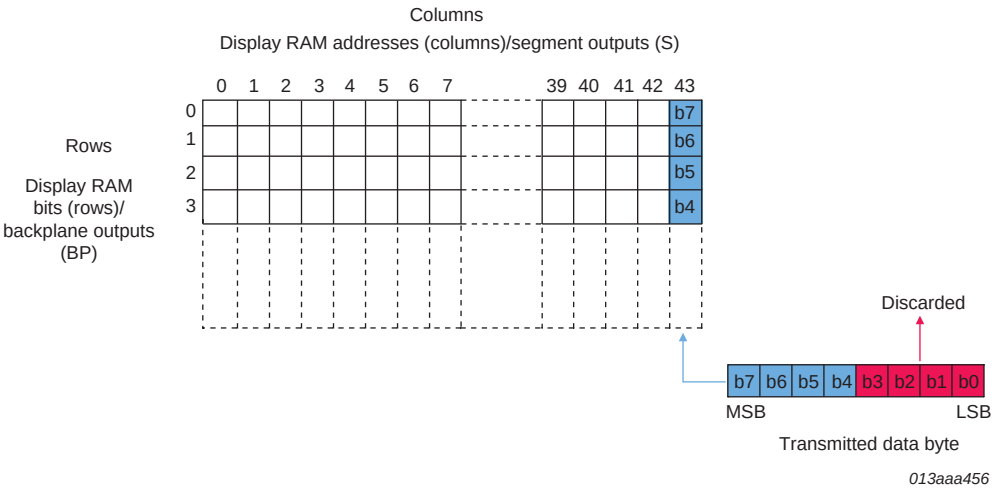


Fig 22. Boundary condition in 1:4 multiplex drive mode

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8.9.3 RAM filling in 1:6 multiplex drive mode

In the 1:6 multiplex drive mode the RAM is organized in six rows and 42 columns. The eight transmitted data bits are placed in such a way, that a column is filled up (see Figure 23).

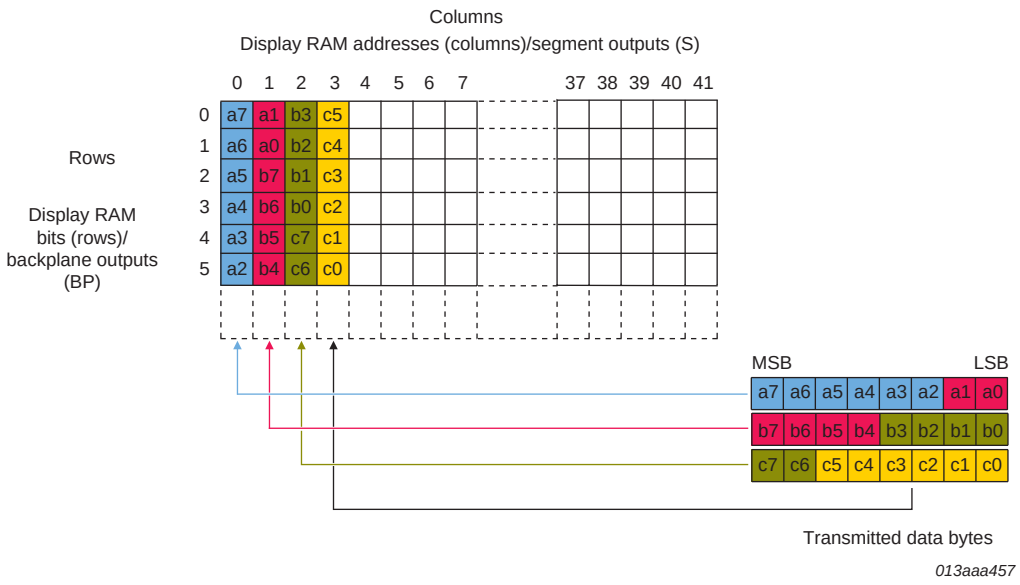


Fig 23. Display RAM filling order in 1:6 multiplex drive mode

The remaining bits are wrapped over into the next column. In order to fill the whole RAM, 31 and a half bytes need to be sent to the PCF8536. After the last byte sent, the data pointer must be reset before the next RAM content update. Additional data bytes sent and any data bits that spill over the RAM will be discarded. Depending on the start address of the data pointer, there are three possible boundary conditions. See Figure 24.

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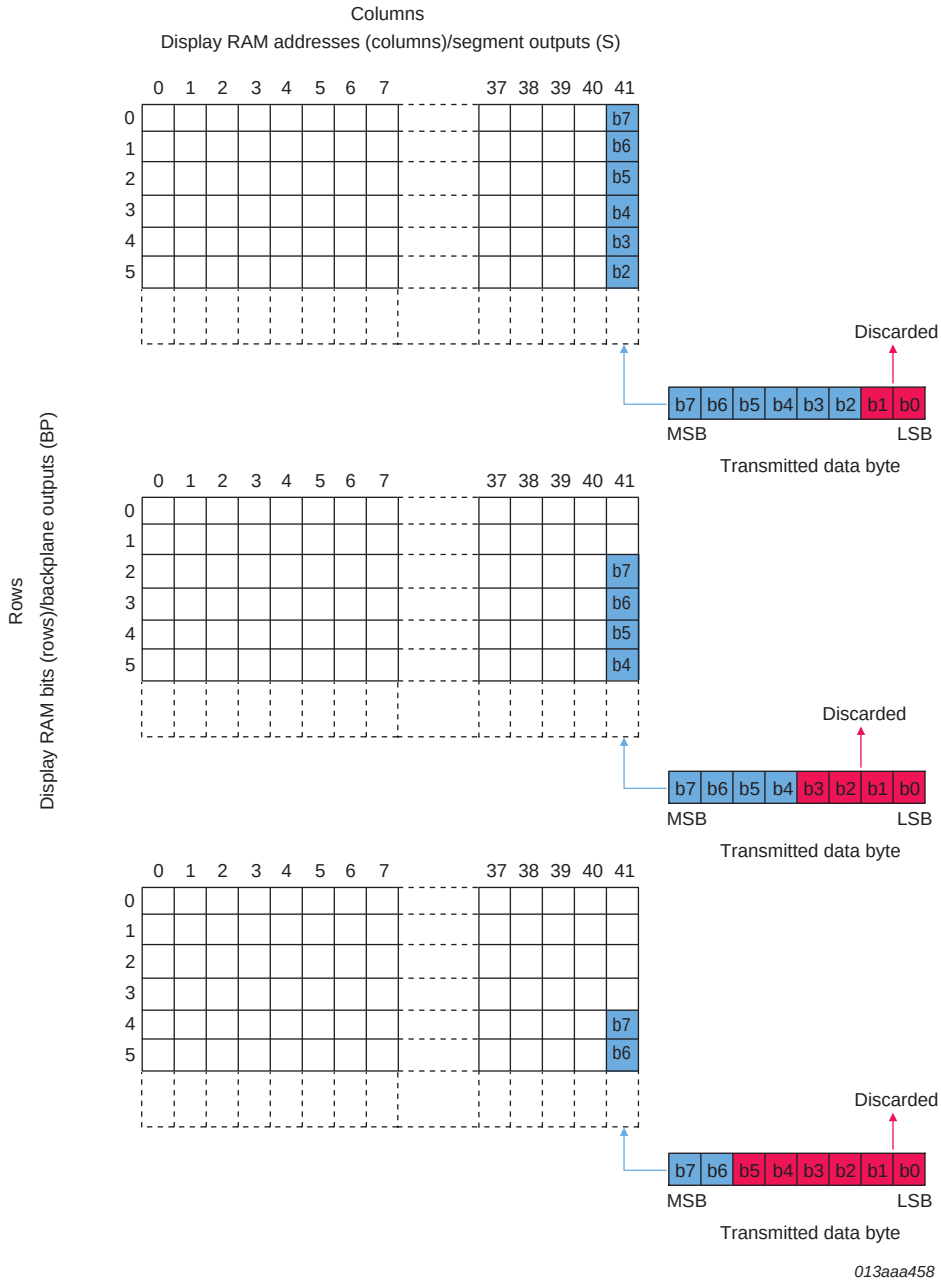


Fig 24. Boundary condition in 1:6 multiplex drive mode

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8.9.4 RAM filling in 1:8 multiplex drive mode

In the 1:8 multiplex drive mode the RAM is organized in eight rows and 40 columns. The eight transmitted data bits are placed into eight rows of one display RAM column (see Figure 25). In order to fill the whole RAM, 40 bytes need to be sent to the PCF8536. After the last byte sent, the data pointer must be reset before the next RAM content update. Additional data bytes sent will be discarded.

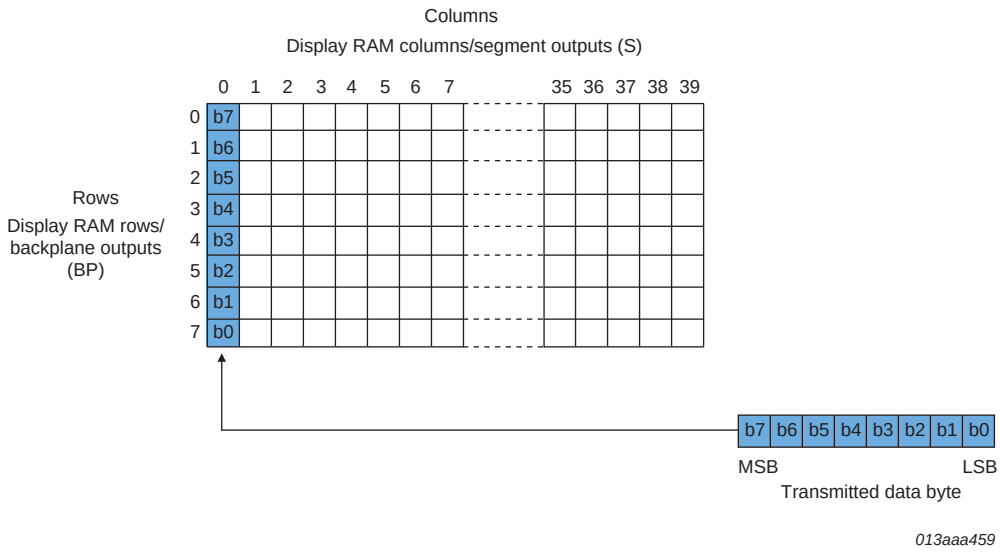


Fig 25. Display RAM filling order in 1:8 multiplex drive mode

There are no boundary conditions in 1:8 multiplex drive mode.

8.10 PWM registers and data pointer (PWM part)

There are six PWM generators which can be independently configured. The values used to define the PWM output are stored here.

The addressing mechanism for the PWM register is realized using the PWM data pointer. This allows the loading of an individual PWM data byte, or a series of data bytes, into any location of the PWM registers. The sequence commences with the initialization of the data pointer by the load-data-pointer-PWM command (see Table 26).

Following this command, an arriving data byte is stored starting at the PWM register address indicated by the PWM data pointer. The data pointer is automatically incremented. That is, after each byte is stored, the contents of the data pointer are incremented. The data pointer will wrap around continuously as long as data is transmitted.

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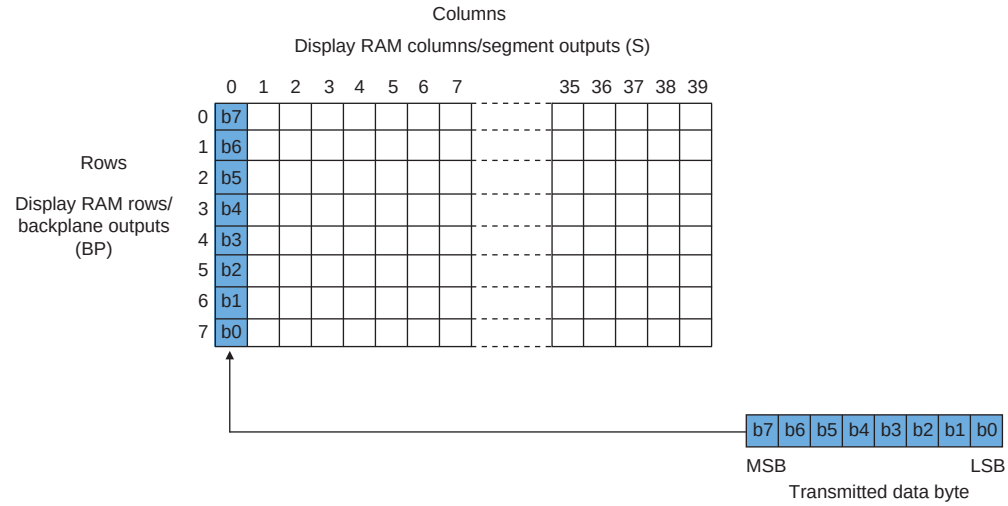


Fig 26. PWM register filling

8.11 GPO output

The PCF8536 contains six independently configured GPO pins (GP0 to GP5). These outputs, when enabled, will replace the function of the corresponding LCD segment outputs.

Each GPO output can supply either a logic 1, a logic 0, or a PWM signal. The PWM signal can be used to control the brightness of an LED.

The PWM generator has 128 possible levels allowing for an output with a variable duty cycle between 0 % and 99.7 %. 100 % can only be achieved by a static 1 output.

The period of the PWM frame frequency described in Section 8.1.10 is divided into 128 time slots. The value in the PWM register determines for how many of these time slots the PWM output is at logic 1.

Table 33. PWM generator

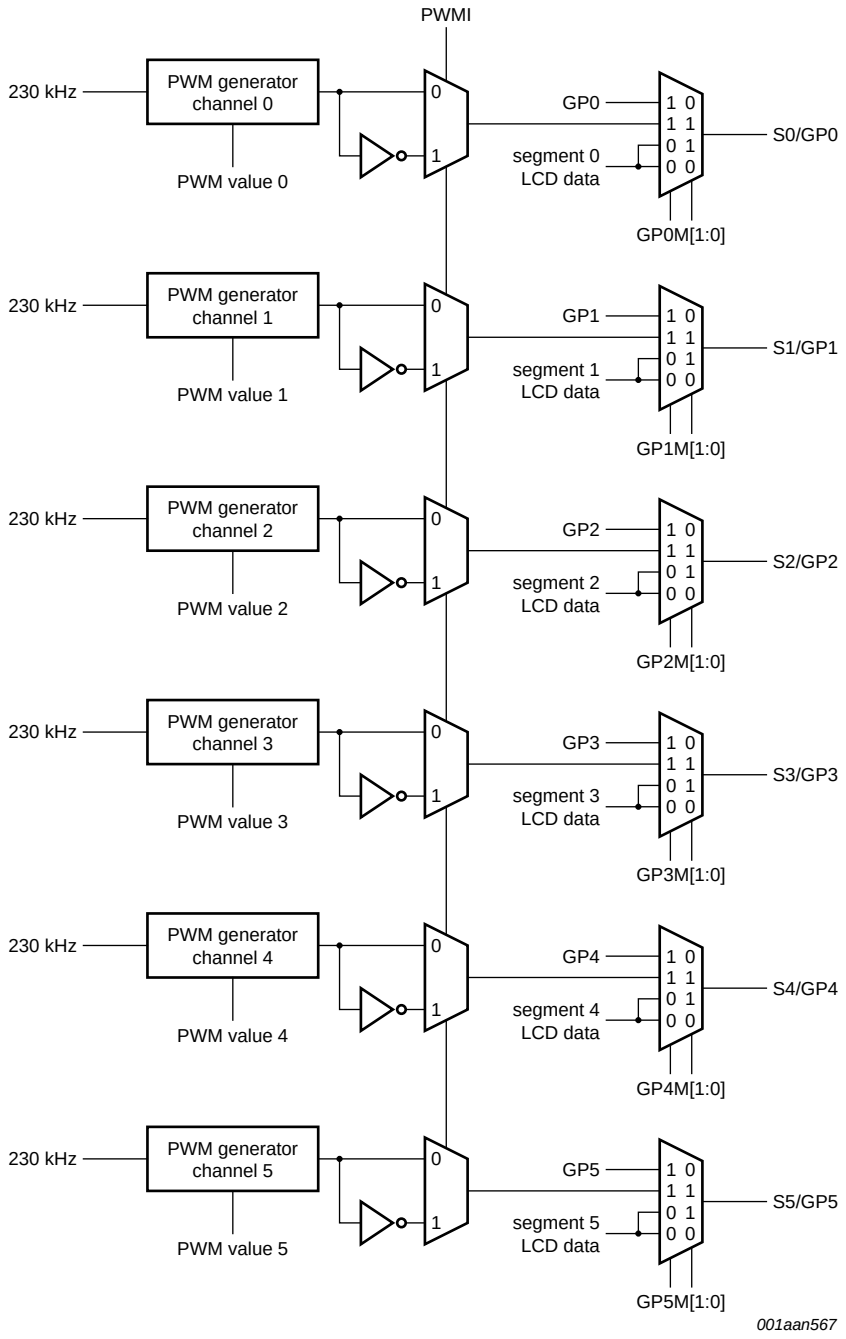
PWM register value	Percentage of ON time (%)	Time slots at 1	Time slots at 0
0	0	0	128
1	0.78	1	127
2	1.56	2	126
:	:	:	:
126	98.4	126	2
127	99.2	127	1

PWM duty cycle may be calculated by:

$$DutyCycle = \frac{PWMvalue}{128} \cdot 100 \quad (9)$$

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There are six independently configured GPO outputs.

Fig 27. General-purpose output block diagram

An example of the PWM waveforms is given in Figure 28.

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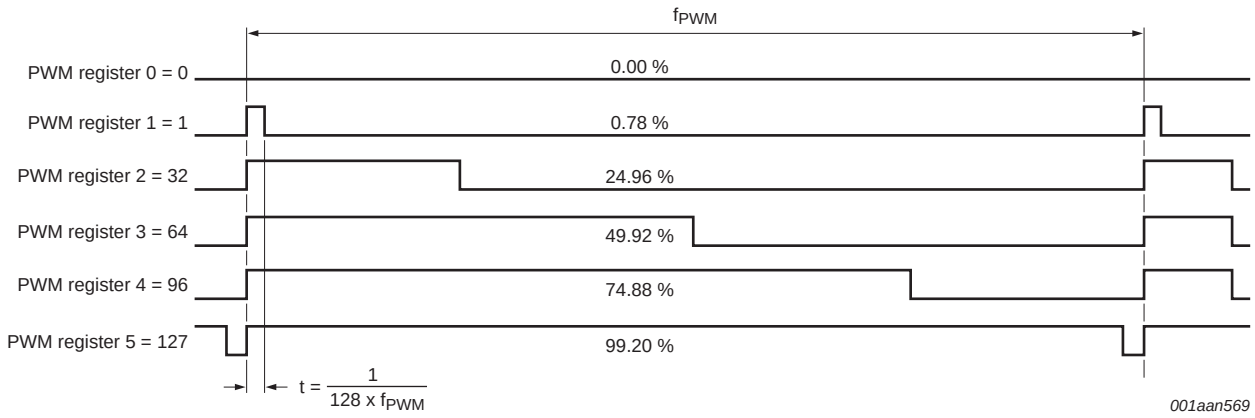


Fig 28. PWM example waveforms for PWMI = 0

8.11.1 RGB color driving

There are six PWM channels that can be arranged as two RGB channels. There are no explicit settings for this feature, only ways of utilizing the PWM channels.

Table 34 gives an example of how two RGB clusters can be configured.

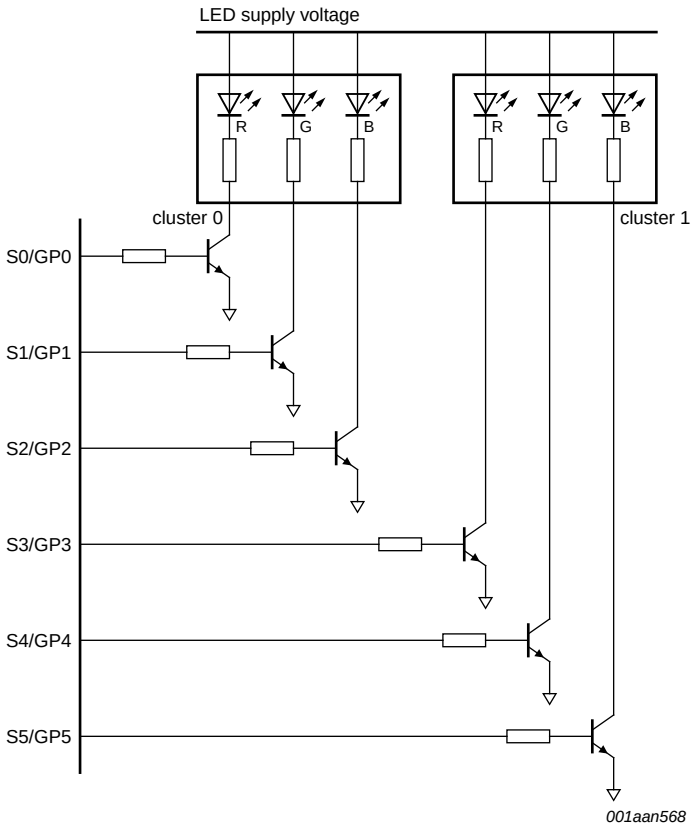
Table 34. Combining PWM channels for RGB

RGB cluster	PWM channel	Component color
0	0	red
	1	green
	2	blue
1	3	red
	4	green
	5	blue

Figure 29 gives an example of how two RGB clusters can be connected.

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There are six independently configured GPO outputs.

Fig 29. Configuration for two RGB clusters

Table 35 gives some examples of programming values for the PWM channels in order to achieve the given colors. By using three PWM channels for one RGB cluster it is possible to generate two million colors.

Table 35. Example PWM values

PWM channel	Component color	PWM channel value	Resultant color
0	red	127	yellow
1	green	127	
2	blue	0	
3	red	127	orange
4	green	82	
5	blue	0	
0	red	0	aqua
1	green	127	
2	blue	127	
3	red	127	gold
4	green	108	
5	blue	0	

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8.11.2 PWM inversion mode

The PWM inversion mode can be enabled by setting the PWMI bit to logic 1 (see Table 7 on page 8). The PWMI mode will invert the PWM waveform.

By default, all PWM outputs will switch HIGH at the same time. If the PWM output is used to drive external LEDs then this could cause a voltage dip on the power supply of the LEDs. With the PWMI mode, it is possible to prevent multiple outputs switching HIGH at the same time by ensuring that the PWM values are not identical.

In the example in Figure 30, none of the six PWM outputs switch HIGH together. All PWM channels instead switch off together; however this will not cause any power supply disturbances.

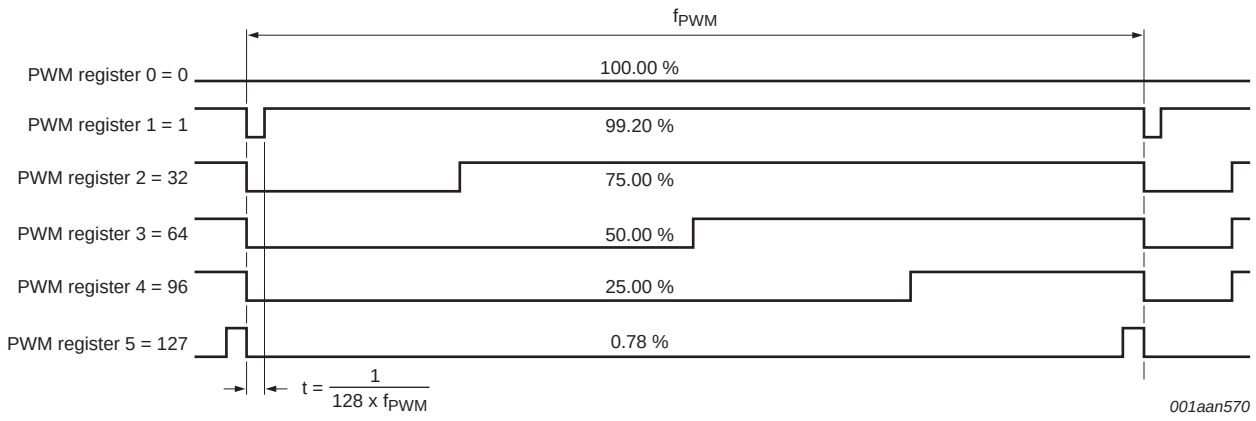


Fig 30. PWM example waveforms for PWMI = 1

When PWM inversion mode is used, the PWM duty cycle can be calculated with:

$$DutyCycle = \frac{128 - PWMvalue}{128} \cdot 100 \quad (10)$$

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9. Bus interfaces

9.1 Control byte and register selection

After initiating the communication over the bus and sending the slave address (I^2C-bus, see Section 9.2) or subaddress (SPI-bus, see Section 9.3), a control byte follows. The purpose of this byte is to indicate both, the content for the following data bytes (RAM, command, or PWM data) and to indicate that more control bytes will follow.

Typical sequences could be:

- Slave address/subaddress - control byte - command byte - command byte - command byte - end
- Slave address/subaddress - control byte - RAM byte - RAM byte - RAM byte - end
- Slave address/subaddress - control byte - command byte - control byte - RAM byte - end

In this way, it is possible to send a mixture of RAM, PWM and command data in one access or alternatively, to send just one type of data in one access.

Table 36. Control byte description

Bit	Symbol	Value	Description
7	CO		**continue bit**
		0	last control byte
		1	control bytes continue
6 to 5	RS[1:0]		**register selection**
		00	command register
		01	RAM data
		10	PWM data
		11	unused
4 to 0	-	-	unused

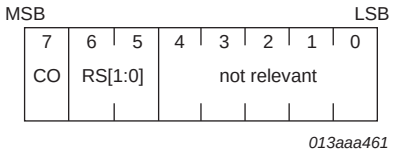


Fig 31. Control byte format

9.2 I^2C-bus interface

The I^2C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial DAta line (SDA) and a Serial CLock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

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9.2.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal (see Figure 32).

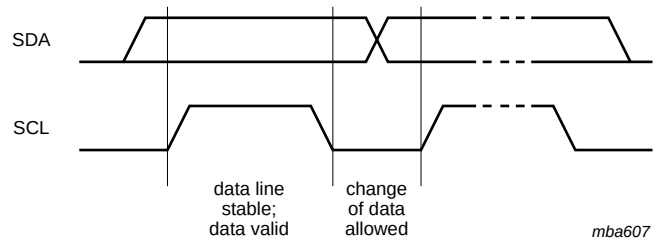


Fig 32. Bit transfer

9.2.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW change of the data line, while the clock is HIGH, is defined as the START condition (S).

A LOW-to-HIGH change of the data line, while the clock is HIGH, is defined as the STOP condition (P).

The START and STOP conditions are shown in Figure 33.

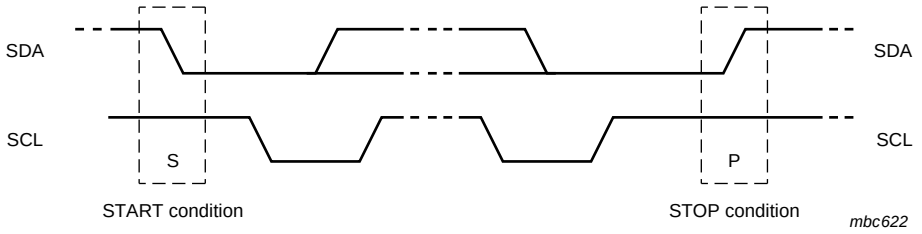


Fig 33. Definition of START and STOP conditions

9.2.3 System configuration

A device generating a message is a transmitter, a device receiving a message is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves. The system configuration is shown in Figure 34.

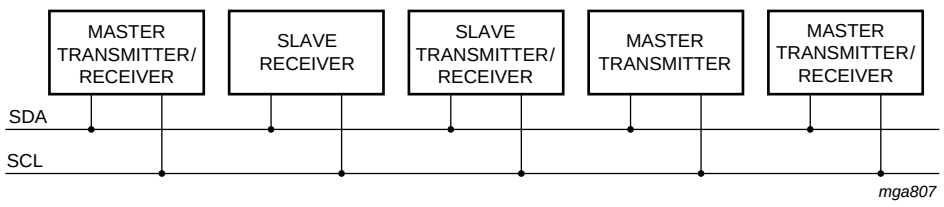


Fig 34. System configuration

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9.2.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of 8 bits is followed by an acknowledge cycle.

- A slave receiver which is addressed must generate an acknowledge after the reception of each byte.
- Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be considered).
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the I^2C-bus is shown in Figure 35.

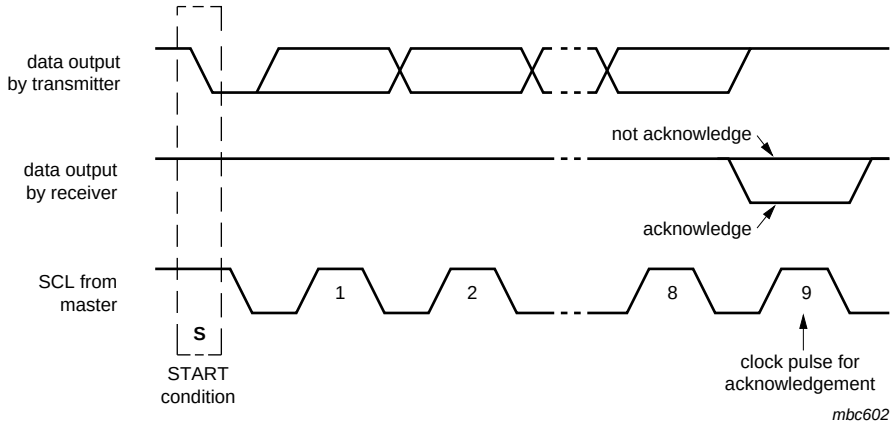


Fig 35. Acknowledgement on the I^2C-bus

9.2.5 I^2C-bus controller

The PCF8536 acts as an I^2C-bus slave receiver. It does not initiate I^2C-bus transfers or transmit data to an I^2C-bus master receiver. Device selection depends on the I^2C-bus slave address.

9.2.6 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

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9.2.7 I²C-bus slave address

Device selection depends on the I²C-bus slave address. Two different I²C-bus slave addresses can be used to address the PCF8536 (see Table 37).

Table 37. I²C slave address

Bit	Slave address							
	7 MSB	6	5	4	3	2	1	0 LSB
	0	1	1	1	0	0	A0	R/$\overline{W}$

The least significant bit of the slave address byte is bit R/$\overline{W}$. Bit 1 of the slave address is defined by connecting the input A0 to either V_{SS} (logic 0) or V_{DD} (logic 1). Therefore, two instances of PCF8536 can be distinguished on the same I²C-bus.

9.2.8 I²C-bus protocol

The I²C-bus protocol is shown in Figure 36. The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by one of the two PCF8536 slave addresses available. All PCF8536 with the corresponding A0 level acknowledge in parallel to the slave address, but any PCF8536 with the alternative A0 level ignore the whole I²C-bus transfer.

After acknowledgement, a control byte follows (see Section 9.1 on page 46).

The display bytes are stored in the display RAM at the address specified by the RAM data pointer and PWM data is stored at the address pointed to by the PWM data pointer.

The acknowledgement after each byte is made only by the addressed PCF8536. After the last data byte, the I²C-bus master issues a STOP condition (P). Alternatively a START may be issued to RESTART an I²C-bus access.

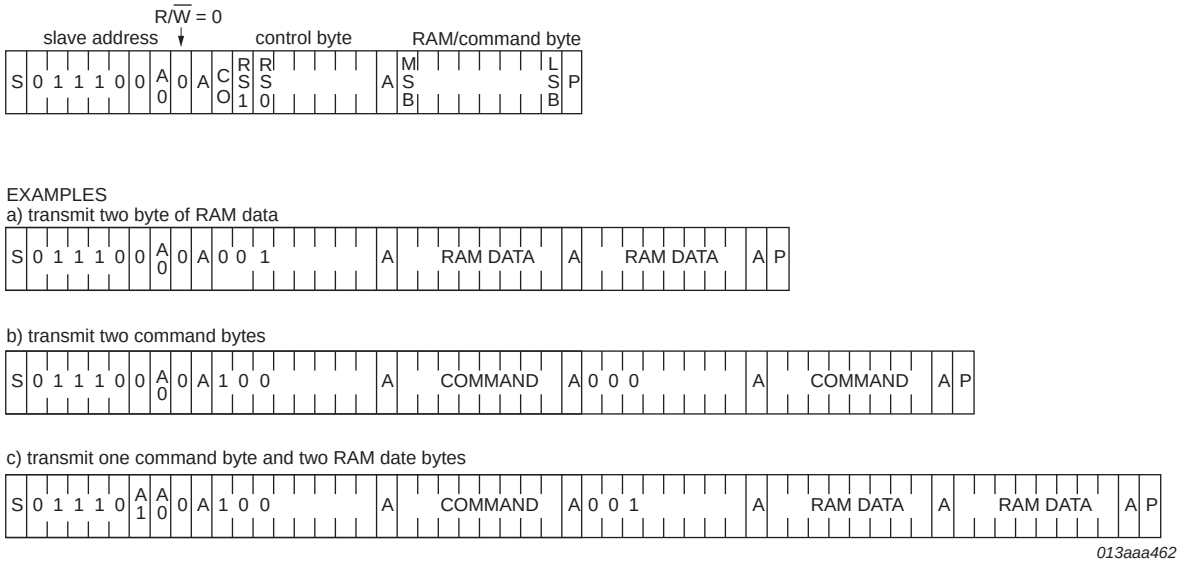


Fig 36. I²C-bus protocol write mode

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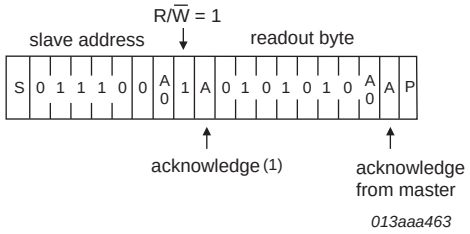
9.2.8.1 Status read out

Status read out for I^2C-bus operation only. This command will initiate the read out of a fixed value plus the slave address bit A0 from the PCF8536. This read out function will allow the I^2C master to confirm the existence of the device on the I^2C-bus.

Table 38. Status read out value

Bit	Symbol	Value	Description
7 to 1	-	0101010	fixed value
0	A0	0	read back value is 01010100
		1	read back value is 01010101

If a readout is made, the R/$\overline{W}$ bit must be logic 1 and then the next data byte following is provided by the PCF8536 as shown in Figure 37.



(1) From PCF8536.

Fig 37. I^2C-bus protocol read mode

In the unlikely case that the chip has entered the internal test mode, detection of this state is possible by using the modified status read out detailed in Table 39. The read out value is modified to indicate that the chip has entered an internal test mode.

Table 39. Modified status read out value

Bit	Symbol	Value	Description
7 to 1	-	1111000	fixed value
0	A0	0	read back value is 1111 0000
		1	read back value is 1111 0001

EMC detection: The PCF8536 is ruggedized against EMC susceptibility; however it is not possible to cover all cases. To detect if a severe EMC event has occurred, it is possible to check the responsiveness of the device by reading its register.

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9.3 SPI-bus interface

Data transfer to the device is made via a 3 line SPI-bus (see Table 40). There is no output data line. The SPI-bus is initialized whenever the chip enable line pin $\overline{CE}$ is inactive.

Table 40. Serial interface

Symbol	Function	Description
$\overline{CE}$	chip enable input[1]; active LOW	when HIGH, the interface is reset
SCL	serial clock input	input may be higher than V_{DD}
SDI	serial data input	input may be higher than V_{DD}; input data is sampled on the rising edge of SCL

[1] The chip enable must not be wired permanently LOW.

9.3.1 Data transmission

The chip enable signal is used to identify the transmitted data. Each data transfer is a byte with the Most Significant Bit (MSB) sent first.

The transmission is controlled by the active LOW chip enable signal $\overline{CE}$. The first byte transmitted is the subaddress byte.

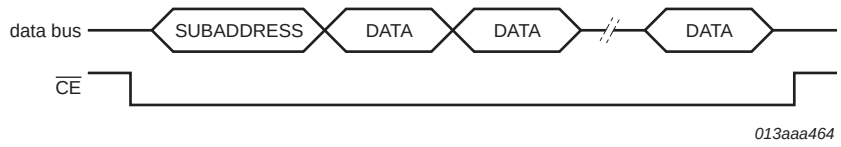


Fig 38. Data transfer overview

The subaddress byte opens the communication with a read/write bit and a subaddress. The subaddress is used to identify multiple devices on one SPI-BUS.

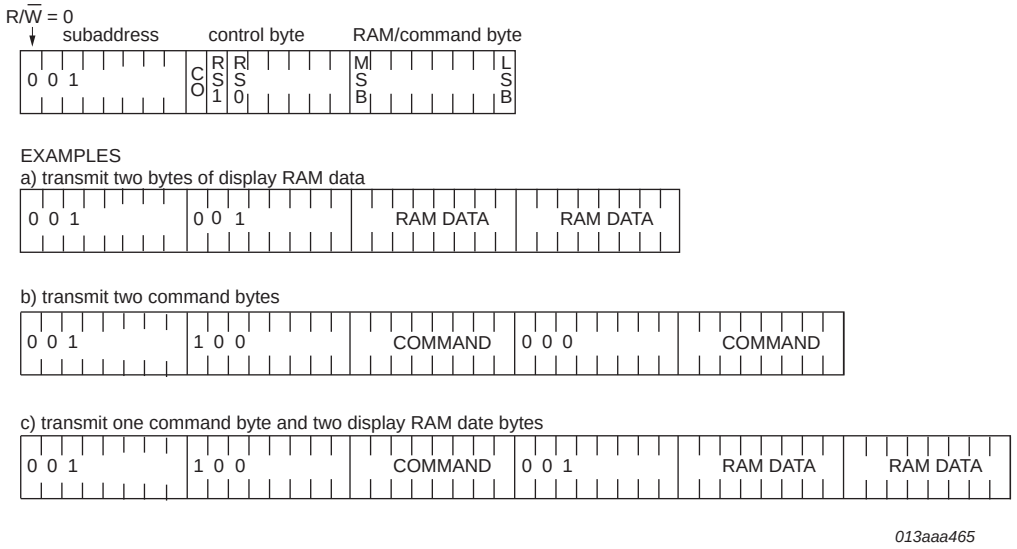
Table 41. Subaddress byte definition

Bit	Symbol	Value	Description
7	R/$\overline{W}$		**data read or write selection**
		0	write data
		1	read data
6 to 5	SA	01	**subaddress**; other codes will cause the device to ignore data transfer
4 to 0	-		unused

After the subaddress byte, a control byte follows (see Section 9.1 on page 46).

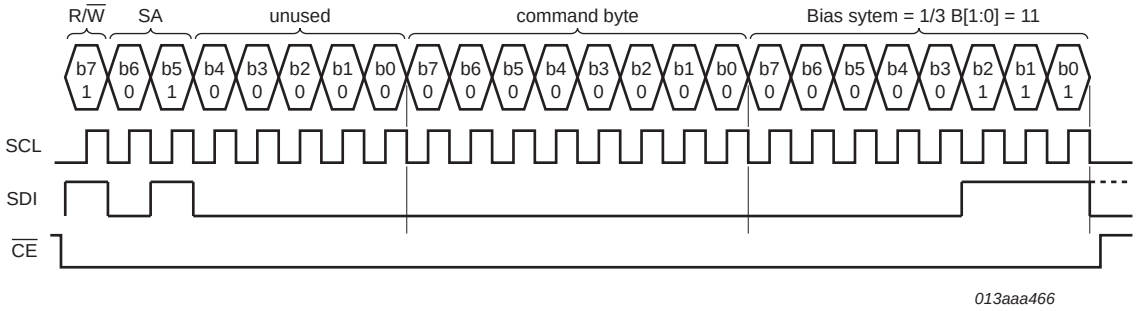
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Data transfers are terminated by de-asserting $\overline{CE}$ (set $\overline{CE}$ to logic 1).

Fig 39. SPI-bus write example



In this example, the bias system is set to $\frac{1}{3}$. The transfer is terminated by $\overline{CE}$ returning to logic 1. After the last bit is transmitted, the state of the SDI line is not important.

Fig 40. SPI-bus example

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10. Internal circuitry

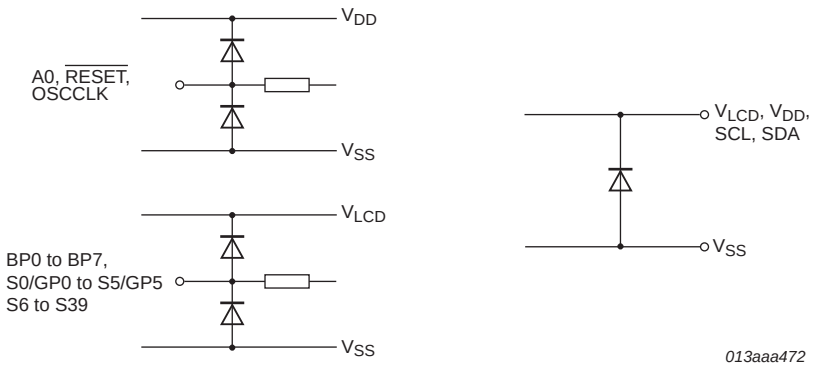


Fig 41. Device protection diagram for PCF8536AT

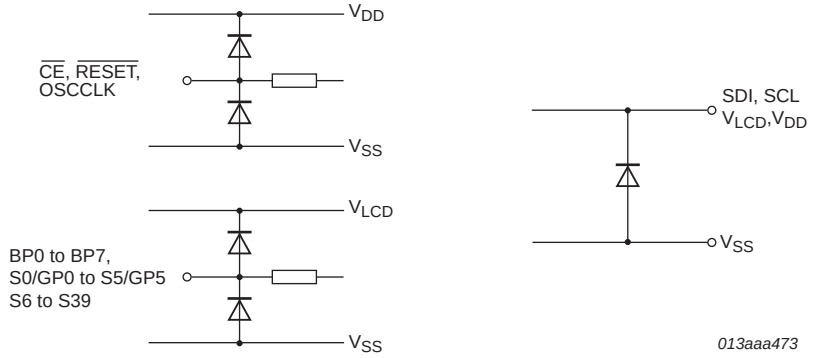


Fig 42. Device protection diagram for PCF8536BT

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11. Limiting values

CAUTION



Static voltages across the liquid crystal display can build up when the LCD supply voltage (V_{LCD}) is on while the IC supply voltage (V_{DD}) is off, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts, V_{LCD} and V_{DD} must be applied or removed together.

Table 42. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.5	+6.5	V
I_{DD}	supply current			–50	+50	mA
V_{LCD}	LCD supply voltage			–0.5	+10	V
$I_{DD(LCD)}$	LCD supply current			–50	+50	mA
V_I	input voltage	PCF8536AT				
		on pins SDA, $\overline{\text{OSCCLK}}$, SCL, A0, $\overline{\text{RESET}}$		–0.5	+6.5	V
		PCF8536BT				
		on pins $\overline{\text{CE}}$, OSCCLK, SCL, SDI, $\overline{\text{RESET}}$		–0.5	+6.5	V
I_I	input current			–10	+10	mA
V_O	output voltage	on pins S0/GP0 to S5/GP5, S6 to S39, BP0 to BP7		–0.5	+10	V
		on pin SDA		–0.5	+6.5	V
I_O	output current			–10	+10	mA
I_{SS}	ground supply current			–50	+50	mA
P_{tot}	total power dissipation			-	400	mW
P/out	power dissipation per output			-	100	mW
V_{ESD}	electrostatic discharge voltage	HBM	[1]	-	±3500	V
		CDM	[2]	-	±1250	V
I_{lu}	latch-up current		[3]	-	200	mA
T_{stg}	storage temperature		[4]	–65	+150	°C
T_{amb}	ambient temperature	operating device		–40	+85	°C

[1] Pass level; Human Body Model (HBM), according to Ref. 5 “JESD22-A114”.

[2] Pass level; Charge Device Model (CDM), according to Ref. 6 “JESD22-C101”.

[3] Pass level; latch-up testing according to Ref. 7 “JESD78” at maximum ambient temperature ($T_{amb(max)}$).

[4] According to the NXP store and transport requirements (see Ref. 9 “NX3-00092”) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %. For long-term storage products deviant conditions are described in that document.

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12. Static characteristics

Table 43. Static characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 V to 9.0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage			1.8	-	5.5	V
V_{LCD}	LCD supply voltage	$V_{LCD} \geq V_{DD}$		2.5	-	9.0	V
$I_{DD(pd)}$	power-down mode supply current		[1]	-	0.5	2	µA
I_{DD}	supply current	see Figure 43					
		external 9.6 kHz clock	[2]	-	10	25	µA
		external 230 kHz clock with PWM	[3]	-	20	40	µA
		internal oscillator	[2]	-	30	60	µA
		internal oscillator with PWM	[3]	-	60	130	µA
$I_{DD(LCD)}$	LCD supply current						
		power-down, see Figure 44	[1][4]	-	7	15	µA
		display active, see Figure 45	[5]	-	55	140	µA
Logic							
V_I	input voltage			V_{SS} − 0.5	-	V_{DD} + 0.5	V
V_{IL}	LOW-level input voltage	on pins $\overline{OSCCLK}$, A0 and $\overline{RESET}$		-	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage	on pins $\overline{OSCCLK}$, A0 and $\overline{RESET}$		$0.7V_{DD}$	-	-	V
V_O	output voltage			−0.5	-	V_{DD} + 0.5	V
V_{OH}	HIGH-level output voltage	driving load of 50 µA on pins OSCCLK and GP0 to GP5		$0.8V_{DD}$	-	-	V
V_{OL}	LOW-level output voltage	driving load of 50 µA on pins OSCCLK and GP0 to GP5		-	-	$0.2V_{DD}$	V
I_{OH}	HIGH-level output current	output source current; $V_{OH} = V_{DD} - 0.4$ V					
		on pin OSCCLK					
		V_{DD} = 1.8 V		0.7	1.6	-	mA
		$V_{DD} \geq 3.3$ V		1.5	4.0	-	mA
		on pins GP0 to GP5					
		V_{DD} = 1.8 V; V_{LCD} = 2.5 V		0.7	1.1	-	mA
		V_{DD} = 3.3 V; $V_{LCD} \geq 5.5$ V		1.5	2.8	-	mA

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Table 43. Static characteristics *...continued*

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 V to 9.0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{OL}	LOW-level output current	output sink current; V_{OL} = 0.4 V				
		on pin OSCCLK				
		V_{DD} = 1.8 V	3	4	-	mA
		$V_{DD} \geq$ 3.3 V	5	10	-	mA
		on pins GP0 to GP5				
		V_{DD} = 1.8 V; V_{LCD} = 2.5 V	0.7	1.1	-	mA
		V_{DD} = 3.3 V; $V_{LCD} \geq$ 5.5 V	1.5	2.4	-	mA
I_L	leakage current	$V_i = V_{DD}$ or V_{SS}; on pin OSCCLK and GP0 to GP5	−1	-	+1	µA
I²C-bus[6]						
On pins SCL and SDA						
V_I	input voltage		V_{SS} − 0.5	-	5.5	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	-	V
V_O	output voltage		−0.5	-	+5.5	V
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}	−1	-	+1	µA
On pin SDA						
I_{OL}	LOW-level output current	output sink current				
		V_{DD} = 1.8 V	3	5.5	-	mA
		V_{DD} = 3.3 V	5	9	-	mA
SPI-bus						
V_I	input voltage					
		on pin SCL	V_{SS} − 0.5	-	5.5	V
		on pins $\overline{CE}$ and SDI	V_{SS} − 0.5	-	V_{DD} + 0.5	V
On pins SCL, $\overline{CE}$ and SDI						
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	-	V
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}	−1	-	+1	µA

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Table 43. Static characteristics *...continued*

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 V to 9.0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
LCD outputs							
ΔV_O	output voltage variation						
		on pins BP0 to BP7	[7]	-	2.5	+10	mV
		on pins S0 to S43	[8]	-	2.5	+10	mV
R_O	output resistance						
		V_{LCD} = 7 V; on pins BP0 to BP7	[9]	-	0.9	5.0	kΩ
		V_{LCD} = 7 V; on pins S0 to S43	[9]	-	1.5	6.0	kΩ

[1] Power-down mode is enabled; I²C-bus or SPI-bus inactive.

[2] 1:8 multiplex drive mode; ¼ bias; display enabled; LCD outputs are open circuit; RAM is all written with logic 1; inputs at V_{SS} or V_{DD}; default display prescale factor; I²C-bus or SPI-bus inactive.

[3] 1:8 multiplex drive mode; ¼ bias; display enabled; LCD outputs are open circuit; RAM is all written with logic 1; inputs at V_{SS} or V_{DD}; default display prescale factor; I²C-bus or SPI-bus inactive; six PWM channels active at 50 % duty.

[4] Strongly linked to V_{LCD} voltage. See Figure 44.

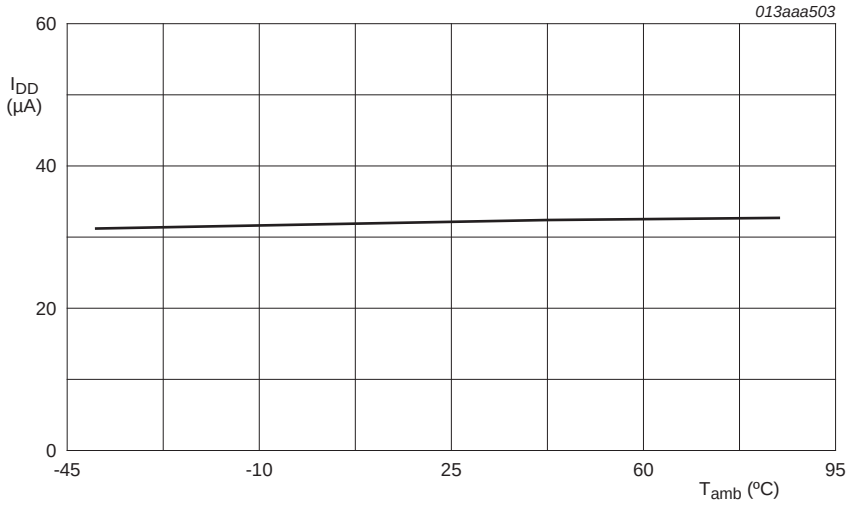
[5] 1:8 multiplex drive mode; ¼ bias; display enabled; LCD outputs are open circuit; RAM is all written with logic 1; default display prescale factor.

[6] The I²C-bus interface of PCF8536 is 5 V tolerant.

[7] Variation between any two backplanes on a given voltage level; static measured.

[8] Variation between any two segments on a given voltage level; static measured.

[9] Outputs measured one at a time.

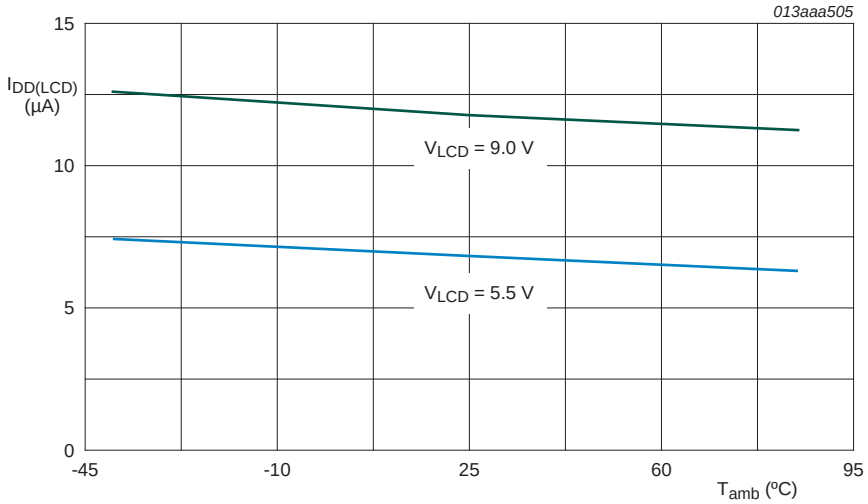


1:8 multiplex drive mode; ¼ bias; internal oscillator; display enabled; LCD outputs are open circuit; RAM is all written with logic 1; inputs at V_{SS} or V_{DD}; default display prescale factor; I²C-bus or SPI-bus inactive. Typical is defined at V_{DD} = 3.3 V, 25 °C.

Fig 43. Typical I_{DD} with respect to temperature

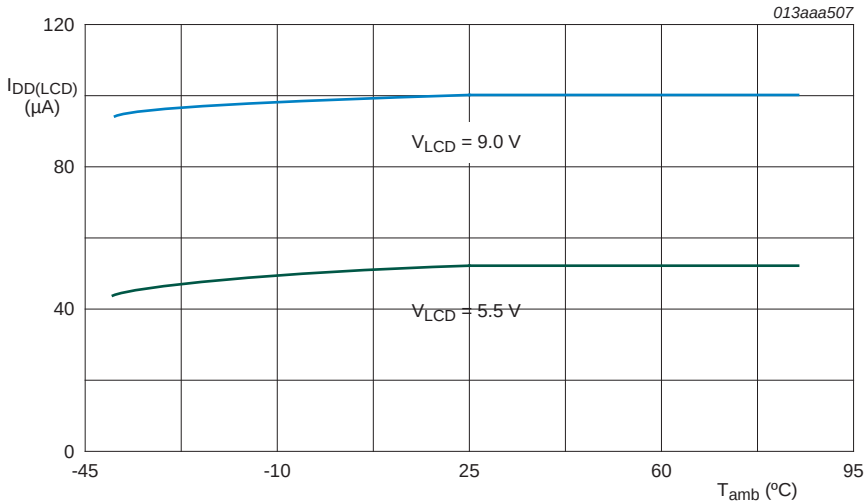
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Power-down mode is enabled; I²C-bus or SPI-bus inactive. Typical is defined at 25 °C.

Fig 44. Typical $I_{DD(LCD)}$ in power-down mode with respect to temperature



1:8 multiplex drive mode; ¼ bias; display enabled; LCD outputs are open circuit; RAM is all written with logic 1; default display prescale factor. Typical is defined at 25 °C.

Fig 45. Typical $I_{DD(LCD)}$ when display is active with respect to temperature

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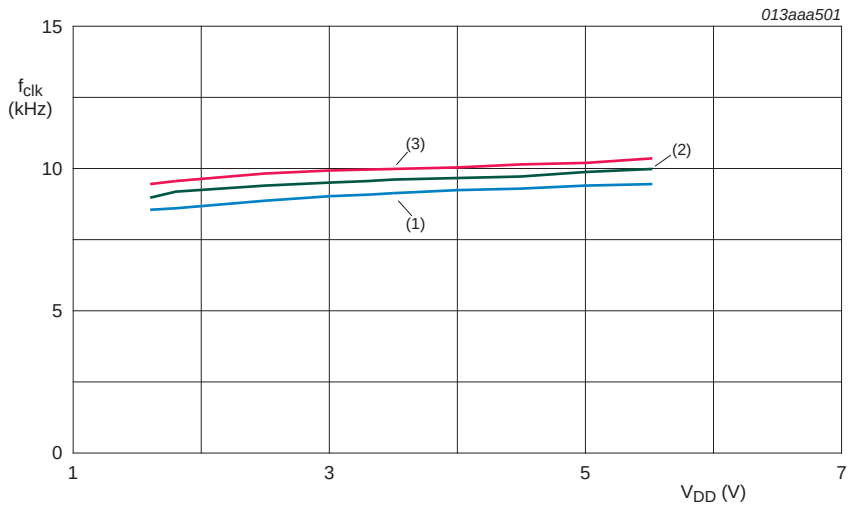
13. Dynamic characteristics

Table 44. Dynamic characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 V to 9.0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{clk}	clock frequency	output on pin OSCCLK; V_{DD} = 3.3 V	[1]	7800	9600	11040	Hz
$f_{clk(ext)}$	external clock frequency	EFR = 0		-	-	250000	Hz
$t_{(RESET_N)}$	RESET_N pulse width	LOW time		400	-	-	ns
External clock source used on pin OSCCLK							
$t_{clk(H)}$	clock HIGH time			33	-	-	µs
$t_{clk(L)}$	clock LOW time			33	-	-	µs

[1] Frequency present on OSCCLK with default display frequency division factor.

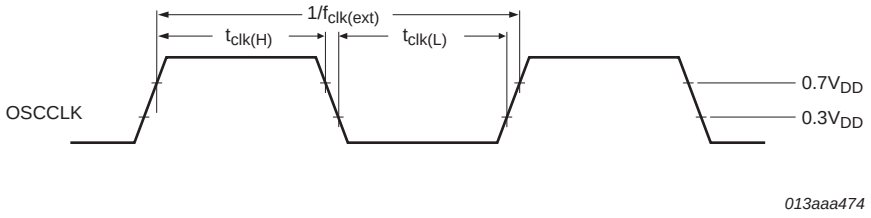


(1) −40 °C.

(2) 25 °C.

(3) 85 °C.

Fig 46. Typical clock frequency with respect to V_{DD} and temperature



External clock source used on pin OSCCLK.

Fig 47. Driver timing waveforms

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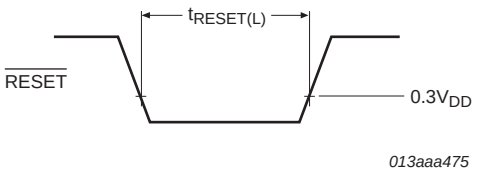


Fig 48. $\overline{\text{RESET}}$ timing

Table 45. Timing characteristics: I²C-bus

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 V to 9.0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified. All timing values are valid within the operating supply voltage and temperature range and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}. Timing waveforms see Figure 49.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Pin SCL							
f_{SCL}	SCL clock frequency		[1]	-	-	400	kHz
t_{LOW}	LOW period of the SCL clock			1.3	-	-	µs
t_{HIGH}	HIGH period of the SCL clock			0.6	-	-	µs
Pin SDA							
$t_{SU;DAT}$	data set-up time			100	-	-	ns
$t_{HD;DAT}$	data hold time			0	-	-	ns
Pins SCL and SDA							
t_{BUF}	bus free time between a STOP and START condition			1.3	-	-	µs
$t_{SU;STO}$	set-up time for STOP condition			0.6	-	-	µs
$t_{HD;STA}$	hold time (repeated) START condition			0.6	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			0.6	-	-	µs
t_r	rise time of both SDA and SCL signals	f_{SCL} = 400 kHz		-	-	0.3	µs
		f_{SCL} = 100 kHz		-	-	1.0	µs
t_f	fall time of both SDA and SCL signals			-	-	0.3	µs
$t_{VD;ACK}$	data valid acknowledge time		[2]	0.6	-	-	µs
$t_{VD;DAT}$	data valid time		[3]	0.6	-	-	µs
C_b	capacitive load for each bus line			-	-	400	pF
t_{SP}	pulse width of spikes that must be suppressed by the input filter		[4]	-	-	50	ns

[1] The minimum SCL clock frequency is limited by the bus time-out feature, which resets the serial bus interface if either the SDA or SCL is held LOW for a minimum of 25 ms. The bus time-out feature must be disabled for DC operation.

[2] $t_{VD;ACK}$ = time for acknowledgement signal from SCL LOW to SDA output LOW.

[3] $t_{VD;DAT}$ = minimum time for valid SDA output following SCL LOW.

[4] Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.

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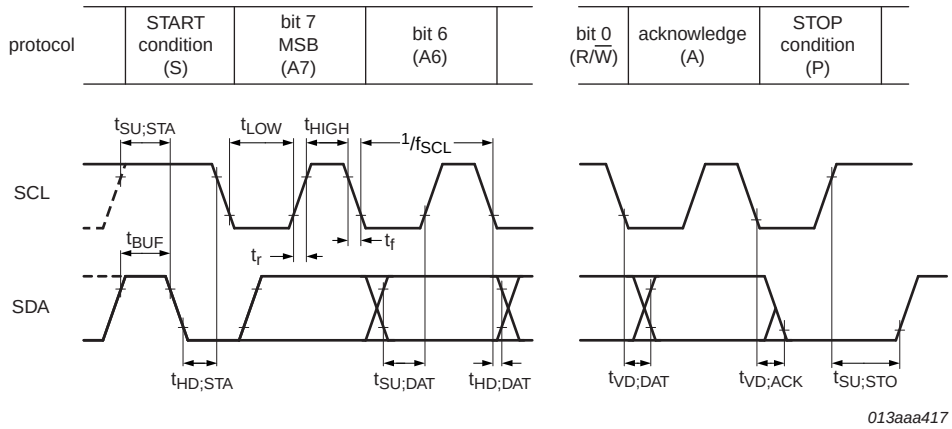


Fig 49. I²C-bus timing waveforms

Table 46. Timing characteristics: SPI-bus

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C. All timing values are valid within the operating supply voltage and temperature range and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}. Timing waveforms see Figure 50.

Symbol	Parameter	Conditions	V_{DD} < 2.7 V		V_{DD} ≥ 2.7 V		Unit
			Min	Max	Min	Max	
$f_{clk(SCL)}$	SCL clock frequency		-	2	-	5	MHz
t_{SCL}	SCL time		500	-	200	-	ns
$t_{clk(H)}$	clock HIGH time		200	-	80	-	ns
$t_{clk(L)}$	clock LOW time		200	-	80	-	ns
t_r	rise time	for SCL signal	-	100	-	100	ns
t_f	fall time	for SCL signal	-	100	-	100	ns
$t_{su(CE_N)}$	CE_N set-up time		150	-	80	-	ns
$t_{h(CE_N)}$	CE_N hold time		0	-	0	-	ns
$t_{rec(CE_N)}$	CE_N recovery time		100	-	100	-	ns
t_{su}	set-up time	set-up time for SDI data	10	-	5	-	ns
t_h	hold time	hold time for SDI data	25	-	10	-	ns

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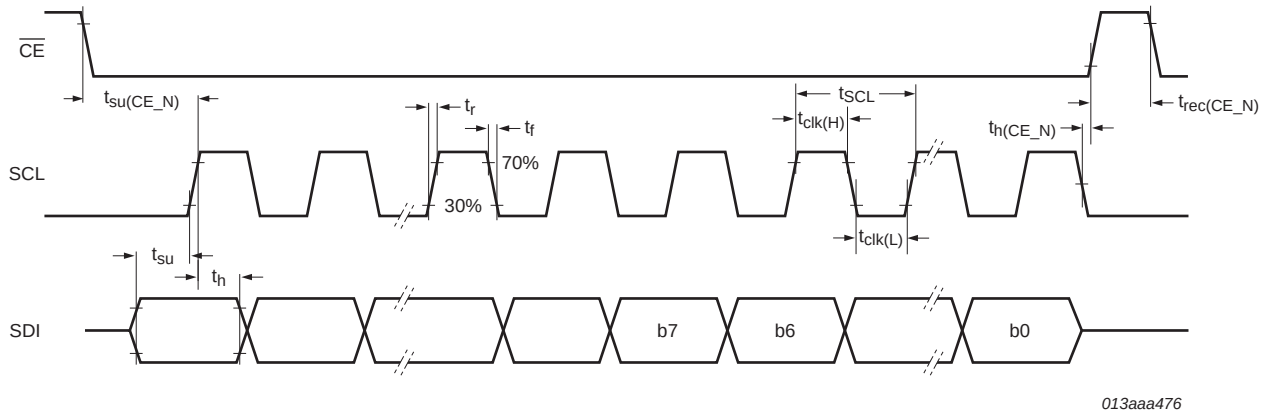


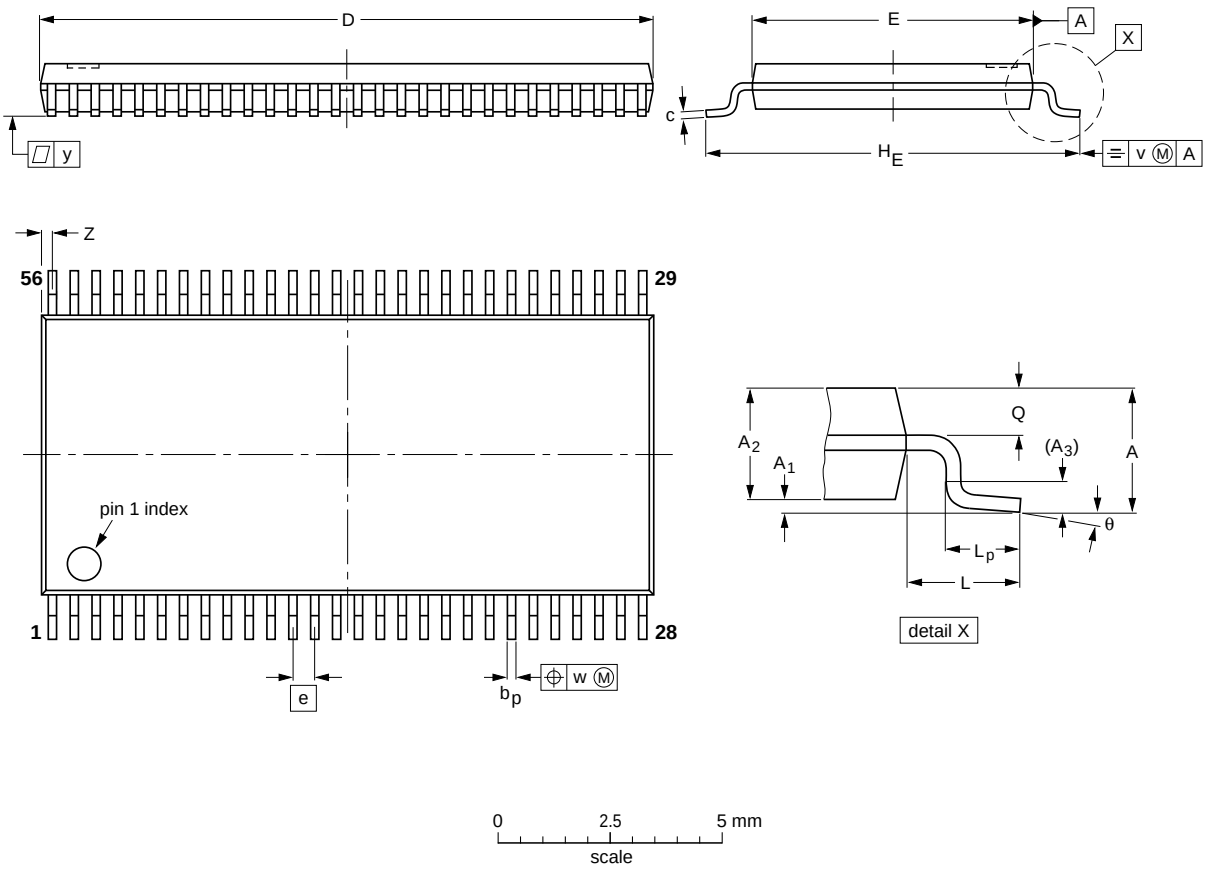
Fig 50. SPI-bus timing

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14. Package outline

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm **SOT364-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT364-1		MO-153				~~99-12-27~~ 03-02-19

Fig 51. Package outline SOT364-1 (TSSOP56)

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15. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

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16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 52) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 47 and 48

Table 47. SnPb eutectic process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 48. Lead-free process (from J-STD-020C)

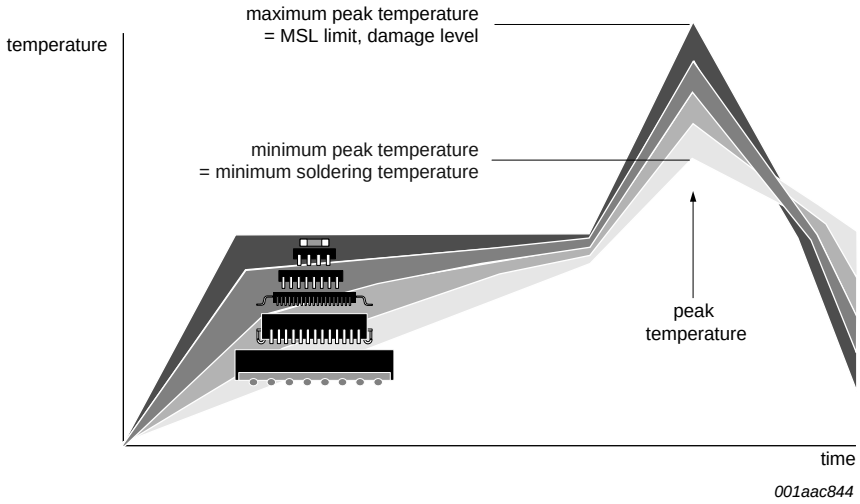
Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 52.

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MSL: Moisture Sensitivity Level

Fig 52. Temperature profiles for large and small components

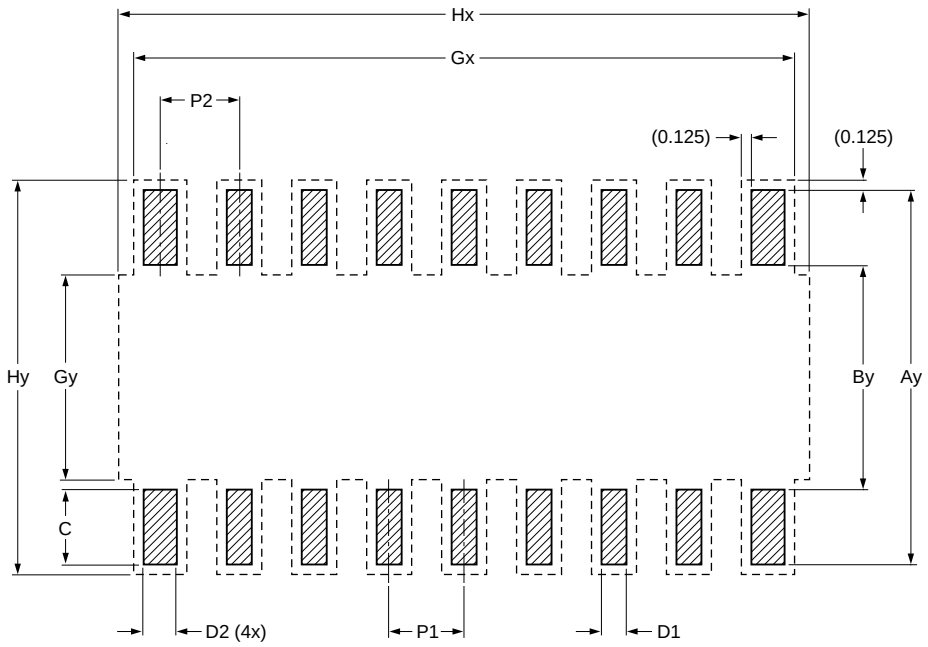
For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

17. Footprint information for reflow soldering

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Footprint information for reflow soldering of TSSOP56 package **SOT364-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	8.900	6.100	1.400	0.280	0.400	14.270	7.000	16.600	9.150

sot364-1_fr

Fig 53. Footprint information for reflow soldering of SOT364-1 (TSSOP56) package

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18. Appendix: possible PWM and LCD frame frequency combinations to avoid flicker

Table 49. LCD and PWM frame frequency combinations to avoid flicker [1]

Experiments have shown that likely no flicker occurs when PWM frame frequency and LCD frame frequency are between 40 Hz and 50 Hz apart and no flicker occurs if they are more than 50 Hz apart.

frame frequencies	PWM (f_{PWM})															
LCD ($f_{fr(LCD)}$)	**59.9**	**69.1**	**81.7**	**89.8**	**99.8**	**112.3**	**119.8**	**128.3**	**138.2**	**149.7**	**163.4**	**179.7**	**199.7**	**224.6**	**256.7**	**299.5**
59.9	0.0	9.2	21.8	29.9	20.0	7.5	0.0	8.6	18.4	29.9	16.3	0.0	20.0	15.0	17.1	0.0
70.5	10.6	1.4	11.2	19.4	29.4	28.6	21.1	12.6	2.7	8.8	22.4	31.7	11.7	13.2	25.2	17.6
79.9	20.0	10.8	1.8	10.0	20.0	32.4	39.9	31.4	21.5	10.0	3.6	20.0	39.9	15.0	17.1	20.0
90.4	29.4	21.3	8.7	0.6	9.4	21.9	29.4	37.9	42.6	31.1	17.5	1.1	18.8	43.8	14.5	28.3
99.8	20.0	30.7	18.2	10.0	0.0	12.5	20.0	28.5	38.4	49.9	36.3	20.0	0.0	25.0	42.8	0.0
108.9	10.9	29.3	27.2	19.1	9.1	3.4	10.9	19.4	29.3	40.8	54.5	38.1	18.2	6.8	38.9	27.2
119.8	0.0	18.4	38.1	29.9	20.0	7.5	0.0	8.6	18.4	29.9	43.6	59.9	39.9	15.0	17.1	59.9
129.5	9.7	8.7	33.8	39.7	29.7	17.2	9.7	1.2	8.7	20.2	33.8	50.2	59.4	34.4	2.3	40.5
140.9	21.1	2.7	22.4	38.8	41.1	28.6	21.1	12.6	2.7	8.8	22.4	38.8	58.7	57.3	25.2	17.6
149.7	29.9	11.5	13.6	29.9	49.9	37.4	29.9	21.4	11.5	0.0	13.6	29.9	49.9	74.9	42.8	0.0
159.7	20.0	21.5	3.6	20.0	39.9	47.4	39.9	31.4	21.5	10.0	3.6	20.0	39.9	64.9	62.7	20.0
171.1	8.6	32.9	7.8	8.6	28.5	53.5	51.3	42.8	32.9	21.4	7.8	8.6	28.5	53.5	85.6	42.8
177.5	2.2	29.9	14.1	2.2	22.2	47.1	57.7	49.1	39.2	27.7	14.1	2.2	22.2	47.1	79.2	55.5
184.3	4.6	23.0	20.9	4.6	15.4	40.3	55.3	55.9	46.1	34.6	20.9	4.6	15.4	40.3	72.4	69.1
191.7	12.0	15.7	28.3	12.0	8.0	32.9	47.9	63.3	53.4	41.9	28.3	12.0	8.0	32.9	65.0	83.9
199.7	20.0	7.7	36.3	20.0	0.0	25.0	39.9	57.0	61.4	49.9	36.3	20.0	0.0	25.0	57.0	99.8
208.3	28.6	1.0	36.7	28.6	8.7	16.3	31.3	48.4	68.1	58.6	45.0	28.6	8.7	16.3	48.4	91.1
217.8	21.8	10.5	27.2	38.1	18.2	6.8	21.8	38.9	58.6	68.1	54.5	38.1	18.2	6.8	38.9	81.7
228.2	11.4	20.8	16.9	41.4	28.5	3.6	11.4	28.5	48.3	71.3	64.8	48.5	28.5	3.6	28.5	71.3
239.6	0.0	32.3	5.4	29.9	39.9	15.0	0.0	17.1	36.9	59.9	76.2	59.9	39.9	15.0	17.1	59.9
252.2	12.6	24.2	7.2	17.3	47.3	27.6	12.6	4.5	24.2	47.3	74.5	72.5	52.5	27.6	4.5	47.3
266.2	26.6	10.2	21.2	3.3	33.3	41.6	26.6	9.5	10.2	33.3	60.5	86.5	66.6	41.6	9.5	33.3
281.9	17.6	5.4	36.8	12.3	17.6	55.1	42.3	25.2	5.4	17.6	44.8	77.5	82.2	57.3	25.2	17.6
299.5	0.0	23.0	27.2	29.9	0.0	37.4	59.9	42.8	23.0	0.0	27.2	59.9	99.8	74.9	42.8	0.0

[1] The table shows the smallest distance (Δf) from one frequency to the next or multiples of the next. Δf = MIN(f1 − n × f2); the values for n are 1 to 6; f1 and f2 can be either f_{PWM} or $f_{fr(LCD)}$; both relationships have to be considered. A PWM frame frequency (f_{PWM}) of less than 60 Hz may show flicker purely from the LCD.

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19. Abbreviations

Table 50. Abbreviations

Acronym	Description
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DC	Direct Current
EMC	ElectroMagnetic Compatibility
EPROM	Erasable Programmable Read-Only Memory
ESD	ElectroStatic Discharge
HBM	Human Body Model
I^2C	Inter-Integrated Circuit bus
IC	Integrated Circuit
LCD	Liquid Crystal Display
LED	Light-Emitting Diode
LSB	Least Significant Bit
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
MUX	Multiplexer
OTP	One Time Programmable
PCB	Printed-Circuit Board
POR	Power-On Reset
PWM	Pulse-Width Modulation
RC	Resistance-Capacitance
RAM	Random Access Memory
RGB	Red Green Blue
RMS	Root Mean Square
SCL	Serial CLock line
SDA	Serial DAta line
SPI	Serial Peripheral Interface

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20. References

[1] **AN10365 —** Surface mount reflow soldering description

[2] **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[3] **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

[4] **IPC/JEDEC J-STD-020D —** Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface-Mount Devices

[5] **JESD22-A114 —** Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[6] **JESD22-C101 —** Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components

[7] **JESD78 —** IC Latch-Up Test

[8] **JESD625-A —** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

[9] **NX3-00092 —** NXP store and transport requirements

[10] **SNV-FA-01-02 —** Marking Formats Integrated Circuits

[11] **UM10204 —** I^2C-bus specification and user manual

21. Revision history

Table 51. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF8536 v.2	20120221	Product Data Sheet	-	PCF8536 v.1
Modifications:	• Fixed typos			
PCF8536 v.1	20111006	Product Data Sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Date of release: 21 February 2012
Document identifier: PCF8536