DATA SHEET

PCF26100
Bluetooth Adapter IC

Preliminary specification
File under Integrated Circuits, IC17

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Philips
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PHILIPS

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1 FEATURES

The PCF26100 performs the following functions:

- Power-on reset (reset)
- System clock generation for baseband controller
- Reference clock generation for the UAA3558
- Low-power clock generation for baseband controller
- Transmit clock generation for baseband controller (1 MHz)
- Serial interface conversion between JTAG and 3-wire S-bus
- Timing control generation for the UAA3558
- Transmit data conversion from digital-to-analog gaussian shaped
- RSSI conversion from analog-to-digital and access through serial JTAG interface
- Transmit PA control information from JTAG interface digital-to-analog conversion
- Provides radio ID through the serial JTAG interface
- System clock oscillator trimming.

2 GENERAL DESCRIPTION

The PCF26100 is a mixed signal based adapter device for wireless Bluetooth systems. The device adapts the baseband interface of the Philips UAA3558 radio to the Philips PCF26002 and PCF26003 baseband controller devices and also to the BlueRF JTAG Unidirectional RxMode 2.

The adapter is provided as a low risk solution to a working Bluetooth system based on existing components. The adapter ASIC implementation incorporates, as much as possible, features to come to a complete Bluetooth system, meeting the Bluetooth RF requirements.

From the Bluetooth system point of view the PCF26100 is a transparent adaptation device between the baseband controller and the UAA3558 radio.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF26100ET	TFBGA48	plastic thin fine-pitch ball grid array package; 48 balls; $5 \times 5 \times 0.8$ mm	SOT641-1

4 BLOCK DIAGRAM

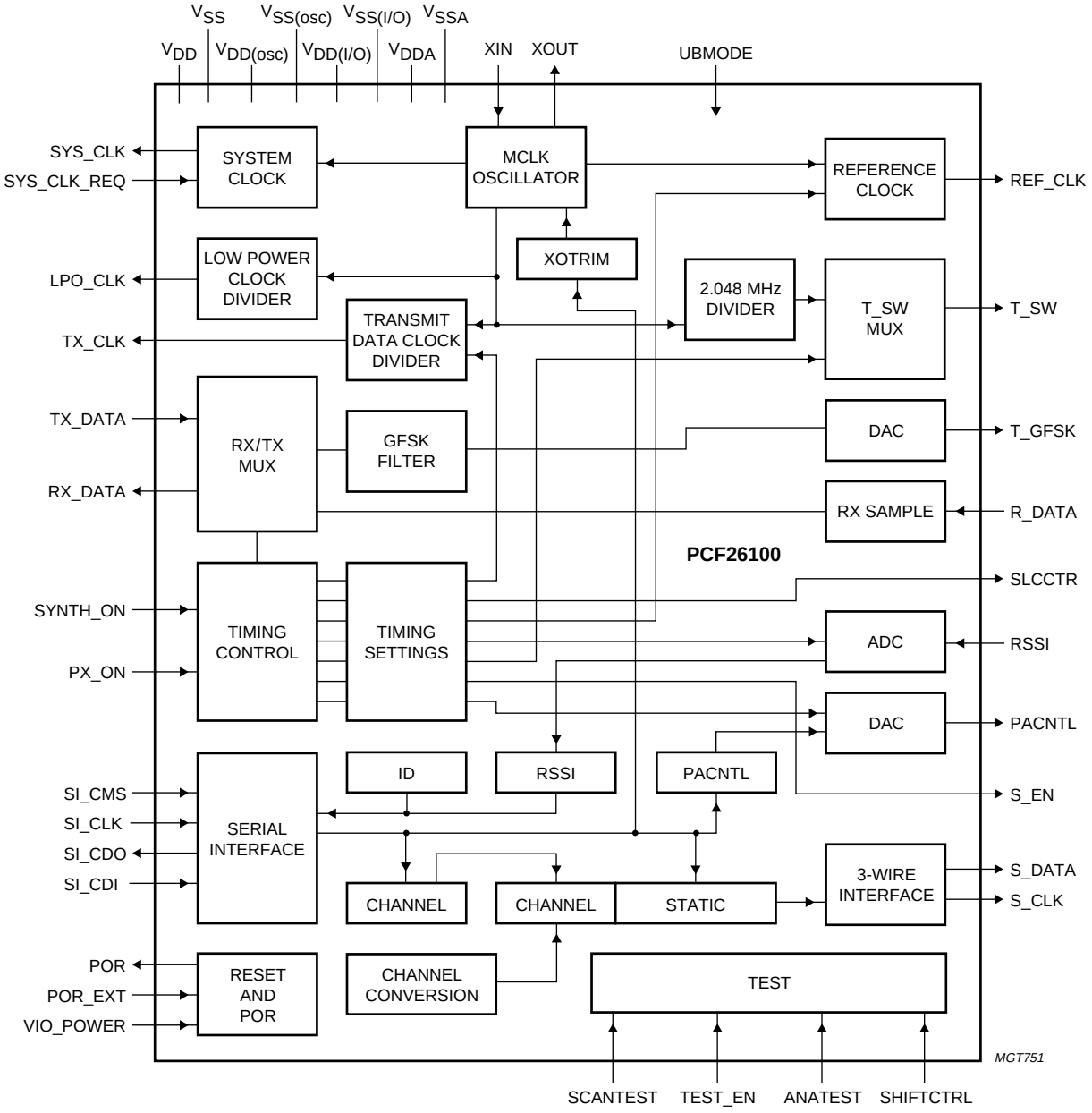


Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

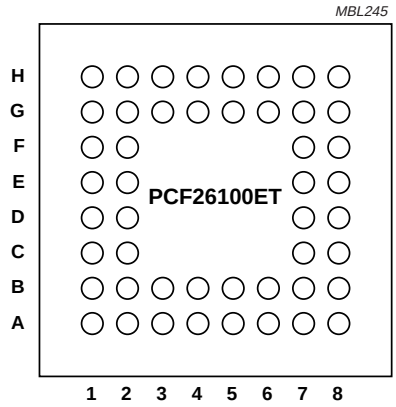


Fig.2 Pin configuration.

5.2 Pin description

Table 1 Pin description for the TFABGA48 package

SYMBOL	BALL	DESCRIPTION	I/O	SIGNAL TYPE	SOURCE
POR	A1	reset output to baseband controller	O	1 × CMOS output	BB
SHIFTCTRL	C2	test mode	I	non-inverting CMOS input with pull-down	test
VIO_POWER	B1	power-on reset reference	I	Schmitt-trigger input	
V_{DD}	C1	core supply voltage	P	core power	
LPO_CLK	D1	3.2 kHz low-power clock to baseband controller	O	1 × CMOS output	BB
PX_ON	E1	receive packet synchronization correlation achieved	I	non-inverting CMOS input	BB
$V_{SS(I/O)}$	E2	I/O ground supply	P	I/O ground	
SYS_CLK_REQ	F1	system clock control input from baseband controller	I	non-inverting CMOS input	BB
SYS_CLK	G1	controlled system clock output to baseband controller	O	3 × CMOS output	BB
TX_CLK	F2	transmit data clock output to baseband controller	O	1 × CMOS output	BB
V_{SS}	G2	core ground supply	P	core ground	
RX_DATA	H1	receive data output to baseband controller	O	1 × CMOS output	BB
ANATEST	G3	test mode	I	non-inverting CMOS input with pull-down	test
$V_{SS(osc)}$	H2	oscillator ground supply	P	oscillator ground	
XOUT	H3	oscillator output	O	oscillator output	misc
XIN	H4	oscillator input	I	oscillator input	misc
$V_{DD(osc)}$	H5	oscillator supply voltage	P	oscillator power	
$V_{DD(I/O)}$	G5	I/O supply voltage	P	I/O power	
POR_EXT	H6	reset and POR on control input	I	non-inverting CMOS input	host
TEST_EN	H7	test mode	I	non-inverting CMOS input with pull-down	test
SLCCTR	G6	DC offset control to UAA3558	O	1 × CMOS output	
$V_{SS(I/O)}$	G7	I/O ground supply	P	I/O ground	
S_EN	H8	serial interface and timing control output to UAA3558	O	1 × CMOS output	UAA
S_CLK	F7	serial interface clock output to UAA3558	O	1 × CMOS output	UAA
S_DATA	G8	serial interface data output to UAA3558	O	1 × CMOS output	UAA
REF_CLK	F8	reference clock output to UAA3558	O	3 × CMOS output	UAA
V_{SSA}	E8, D8	analog ground supply	P	analog ground	
RSSI	D7	RSSI analog input from UAA3558	I	analog input	UAA
T_GFSK	C8	analog transmit data output to UAA3558	O	analog output	UAA

SYMBOL	BALL	DESCRIPTION	I/O	SIGNAL TYPE	SOURCE
PACNTL	B8	analog PA control output to external PA	O	analog output	misc
V_{DDA}	C7	analog supply voltage	P	analog power	
R_DATA	B7	receive data input from UAA3558 (UAA3558 output = 0 to 2.2 V)	I	non-inverting CMOS input	UAA
T_SW	A8	transmit switch timing control to UAA3558 multiplexed with 2.048 MHz clock output	O	3 × CMOS output	UAA
SCANTEST	B6	test mode	I	non-inverting CMOS input with pull-down	test
TX_DATA	A7	transmit data	I	non-inverting CMOS input	BB
$V_{SS(I/O)}$	A6	I/O ground supply	P	I/O ground	
SYNTH_ON	A5	timing control input from baseband controller	I	non-inverting CMOS input	BB
UBMODE	A4	unidirectional/bidirectional mode selection	I	non-inverting CMOS input	misc
$V_{DD(I/O)}$	B4	I/O supply voltage	P	I/O power	
SI_CLK	A3	serial interface clock input from baseband controller	I	non-inverting CMOS input	BB
SI_CMS	A2	serial interface mode select input from baseband controller	I	non-inverting CMOS input	BB
SI_CDI	B3	serial interface data input from baseband controller	I	non-inverting CMOS input	BB
SI_CDO	B2	serial interface data output to baseband controller	O	1 × CMOS output	BB

6 FUNCTIONAL DESCRIPTION

6.1 PCF26100 overview

The adapter features a Power-on reset which is used to reset the adapter logic. There is also a POR_EXT signal which is used for controlling the reset of the PCF26100 within the application.

The system clock for the application is generated by the PCF26100. The system clock is then provided to the baseband SYS_CLK and the radio REF_CLK. Both the SYS_CLK and REF_CLK clocks are controlled within the PCF26100.

From the system clock a low-power 3.2 kHz clock LPO_CLK is generated.

From the PCF26100 a 1 MHz TX_CLK is generated to be used in the baseband controller to clock out the transmit data on TX_DATA.

The serial interface to the baseband controller is a JTAG interface. This interface is used to initialize and control the PCF26100 and subsequently the radio. The channel information received from the JTAG interface is converted and forwarded to the radio 3-wire S-bus interface.

The timing control signals to the UAA3558 radio are generated in the PCF26100. For this a minimum number of reference timing signals from the baseband controller are used. The exact timing of the control signals is programmable in the PCF26100.

The PCF26100 converts the digital transmit data from the baseband controller to analog gaussian shaped transmit data to the radio.

The analog RSSI from the radio is converted to digital and made available to the baseband controller via the JTAG interface.

The digital power amplifier control information communicated from the baseband controller to the PCF26100 is converted to an analog control voltage for the radio.

The PCF26100 provides an identification number, which can be read by the baseband controller through the JTAG interface.

For frequency compensation and tuning, the PCF26100 provides a tuning capability on the system oscillator.

6.2 BlueRF pin mapping

Table 2 Adapter and BlueRF unidirectional pin mapping.

ADAPTER TO BASEBAND PIN NAME	BLUERF PIN NAME JTAG UNIDIRECTIONAL RXMODE 2
POR_EXT	BnPWR
POR	not applicable
LPO_CLK	not applicable
SYS_CLK	not applicable
SYS_CLK_REQ	BXTLEN
TX_CLK	BRCLK
TX_DATA	BTXD/BDATA1
RX_DATA	BRXD
SYNTH_ON	BSEN
PX_ON	BPKTCTL/BDATA2
SI_CMS	BnDEN
SI_CLK	BDCLK
SI_CDI	BMOSI/BDDATA
SI_CDO	BMISO
VIO_POWER	not applicable

6.3 Timing

The timing for the radio is generated in the PCF26100 using a minimal number of baseband signals. The channel programming is received from the JTAG serial interface. The SYNTH_ON signal is used to determine the start and end of the packet. The radio SLCCTR signals is also controlled with PX_ON.

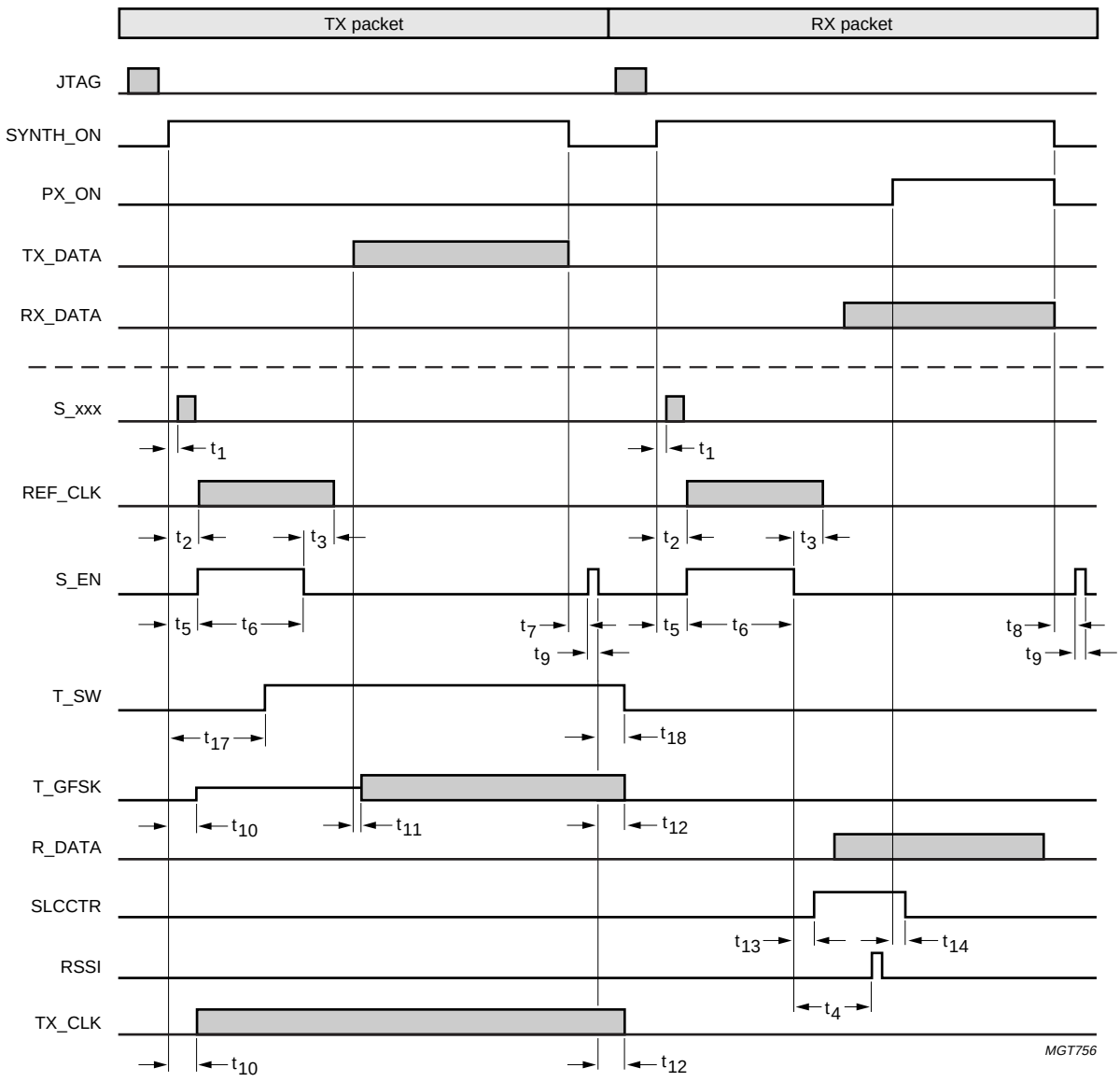


Fig.3 Detailed timing diagram.

Table 3 Adapter timing parameters

PARAMETER	DESCRIPTION	VALUE	UNIT
t_1	SYNTH_ON rising edge to 3-wire serial data	0.35	µs
t_2	SYNTH_ON rising edge to REFCLK start	S_EN start	µs
t_3	S_EN falling edge to REFCLK stop delay	2	µs
t_4	S_EN falling edge to RSSI measurement	RSSI_start	µs
t_5	SYNTH_ON rising edge to S_EN rising edge	S_EN start	µs
t_6	S_EN width	S_EN width	µs
t_7	SYNTH_ON falling edge to S_EN pulse rising edge	S_EN pulse start	µs
t_8	SYNTH_ON falling edge to S_EN pulse rising edge	S_EN pulse start	µs
t_9	S_EN pulse width	2	µs
t_{10}	SYNTH_ON rising edge to T_GFSK DC bias and TXCLK enable	GFSK_DC_bias start	µs
t_{11}	TX_DATA digital in to T_GFSK analog out delay	14	13 MHz cycles
t_{12}	S_EN pulse falling edge to T_GFSK LOW and TXCLK disable	0	µs
t_{13}	S_EN falling edge to SLCCTR rising edge	SLCCTR start	µs
t_{14}	PX_ON rising edge to SLCCTR falling edge	0	µs
t_{17}	SYNTH_ON rising edge to T_SW rising edge	T_SW start	µs
t_{18}	S_EN pulse falling edge to T_SW falling edge	0	µs

6.3.1 T_GFSK

The T_GFSK data output has 3 phases:

1. Idle phase
2. DCbias phase
3. Txdata phase.

The Idle phase is used outside transmit packets. In this phase the T_GFSK output state is defined by the ‘gfsk float’ bit in the Enable Register. If the ‘gfsk float’ bit is set to a logic 0, the T_GFSK output is pulled to ground; if set to a logic 1 the T_GFSK output is floating.

The DCbias phase is used during the transmit slot as start-up phase before the transmit data. The DCbias phase is active GFSK_DC_BIAS_Start delay following the S_EN rising edge until the first transmit data bit on TX_DATA.

During this phase a DC bias is generated by the GFSK filter, which is achieved by selecting the GFSK table mid-value as the output of the GFSK filter.

The Txdata phase is used when TXDATA is present. In this phase the TX_DATA is fed into the GFSK filter. The presence of TXDATA is determined by detecting the first TXDATA edge. The end of the TXDATA is detected by the end of packet from the baseband controller. To not lose TXDATA information in the T_GFSK output, due to the data detection, the data from the GFSK input is delayed with 1-bit.

The T_GFSK output requires an external low-pass filter. The reference voltage for the T_GFSK comes directly from the V_{DDA} power supply. Any variation on V_{DDA} has a direct relation to a variation in the T_GFSK levels. The V_{DDA} power supply should be provided from a voltage reference.

The TX_CLK output is activated during the DC_BIAS phase and the Txdata phase.

6.3.2 RESET

The PCF26100 is reset with a Power-on reset using the VIO_POWER signal. This will reset all registers and put the device into a known state. The POR_EXT reset signal will also reset the device and put it in the same state as the Power-on reset. However, POR_EXT is intended to be used for a reset from a host.

Following the Power-on reset or a reset by POR_EXT, the system oscillator is started and the SYS_CLK output is activated (enabled). The SYS_CLK output can be controlled by the SYS_CLK_REQ signal but only if the 'rdy' bit in the Control Register has been set to logic 1.

The function of SYS_CLK_REQ has 2 phases:

1. After reset, SYS_CLK_REQ is not taken into account for the generation of SYS_CLK. After reset the 13 MHz system clock is enabled on SYS_CLK.
2. Once the 'rdy' bit is set to logic 1, the 13 MHz clock on the SYS_CLK is controlled with SYS_CLK_REQ.

The SYS_CLK_REQ signal will not control or disable the oscillator.

The LPO_CLK output is only controlled by the POR_EXT signal which also controls the POR output. The POR is activated 4 SYS_CLK cycles after POR_EXT.

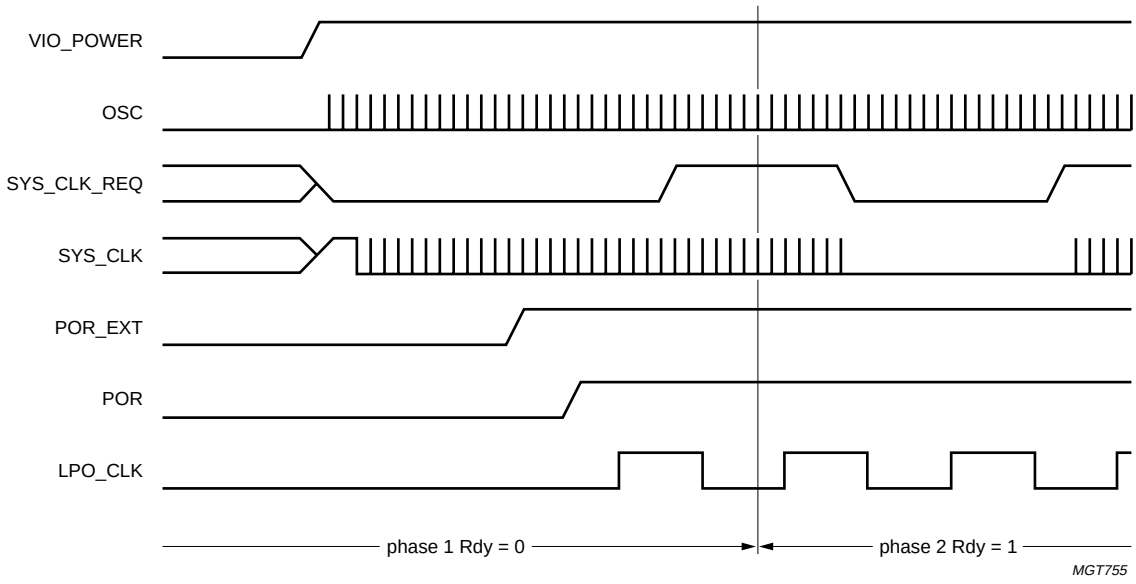


Fig.4 Reset timing.

6.4 Serial interface

6.4.1 3-WIRE S-BUS

The 3-wire S-bus at the radio side is a 32-bit serial interface which is used for control, TX/RX and channel information. The 32-bit definition is given in Tables 4 and 5.

Bits 31 to 9 are static values and will not change dynamically, the value for these bits come from the static registers. Only the trx and main divider fields will control the UAA3558 on a slot-by-slot basis. The trx and main divider information comes from the baseband controller serial interface channel word; see Section 6.5.1. However, the baseband controller channel information needs a conversion to get the correct main divider information for the UAA3558.

Table 4 UAA3558 3-wire programming word

31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
test				dpo	BW adjust				strc	sdsn	sdco	ssqs	ssth	dmo	tin

Table 5 UAA3558 3-wire programming word (continued)

15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
tsw	tamp	ref1	ref0	txp1	txp0	pll	trx	main divider (n)							

6.4.2 JTAG

The JTAG serial interface is used to control the PCF26100 and subsequently the radio. The PCF26100 must be the only slave on the JTAG bus as the PCF26100 does not allow for multi-slave operation. The JTAG interface protocol used is fully compliant with the standard set out in *"IEEE Std 1149.1-1990"*. The following features are supported:

- 5-bit register address
- 8-bit data
- Set instruction register
- Read/write data register (note: some addresses have a separate read and write data register).

The JTAG interface allows for 2 ways of accessing a register. One is the communicate address and data, and the second one is for successive accesses to the same registers where only the data is communicated. This can, for example, be used for updating the channel information before every packet.

6.5 Registers

The registers that are controlled via the serial interface are shown in Table 6.

Table 6 Register map

REGISTER	TYPE	ADDRESS (DECIMAL)	RESET (HEX)	DESCRIPTION
S_EN_start	R/W	8	0C	S_EN start delay
S_EN_width	R/W	9	C8	S_EN width
T_SW_start	R/W	10	64	T_SW start delay
SLCCTR_start	R/W	11	0A	SLCCTR start delay
S_EN_PULSE_start	R/W	12	02	S_EN pulse start delay
RSSI_start	R/W	13	64	RSSI measurement position
STATIC_B15_9	R/W	14	24	UAA3558 serial word static values
STATIC_B23_16	R/W	15	12	UAA3558 serial word static values
STATIC_B31_24	R/W	16	00	UAA3558 serial word static values
CHANNEL	W	18	00	frequency channel number and TX/RX information
RSSI	R	18	00	RSSI
XO-trim	W	19	80	trim value for the system clock oscillator
ID	R	19	A1	device identification
CONTROL	R/W	22	00	system clock control
PACONTROL	R/W	24	00	for external PA power control
ENABLE	R/W	25	00	adapter control
GFSK_DC_BIAS_start	R/W	26	64	GFSK DC bias start delay
GFSK_TABLE	R/W	28	00	GFSK look-up table values
RXFREQ	W	30	61	RX channel conversion number
TXFREQ	W	31	60	TX channel conversion number

6.5.1 CHANNEL PROGRAMMING

The serial interface channel programming word is forwarded to the UAA3558 3-wire interface. The channel information cannot normally be used directly and needs a conversion to get the right number for the UAA3558.

Table 7 Channel programming word

ADDRESS	7	6	5	4	3	2	1	0
18 (decimal)	trx	channel number (m)						

Table 8 Description of Channel programming word bits

BIT	DESCRIPTION
7	If trx = 0, then device in Transmit mode. If trx = 1, then device in Receive mode.
6 to 0	These 7 bits determine the channel number (m).

6.5.2 Frequency channel conversion

The conversion number is programmable for TX and RX. The function implemented is:

TX frequency = 2304 + m + TXFREQ; where m is the BT channel number and TXFREQ is programmable between 0 and 255

RX frequency = 2304 + m + RXFREQ; where m is the BT channel number and RXFREQ is programmable between 0 and 255.

Table 9 Frequency conversion word RXFREQ

ADDRESS	7	6	5	4	3	2	1	0
30 (decimal)	RXFREQ							

Table 10 Frequency conversion word TXFREQ

ADDRESS	7	6	5	4	3	2	1	0
31 (decimal)	TXFREQ							

6.5.3 Static values

The UAA3558 bits 31 to 9 are static values and will not change dynamically. These values are programmed into the adapter via the serial interface. The static words are: STATIC_B15_9, STATIC_B23_16 and STATIC_B31_24.

Table 11 Static word STATIC_B15_9

ADDRESS	7	6	5	4	3	2	1	0
14 (decimal)	static value bits 15 to 9							not used

Table 12 Static word STATIC_B23_16

ADDRESS	7	6	5	4	3	2	1	0
15 (decimal)	static value bits 23 to 16							

Table 13 Static word STATIC_B31_24

ADDRESS	7	6	5	4	3	2	1	0
16 (decimal)	static value bits 31 to 24							

6.5.4 TIMING VALUES

The UAA3558 needs some timing signals which do not have a corresponding signal at the BlueRF interface. These signals are generated internally in the adapter. The timing values for these will not change dynamically. These values are programmed into the adapter via the serial interface. The timing words are: S_EN_start, S_EN_width, T_SW_start, SLCCTR_start, S_EN_PULSE_start, RSSI_start, and GFSK_DC_bias.

Table 14 Timing control word S_EN_start

ADDRESS	7	6	5	4	3	2	1	0
8 (decimal)	programmed timing value (resolution of 1-bit = 1 μs)							

Table 15 Timing control word S_EN_width

ADDRESS	7	6	5	4	3	2	1	0
9 (decimal)	programmed timing value (resolution of 1-bit = 1 μs)							

Table 16 Timing control word T_SW_start

ADDRESS	7	6	5	4	3	2	1	0
10 (decimal)	programmed timing value (resolution of 1-bit = 1 μs)							

Table 17 Timing control word SLCCTR_start

ADDRESS	7	6	5	4	3	2	1	0
11 (decimal)	programmed timing value (resolution of 1-bit = 1 μs)							

Table 18 Timing control word S_EN_PULSE_start

ADDRESS	7	6	5	4	3	2	1	0
12 (decimal)	programmed timing value (resolution of 1-bit = 1 μs)							

Table 19 Timing control word RSSI_start

ADDRESS	7	6	5	4	3	2	1	0
13 (decimal)	programmed timing value (resolution of 1-bit = 1 μs)							

Table 20 Timing control word GFSK_DC_bias

ADDRESS	7	6	5	4	3	2	1	0
26 (decimal)	programmed timing value (resolution of 1-bit = 1 μs)							

Table 21 Register values range and actual timings

REGISTER	RANGE	TIMING	ACTUAL VALUE	UNIT
S_EN_START	0 < x < 256	t_2 and t_5	S_EN_START + (0 to 1)	µs
S_EN_WIDTH	0 < x < 256	t_6	S_EN_WIDTH	µs
T_SW_START	S_EN_START < x < 256	t_{17}	T_SW_START + (0 to 1)	µs
SLCCTR_START	0 < x < 256	t_{13}	SLCCTR_START + 1	µs
S_EN_PULSE_DEL	0 < x < 256	t_7 and t_8	S_EN_PULSE_DEL + (0 to 1)	µs
RSSI_START	0 < x < 256	t_4	RSSI_START	µs
GFSK_DC_BIAS	0 < x < 256	t_{10}	GFSK_DC_BIAS + (0 to 1)	µs

6.5.5 RSSI

The RSSI is read via the serial interface. The UAA3558 provides an analog RSSI output. The interface logic converts the analog RSSI value and stores the result in a serial interface register. The timing for converting the RSSI is programmed using the RSSI_start register. The RSSI can only be measured starting 10 µs after the S_EN falling edge. The RSSI value can only be read from the serial interface register after the measurement has been completed, this is at the end of the packet. RSSI measurements are only done in receive packets.

Table 22 RSSI control word

ADDRESS	7	6	5	4	3	2	1	0
18 (decimal)	RSSI							

6.5.6 Transmit power control

The transmit power can be controlled from a serial interface register. The 8-bit transmit power control word is used to control the PA DAC. Writing to the PA DAC register will directly change the PA DAC output. The PA control register should be written when the transmitter is not active.

Table 23 Unidirectional JTAG PA control word

ADDRESS	7	6	5	4	3	2	1	0
24 (decimal)	PA power control							

6.5.7 GFSK table

The values for the GFSK filter are stored in a 13-byte GFSK table. The GFSK table is accessed through a single control word which is used to store the data in the GFSK table on subsequent writes. To align the writing to the GFSK table a table address reset bit is available in the Enable register. When the reset bit ‘grst’ in the Enable register is set to a logic 1 the GFSK table address will be reset and the next GFSK control word is written at location 0 in the GFSK table. Every subsequent write to the GFSK control word will be stored at the next address in the GFSK table. If the last address is reached, subsequent writes will continue to effect the last address.

The values for the GFSK table depend on the reference voltage on V_{DDA}. The T_GFSK signal should have a DC_Bias of 1.2 V with a peak-to-peak swing of 1 V (amplitude = 0.5 V). For this the values for the GFSK table are calculated as shown in Table 26.

Table 24 Unidirectional JTAG GFSK control word

GFSK_TABLE	7	6	5	4	3	2	1	0
28 (decimal)	GFSK table value							

Table 25 GFSK table reset values

TABLE ADDRESS (DECIMAL)	RESET VALUE (HEX)
12	91
11	90
10	8E
9	89
8	81
7	74
6	64
5	54
4	47
3	3E
2	3A
1	38
0	37

Table 26 GFSK value calculation

TABLE ADDRESS (DECIMAL)	CALCULATION[1]	VALUE AT 3 V	
		DECIMAL	HEX
0	$[DCBias + (A \times -96)] \times B$	59	3B
1	$[DCBias + (A \times -94)] \times B$	60	3C
2	$[DCBias + (A \times -90)] \times B$	62	3E
3	$[DCBias + (A \times -80)] \times B$	66	42
4	$[DCBias + (A \times -62)] \times B$	74	4A
5	$[DCBias + (A \times -34)] \times B$	87	57
6	$[DCBias + (A \times 0)] \times B$	102	66
7	$[DCBias + (A \times 34)] \times B$	117	75
8	$[DCBias + (A \times 62)] \times B$	130	82
9	$[DCBias + (A \times 80)] \times B$	138	8A
10	$[DCBias + (A \times 90)] \times B$	142	8E
11	$[DCBias + (A \times 94)] \times B$	144	90
12	$[DCBias + (A \times 96)] \times B$	145	91

Note

1. Where $A = \frac{Amp}{96}$ and $B = \frac{255}{V_{DDA}}$

6.5.8 CONTROL REGISTER (CONTROL)

The Control Register is used to control SYS_CLK in the adapter.

Table 27 Control Register

ADDRESS	7	6	5	4	3	2	1	0
22 (decimal)	–	–	–	–	–	rdy	–	–

Table 28 Description of CONTROL bits

BIT	SYMBOL	DESCRIPTION
7 to 3	–	These 5 bits are reserved and are not to be used.
2	rdy	**Baseband ready.** This bit is used to control the function of SYS_CLK_REQ.
1	–	These 2 bits are reserved and are not to be used.
0	–	

6.5.9 ENABLE REGISTER (ENABLE)

The Enable Register is used to control functions in the adapter.

Table 29 Enable Register

ADDRESS	7	6	5	4	3	2	1	0
25 (decimal)	gfsk float	grst	pa float	clk en	test.2	test.1	test.0	–

Table 30 Description of ENABLE bits

BIT	SYMBOL	DESCRIPTION
7	gfsk float	Controls the T_GFSK output outside TX packet. If gfsk = 0, then output tied to ground. If gfsk = 1, then output floats.
6	grst	GFSK table address reset. Writing a logic 1 will reset the GFSK table addressing.
5	pa float	Controls the PA output outside TX packet. If pa float = 0, then output tied to ground. If pa float = 1, then output floats.
4	clk en	Enables the 2.048 MHz clock on T_SW. If clk en = 0, then pin T_SW = T_SW. If clk en = 1, then pin T_SW = 2.048 MHz.
3	test.2	These 3 bits are used for test purposes.
2	test.1	
1	test.0	
0	–	This bit is reserved and should not be used.

6.5.10 Oscillator Trim Register (XO_trim)

The Oscillator Trim Register is used to control the frequency of the 13 MHz oscillator. This is achieved by controlling the capacitive load on the XIN and XOUT pins.

Table 31 Oscillator Trim Register

ADDRESS	7	6	5	4	3	2	1	0
19 (decimal)	–	XO_trim.6	XO_trim.5	XO_trim.4	XO_trim.3	XO_trim.2	XO_trim.1	XO_trim.0

Table 32 Description of XO_trim bits

BIT	SYMBOL	DESCRIPTION
7	–	This bit is reserved and should not be used.
6	XO_trim.6	add 6 pF to XIN and XOUT
5	XO_trim.5	add 3 pF to XIN and XOUT
4	XO_trim.4	add 1.5 pF to XIN and XOUT
3	XO_trim.3	add 0.75 pF to XIN and XOUT
2	XO_trim.2	add 0.375 pF to XIN and XOUT
1	XO_trim.1	add 0.1875 pF to XIN and XOUT
0	XO_trim.0	add 0.09375 pF to XIN and XOUT

6.5.11 Identification Register (ID)

The Identification Register is used to identify the radio chip set from the baseband controller. This is a read only register.

Table 33 Identification Register

ADDRESS	7	6	5	4	3	2	1	0
19 (decimal)	ID.7	ID.6	ID.5	ID.4	ID.3	ID.2	ID.1	ID.0

Table 34 Description of ID bits

BIT	SYMBOL	DESCRIPTION
7 to 0	ID.[7:0]	These 8 bits determine the radio chip set identification (value = A1H).

7 REFERENCE DOCUMENTS

1. UAA3558 Bluetooth RF Transceiver (Philips data sheet).
2. PCF26002 Bluetooth baseband controller (Philips data sheet).
3. BlueRF specification (ARM Ltd).

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
V_{DD}	core supply voltage	V_{SS} – 0.5	V_{SS} + 3.6	V
V_{DDA}	analog supply voltage	V_{SS} – 0.5	V_{SS} + 3.6	V
$V_{DD(I/O)}$	I/O supply voltage	V_{SS} – 0.5	V_{SS} + 3.6	V
$V_{DD(osc)}$	oscillator supply voltage	V_{SS} – 0.5	V_{SS} + 3.6	V
V_{in}	input voltage	V_{SS} – 0.5	V_{DD} + 0.3	V
T_{stg}	storage temperature	–50	+150	°C
T_{oper}	operating temperature	0	+70	°C

9 DC CHARACTERISTICS

SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
V_{DD}	core supply voltage	2.7	3.0 to 3.3	3.6	V
V_{DDA}	analog supply voltage for ADC and DAC; note 1	2.7	3.0 to 3.3	3.6	V
$V_{DD(I/O)}$	I/O supply voltage	2.7	3.0 to 3.3	3.6	V
$V_{DD(osc)}$	oscillator supply voltage	2.7	3.0 to 3.3	3.6	V
P_{tx}	transmit power consumption	–	22	–	mW
P_{rx}	receive power consumption	–	14	–	mW
P_{stb}	standby power consumption; note 2	–	3	–	mW
V_{IL}	LOW-level input voltage	–0.5	–	$+0.3V_{DD(I/O)}$	V
V_{IH}	HIGH-level input voltage	$0.7V_{DD(I/O)}$	–	V_{DD} + 0.3	V
V_{OL}	LOW-level output voltage	–	–	0.5	V
V_{OH}	HIGH-level output voltage	2.4	–	–	V
I_{LI}	input leakage current	–10	–	+10	µA

Notes

1. V_{DDA} should be supplied from a stable source.
2. Standby power consumption is measured when SYS_CLK_REQ = 0.

10 AC CHARACTERISTICS

SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
Frequency					
f_{sys}	system clock frequency	–	13	–	MHz
$f_{clk(LP)}$	low power clock frequency	–	3.2	–	MHz
$f_{s\text{-}bus}$	3-wire S-bus frequency	–	6.5	–	MHz
f_{JTAG}	JTAG clock frequency	1	–	5	MHz
f_{clock}	2.048 MHz clock output	–	2.048	–	MHz
D_{clock}	duty cycle 2.048 MHz clock output	–	40/60	–	%
RSSI ADC					
$RES_{(ADC)}$	RSSI ADC resolution	–	8	–	bit
$LE_{(ADC)}$	RSSI ADC linearity error	–0.5	0	+0.5	LSB
$E_{offset(ADC)}$	RSSI ADC offset error	–50	0	+50	mV
$E_{FS(ADC)}$	RSSI ADC full-scale error	–50	0	+50	mV
$V_{i(ADC)}$	RSSI ADC signal input voltage range	0	–	V_{DDA}	V
$Z_{i(ADC)}$	RSSI ADC input impedance	–	10	–	MΩ
GFSK DAC					
$RES_{(DAC)}$	DAC resolution	–	8	–	bit
$LE_{DAC(i)}$	DAC integral linearity error	–1.0	–	+1.0	LSB
$LE_{DAC(diff)}$	DAC differential linearity error	–0.5	–	+0.5	LSB
$E_{offset(DAC)}$	DAC offset error	–50	–	+50	mV
$E_{FS(DAC)}$	DAC full-scale error	–50	–	+50	mV
$V_{o(DAC)}$	DAC signal output voltage range	0	–	V_{DDA}	V
$R_{L(DAC)}$	DAC load resistance	600	–	–	LSB
$C_{L(DAC)}$	DAC load capacitance	–	–	20	pF

11 APPLICATIONS

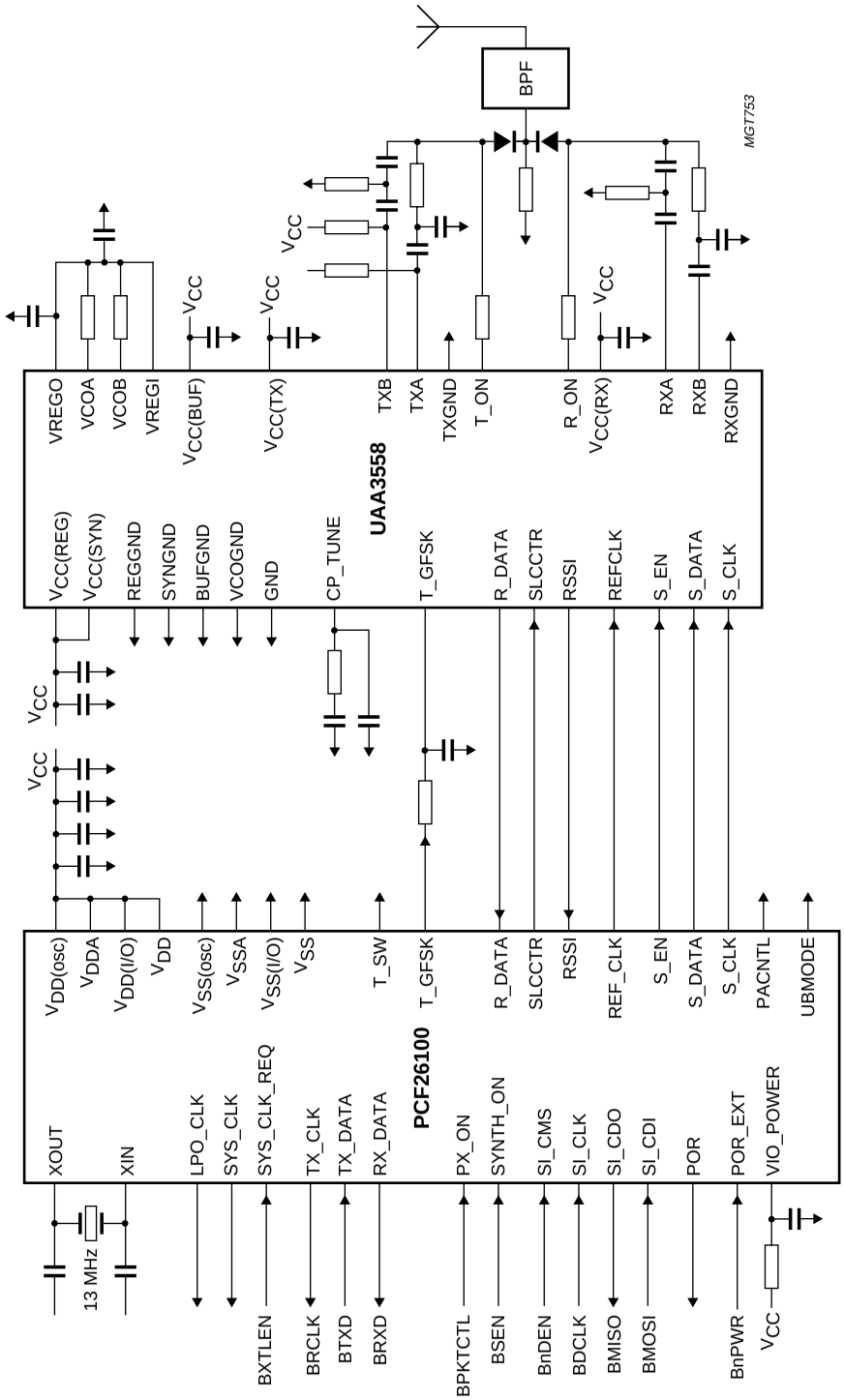


Fig.5 Application diagram BlueRF JTAG Unidirectional RxMode 2.

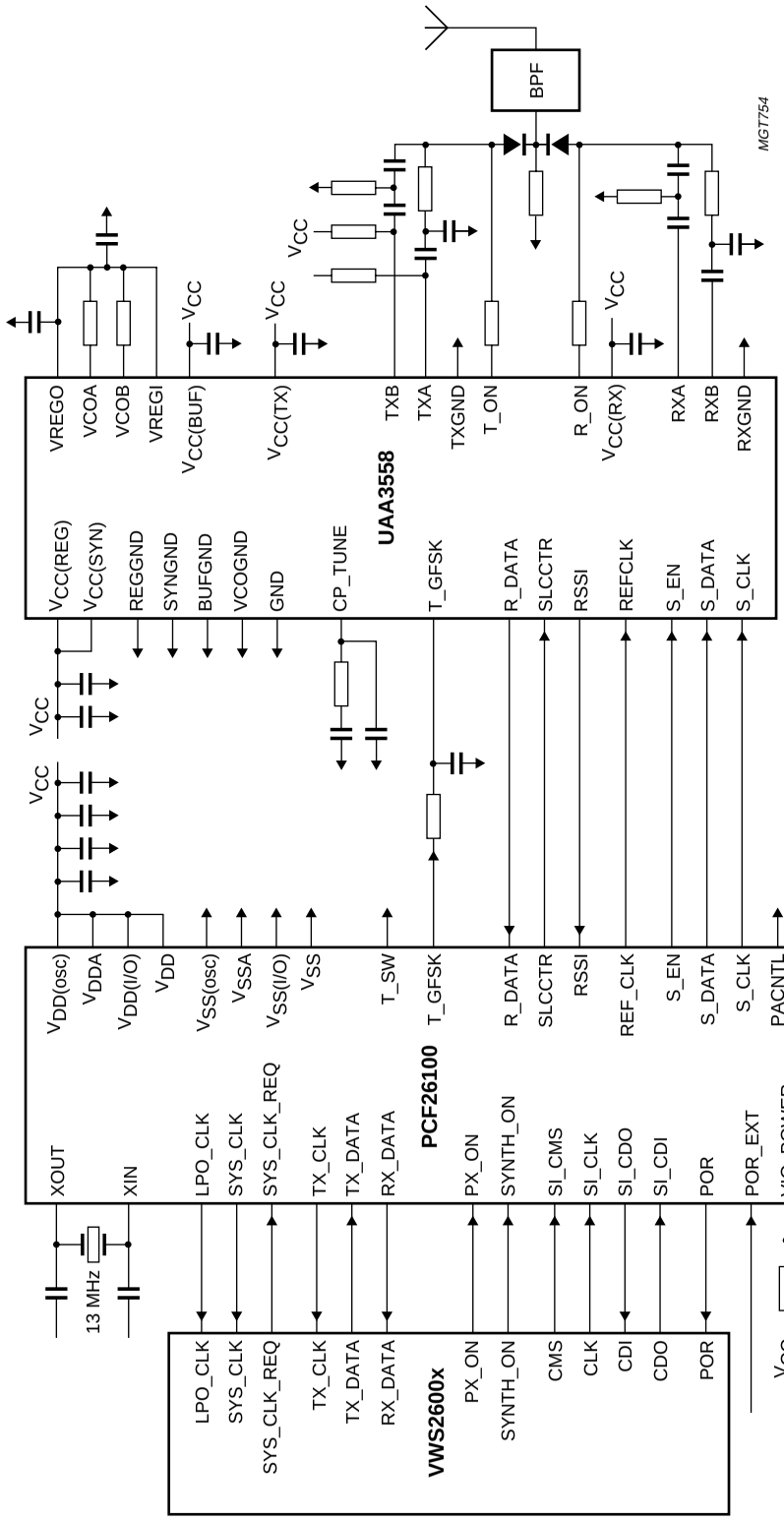
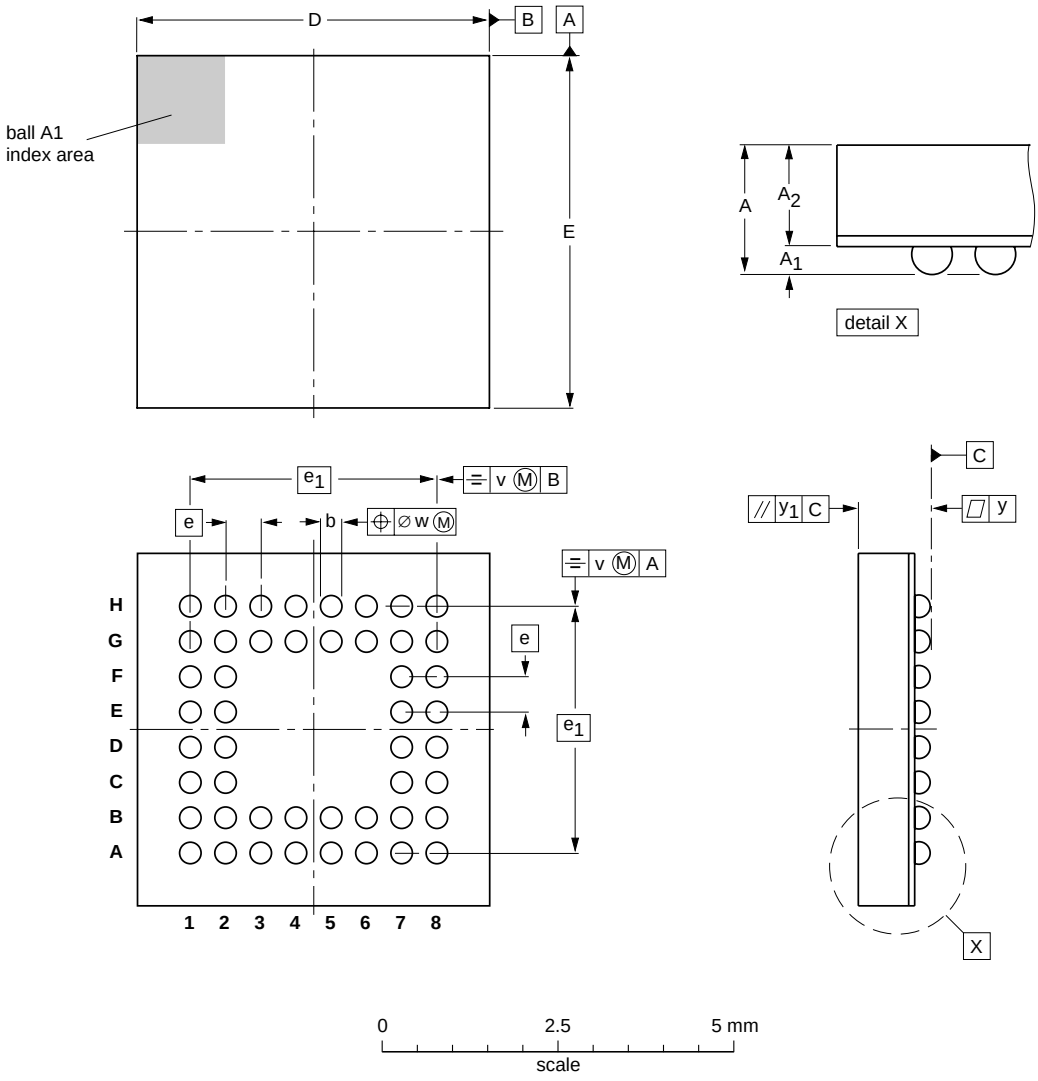


Fig.6 Application diagram VWS2600x.

12 PACKAGE OUTLINE

TFBGA48: plastic thin fine-pitch ball grid array package; 48 balls; body 5 x 5 x 0.8 mm **SOT641-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	E	e	e_1	v	w	y	y_1
mm	1.12	0.28 0.16	0.84 0.76	0.37 0.27	5.1 4.9	5.1 4.9	0.5	3.5	0.15	0.1	0.12	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT641-1		MO-211				00-10-10

13 SOLDERING

13.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

13.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

13.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

13.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

13.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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