PCAL6534

Ultra low-voltage translating 34-bit Fm+ I²C-bus/SMBus I/O expander with Agile I/O features, interrupt output and reset

Rev. 1 — 11 January 2019 Product data sheet

1. General description

The PCAL6534 is a 34-bit general purpose I/O expander that provides remote I/O expansion for most microcontroller families via the Fast-mode Plus (Fm+) I²C-bus interface. The ultra low-voltage interface allows for direct connection to a microcontroller operating down to 0.8 V.

NXP I/O expanders provide a simple solution when additional I/Os are needed while keeping interconnections to a minimum, for example, in battery-powered mobile applications for interfacing to sensors, push buttons, keypad, etc. In addition to providing a flexible set of GPIOs, it simplifies interconnection of a processor running at one voltage level down to 0.8 V to I/O devices operating at a different voltage level 1.65 V to 5.5 V. The PCAL6534 has built-in level shifting feature that makes these devices extremely flexible in mixed power supply systems where communication between incompatible I/O voltages is required, allowing seamless communications with next-generation low voltage microprocessors and microcontrollers on the interface side (SDA/SCL) and peripherals at a higher voltage on the port side.

There are two supply voltages for PCAL6534: $V_{DD(I2C\text{-}bus)}$ and $V_{DD(P)}$. $V_{DD(I2C\text{-}bus)}$ provides the supply voltage for the interface at the master side (for example, a microcontroller) and the $V_{DD(P)}$ provides the supply for core circuits and Port P. The bidirectional voltage level translation in the PCAL6534 is provided through $V_{DD(I2C\text{-}bus)}$. $V_{DD(I2C\text{-}bus)}$ should be connected to the V_{DD} of the external SCL/SDA lines. This indicates the V_{DD} level of the I²C-bus to the PCAL6534, while the voltage level on Port P of the PCAL6534 is determined by the $V_{DD(P)}$.

The PCAL6534 fully meets the Fm+ I²C-bus specification at speeds to 1 MHz and implements Agile I/O, which are additional features specifically designed to enhance the I/O. These additional features are: programmable output drive strength, latchable inputs, programmable pull-up/pull-down resistors, maskable interrupt, interrupt status register, programmable open-drain or push-pull outputs.

Additional Agile I/O Plus features include I²C software reset and Device ID. Interrupts can be specified by level or edge, and can be cleared individually without disturbing the other interrupt events. Also, switch debounce hardware is implemented.

At power-on, the I/Os are configured as inputs. However, the system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding input or output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register, saving external logic gates. Programmable pull-up and pull-down resistors eliminate the need for discrete components.

The power-on reset puts the registers in their default state and initializes the I²C-bus/SMBus state machine. The $\overline{\text{RESET}}$ pin causes the same reset/initialization to occur without depowering the part. The system master can also accomplish a reset via an I²C command and initialize all registers to their default state.

The PCAL6534 open-drain interrupt ($\overline{\text{INT}}$) output is activated when any input state differs from its corresponding Input Port register state. As well, the $\overline{\text{INT}}$ output can be specified to activate on input pin edges. There are a large number of interrupt mask functions available to maximize flexibility.

$\overline{\text{INT}}$ can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without communication via the I²C-bus. Thus, the PCAL6534 can remain a simple slave device. The input latch feature holds or latches the input pin state and keeps the logic values that created the interrupt until the master can service the interrupt. This minimizes the host's interrupt service response for fast moving inputs.

The device Port P outputs have 25 mA sink capabilities for directly driving LEDs while consuming low device current.

One hardware pin (ADDR) can be used to program and vary the fixed I²C-bus address and allow up to four devices to share the same I²C-bus or SMBus.

2. Features and benefits

- I²C-bus to parallel port expander
- 1 MHz Fast-mode Plus I²C-bus
- Operating power supply voltage range of 0.8 V to 3.6 V on the I²C-bus side
- Allows bidirectional voltage-level translation and GPIO expansion between 0.8 V to 3.6 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V, 5.5 V Port P
- Low standby current consumption: 2.0 μA typical at 3.3 V $V_{DD(P)}$
- Schmitt trigger action allows slow input transition and better switching noise immunity at the SCL and SDA inputs
  - V_{hys} = 0.05 V (typical) at 0.8 V
  - V_{hys} = 0.18 V (typical) at 1.8 V
  - V_{hys} = 0.33 V (typical) at 3.3 V
- 5.5 V tolerant I/O ports and 3.6 V tolerant I²C-bus pins
- Active LOW reset input ($\overline{\text{RESET}}$)
- Open-drain active LOW interrupt output ($\overline{\text{INT}}$)
- Internal power-on reset
- Noise filter on SCL/SDA inputs
- Latched outputs with 25 mA drive maximum capability for directly driving LEDs
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD protection exceeds JESD 22
  - 2000 V Human-Body Model (A114-A)
  - 1000 V Charged-Device Model (C101)
- Packages offered: VFBGA42

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2.1 Agile I/O features

- Output port configuration: bank selectable or pin selectable push-pull or open-drain output stages
- Interrupt status: read-only register identifies the source of an interrupt
- Bit-wise I/O programming features:
  - Output drive strength: four programmable drive strengths to reduce rise and fall times in low-capacitance applications
  - Input latch: Input Port register values changes are kept until the Input Port register is read
  - Pull-up/pull-down enable: floating input or pull-up/pull-down resistor enable
  - Pull-up/pull-down selection: 100 kΩ pull-up/pull-down resistor selection
  - Interrupt mask: mask prevents the generation of the interrupt when input changes state to prevent spurious interrupts

2.2 Additional Agile I/O Plus features

- Interrupt edge specification on a bit-by-bit basis
- Interrupt individual clear without disturbing other events
- Read all interrupt events without clear
- Switch debounce hardware
- General call software reset
- I²C software Device ID function

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3. Ordering information

Table 1. Ordering information

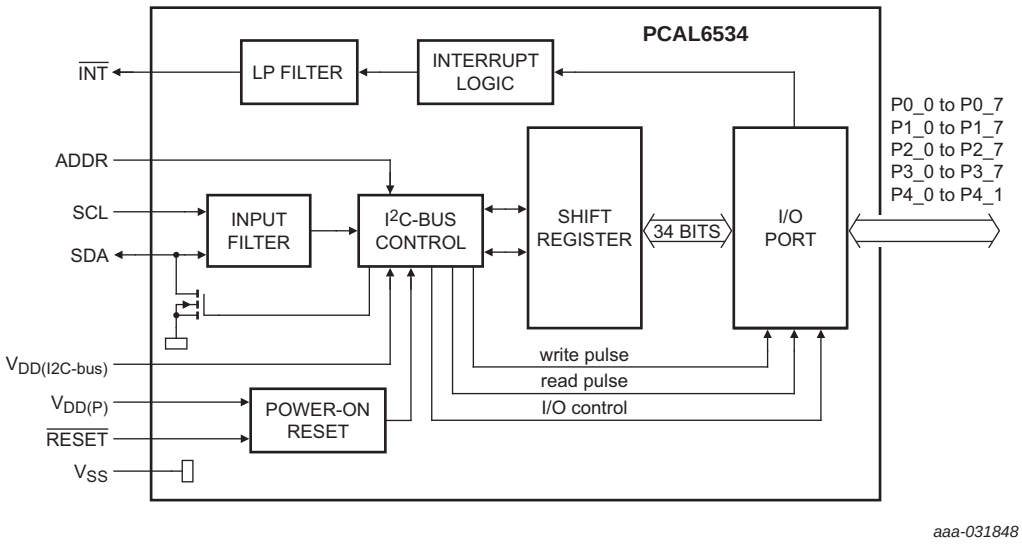
Type number	Topside marking	Package		
		Name	Description	Version
PCAL6534EV	534	VFBGA42	plastic very fine-pitch ball grid array package, body 2.6 x 3.0 mm	SOT1963-1

3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCAL6534EV	PCAL6534EVJ	VFBGA42	REEL 13" Q1/T1 NDP	5000	T_{amb} = –40 °C to +85 °C

4. Block diagram



All I/Os are set to high impedance inputs at reset.

Fig 1. Block diagram (positive logic)

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5. Pinning information

5.1 Pinning

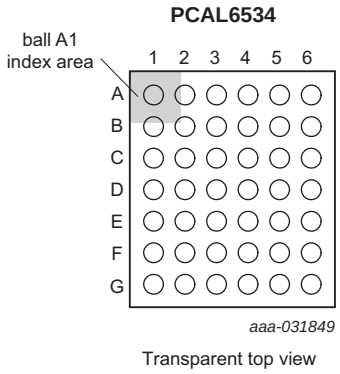


Fig 2. Pin configuration for VFBGA42

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5.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
SCL	A3	I	Serial clock line. Connect to $V_{DD(I2C\text{-}bus)}$ through a pull-up resistor.
SDA	A2	I/O	Serial data line. Connect to $V_{DD(I2C\text{-}bus)}$ through a pull-up resistor.
$V_{DD(I2C\text{-}bus)}$	A1	power supply	Supply voltage of I²C-bus. Connect directly to the V_{DD} of the external I²C-bus master. Provides voltage-level translation.
$\overline{INT}$	B1	O	Interrupt output. Connect to $V_{DD(I2C\text{-}bus)}$ or $V_{DD(P)}$ through a pull-up resistor.
P0_0[1]	C1	I/O	Port 0 input/output 0.
P0_1[1]	B2	I/O	Port 0 input/output 1.
P0_2[1]	B3	I/O	Port 0 input/output 2.
P0_3[1]	D1	I/O	Port 0 input/output 3.
P0_4[1]	C2	I/O	Port 0 input/output 4.
P0_5[1]	C3	I/O	Port 0 input/output 5.
P0_6[1]	E1	I/O	Port 0 input/output 6.
P0_7[1]	D2	I/O	Port 0 input/output 7.
P1_0[2]	D3	I/O	Port 1 input/output 0.
P1_1[2]	F1	I/O	Port 1 input/output 1.
P1_2[2]	E2	I/O	Port 1 input/output 2.
P1_3[2]	G1	I/O	Port 1 input/output 3.
P1_4[2]	G2	I/O	Port 1 input/output 4.
P1_5[2]	F2	I/O	Port 1 input/output 5.
P1_6[2]	G3	I/O	Port 1 input/output 6.
P1_7[2]	F3	I/O	Port 1 input/output 7.
P2_0[3]	E3	I/O	Port 2 input/output 0.
P2_1[3]	F4	I/O	Port 2 input/output 1.
P2_2[3]	G4	I/O	Port 2 input/output 2.
P2_3[3]	G5	I/O	Port 2 input/output 3.
P2_4[3]	G6	I/O	Port 2 input/output 4.
P2_5[3]	F6	I/O	Port 2 input/output 5.
P2_6[3]	F5	I/O	Port 2 input/output 6.
P2_7[3]	E5	I/O	Port 2 input/output 7.
P3_0[4]	E6	I/O	Port 3 input/output 0.
P3_1[4]	E4	I/O	Port 3 input/output 1.
P3_2[4]	D5	I/O	Port 3 input/output 2.
P3_3[4]	D6	I/O	Port 3 input/output 3.
P3_4[4]	D4	I/O	Port 3 input/output 4.
P3_5[4]	C5	I/O	Port 3 input/output 5.
P3_6[4]	C6	I/O	Port 3 input/output 6.
P3_7[4]	C4	I/O	Port 3 input/output 7.
P4_0[5]	B5	I/O	Port 4 input/output 0.
P4_1[5]	B4	I/O	Port 4 input/output 1.
ADDR	A4	I	Address input. Connect directly to $V_{DD(I2C\text{-}bus)}$, ground, SCL or SDA.

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Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
V_{SS}	B6	ground	Supply ground.
$V_{DD(P)}$	A6	power supply	Supply voltage of PCAL6534 for Port P. 0.22 uF bypass capacitor required on this supply located as close to package as practical.
$\overline{RESET}$	A5	I	Active LOW reset input. Connect to $V_{DD(I2C\text{-}bus)}$ through a pull-up resistor if no active connection is used.

[1] Pins P0_0 to P0_7 correspond to bits P0.0 to P0.7. At power-on, all I/Os are configured as inputs.

[2] Pins P1_0 to P1_7 correspond to bits P1.0 to P1.7. At power-on, all I/Os are configured as inputs.

[3] Pins P2_0 to P2_7 correspond to bits P2.0 to P2.7. At power-on, all I/Os are configured as inputs.

[4] Pins P3_0 to P3_7 correspond to bits P3.0 to P3.7. At power-on, all I/Os are configured as inputs.

[5] Pins P4_0 to P4_1 correspond to bits P4.0 to P4.1. At power-on, all I/Os are configured as inputs.

6. Functional description

Refer to Figure 1 “Block diagram (positive logic)”.

6.1 Device address

Following a START condition, the bus master must send the target slave address followed by a read (R/$\overline{W}$ = 1) or write (R/$\overline{W}$ = 0) operation bit. The slave address of the PCAL6534 is shown in Figure 3. Slave address pin ADDR chooses one of four slave addresses. Table 4 shows all four slave addresses by connecting the ADDR pin to SCL, SDA, V_{SS}, or V_{DD}.

Table 4. PCAL6534 address map

ADDR	Device family high-order address bits					Variable portion of address		Address
	A6	A5	A4	A3	A2	A1	A0	
SCL	0	1	0	0	0	0	0	40h
SDA	0	1	0	0	0	0	1	42h
V_{SS}	0	1	0	0	0	1	0	44h
V_{DD}	0	1	0	0	0	1	1	46h

The last bit of the first byte defines the reading from or writing to the PCAL6534. When set to logic 1 a read is selected, while logic 0 selects a write operation.

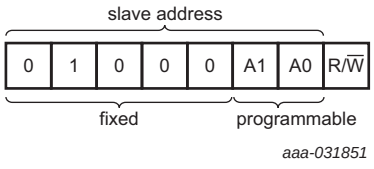


Fig 3. PCAL6534 device address

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6.2 Interface definition

Table 5. Interface definition

Byte	Bit							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I²C-bus slave address	L	H	L	L	L	A1	A0	R/$\overline{W}$
I/O data bus	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
							P4.1	P4.0

6.3 Software Reset Call, and Device ID addresses

Two other different addresses can be sent to the device.

- General Call address: allows to reset the device through the I²C-bus upon reception of the right I²C-bus sequence. See Section 6.3.1 “Software Reset” for more information.
- Device ID address: allows to read ID information from the device (manufacturer, part identification, revision). See Section 6.3.2 “Device ID (PCAL6534 ID field)” for more information.

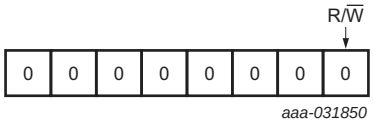


Fig 4. General call address

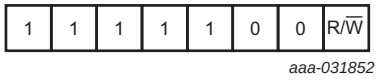


Fig 5. Device ID address

6.3.1 Software Reset

The Software Reset Call allows all the devices in the I²C-bus to be reset to the power-up state value through a specific formatted I²C-bus command. To be performed correctly, it implies that the I²C-bus is functional and that there is no device hanging the bus.

The Software Reset sequence is defined as following:

1. A START command is sent by the I²C-bus master.
2. The reserved General Call I²C-bus address ‘0000 000’ with the R/$\overline{W}$ bit set to 0 (write) is sent by the I²C-bus master.
3. The device acknowledges after seeing the General Call address ‘0000 0000’ (00h) only. If the R/$\overline{W}$ bit is set to 1 (read), no acknowledge is returned to the I²C-bus master.
4. Once the General Call address has been sent and acknowledged, the master sends 1 byte. The value of the byte must be equal to 06h.
   a. The device acknowledges this value only. If the byte is not equal to 06h, the device does not acknowledge it.

   If more than 1 byte of data is sent, the device does not acknowledge any more.

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5. Once the right byte has been sent and correctly acknowledged, the master sends a STOP command to end the Software Reset sequence: the device then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time. If the master sends a Repeated START instead, no reset is performed.

The I²C-bus master must interpret a non-acknowledge from the device (at any time) as a 'Software Reset Abort'. The device does not initiate a reset of its registers.

The unique sequence that initiates a Software Reset is described in Figure 6.

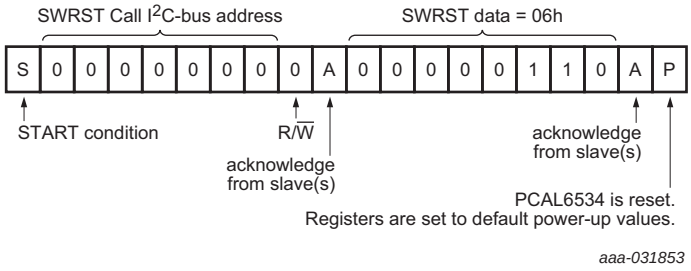


Fig 6. Software Reset sequence

6.3.2 Device ID (PCAL6534 ID field)

The Device ID field is a 3-byte read-only (24 bits) word giving the following information:

- 12 bits with the manufacturer name, unique per manufacturer (for example, NXP).
- 9 bits with the part identification, assigned by manufacturer.
- 3 bits with the die revision, assigned by manufacturer (for example, Rev X).

The Device ID is read-only, hardwired in the device and can be accessed as follows:

1. START command
2. The master sends the Reserved Device ID I²C-bus address followed by the R/$\overline{W}$ bit set to 0 (write): '1111 1000'.
3. The master sends the I²C-bus slave address of the slave device it needs to identify. The LSB is a 'Don't care' value. Only one device must acknowledge this byte (the one that has the I²C-bus slave address).
4. The master sends a Re-START command.

   Remark: A STOP command followed by a START command will reset the slave state machine and the Device ID read cannot be performed. Also, a STOP command or a Re-START command followed by an access to another slave device will reset the slave state machine and the Device ID Read cannot be performed.
5. The master sends the Reserved Device ID I²C-bus address followed by the R/$\overline{W}$ bit set to 1 (read): '1111 1001'.
6. The Device ID Read can be done, starting with the 12 manufacturer bits (first byte + 4 MSB of the second byte), followed by the 9 part identification bits (4 LSBs of the second byte + 5 MSBs of the third byte), and then the 3 die revision bits (3 LSBs of the third byte).
7. The master ends the reading sequence by NACKing the last byte, thus resetting the slave device state machine and allowing the master to send the STOP command.

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Remark: The reading of the Device ID can be stopped anytime by sending a NACK command.

If the master continues to ACK the bytes after the third byte, the slave rolls back to the first byte and keeps sending the Device ID sequence until a NACK has been detected.

For the PCAL6534, the Device ID is as shown in Figure 7.

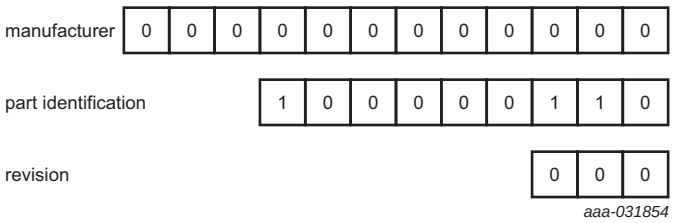
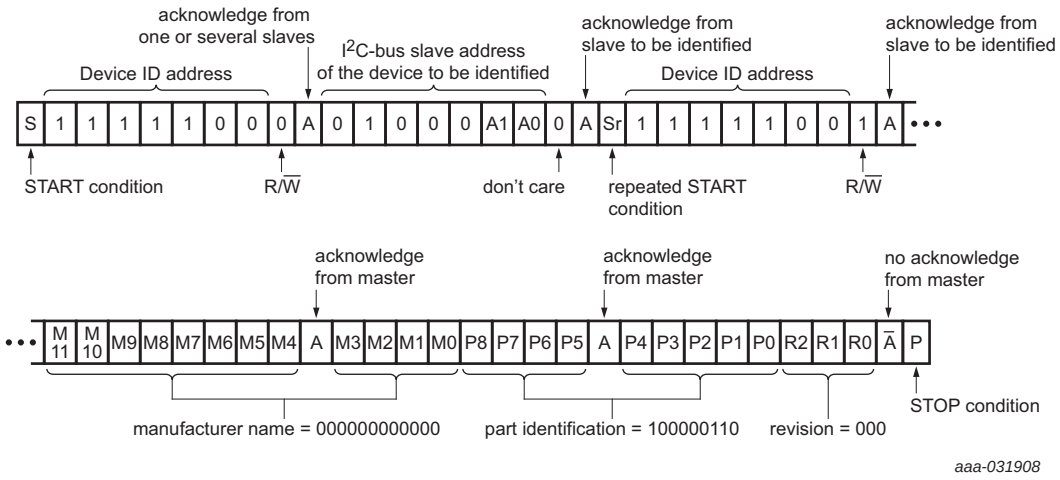


Fig 7. PCAL6534 Device ID field



If more than 3 bytes are read, the slave device loops back to the first byte (manufacturer byte) and keeps sending data until the master generates a 'no acknowledge'.

Fig 8. Device ID field reading

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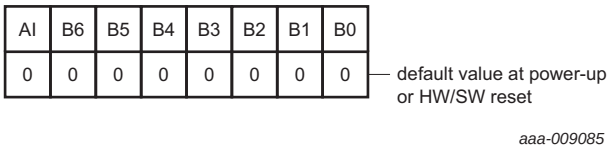
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6.4 Pointer register and command byte

Following the successful acknowledgement of the slave address byte, the bus master sends a command byte, which is write only and stored in the pointer register in the PCAL6534. The lowest 7 bits (B[6:0] in Table 6) are used as a pointer to determine which register is accessed and the highest bit is used as Auto-Increment (AI) as shown in Figure 9. At power-up, hardware or software reset, the pointer register defaults to 00h, with the AI bit set to '0' and the lowest seven bits set to '000 0000'.

When the Auto-Increment bit is set (AI = 1), the seven low-order bits of the pointer register are automatically incremented after a read or write until a STOP condition is encountered. This allows the user to program the registers sequentially without modifying the pointer register. The contents of these bits will roll over to '000 0000' after the last register (address = 6Fh) is accessed. Unimplemented register addresses (reserved registers) are skipped. If more than 82 bytes are written, the address will loop back to the register which is indicated by the seven low-order bits in the pointer register, and previously-written data will be overwritten. A STOP condition will keep the pointer register value in the last read or write location.

When the Auto-Increment bit is cleared (AI = 0), the content of pointer register bits are automatically incremented after a read or write for 5-register group which allows the user to program each of the 5-register group sequentially. If more than 5 bytes of data are read or written when AI is 0, previous data in the selected registers will be overwritten. For example: if input port 3 is read first, the next 2nd byte will be input port 4, and next 3nd byte will be input port 0, there is no limit on the number of data bytes for this read operation. There are two special 9-register groups: output drive strength (30h~38h) and interrupt edge (54h~5Ch) registers will allow user to program each of the 9-register group sequentially. There is one special 3-register group: switch debounce (6Dh ~ 6Fh) registers will allow user to program each of the 3-register group sequentially. Only Output port configuration register location (53h) remains in the same location after a successive read or write.



AI = Auto-Increment

Fig 9. Pointer register bits

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Table 6. Command byte

Pointer register bits							Command byte (hexadecimal)	Register	Protocol	Power-up default
B6	B5	B4	B3	B2	B1	B0				
0	0	0	0	0	0	0	00h	Input port 0	read byte	xxxx xxxx[1]
0	0	0	0	0	0	1	01h	Input port 1	read byte	xxxx xxxx[1]
0	0	0	0	0	1	0	02h	Input port 2	read byte	xxxx xxxx[1]
0	0	0	0	0	1	1	03h	Input port 3	read byte	xxxx xxxx[1]
0	0	0	0	1	0	0	04h	Input port 4	read byte	0000 00xx[1]
0	0	0	0	1	0	1	05h	Output port 0	read/write byte	1111 1111
0	0	0	0	1	1	0	06h	Output port 1	read/write byte	1111 1111
0	0	0	0	1	1	1	07h	Output port 2	read/write byte	1111 1111
0	0	0	1	0	0	0	08h	Output port 3	read/write byte	1111 1111
0	0	0	1	0	0	1	09h	Output port 4	read/write byte	0000 0011
0	0	0	1	0	1	0	0Ah	Polarity Inversion port 0	read/write byte	0000 0000
0	0	0	1	0	1	1	0Bh	Polarity Inversion port 1	read/write byte	0000 0000
0	0	0	1	1	0	0	0Ch	Polarity Inversion port 2	read/write byte	0000 0000
0	0	0	1	1	0	1	0Dh	Polarity Inversion port 3	read/write byte	0000 0000
0	0	0	1	1	1	0	0Eh	Polarity Inversion port 4	read/write byte	0000 0000
0	0	0	1	1	1	1	0Fh	Configuration port 0	read/write byte	1111 1111
0	0	1	0	0	0	0	10h	Configuration port 1	read/write byte	1111 1111
0	0	1	0	0	0	1	11h	Configuration port 2	read/write byte	1111 1111
0	0	1	0	0	1	0	12h	Configuration port 3	read/write byte	1111 1111
0	0	1	0	0	1	1	13h	Configuration port 4	read/write byte	0000 0011
-	-	-	-	-	-	-	14h to 2Fh	reserved[3]	reserved	reserved
0	1	1	0	0	0	0	30h	Output drive strength register port 0A	read/write byte	1111 1111
0	1	1	0	0	0	1	31h	Output drive strength register port 0B	read/write byte	1111 1111
0	1	1	0	0	1	0	32h	Output drive strength register port 1A	read/write byte	1111 1111
0	1	1	0	0	1	1	33h	Output drive strength register port 1B	read/write byte	1111 1111
0	1	1	0	1	0	0	34h	Output drive strength register port 2A	read/write byte	1111 1111
0	1	1	0	1	0	1	35h	Output drive strength register port 2B	read/write byte	1111 1111
0	1	1	0	1	1	0	36h	Output drive strength register port 3A	read/write byte	1111 1111
0	1	1	0	1	1	1	37h	Output drive strength register port 3B	read/write byte	1111 1111
0	1	1	1	0	0	0	38h	Output drive strength register port 4A	read/write byte	0000 1111
0	1	1	1	0	0	1	39h	reserved[3]	reserved	reserved
0	1	1	1	0	1	0	3Ah	Input latch register port 0	read/write byte	0000 0000
0	1	1	1	0	1	1	3Bh	Input latch register port 1	read/write byte	0000 0000
0	1	1	1	1	0	0	3Ch	Input latch register port 2	read/write byte	0000 0000
0	1	1	1	1	0	1	3Dh	Input latch register port 3	read/write byte	0000 0000
0	1	1	1	1	1	0	3Eh	Input latch register port 4	read/write byte	0000 0000
0	1	1	1	1	1	1	3Fh	Pull-up/pull-down enable register port 0	read/write byte	0000 0000
1	0	0	0	0	0	0	40h	Pull-up/pull-down enable register port 1	read/write byte	0000 0000

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Table 6. Command byte *...continued*

Pointer register bits							Command byte (hexadecimal)	Register	Protocol	Power-up default
B6	B5	B4	B3	B2	B1	B0				
1	0	0	0	0	0	1	41h	Pull-up/pull-down enable register port 2	read/write byte	0000 0000
1	0	0	0	0	1	0	42h	Pull-up/pull-down enable register port 3	read/write byte	0000 0000
1	0	0	0	0	1	1	43h	Pull-up/pull-down enable register port 4	read/write byte	0000 0000
1	0	0	0	1	0	0	44h	Pull-up/pull-down selection register port 0	read/write byte	1111 1111
1	0	0	0	1	0	1	45h	Pull-up/pull-down selection register port 1	read/write byte	1111 1111
1	0	0	0	1	1	0	46h	Pull-up/pull-down selection register port 2	read/write byte	1111 1111
1	0	0	0	1	1	1	47h	Pull-up/pull-down selection register port 3	read/write byte	1111 1111
1	0	0	1	0	0	0	48h	Pull-up/pull-down selection register port 4	read/write byte	0000 0011
1	0	0	1	0	0	1	49h	Interrupt mask register port 0	read/write byte	1111 1111
1	0	0	1	0	1	0	4Ah	Interrupt mask register port 1	read/write byte	1111 1111
1	0	0	1	0	1	1	4Bh	Interrupt mask register port 2	read/write byte	1111 1111
1	0	0	1	1	0	0	4Ch	Interrupt mask register port 3	read/write byte	1111 1111
1	0	0	1	1	0	1	4Dh	Interrupt mask register port 4	read/write byte	0000 0011
1	0	0	1	1	1	0	4Eh	Interrupt status register port 0	read byte	0000 0000
1	0	0	1	1	1	1	4Fh	Interrupt status register port 1	read byte	0000 0000
1	0	1	0	0	0	0	50h	Interrupt status register port 2	read byte	0000 0000
1	0	1	0	0	0	1	51h	Interrupt status register port 3	read byte	0000 0000
1	0	1	0	0	1	0	52h	Interrupt status register port 4	read byte	0000 0000
1	0	1	0	0	1	1	53h[2]	Output port configuration register	read/write byte	0000 0000
1	0	1	0	1	0	0	54h	Interrupt edge register port 0A	read/write byte	0000 0000
1	0	1	0	1	0	1	55h	Interrupt edge register port 0B	read/write byte	0000 0000
1	0	1	0	1	1	0	56h	Interrupt edge register port 1A	read/write byte	0000 0000
1	0	1	0	1	1	1	57h	Interrupt edge register port 1B	read/write byte	0000 0000
1	0	1	1	0	0	0	58h	Interrupt edge register port 2A	read/write byte	0000 0000
1	0	1	1	0	0	1	59h	Interrupt edge register port 2B	read/write byte	0000 0000
1	0	1	1	0	1	0	5Ah	Interrupt edge register port 3A	read/write byte	0000 0000
1	0	1	1	0	1	1	5Bh	Interrupt edge register port 3B	read/write byte	0000 0000
1	0	1	1	1	0	0	5Ch	Interrupt edge register port 4A	read/write byte	0000 0000
1	0	1	1	1	0	1	5Dh	reserved[3]	reserved	reserved
1	0	1	1	1	1	0	5Eh	Interrupt clear register port 0	write byte	0000 0000
1	0	1	1	1	1	1	5Fh	Interrupt clear register port 1	write byte	0000 0000
1	1	0	0	0	0	0	60h	Interrupt clear register port 2	write byte	0000 0000
1	1	0	0	0	0	1	61h	Interrupt clear register port 3	write byte	0000 0000

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Table 6. Command byte *...continued*

Pointer register bits							Command byte (hexadecimal)	Register	Protocol	Power-up default
B6	B5	B4	B3	B2	B1	B0				
1	1	0	0	0	1	0	62h	Interrupt clear register port 4	write byte	0000 0000
1	1	0	0	0	1	1	63h	Input status port 0	read byte	xxxx xxxx[1]
1	1	0	0	1	0	0	64h	Input status port 1	read byte	xxxx xxxx[1]
1	1	0	0	1	0	1	65h	Input status port 2	read byte	xxxx xxxx[1]
1	1	0	0	1	1	0	66h	Input status port 3	read byte	xxxx xxxx[1]
1	1	0	0	1	1	1	67h	Input status port 4	read byte	0000 00xx[1]
1	1	0	1	0	0	0	68h	Individual pin output port 0 configuration register	read/write byte	0000 0000
1	1	0	1	0	0	1	69h	Individual pin output port 1 configuration register	read/write byte	0000 0000
1	1	0	1	0	1	0	6Ah	Individual pin output port 2 configuration register	read/write byte	0000 0000
1	1	0	1	0	1	1	6Bh	Individual pin output port 3 configuration register	read/write byte	0000 0000
1	1	0	1	1	0	0	6Ch	Individual pin output port 4 configuration register	read/write byte	0000 0000
1	1	0	1	1	0	1	6Dh	Switch debounce enable 0	read/write byte	0000 0000
1	1	0	1	1	1	0	6Eh	Switch debounce enable 1	read/write byte	0000 0000
1	1	0	1	1	1	1	6Fh	Switch debounce count	read/write byte	0000 0000
-	-	-	-	-	-	-	70h to 7Fh	reserved[3]	reserved	reserved

[1] Undefined.

[2] Successive read and write accesses to remain at this register address.

[3] These registers marked “reserved” should not be written, and the master will not be acknowledged when accessed.

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6.5 Register descriptions

6.5.1 Input port registers (00h, 01h, 02h, 03h, 04h)

The Input port registers (registers 00h, 01h, 02h, 03h, 04h) reflect the incoming logic levels of the pins. The Input port registers are read only; writes to these registers have no effect and the transaction will be acknowledged (ACK). The default value 'X' is determined by the externally applied logic level. If a pin is configured as an output (registers 05h, 06h, 07h, 08h, 09h), the port value is equal to the actual voltage level on that pin. If the output is configured as open-drain (register 53h and registers 68h, 69h, 6Ah, 6Bh, 6Ch), the input port value is forced to 0. An Input port register group read operation is performed as described in Section 7.2.

After reading input port registers, all interrupts will be cleared.

Table 7. Input port 0 register (address 00h)

Bit	7	6	5	4	3	2	1	0
Symbol	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X

Table 8. Input port 1 register (address 01h)

Bit	7	6	5	4	3	2	1	0
Symbol	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

Table 9. Input port 2 register (address 02h)

Bit	7	6	5	4	3	2	1	0
Symbol	I2.7	I2.6	I2.5	I2.4	I2.3	I2.2	I2.1	I2.0
Default	X	X	X	X	X	X	X	X

Table 10. Input port 3 register (address 03h)

Bit	7	6	5	4	3	2	1	0
Symbol	I3.7	I3.6	I3.5	I3.4	I3.3	I3.2	I3.1	I3.0
Default	X	X	X	X	X	X	X	X

Table 11. Input port 4 register (address 04h)

Bit	7	6	5	4	3	2	1	0
Symbol	X	X	X	X	X	X	I4.1	I4.0
Default	X	X	X	X	X	X	X	X

6.5.2 Output port registers (05h, 06h, 07h, 08h, 09h)

The Output port registers (registers 05h, 06h, 07h, 08h, 09h) show the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in these registers have no effect on pins defined as inputs. In turn, reads from these registers reflect the value that was written to these registers, **not** the actual pin value. A register group write is described in Section 7.1 and a register group read is described in Section 7.2.

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Table 12. Output port 0 register (address 05h)

Bit	7	6	5	4	3	2	1	0
Symbol	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1

Table 13. Output port 1 register (address 06h)

Bit	7	6	5	4	3	2	1	0
Symbol	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

Table 14. Output port 2 register (address 07h)

Bit	7	6	5	4	3	2	1	0
Symbol	O2.7	O2.6	O2.5	O2.4	O2.3	O2.2	O2.1	O2.0
Default	1	1	1	1	1	1	1	1

Table 15. Output port 3 register (address 08h)

Bit	7	6	5	4	3	2	1	0
Symbol	O3.7	O3.6	O3.5	O3.4	O3.3	O3.2	O3.1	O3.0
Default	1	1	1	1	1	1	1	1

Table 16. Output port 4 register (address 09h)

Bit	7	6	5	4	3	2	1	0
Symbol	X	X	X	X	X	X	O4.1	O4.2
Default	X	X	X	X	X	X	1	1

6.5.3 Polarity inversion registers (0Ah, 0Bh, 0Ch, 0Dh, 0Eh)

The Polarity inversion registers (registers 0Ah, 0Bh, 0Ch, 0Dh, 0Eh) allow polarity inversion of pins defined as inputs by the Configuration register. If a bit in these registers is set (written with '1'), the corresponding port pin's polarity is inverted in the input register. If a bit in this register is cleared (written with a '0'), the corresponding port pin's polarity is retained. A register group write is described in Section 7.1 and a register group read is described in Section 7.2.

Table 17. Polarity inversion port 0 register (address 0Ah)

Bit	7	6	5	4	3	2	1	0
Symbol	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0

Table 18. Polarity inversion port 1 register (address 0Bh)

Bit	7	6	5	4	3	2	1	0
Symbol	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

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Table 19. Polarity inversion port 2 register (address 0Ch)

Bit	7	6	5	4	3	2	1	0
Symbol	N2.7	N2.6	N2.5	N2.4	N2.3	N2.2	N2.1	N2.0
Default	0	0	0	0	0	0	0	0

Table 20. Polarity inversion port 3 register (address 0Dh)

Bit	7	6	5	4	3	2	1	0
Symbol	N3.7	N3.6	N3.5	N3.4	N3.3	N3.2	N3.1	N3.0
Default	0	0	0	0	0	0	0	0

Table 21. Polarity inversion port 4 register (address 0Eh)

Bit	7	6	5	4	3	2	1	0
Symbol	X	X	X	X	X	X	N4.1	N4.0
Default	X	X	X	X	X	X	0	0

6.5.4 Configuration registers (0Fh, 10h, 11h, 12h, 13h)

The Configuration registers (registers 0Fh, 10h, 11h, 12h, 13h) configure the direction of the I/O pins. If a bit in these registers is set to 1, the corresponding port pin is enabled as a high-impedance input. If a bit in these registers is cleared to 0, the corresponding port pin is enabled as an output. A register group write is described in Section 7.1 and a register group read is described in Section 7.2.

Table 22. Configuration port 0 register (address 0Fh)

Bit	7	6	5	4	3	2	1	0
Symbol	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1

Table 23. Configuration port 1 register (address 10h)

Bit	7	6	5	4	3	2	1	0
Symbol	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

Table 24. Configuration port 2 register (address 11h)

Bit	7	6	5	4	3	2	1	0
Symbol	C2.7	C2.6	C2.5	C2.4	C2.3	C2.2	C2.1	C2.0
Default	1	1	1	1	1	1	1	1

Table 25. Configuration port 3 register (address 12h)

Bit	7	6	5	4	3	2	1	0
Symbol	C3.7	C3.6	C3.5	C3.4	C3.3	C3.2	C3.1	C3.0
Default	1	1	1	1	1	1	1	1

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Table 26. Configuration port 4 register (address 13h)

Bit	7	6	5	4	3	2	1	0
Symbol	X	X	X	X	X	X	C4.1	C4.0
Default	X	X	X	X	X	X	1	1

6.5.5 Output drive strength registers (30h, 31h, 32h, 33h, 34h, 35h, 36h, 37h, 38h)

The Output drive strength registers control the output drive level of the GPIO. Each GPIO can be configured independently to a certain output current level by two register control bits. For example Port 0.7 is controlled by register 31h CC0.7 (bits [7:6]), Port 0.6 is controlled by register 31h CC0.6 (bits [5:4]). The output drive level of the GPIO is programmed 00b = 0.25×, 01b = 0.5×, 10b = 0.75× or 11b = 1× of the drive capability of the I/O. See Section 8.1 “Output drive strength control” for more details. A register group write operation is described in Section 7.1. A register group read operation is described in Section 7.2.

Table 27. Current control port 0A register (address 30h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC0.3		CC0.2		CC0.1		CC0.0	
Default	1	1	1	1	1	1	1	1

Table 28. Current control port 0B register (address 31h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC0.7		CC0.6		CC0.5		CC0.4	
Default	1	1	1	1	1	1	1	1

Table 29. Current control port 1A register (address 32h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC1.3		CC1.2		CC1.1		CC1.0	
Default	1	1	1	1	1	1	1	1

Table 30. Current control port 1B register (address 33h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC1.7		CC1.6		CC1.5		CC1.4	
Default	1	1	1	1	1	1	1	1

Table 31. Current control port 2A register (address 34h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC2.3		CC2.2		CC2.1		CC2.0	
Default	1	1	1	1	1	1	1	1

Table 32. Current control port 2B register (address 35h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC2.7		CC2.6		CC2.5		CC2.4	
Default	1	1	1	1	1	1	1	1

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Table 33. Current control port 3A register (address 36h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC3.3		CC3.2		CC3.1		CC3.0	
Default	1	1	1	1	1	1	1	1

Table 34. Current control port 3B register (address 37h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC3.7		CC3.6		CC3.5		CC3.4	
Default	1	1	1	1	1	1	1	1

Table 35. Current control port 4A register (address 38h)

Bit	7	6	5	4	3	2	1	0
Symbol	X	X	X	X	CC4.1		CC4.0	
Default	X	X	X	X	1	1	1	1

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6.5.6 Input latch registers (3Ah, 3Bh, 3Ch, 3Dh, 3Eh)

The input latch registers (registers 3Ah, 3Bh, 3Ch, 3Dh, 3Eh) enable and disable the input latch of the I/O pins. These registers are effective only when the pin is configured as an input port. When an input latch register bit is 0, the corresponding input pin state is not latched. A state change in the corresponding input pin generates an interrupt. A read of the input register clears the interrupt. If the input goes back to its initial logic state before the input port register is read, then the interrupt is cleared.

When an input latch register bit is 1, the corresponding input pin state is latched. A change of state of the input generates an interrupt and the input logic value is loaded into the corresponding bit of the input port register (registers 0, 1, 2, 3 and 4). A read of the input port register clears the interrupt. If the input pin returns to its initial logic state before the input port register is read, then the interrupt is not cleared and the corresponding bit of the input port register keeps the logic value that initiated the interrupt. See Figure 19.

For example, if the P0_4 input was as logic 0 and the input goes to logic 1 then back to logic 0, the input port 0 register will capture this change and an interrupt is generated (if unmasked). When the read is performed on the input port 0 register, the interrupt is cleared, assuming there were no additional input(s) that have changed, and bit 4 of the input port 0 register will read '1'. The next read of the input port register bit 4 register should now read '0'.

An interrupt remains active when a non-latched input simultaneously switches state with a latched input and then returns to its original state. A read of the input register reflects only the change of state of the latched input and also clears the interrupt. The interrupt is cleared if the input latch register changes from latched to non-latched configuration and I/O pin returns to its original state.

If the input pin is changed from latched to non-latched input, a read from the input port register reflects the current port logic level. If the input pin is changed from non-latched to latched input, the read from the input register reflects the latched logic level. A register group write operation is described in Section 7.1. A register group read operation is described in Section 7.2.

Table 36. Input latch port 0 register (address 3Ah)

Bit	7	6	5	4	3	2	1	0
Symbol	L0.7	L0.6	L0.5	L0.4	L0.3	L0.2	L0.1	L0.0
Default	0	0	0	0	0	0	0	0

Table 37. Input latch port 1 register (address 3Bh)

Bit	7	6	5	4	3	2	1	0
Symbol	L1.7	L1.6	L1.5	L1.4	L1.3	L1.2	L1.1	L1.0
Default	0	0	0	0	0	0	0	0

Table 38. Input latch port 2 register (address 3Ch)

Bit	7	6	5	4	3	2	1	0
Symbol	L2.7	L2.6	L2.5	L2.4	L2.3	L2.2	L2.1	L2.0
Default	0	0	0	0	0	0	0	0

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Table 39. Input latch port 3 register (address 3Dh)

Bit	7	6	5	4	3	2	1	0
Symbol	L3.7	L3.6	L3.5	L3.4	L3.3	L3.2	L3.1	L3.0
Default	0	0	0	0	0	0	0	0

Table 40. Input latch port 4 register (address 3Eh)

Bit	7	6	5	4	3	2	1	0
Symbol	X	X	X	X	X	X	L4.1	L4.0
Default	X	X	X	X	X	X	0	0

6.5.7 Pull-up/pull-down enable registers (3Fh, 40h, 41h, 42h, 43h)

The pull-up and pull-down enable registers allow the user to enable or disable pull-up/pull-down resistors on the I/O pins. Setting the bit to logic 1 enables the selection of pull-up/pull-down resistors. Setting the bit to logic 0 disconnects the pull-up/pull-down resistors from the I/O pins. Also, the resistors will be disconnected when the outputs are configured as open-drain outputs (see Section 6.5.11 and Section 6.5.15). Use the pull-up/pull-down registers to select either a pull-up or pull-down resistor. A register group write operation is described in Section 7.1. A register group read operation is described in Section 7.2.

Table 41. Pull-up/pull-down enable port 0 register (address 3Fh)

Bit	7	6	5	4	3	2	1	0
Symbol	PE0.7	PE0.6	PE0.5	PE0.4	PE0.3	PE0.2	PE0.1	PE0.0
Default	0	0	0	0	0	0	0	0

Table 42. Pull-up/pull-down enable port 1 register (address 40h)

Bit	7	6	5	4	3	2	1	0
Symbol	PE1.7	PE1.6	PE1.5	PE1.4	PE1.3	PE1.2	PE1.1	PE1.0
Default	0	0	0	0	0	0	0	0

Table 43. Pull-up/pull-down enable port 2 register (address 41h)

Bit	7	6	5	4	3	2	1	0
Symbol	PE2.7	PE2.6	PE2.5	PE2.4	PE2.3	PE2.2	PE2.1	PE2.0
Default	0	0	0	0	0	0	0	0

Table 44. Pull-up/pull-down enable port 3 register (address 42h)

Bit	7	6	5	4	3	2	1	0
Symbol	PE3.7	PE3.6	PE3.5	PE3.4	PE3.3	PE3.2	PE3.1	PE3.0
Default	0	0	0	0	0	0	0	0

Table 45. Pull-up/pull-down enable port 4 register (address 43h)

Bit	7	6	5	4	3	2	1	0
Symbol	X	X	X	X	X	X	PE4.1	PE4.0
Default	X	X	X	X	X	X	0	0

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6.5.8 Pull-up/pull-down selection registers (44h, 45h, 46h, 47h, 48h)

The I/O port can be configured to have pull-up or pull-down resistor by programming the pull-up/pull-down selection register. Setting a bit to logic 1 selects a 100 kΩ pull-up resistor for that I/O pin. Setting a bit to logic 0 selects a 100 kΩ pull-down resistor for that I/O pin. If the pull-up/down feature is disconnected, writing to this register will have no effect on I/O pin. Typical value is 100 kΩ with minimum of 50 kΩ and maximum of 150 kΩ. A register group write operation is described in Section 7.1. A register group read operation is described in Section 7.2.

Table 46. Pull-up/pull-down selection port 0 register (address 44h)

Bit	7	6	5	4	3	2	1	0
Symbol	PUD0.7	PUD0.6	PUD0.5	PUD0.4	PUD0.3	PUD0.2	PUD0.1	PUD0.0
Default	1	1	1	1	1	1	1	1

Table 47. Pull-up/pull-down selection port 1 register (address 45h)

Bit	7	6	5	4	3	2	1	0
Symbol	PUD1.7	PUD1.6	PUD1.5	PUD1.4	PUD1.3	PUD1.2	PUD1.1	PUD1.0
Default	1	1	1	1	1	1	1	1

Table 48. Pull-up/pull-down selection port 2 register (address 46h)

Bit	7	6	5	4	3	2	1	0
Symbol	PUD2.7	PUD2.6	PUD2.5	PUD2.4	PUD2.3	PUD2.2	PUD2.1	PUD2.0
Default	1	1	1	1	1	1	1	1

Table 49. Pull-up/pull-down selection port 3 register (address 47h)

Bit	7	6	5	4	3	2	1	0
Symbol	PUD3.7	PUD3.6	PUD3.5	PUD3.4	PUD3.3	PUD3.2	PUD3.1	PUD3.0
Default	1	1	1	1	1	1	1	1

Table 50. Pull-up/pull-down selection port 4 register (address 48h)

Bit	7	6	5	4	3	2	1	0
Symbol	X	X	X	X	X	X	PUD4.1	PUD4.0
Default	X	X	X	X	X	X	1	1

6.5.9 Interrupt mask registers (49h, 4Ah, 4Bh, 4Ch, 4Dh)

Interrupt mask registers are set to logic 1 upon power-on, disabling interrupts during system start-up. Interrupts may be enabled by setting corresponding mask bits to logic 0.

If an input changes state and the corresponding bit in the Interrupt mask register is set to 1, the interrupt is masked and the interrupt pin will not be asserted. If the corresponding bit in the Interrupt mask register is set to 0, the interrupt pin will be asserted.

When an input changes state and the resulting interrupt is masked (interrupt mask bit is 1), setting the input mask register bit to 0 will cause the interrupt pin to be asserted. If the interrupt mask bit of an input that is currently the source of an interrupt is set to 1, the interrupt pin will be de-asserted. A register group write operation is described in Section 7.1. A register group read operation is described in Section 7.2.

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Table 51. Interrupt mask port 0 register (address 49h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	M0.7	M0.6	M0.5	M0.4	M0.3	M0.2	M0.1	M0.0
Default	1	1	1	1	1	1	1	1

Table 52. Interrupt mask port 1 register (address 4Ah) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	M1.7	M1.6	M1.5	M1.4	M1.3	M1.2	M1.1	M1.0
Default	1	1	1	1	1	1	1	1

Table 53. Interrupt mask port 2 register (address 4Bh) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	M2.7	M2.6	M2.5	M2.4	M2.3	M2.2	M2.1	M2.0
Default	1	1	1	1	1	1	1	1

Table 54. Interrupt mask port 3 register (address 4Ch) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	M3.7	M3.6	M3.5	M3.4	M3.3	M3.2	M3.1	M3.0
Default	1	1	1	1	1	1	1	1

Table 55. Interrupt mask port 4 register (address 4Dh) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	X	X	X	X	X	X	M4.1	M4.0
Default	X	X	X	X	X	X	1	1

6.5.10 Interrupt status registers (4Eh, 4Fh, 50h, 51h, 52h)

The read-only interrupt status registers are used to identify the source of an interrupt. When read, a logic 1 indicates that the corresponding input pin was the source of the interrupt. A logic 0 indicates that the input pin is not the source of an interrupt.

When a corresponding bit in the interrupt mask register is set to 1 (masked), the interrupt status bit will return logic 0. A register group read operation is described in Section 7.2.

Table 56. Interrupt status port 0 register (address 4Eh) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	S0.7	S0.6	S0.5	S0.4	S0.3	S0.2	S0.1	S0.0
Default	0	0	0	0	0	0	0	0

Table 57. Interrupt status port 1 register (address 4Fh) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	S1.7	S1.6	S1.5	S1.4	S1.3	S1.2	S1.1	S1.0
Default	0	0	0	0	0	0	0	0

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Table 58. Interrupt status port 2 register (address 50h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	S2.7	S2.6	S2.5	S2.4	S2.3	S2.2	S2.1	S2.0
Default	0	0	0	0	0	0	0	0

Table 59. Interrupt status port 3 register (address 51h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	S3.7	S3.6	S3.5	S3.4	S3.3	S3.2	S3.1	S3.0
Default	0	0	0	0	0	0	0	0

Table 60. Interrupt status port 4 register (address 52h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	X	X	X	X	X	X	S4.1	S4.0
Default	X	X	X	X	X	X	0	0

6.5.11 Output port configuration register (53h)

The output port configuration register selects port-wise push-pull or open-drain I/O stage. A logic 0 configures the I/O as push-pull (Q1 and Q2 are active, see Figure 10). A logic 1 configures the I/O as open-drain (Q1 is disabled, Q2 is active) and the recommended command sequence is to program this register (53h) before the Configuration register (0Fh, 10h, 11h, 12h, 13h) sets the port pins as outputs.

ODEN0 configures Port 0_x, ODEN1 configures Port 1_x, ODEN2 configures Port 2_x, ODEN3 configures Port 3_x, and ODEN4 configures Port 4_x.

Individual pins may be programmed as open-drain or push-pull by programming Individual Pin Output Configuration registers (68h, 69h, 6Ah, 6Bh, 6Ch). See Section 6.5.15 for more information.

A register group read or write operation is not allowed on this register. Successive read or write accesses will remain at this register address.

Table 61. Output port configuration register (address 53h)

Bit	7	6	5	4	3	2	1	0
Symbol	reserved			ODEN4	ODEN3	ODEN2	ODEN1	ODEN0
Default	0	0	0	0	0	0	0	0

6.5.12 Interrupt edge registers (54h, 55h, 56h, 57h, 58h, 59h, 5Ah, 5Bh and 5Ch)

The interrupt edge registers determine what action on an input pin will cause an interrupt along with the Interrupt Mask registers (49h, 4Ah, 4Bh, 4Ch and 4Dh). If the Interrupt is enabled (set '0' in the Mask register) and the action at the corresponding pin matches the required activity, the $\overline{INT}$ output will become active. The default value for each pin is 00b or level triggered, meaning a level change on the pin will cause an interrupt event. A level triggered action means a change in logic state (HIGH-to-LOW or LOW-to-HIGH), since the last read of the Input port (00h, 01h, 02h, 03h or 04h) which can be latched with a corresponding '1' set in the Input Latch register (3Ah, 3Bh, 3Ch, 3Dh, 3Eh). If the Interrupt edge register entry is set to 11b, any edge, positive- or negative-going, causes an interrupt event. If an entry is 01b, only a positive-going edge will cause an interrupt event, while a 10b will require a negative-going edge to cause an interrupt event. These edge

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interrupt events are latched, regardless of the status of the Input Latch register. These edged interrupts can be cleared in a number of ways: Reading input port registers (00h, 01h, 02h, 03h, 04h); setting the Interrupt Mask register (49h, 4Ah, 4Bh, 4Ch, 4Dh) to 1 (masked); setting the Interrupt Clear register (5Eh, 5Fh, 60h, 61h, 62h) to 1 (this is a write-only register); resetting the Interrupt Edge register (54h to 5Ch) back to 0. A register group write operation is described in Section 7.1. A register group read operation is described in Section 7.2.

Table 62. Interrupt edge port 0A register (address 54h)

Bit	7	6	5	4	3	2	1	0
Symbol	IE0.3		IE0.2		IE0.1		IE0.0	
Default	0	0	0	0	0	0	0	0

Table 63. Interrupt edge port 0B register (address 55h)

Bit	7	6	5	4	3	2	1	0
Symbol	IE0.7		IE0.6		IE0.5		IE0.4	
Default	0	0	0	0	0	0	0	0

Table 64. Interrupt edge port 1A register (address 56h)

Bit	7	6	5	4	3	2	1	0
Symbol	IE1.3		IE1.2		IE1.1		IE1.0	
Default	0	0	0	0	0	0	0	0

Table 65. Interrupt edge port 1B register (address 57h)

Bit	7	6	5	4	3	2	1	0
Symbol	IE1.7		IE1.6		IE1.5		IE1.4	
Default	0	0	0	0	0	0	0	0

Table 66. Interrupt edge port 2A register (address 58h)

Bit	7	6	5	4	3	2	1	0
Symbol	IE2.3		IE2.2		IE2.1		IE2.0	
Default	0	0	0	0	0	0	0	0

Table 67. Interrupt edge port 2B register (address 59h)

Bit	7	6	5	4	3	2	1	0
Symbol	IE2.7		IE2.6		IE2.5		IE2.4	
Default	0	0	0	0	0	0	0	0

Table 68. Interrupt edge port 3A register (address 5Ah)

Bit	7	6	5	4	3	2	1	0
Symbol	IE3.3		IE3.2		IE3.1		IE3.0	
Default	0	0	0	0	0	0	0	0

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Table 69. Interrupt edge port 3B register (address 5Bh)

Bit	7	6	5	4	3	2	1	0
Symbol	IE3.7		IE3.6		IE3.5		IE3.4	
Default	0	0	0	0	0	0	0	0

Table 70. Interrupt edge port 4A register (address 5Ch)

Bit	7	6	5	4	3	2	1	0
Symbol	X	X	X	X	IE4.1		IE4.0	
Default	X	X	X	X	0	0	0	0

Table 71. Interrupt edge bits (IEx.x)

Bit 1	Bit 0	Description
0	0	level-triggered interrupt
0	1	positive-going (rising) edge triggered interrupt
1	0	negative-going (falling) edge triggered interrupt
1	1	any edge (positive or negative-going) triggered interrupt

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6.5.13 Interrupt clear registers (5Eh, 5Fh, 60h, 61h, 62h)

The write-only interrupt clear registers clear individual interrupt sources (status bit). Setting an individual bit or any combination of bits to logic 1 will reset the corresponding interrupt source, so if that source was the only event causing an interrupt, the $\overline{INT}$ will be cleared. After writing a logic 1 the bit returns to logic 0. A register group write operation is described in Section 7.1.

Table 72. Interrupt clear port 0 register (address 5Eh) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	IC0.7	IC0.6	IC0.5	IC0.4	IC0.3	IC0.2	IC0.1	IC0.0
Default	0	0	0	0	0	0	0	0

Table 73. Interrupt clear port 1 register (address 5Fh) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	IC1.7	IC1.6	IC1.5	IC1.4	IC1.3	IC1.2	IC1.1	IC1.0
Default	0	0	0	0	0	0	0	0

Table 74. Interrupt clear port 2 register (address 60h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	IC2.7	IC2.6	IC2.5	IC2.4	IC2.3	IC2.2	IC2.1	IC2.0
Default	0	0	0	0	0	0	0	0

Table 75. Interrupt clear port 3 register (address 61h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	IC3.7	IC3.6	IC3.5	IC3.4	IC3.3	IC3.2	IC3.1	IC3.0
Default	0	0	0	0	0	0	0	0

Table 76. Interrupt clear port 4 register (address 62h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	X	X	X	X	X	X	IC4.1	IC4.0
Default	X	X	X	X	X	X	0	0

6.5.14 Input status registers (63h, 64h, 65h, 66h, 67h)

The read-only input status registers function exactly like Input Port 0, 1, 2, 3 and 4 (00h, 01h, 02h, 03h, 04h) without resetting the interrupt logic. This allows inspection of the actual state of the input pins without upsetting internal logic. If the pin is configured as an input, the port read is unaffected by input latch logic or other features, the state of the register is simply a reflection of the current state of the input pins. If a pin is configured as an output by the Configuration register (0Fh, 10h, 11h, 12h, 13h), and is also configured as open-drain (register 53h and 68h, 69h, 6Ah, 6Bh, 6Ch), the read for that pin will always return 0, otherwise that state of that pin is returned. A register group read operation is described in Section 7.2.

Table 77. Input status port 0 register (address 63h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	II0.7	II0.6	II0.5	II0.4	II0.3	II0.2	II0.1	II0.0
Default	X	X	X	X	X	X	X	X

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Table 78. Input status port 1 register (address 64h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	II1.7	II1.6	II1.5	II1.4	II1.3	II1.2	II1.1	II1.0
Default	X	X	X	X	X	X	X	X

Table 79. Input status port 2 register (address 65h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	II2.7	II2.6	II2.5	II2.4	II2.3	II2.2	II2.1	II2.0
Default	X	X	X	X	X	X	X	X

Table 80. Input status port 3 register (address 66h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	II3.7	II3.6	II3.5	II3.4	II3.3	II3.2	II3.1	II3.0
Default	X	X	X	X	X	X	X	X

Table 81. Input status port 4 register (address 67h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	X	X	X	X	X	X	II4.1	II4.0
Default	X	X	X	X	X	X	X	X

6.5.15 Individual pin output configuration registers (68h, 69h, 6Ah, 6Bh, 6Ch)

The individual pin output configuration registers modify output configuration (push-pull or open-drain) set by the Output Port Configuration register (53h).

If the ODENx bit is set at logic 0 (push-pull), any bit set to logic 1 in the IOCRx register will reverse the output state of that pin only to open-drain. When ODENx bit is set at logic 1 (open-drain), a logic 1 in IOCRx will set that pin to push-pull.

The recommended command sequence to program the output pin is to program ODENx (53h), the IOCRx, and finally the Configuration register (0Fh, 10h, 11h, 12h, 13h) to set the pins as outputs. A register group write operation is described in Section 7.1. A register group read operation is described in Section 7.2.

Table 82. Individual pin output configuration register 0 (address 68h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	IOCR0.7	IOCR0.6	IOCR0.5	IOCR0.4	IOCR0.3	IOCR0.2	IOCR0.1	IOCR0.0
Default	0	0	0	0	0	0	0	0

Table 83. Individual pin output configuration register 1 (address 69h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	IOCR1.7	IOCR1.6	IOCR1.5	IOCR1.4	IOCR1.3	IOCR1.2	IOCR1.1	IOCR1.0
Default	0	0	0	0	0	0	0	0

Table 84. Individual pin output configuration register 2 (address 6Ah) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	IOCR2.7	IOCR2.6	IOCR2.5	IOCR2.4	IOCR2.3	IOCR2.2	IOCR2.1	IOCR2.0
Default	0	0	0	0	0	0	0	0

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Table 85. Individual pin output configuration register 3 (address 6Bh) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	IOCR3.7	IOCR3.6	IOCR3.5	IOCR3.4	IOCR3.3	IOCR3.2	IOCR3.1	IOCR3.0
Default	0	0	0	0	0	0	0	0

Table 86. Individual pin output configuration register 4 (address 6Ch) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	X	X	X	X	X	X	IOCR4.1	IOCR4.0
Default	X	X	X	X	X	X	0	0

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6.5.16 Switch debounce enable registers (6Dh, 6Eh)

The switch debounce enable registers enable the switch debounce function for Port 0 and Port 1 pins. If a pin on Port 0 or Port 1 is designated as an input, a logic 1 in the Switch debounce enable register will connect debounce logic to that pin. If a pin is assigned as an output (via Configuration Port 0 or Port 1 register) the debounce logic is not connected to that pin and it will function as a normal output. The switch debounce logic requires an oscillator time base input and if this function is used, P2_0 is designated as the oscillator input. If P2_0 is not configured as input, then switch debounce logic is not connected to any pin. See Section 6.10 “Switch debounce circuitry” for additional information about Switch debounce logic functionality.

Table 87. Switch debounce enable Port 0 register (address 6Dh) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	SD0.7	SD0.6	SD0.5	SD0.4	SD0.3	SD0.2	SD0.1	SD0.0
Default	0	0	0	0	0	0	0	0

Table 88. Switch debounce enable Port 1 register (address 6Eh) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	SD1.7	SD1.6	SD1.5	SD1.4	SD1.3	SD1.2	SD1.1	SD1.0
Default	0	0	0	0	0	0	0	0

6.5.17 Switch debounce count register (6Fh)

The switch debounce count register is used to count the debounce time that the switch debounce logic uses to determine if a switch connected to one of the Port 0 or Port 1 pins finally stays open (logic 1) or closed (logic 0). This number, together with the oscillator frequency supplied to P2_0, determines the debounce time (for example, the debounce time will be 10 μs if this register is set to 0Ah and external oscillator frequency is 1 MHz). See Section 6.10 “Switch debounce circuitry” for further information.

Table 89. Switch debounce count register (address 66h) bit description [1]

Bit	7	6	5	4	3	2	1	0
Symbol	SDC0.7	SDC0.6	SDC0.5	SDC0.4	SDC0.3	SDC0.2	SDC0.1	SDC0.0
Default	0	0	0	0	0	0	0	0

[1] The switch debounce logic is disabled if this register is set to 00h.

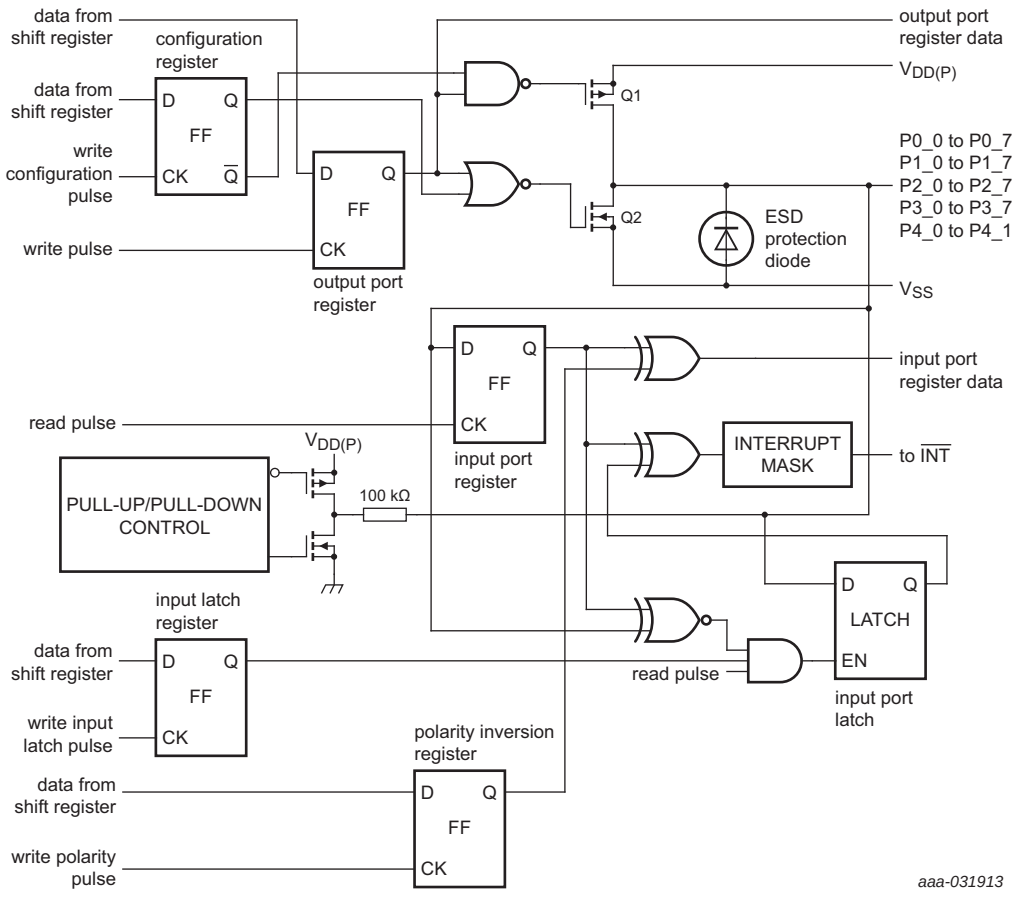
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6.6 I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, which creates a high-impedance input. The input voltage may be raised above $V_{DD(P)}$ to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the Output port register. In this case, there are low-impedance paths between the I/O pin and either $V_{DD(P)}$ or V_{SS}. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation. To avoid internal noise generation when multiple outputs switch simultaneously, a 0.22 uF bypass capacitor is required on the $V_{DD(P)}$ pin as close to the package as practical.



On power-up or reset, all registers return to default values.

Fig 10. Simplified schematic of P0_0 to P4_1

6.7 Power-on reset

When power (from 0 V) is applied to $V_{DD(P)}$, an internal power-on reset holds the PCAL6534 in a reset condition until $V_{DD(P)}$ has reached V_{POR}. At that time, the reset condition is released and the PCAL6534 registers and I²C-bus/SMBus state machine initializes to their default states. After that, $V_{DD(P)}$ must be lowered to below V_{POR} and back up to the operating voltage for a power-reset cycle. See Section 8.2 “Power-on reset requirements”.

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6.8 Reset input ($\overline{\text{RESET}}$)

The $\overline{\text{RESET}}$ input can be asserted to initialize the system while keeping the $V_{DD(P)}$ at its operating level. A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin LOW for a minimum of $t_{w(rst)}$. The PCAL6534 registers and I²C-bus/SMBus state machine are changed to their default state once $\overline{\text{RESET}}$ is LOW (0). When $\overline{\text{RESET}}$ is HIGH (1), the I/O levels at the P port can be changed externally or through the master. This input requires a pull-up resistor to $V_{DD(I2C\text{-}bus)}$ if no active connection is used.

6.9 Interrupt output ($\overline{\text{INT}}$)

The $\overline{\text{INT}}$ output has an open-drain structure and requires pull-up resistor to $V_{DD(P)}$ or $V_{DD(I2C\text{-}bus)}$ depending on the application. When any current input port state differs from its corresponding input port register state, the interrupt output pin is asserted (logic 0) to indicate the system master (MCU) that one of input port states has changed. A pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the input port register.

In order to enable the interrupt output, the following three conditions must be satisfied:

- The GPIO must be configured as an input port by writing "1" to configuration port registers (0Fh, 10h, 11h, 12h, 13h)
- The interrupt mask registers (49h, 4Ah, 4Bh, 4Ch, 4Dh) must set to "0" to unmask interrupt sources.
- The interrupt edge registers (54h to 5Ch) select what action on each input pin will cause an interrupt; there are four different interrupt trigger modes: level trigger, rising-edge trigger, falling-edge trigger, or any edge trigger.

The input latch registers (3Ah, 3Bh, 3Ch, 3Dh, 3Eh) control each input pin either to enable latched input state or non-latched input state. When input pin is set to latch state, it will hold or latch the input pin state (keep the logic value) and generate an interrupt until the master can service the interrupt. This minimizes the host's interrupt service response for fast moving inputs.

Any interrupt status bit can be cleared and $\overline{\text{INT}}$ pin de-asserted by using one of the following methods and conditions:

- Power on reset (POR), hardware reset from $\overline{\text{RESET}}$ pin, or software reset call
- Read input port registers (00h, 01h, 02h, 03h, 04h)
- Write logic 1 to interrupt clear registers (5Eh, 5Fh, 60h, 61h, 62h)
- Write logic 1 to interrupt mask registers (49h, 4Ah, 4Bh, 4Ch, 4Dh)
- Write logic 0 to configuration registers (0Fh, 10h, 11h, 12h, 13h), set pin as output port.
- Input pin goes back to its initial state in level trigger and non-latch mode
- Input pin goes back to its initial state in level trigger and change latch to non-latch mode
- Change the interrupt trigger mode from level trigger to edge trigger or vice versa in interrupt edge registers

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When using the input latch feature, the input pin state is latched. The interrupt is de-asserted only when data is read from the port that generated the interrupt. The interrupt reset occurs in the read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Any change of the inputs after resetting is detected and is transmitted as $\overline{INT}$.

6.10 Switch debounce circuitry

Mechanical switches do not make clean make-or-break connections and the contacts can 'bounce' for a significant period of time before settling into a steady-state condition. This can confuse fast processors and make the physical interface difficult to design and the software interface difficult to make reliable.

The PCAL6534 implements hardware to ease the hardware interface by debouncing switch closures with dedicated circuitry. P0_0 to P0_7, P1_0 to P1_7 can connect to this debounce hardware on a pin-by-pin basis. These switch debouncers remove bounce when a switch opens or closes by requiring that sequentially clocked inputs remain in the same state for a number of sampling periods. The output does not change until the input is stable for a programmable duration. The circuit block diagram (Figure 12) shows the functional blocks consisting of an external oscillator, counter, edge detector, and D flip-flop. When the switch input state changes, the edge detector will reset the counter. When the switch input state is stable for the full qualification period, the counter clocks the flip-flop, updating the output. Figure 13 shows the typical opening and closing switch debounce operation timing.

To use the debounce circuitry, set the port pins (P0_0 to P0_7, and P1_0 to P1_7) with switches attached in the Switch Debounce Enable 0 and 1 registers (6Dh, 6Eh). Connect an external oscillator signal on P2_0, which serves as a time base to the debounce timer. Finally, set a delay time in the Switch Debounce Count register (6Fh). The combination of time base of the external oscillator and the debounce count sets the qualification debounce period or t_{DP} in Figure 13. Note that all debounce counters will use the same time base and count, but they all function independently.

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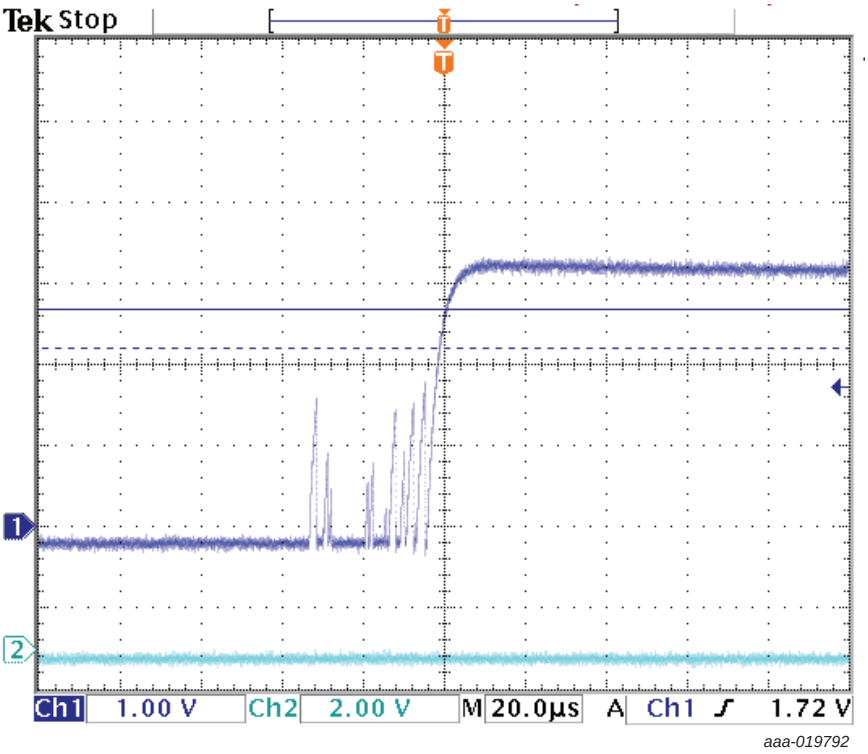
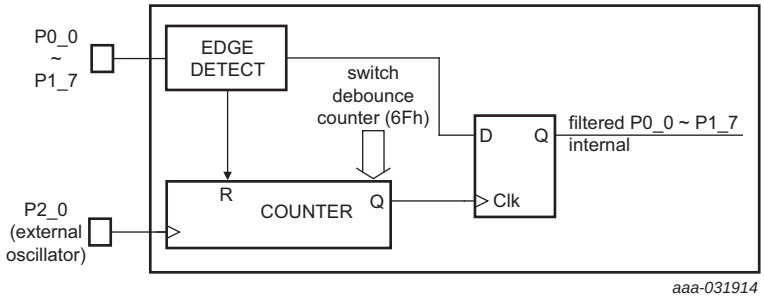


Fig 11. Switch contact bounce

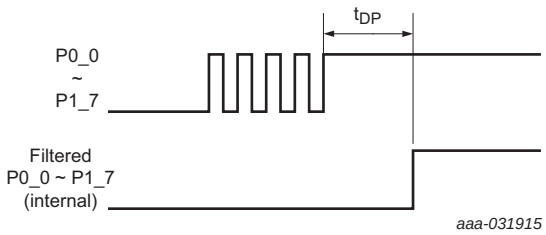


The first time external clock is connected, external clock is required to wait 9 clock cycles for the debounce circuit in normal operation.

Fig 12. Debouncer block diagram

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t_{DP} = [PERIOD of EXT CLOCK] * [Debounce counter(66h)] = 1 μs * 10 = 10 μs (if external clock = 1 MHz, debounce count register (6Fh) = 0Ah)

Fig 13. Switch debounce timing

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7. Bus transactions

The PCAL6534 is an I²C-bus slave device. Data is exchanged between the master and PCAL6534 through write and read commands using I²C-bus. The two communication lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

7.1 Write commands

Data is transmitted to the PCAL6534 by sending the device address with the Least Significant Bit (LSB) set to a logic 0 (see Figure 3 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte.

Many of the registers within the PCAL6534 are configured to operate as register quinary. The 5-register groups are input ports, output ports, polarity inversion and configuration registers, as well as Input latch, Pull-up/pull-down enable and selection registers, Interrupt mask and Interrupt status, Interrupt clear, and Input port (status) without Interrupt clear registers, Individual pin output port configuration registers. After sending data to one register, the next data byte is sent to the next register in the group. For example, if the first byte is sent to Output Port 1 (register 06h), the next byte is stored in Output Port 2 (register 07h). The next byte sent is stored in Output Port 3 (register 08h) and the next byte will Output Port 4 (register 09h). Since every new write access after a STOP condition requires a Command byte, which sets the Pointer register, the next new write access will be to an arbitrary register.

There is no limit on the number of data bytes sent in one write transmission. In this way, the host can continuously update a register group independently of the other registers or the host can simply update a single register.

There is one 3-register group: switch debounce (6Dh ~ 6Fh) registers and two 9-register groups: Output drive strength (30h to 38h) and interrupt edge (54h to 5Ch) registers which can be programmed continuously in this group.

There is one register that is not part of a register group: Output port configuration (53h). When this register is accessed multiple times, the register address remains fixed on the same address.

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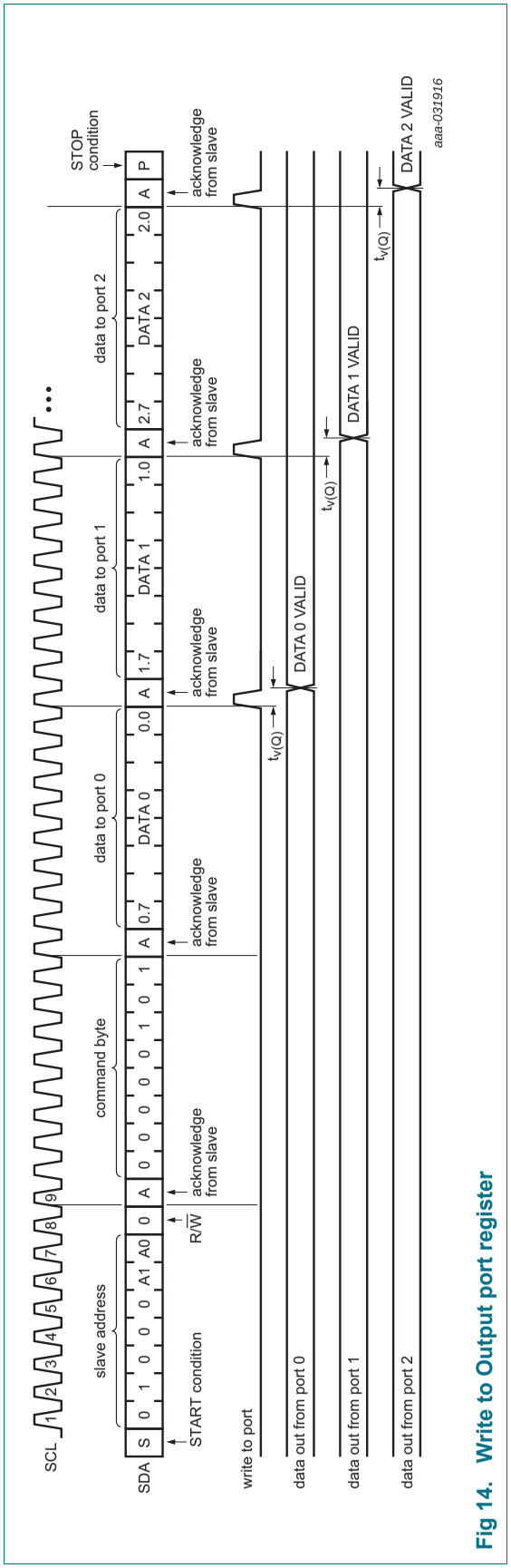


Fig 14. Write to Output port register

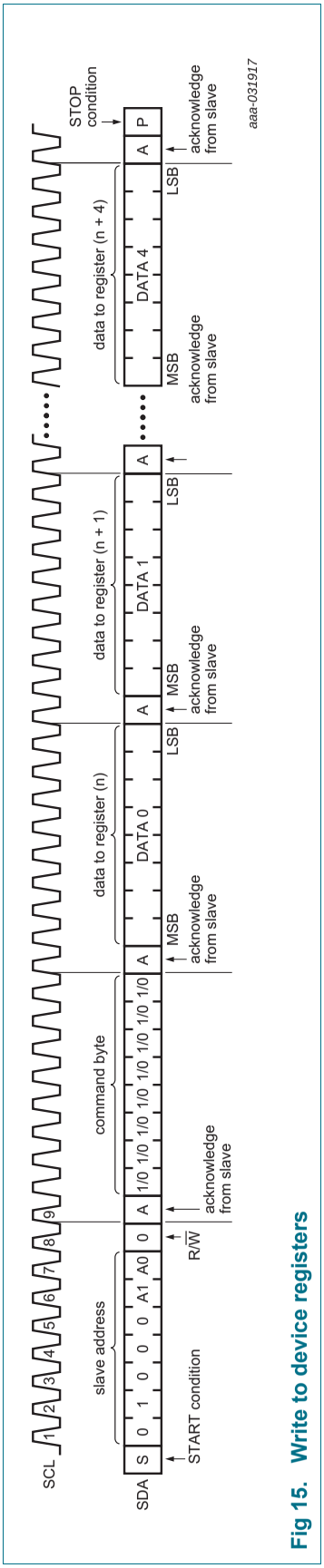


Fig 15. Write to device registers

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7.2 Read commands

To read data from the PCAL6534, the bus master must first send the PCAL6534 address with the least significant bit set to a logic 0 (see Figure 3 for device address). The command byte is sent after the address and determines which register is to be accessed.

After a restart or a STOP followed by a START condition, the device address is sent again, but this time the least significant bit is set to a logic 1 to read data. Data from the register defined by the command byte is sent by the PCAL6534 (see Figure 16 to Figure 19). Additional bytes may be read after the first byte read is complete and will reflect the next register in the group. For example, if Input Port 1 is read, the next byte read is Input Port 2. There is no limit on the number of data bytes received in one read transmission, but on the final byte received the bus master must not acknowledge the data.

After a subsequent restart or a STOP followed by a START condition, the command byte contains the value of the next register to be read in the group. For example, if Input Port 1 was read last before the restart, the register that is read after the restart is the Input Port 2.

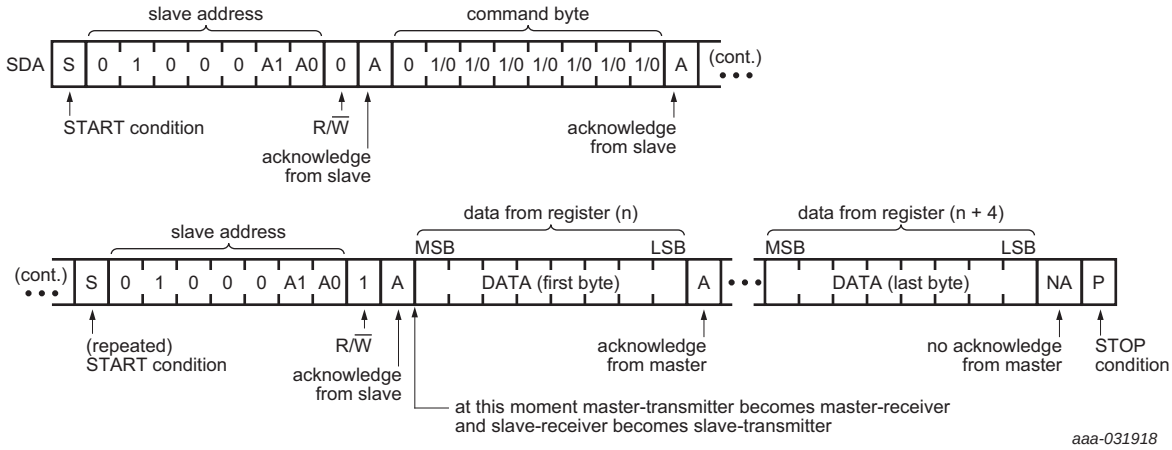
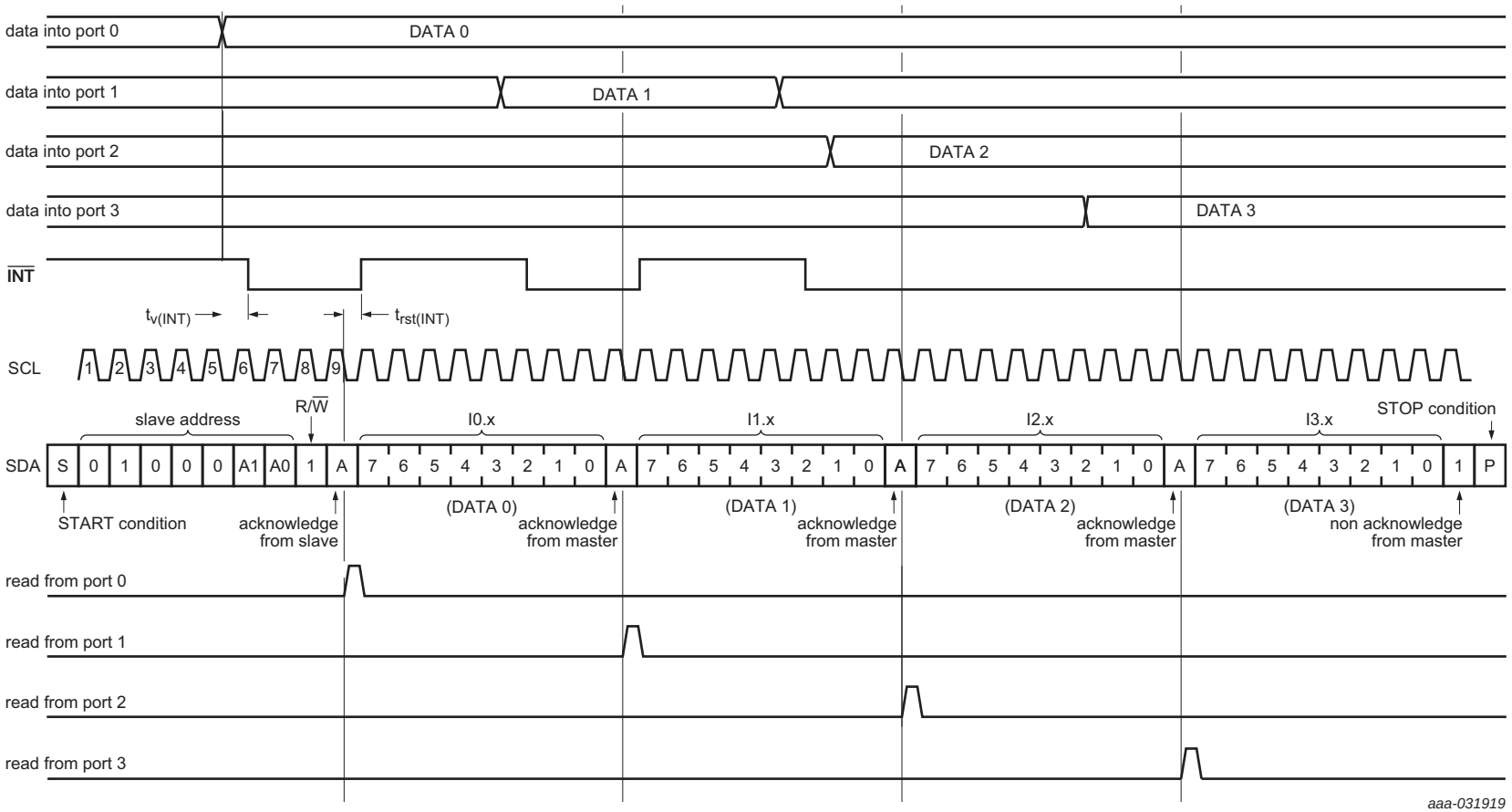


Fig 16. Read from device registers

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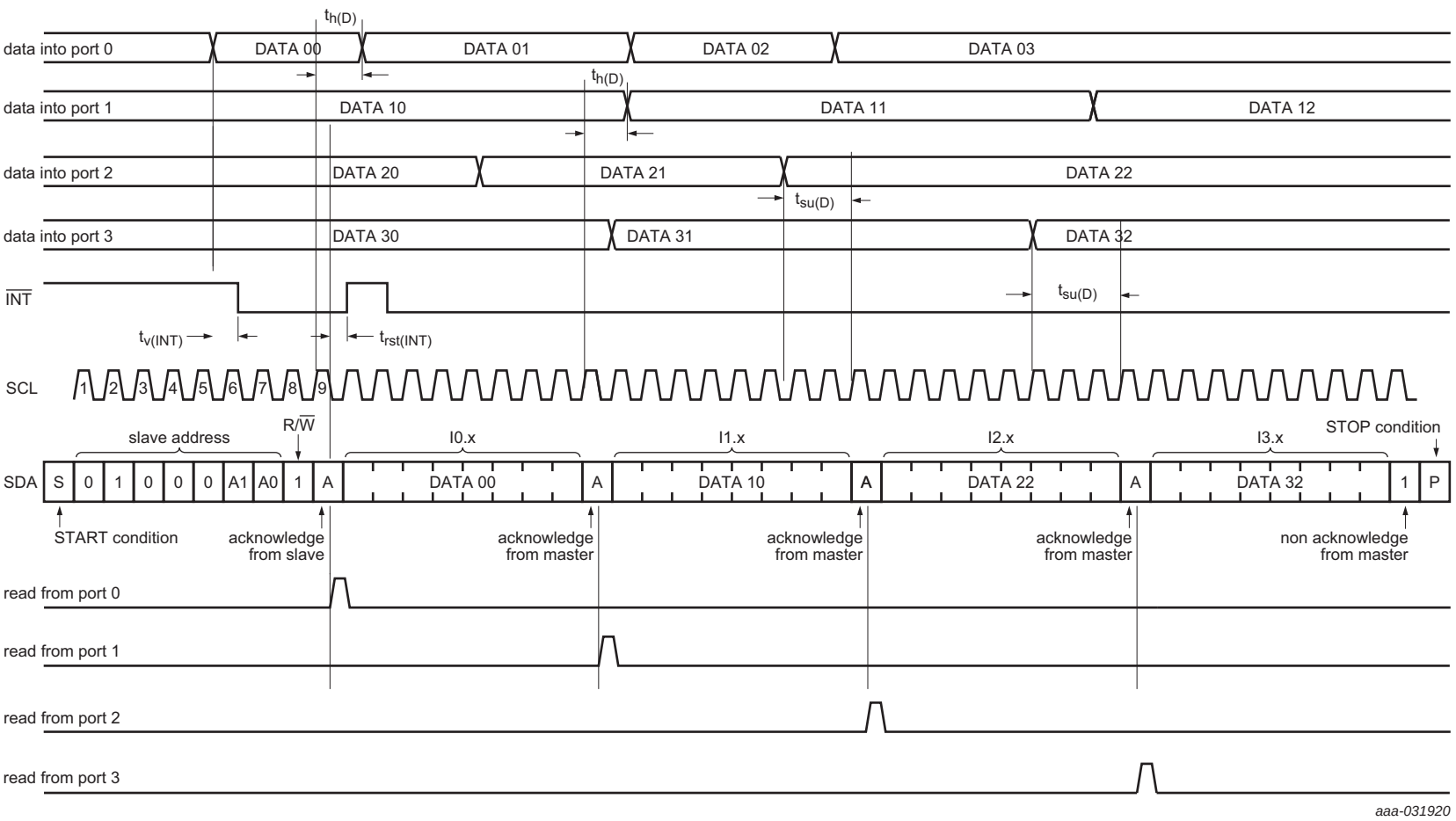
Remark: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read input port register).

This figure eliminates the command byte transfers and a restart between the initial slave address call and actual data transfer from P port (see Figure 16).

Fig 17. Read input port register (non-latched), scenario 1

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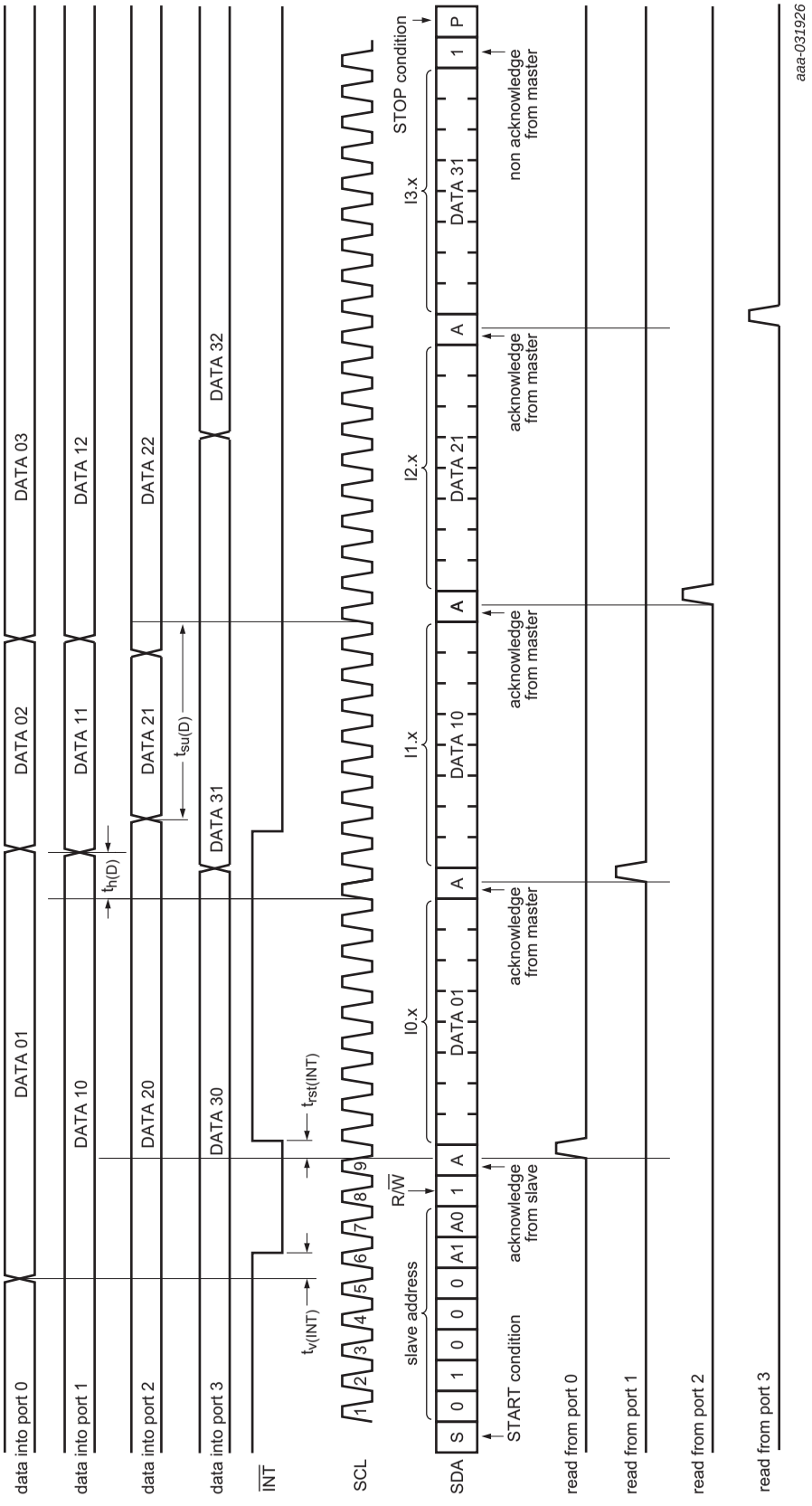
Remark: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read input port register).

This figure eliminates the command byte transfers and a restart between the initial slave address call and actual data transfer from P port (see Figure 16).

Fig 18. Read input port register (non-latched), scenario 2

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Remark: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read input port register).

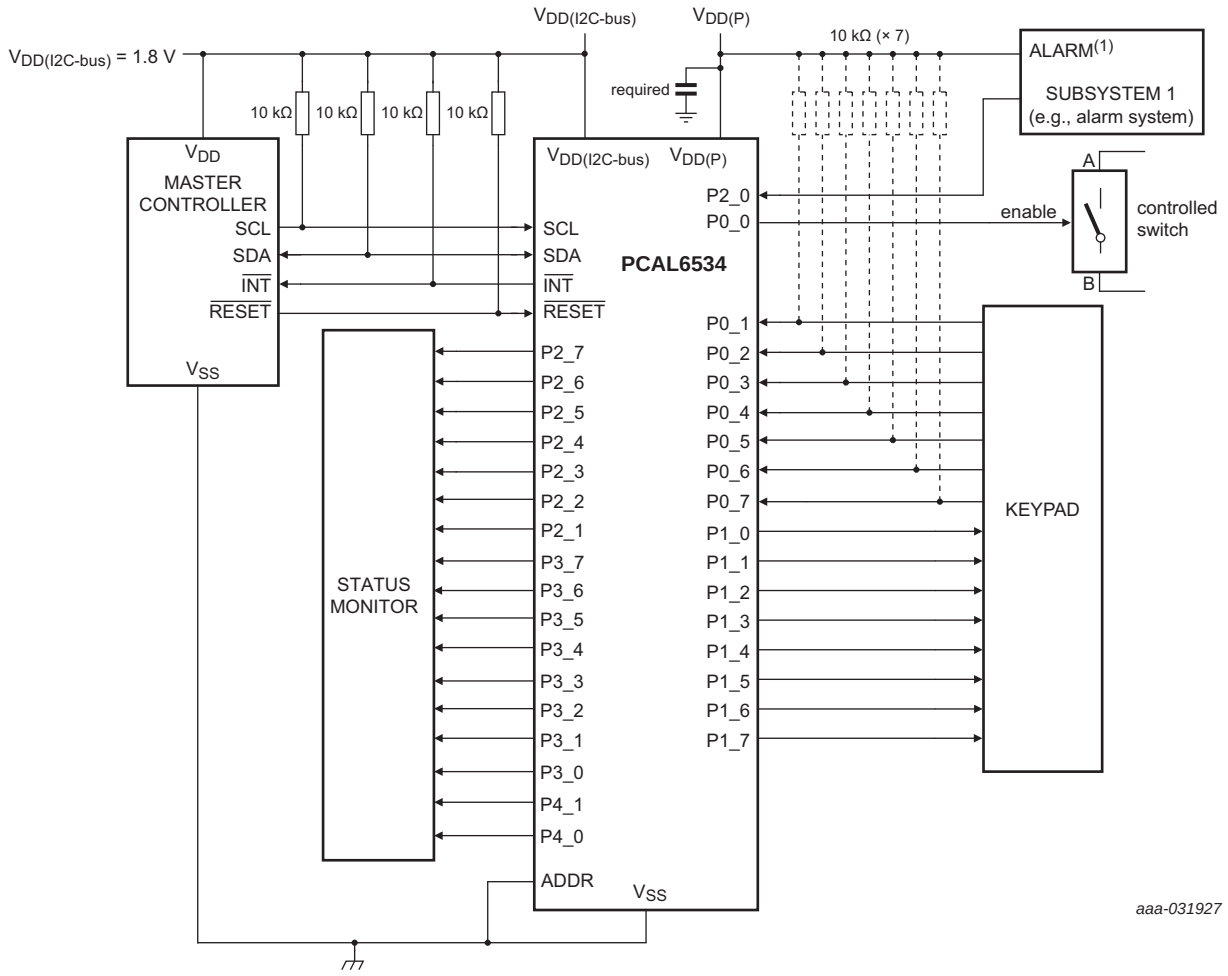
This figure eliminates the command byte transfers and a restart between the initial slave address call and actual data transfer from P port (see Figure 16).

Fig 19. Read input port register (latch enabled), scenario 3

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8. Application design-in information



Device address configured as 0100 010x for this example.

P2_0 and P0_1 through P0_7 are configured as inputs.

P1_0 through P4_1(except P2_0) are configured as outputs.

(1) External resistors are required for inputs (on P port) that may float. If a driver to an input will never let the input float, a resistor is not needed with internal pull-up or pull-down resistor option. If an output in the P port is configured as an output, there is no need for external pull-up resistors.

Fig 20. Typical application

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8.1 Output drive strength control

The Output drive strength registers allow the user to control the output drive level of the GPIO. Each GPIO can be configured independently to one of the four possible output current levels. By programming these bits the user is changing the number of transistor pairs or 'fingers' that drive the I/O pad.

Figure 21 shows a simplified output stage. The behavior of the pad is affected by the Configuration register, the output port data, and the current control register. When the Current Control register bits are programmed to 01b, then only two of the fingers are active, reducing the current drive capability by 50 %.

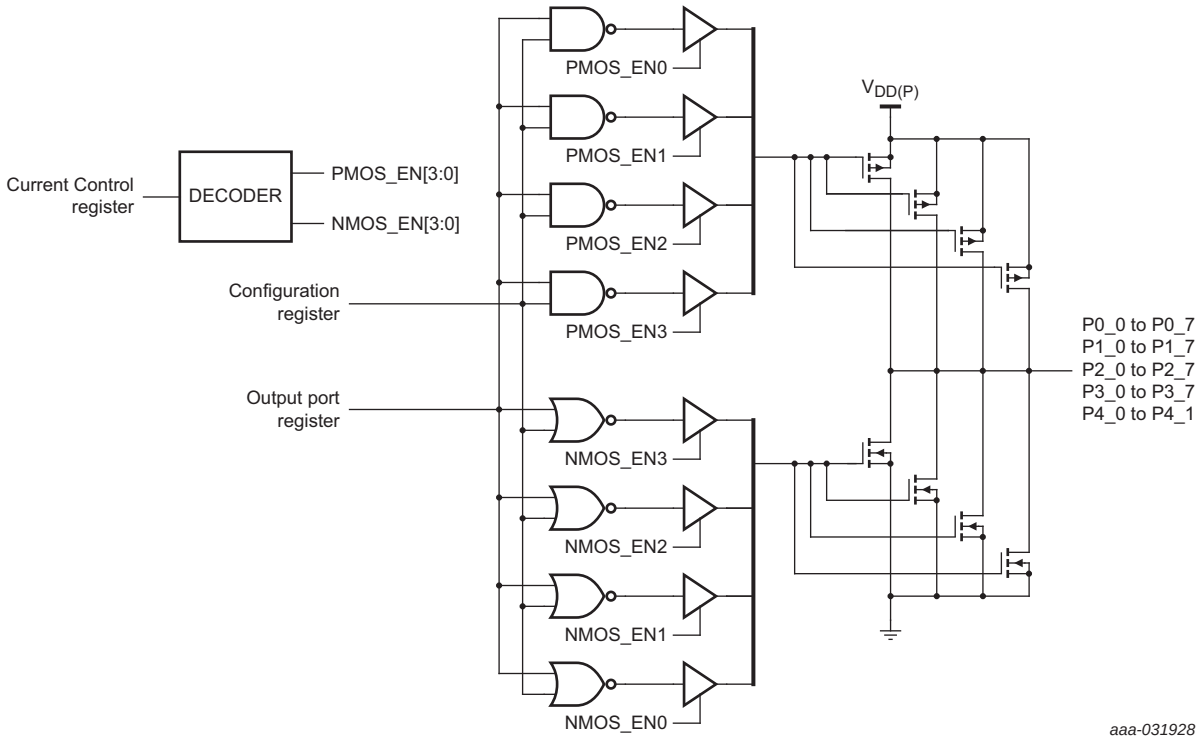


Fig 21. Simplified output stage

Reducing the current drive capability may be desirable to reduce system noise. When the output switches (transitions from H/L), there is a peak current that is a function of the output drive selection. This peak current runs through V_{DD} and V_{SS} package inductance and will create noise (some radiated, but more critically Simultaneous Switching Noise (SSN)). In other words, switching many outputs at the same time will create ground and supply noise. The output drive strength control through the Output Drive Strength registers allows the user to mitigate SSN issues without the need of additional external components.

In any case, a 0.22 uF bypass capacitor is required on the $V_{DD(P)}$ pin, located as close to the package as practical.

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8.2 Power-on reset requirements

In the event of a glitch or data corruption, PCAL6534 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in Figure 22 and Figure 23.

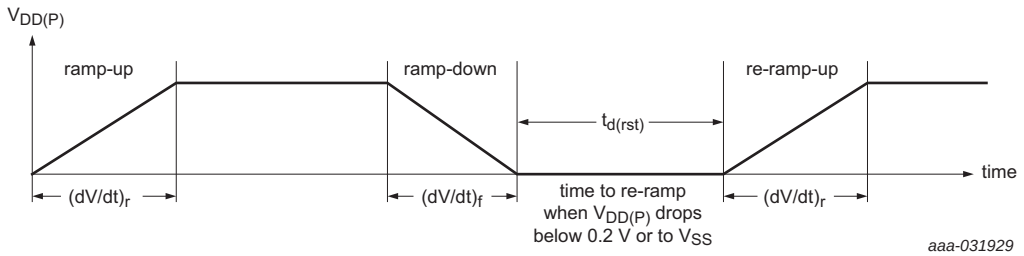


Fig 22. $V_{DD(P)}$ is lowered below 0.2 V or to 0 V and then ramped up to $V_{DD(P)}$

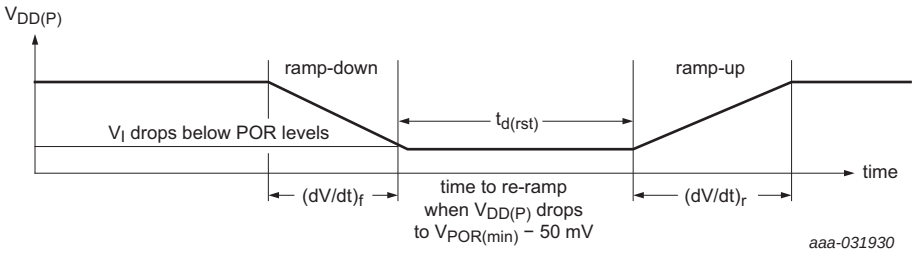


Fig 23. $V_{DD(P)}$ is lowered below the POR threshold, then ramped back up to $V_{DD(P)}$

Table 90 specifies the performance of the power-on reset feature for PCAL6534 for both types of power-on reset.

Table 90. Recommended supply sequencing and ramp rates

T_{amb} = 25 °C (unless otherwise noted). Not tested; specified by design.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$(dV/dt)_f$	fall rate of change of voltage	Figure 22	0.1	-	2000	ms
$(dV/dt)_r$	rise rate of change of voltage	Figure 22	0.1	-	2000	ms
$t_{d(rst)}$	reset delay time	Figure 22; re-ramp time when $V_{DD(P)}$ drops below 0.2 V or to V_{SS}	1	-	-	µs
		Figure 23; re-ramp time when $V_{DD(P)}$ drops to $V_{POR(min)}$ − 50 mV	1	-	-	µs
$\Delta V_{DD(gl)}$	glitch supply voltage difference	Figure 24 [1]	-	-	1.0	V
$t_{w(gl)VDD}$	supply voltage glitch pulse width	Figure 24 [2]	-	-	10	µs
$V_{POR(trip)}$	power-on reset trip voltage	falling $V_{DD(P)}$	0.7	-	-	V
		rising $V_{DD(P)}$	-	-	1.5	V

[1] Level that $V_{DD(P)}$ can glitch down to with a ramp rate at 0.4 µs/V, but not cause a functional disruption when $t_{w(gl)VDD}$ < 1 µs.

[2] Glitch width that will not cause a functional disruption when $\Delta V_{DD(gl)} = 0.5 \times V_{DD(P)}$.

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Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ($t_{w(gl)VDD}$) and glitch height ($\Delta V_{DD(gl)}$) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 24 and Table 90 provide more information on how to measure these specifications.

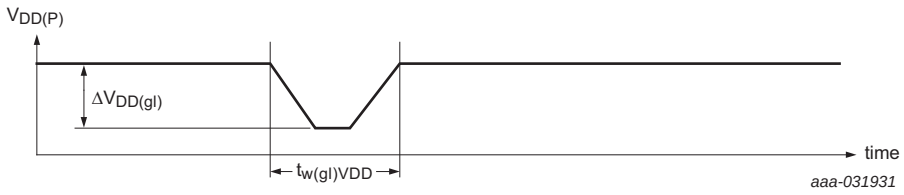


Fig 24. Glitch width and glitch height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I²C-bus/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{DD} being lowered to or from 0 V. Figure 25 and Table 90 provide more details on this specification.

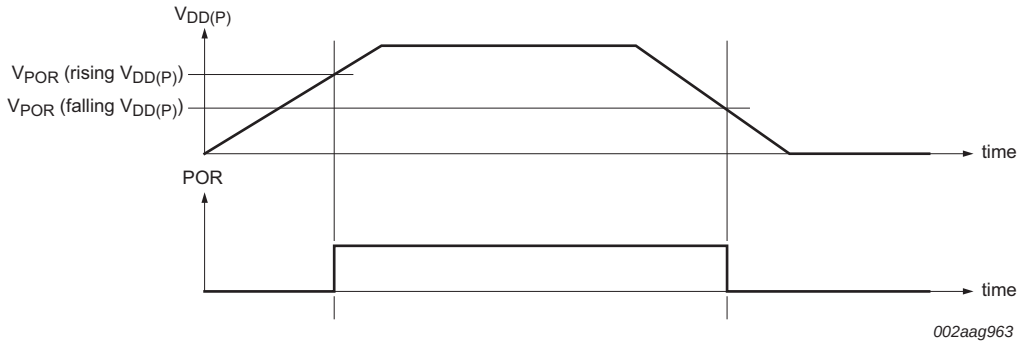


Fig 25. Power-on reset voltage (V_{POR})

8.3 Device current consumption with internal pull-up and pull-down resistors

The PCAL6534 integrates programmable pull-up and pull-down resistors to eliminate external components when pins are configured as inputs and pull-up or pull-down resistors are required (for example, nothing is driving the inputs to the power supply rails. Since these pull-up and pull-down resistors are internal to the device itself, they contribute to the current consumption of the device and must be considered in the overall system design.

The pull-up or pull-down function is selected in registers 44h, 45h, 46h, 47h and 48h, while the resistor is connected by the enable registers 3Fh, 40h, 41h, 42h and 43h. The configuration of the resistors is shown in Figure 10.

If the resistor is configured as a pull-up, that is, connected to V_{DD}, a current will flow from the $V_{DD(P)}$ pin through the resistor to ground when the pin is held LOW. This current will appear as additional I_{DD} upsetting any current consumption measurements.

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In the same manner, if the resistor is configured as a pull-down and the pin is held HIGH, current will flow from the power supply through the pin to the V_{SS} pin. While this current will not be measured as part of I_{DD}, one must be mindful of the 200 mA limiting value through V_{SS}.

The pull-up and pull-down resistors are simple resistors and the current is linear with voltage. The resistance specification for these devices spans from 50 kΩ with a nominal 100 kΩ value. Any current flow through these resistors is additive by the number of pins held HIGH or LOW and the current can be calculated by Ohm's law. See Figure 29 for a graph of supply current vs the number of pull-up resistors.

8.4 I²C-bus error recovery techniques

There are a number of techniques to recover from error conditions on the I²C-bus. Slave devices like the PCAL6534 use a state machine to implement the I²C protocol and expect a certain sequence of events to occur to function properly. Unexpected events at the I²C master can wreak havoc with the slaves connected on the bus. However, it is usually possible to recover deterministically to a known bus state with careful protocol manipulation.

A hard slave reset, either through power-on reset or by activating the $\overline{\text{RESET}}$ pin, will set the device back into the default state. Of course, this means the input/output pins and their configuration will be lost, which might cause some system issues.

A STOP condition, which is only initiated by the master, will reset the slave state machine into a known condition where SDA is not driven LOW by the slave and logically, the slave is waiting for a START condition. A STOP condition is defined as SDA transitioning from LOW to HIGH while SCL is HIGH.

If the master is interrupted during a packet transmission, the slave may be sending data or performing an Acknowledge, driving the I²C-bus SDA line LOW. Since SDA is LOW, it effectively blocks any other I²C-bus transaction. A deterministic method to clear this situation, once the master recognizes a 'stuck bus' state, is for the master to blindly transmit nine clocks on SCL. If the slave was transmitting data or acknowledging, nine or more clocks ensures the slave state machine returns to a known, idle state since the protocol calls for eight data bits and one ACK bit. It does not matter when the slave state machine finishes its transmission, extra clocks will be recognized as STOP conditions.

The PCAL6534 SCL pin is an input only. If SCL is stuck LOW, then only the bus master or a slave performing a clock stretch operation can cause this condition.

With careful design of the bus master error recovery firmware, many I²C-bus protocol problems can be avoided.

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9. Limiting values

Table 91. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD(I2C\text{-}bus)}$	I²C-bus supply voltage		–0.5	+4.0	V
$V_{DD(P)}$	supply voltage port P		–0.5	+6.5	V
$V_{I(P)}$	input voltage on all ports	[1]	–0.5	+6.5	V
$V_{O(P)}$	output voltage on all ports	[1]	–0.5	+6.5	V
$V_{I(I)}$	input voltage on I²C-bus, $\overline{RESET}$, ADDR		–0.5	+4.0	V
$V_{O(I)}$	output voltage on I²C-bus, $\overline{INT}$		–0.5	+4.0	V
I_{IK}	input clamping current	ADDR, $\overline{RESET}$, SCL; $V_I < 0$ V	-	±20	mA
I_{OK}	output clamping current	$\overline{INT}$; $V_O < 0$ V	-	±20	mA
I_{IOK}	input/output clamping current	P port; $V_O < 0$ V or $V_O > V_{DD(P)}$	-	±20	mA
		SDA; $V_O < 0$ V or $V_O > V_{DD(I2C\text{-}bus)}$	-	±20	mA
I_{OL}	LOW-level output current	continuous; P port; $V_O = 0$ V to $V_{DD(P)}$	-	50	mA
		continuous; SDA, $\overline{INT}$; $V_O = 0$ V to $V_{DD(I2C\text{-}bus)}$	-	25	mA
I_{OH}	HIGH-level output current	continuous; P port; $V_O = 0$ V to $V_{DD(P)}$	-	25	mA
I_{DD}	supply current	continuous through V_{SS}	-	500	mA
$I_{DD(P)}$	supply current port P	continuous through $V_{DD(P)}$	-	400	mA
$I_{DD(I2C\text{-}bus)}$	I²C-bus supply current	continuous through $V_{DD(I2C\text{-}bus)}$	-	10	mA
T_{stg}	storage temperature		–65	+150	°C
$T_{j(max)}$	maximum junction temperature		-	125	°C

[1] The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

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10. Recommended operating conditions

Table 92. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD(I2C\text{-}bus)}$	I²C-bus supply voltage		0.8	3.6	V
$V_{DD(P)}$	supply voltage port P	A 0.22 uF bypass capacitor is required on $V_{DD(P)}$ pin as close to the package as practical	1.65	5.5	V
V_{IH}	HIGH-level input voltage	SCL, SDA, $\overline{RESET}$, ADDR			
		$V_{DD(I2C\text{-}bus)} \leq 1.1$ V	$0.8 \times V_{DD(I2C\text{-}bus)}$	3.6	V
		$V_{DD(I2C\text{-}bus)} > 1.1$ V	$0.7 \times V_{DD(I2C\text{-}bus)}$	3.6	V
		P4_1 to P0_0	$0.7 \times V_{DD(P)}$	5.5	V
V_{IL}	LOW-level input voltage	SCL, SDA, $\overline{RESET}$, ADDR			
		$V_{DD(I2C\text{-}bus)} \leq 1.1$ V	−0.5	$0.2 \times V_{DD(I2C\text{-}bus)}$	V
		$V_{DD(I2C\text{-}bus)} > 1.1$ V	−0.5	$0.3 \times V_{DD(I2C\text{-}bus)}$	V
		P4_1 to P0_0	−0.5	$0.3 \times V_{DD(P)}$	V
I_{OH}	HIGH-level output current	P4_1 to P0_0	-	10	mA
I_{OL}	LOW-level output current	P4_1 to P0_0	-	25	mA
T_{amb}	ambient temperature	operating in free air	−40	+85	°C

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11. Thermal characteristics

Table 93. Thermal characteristics

Symbol	Parameter	Conditions	Value (typ)	Unit
$R_{th(j-a)}$	Thermal resistance from junction to ambient on a JEDEC 2S2P board[1]	VFBGA42 package	61.3	°C/W

[1] The package thermal resistance is calculated in accordance with JESD 51-7.

12. Static characteristics

Table 94. Static characteristics

T_{amb} = −40 °C to +85 °C; $V_{DD(I2C\text{-}bus)}$ = 0.8 V to 3.6 V; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{IK}	input clamping voltage	I_I = −18 mA	−1.2	-	-	V
V_{POR}	power-on reset voltage	$V_I = V_{DD(P)}$ or V_{SS}; I_O = 0 mA	-	1.2	1.5	V
V_{OH}	HIGH-level output voltage[2]	P port; I_{OH} = −8 mA; CCX.X = 11b				
		$V_{DD(P)}$ = 1.65 V	1.2	-	-	V
		$V_{DD(P)}$ = 2.3 V	1.8	-	-	V
		$V_{DD(P)}$ = 3 V	2.6	-	-	V
		$V_{DD(P)}$ = 4.5 V	4.1	-	-	V
		P port; I_{OH} = −2.5 mA and CCX.X = 00b; I_{OH} = −5 mA and CCX.X = 01b; I_{OH} = −7.5 mA and CCX.X = 10b; I_{OH} = −10 mA and CCX.X = 11b;				
		$V_{DD(P)}$ = 1.65 V	1.1	-	-	V
		$V_{DD(P)}$ = 2.3 V	1.7	-	-	V
		$V_{DD(P)}$ = 3 V	2.5	-	-	V
		$V_{DD(P)}$ = 4.5 V	4.0	-	-	V
V_{OL}	LOW-level output voltage[2]	P port; I_{OL} = 8 mA; CCX.X = 11b				
		$V_{DD(P)}$ = 1.65 V	-	-	0.45	V
		$V_{DD(P)}$ = 2.3 V	-	-	0.25	V
		$V_{DD(P)}$ = 3 V	-	-	0.25	V
		$V_{DD(P)}$ = 4.5 V	-	-	0.20	V
		P port; I_{OL} = 2.5 mA and CCX.X = 00b; I_{OL} = 5 mA and CCX.X = 01b; I_{OL} = 7.5 mA and CCX.X = 10b; I_{OL} = 10 mA and CCX.X = 11b;				
		$V_{DD(P)}$ = 1.65 V	-	-	0.5	V
		$V_{DD(P)}$ = 2.3 V	-	-	0.3	V
		$V_{DD(P)}$ = 3 V	-	-	0.25	V
		$V_{DD(P)}$ = 4.5 V	-	-	0.2	V
I_{OL}	LOW-level output current[3]	SDA				
		V_{OL} = 0.4 V; $V_{DD(I2C\text{-}bus)} \leq$ 2 V	15	-	-	mA
		V_{OL} = 0.4 V; $V_{DD(I2C\text{-}bus)}$ > 2 V	20	-	-	mA
		$\overline{INT}$; V_{OL} = 0.4 V; $V_{DD(I2C\text{-}bus)}$ = 1.65 V to 5.5 V	3	[4]	-	mA

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Table 94. Static characteristics *...continued*

T_{amb} = −40 °C to +85 °C; $V_{DD(I2C\text{-}bus)}$ = 0.8 V to 3.6 V; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I_I	input current	ADDR, SCL, SDA, $\overline{RESET}$; $V_{DD(P)}$ = 1.65 V to 5.5 V; V_I = $V_{DD(I2C\text{-}bus)}$ or V_{SS}	-	-	±1	µA
I_{IH}	HIGH-level input current	P port; V_I = $V_{DD(P)}$; $V_{DD(P)}$ = 1.65 V to 5.5 V	-	-	1	µA
I_{IL}	LOW-level input current	P port; V_I = V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V	-	-	1	µA
I_{DD}	supply current	Clocked mode; $I_{DD(I2C\text{-}bus)}$ + $I_{DD(P)}$; SDA, P port, ADDR, $\overline{RESET}$; V_I on ADDR, SDA and $\overline{RESET}$ = $V_{DD(I2C\text{-}bus)}$ or V_{SS}; V_I on P port = $V_{DD(P)}$; I_O = 0 mA; I/O = inputs				
		$V_{DD(P)}$ = 3.6 V to 5.5 V; f_{SCL} = 0 kHz	-	3	11.5	µA
		$V_{DD(P)}$ = 2.3 V to 3.6 V; f_{SCL} = 0 kHz	-	2	6.8	µA
		$V_{DD(P)}$ = 1.65 V to 2.3 V; f_{SCL} = 0 kHz	-	1.5	5.25	µA
		$V_{DD(P)}$ = 3.6 V to 5.5 V; f_{SCL} = 400 kHz	-	27	51	µA
		$V_{DD(P)}$ = 2.3 V to 3.6 V; f_{SCL} = 400 kHz	-	15	30	µA
		$V_{DD(P)}$ = 1.65 V to 2.3 V; f_{SCL} = 400 kHz	-	9.5	19	µA
		$V_{DD(P)}$ = 3.6 V to 5.5 V; f_{SCL} = 1 MHz	-	72	110	µA
		$V_{DD(P)}$ = 2.3 V to 3.6 V; f_{SCL} = 1 MHz	-	36	60	µA
		$V_{DD(P)}$ = 1.65 V to 2.3 V; f_{SCL} = 1 MHz	-	22	40	µA
		Active mode; $I_{DD(I2C\text{-}bus)}$ + $I_{DD(P)}$; P port, ADDR, $\overline{RESET}$; V_I on ADDR, $\overline{RESET}$ = $V_{DD(I2C\text{-}bus)}$; V_I on P port = $V_{DD(P)}$; I_O = 0 mA; I/O = inputs; continuous register read				
		$V_{DD(P)}$ = 3.6 V to 5.5 V; f_{SCL} = 400 kHz	-	150	250	µA
		$V_{DD(P)}$ = 2.3 V to 3.6 V; f_{SCL} = 400 kHz	-	120	200	µA
		$V_{DD(P)}$ = 1.65 V to 2.3 V; f_{SCL} = 400 kHz	-	75	150	µA
		$V_{DD(P)}$ = 3.6 V to 5.5 V; f_{SCL} = 1 MHz	-	450	625	µA
		$V_{DD(P)}$ = 2.3 V to 3.6 V; f_{SCL} = 1 MHz	-	270	500	µA
		$V_{DD(P)}$ = 1.65 V to 2.3 V; f_{SCL} = 1 MHz	-	160	210	µA
		with pull-ups enabled; $I_{DD(I2C\text{-}bus)}$ + $I_{DD(P)}$; P port, ADDR, $\overline{RESET}$; V_I on ADDR, SCL, SDA and $\overline{RESET}$ = $V_{DD(I2C\text{-}bus)}$ or V_{SS}; V_I on P port = V_{SS}; I_O = 0 mA; I/O = inputs with pull-up enabled; f_{SCL} = 0 kHz				
		$V_{DD(P)}$ = 1.65 V to 5.5 V	-	1.7	3.3	mA
ΔI_{DD}	additional quiescent supply current[5]	ADDR, SCL, SDA, $\overline{RESET}$; one input at $V_{DD(I2C\text{-}bus)}$ − 0.6 V, other inputs at $V_{DD(I2C\text{-}bus)}$ or V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V	-	-	30	µA
		P port; one input at $V_{DD(P)}$ − 0.6 V, other inputs at $V_{DD(P)}$ or V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V	-	-	80	µA

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Table 94. Static characteristics *...continued*

T_{amb} = −40 °C to +85 °C; $V_{DD(I2C\text{-}bus)}$ = 0.8 V to 3.6 V; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
C_i	input capacitance[6]	$V_I = V_{DD(I2C\text{-}bus)}$ or V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V	-	6	-	pF
C_{io}	input/output capacitance[6]	$V_{I/O} = V_{DD(I2C\text{-}bus)}$ or V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V	-	7	-	pF
		$V_{I/O} = V_{DD(P)}$ or V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V	-	7.5	-	pF
$R_{pu(int)}$	internal pull-up resistance	input/output	50	100	150	kΩ
$R_{pd(int)}$	internal pull-down resistance	input/output	50	100	150	kΩ

[1] For I_{DD}, all typical values are at nominal supply voltage (1.8 V, 2.5 V, 3.3 V or 3.6 V V_{DD}) and T_{amb} = 25 °C. Except for I_{DD}, the typical values are at $V_{DD(P)} = V_{DD(I2C\text{-}bus)}$ = 3.3 V and T_{amb} = 25 °C.

[2] The total current sourced by all I/Os must be limited to 160 mA.

[3] Each I/O must be externally limited to a maximum of 25 mA and each octal (P0_0 to P0_7 and P1_0 to P1_7) must be limited to a maximum current of 100 mA, for a device total of 500 mA.

[4] Typical value for T_{amb} = 25 °C. V_{OL} = 0.4 V and $V_{DD(I2C\text{-}bus)} = V_{DD(P)}$ = 3.3 V. Typical value for $V_{DD(I2C\text{-}bus)} = V_{DD(P)} < 2.5$ V, V_{OL} = 0.6 V.

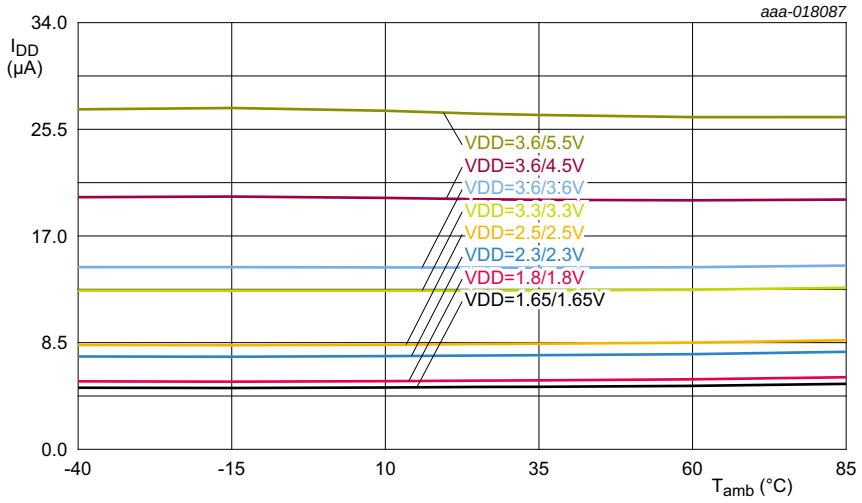
[5] Internal pull-up/pull-down resistors disabled.

[6] Value not tested in production, but guaranteed by design and characterization.

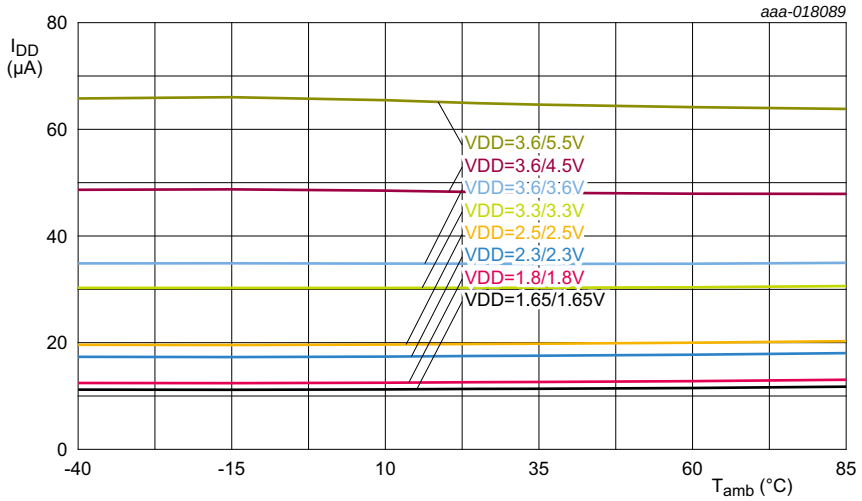
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12.1 Typical characteristics



a. SCL = 400 KHz



b. SCL = 1 MHz

Fig 26. Supply current vs ambient temperature

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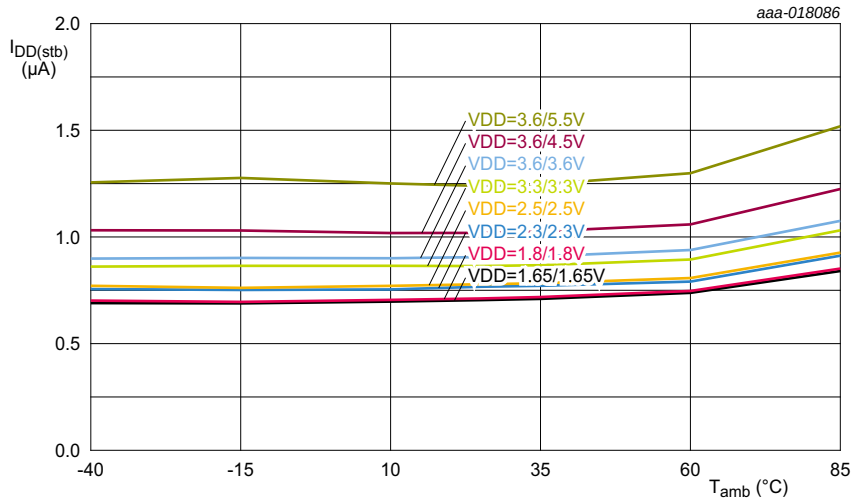
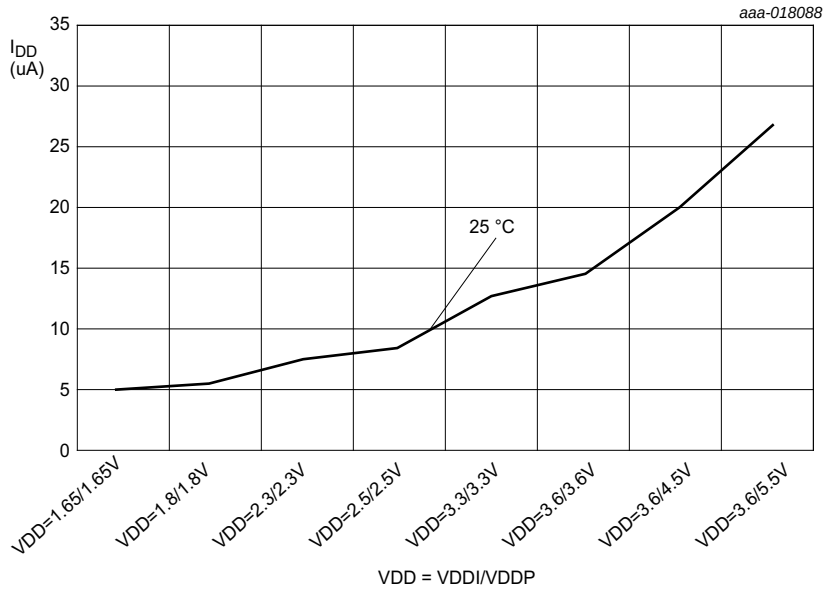


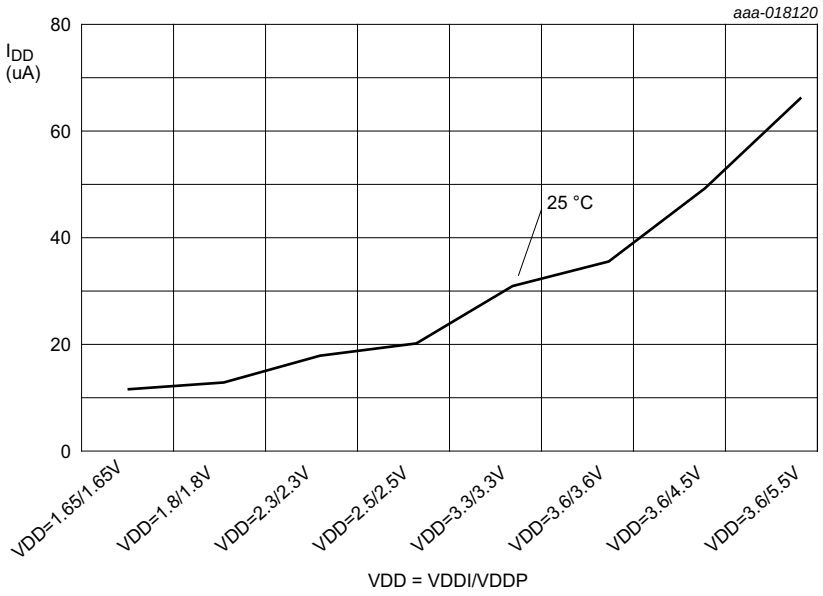
Fig 27. Standby supply current vs ambient temperature

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a. SCL = 400 KHz



b. SCL = 1 MHz

Fig 28. Supply current vs supply voltage

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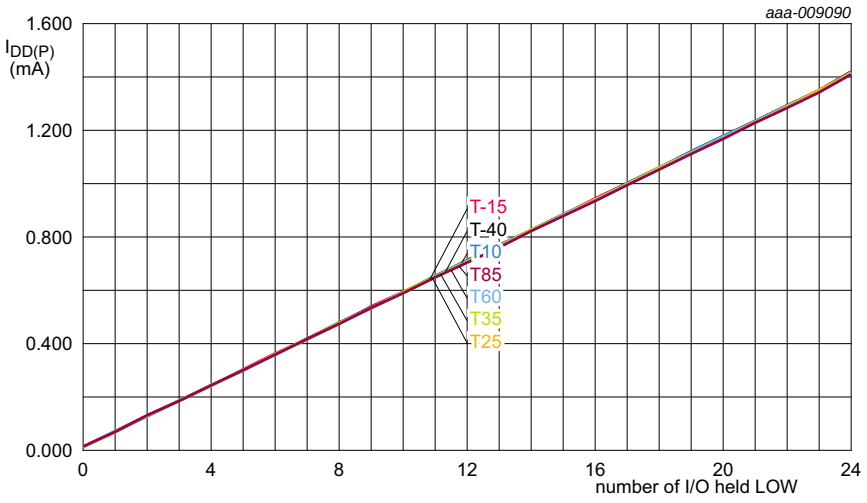


Fig 29. Supply current vs number of I/O held LOW

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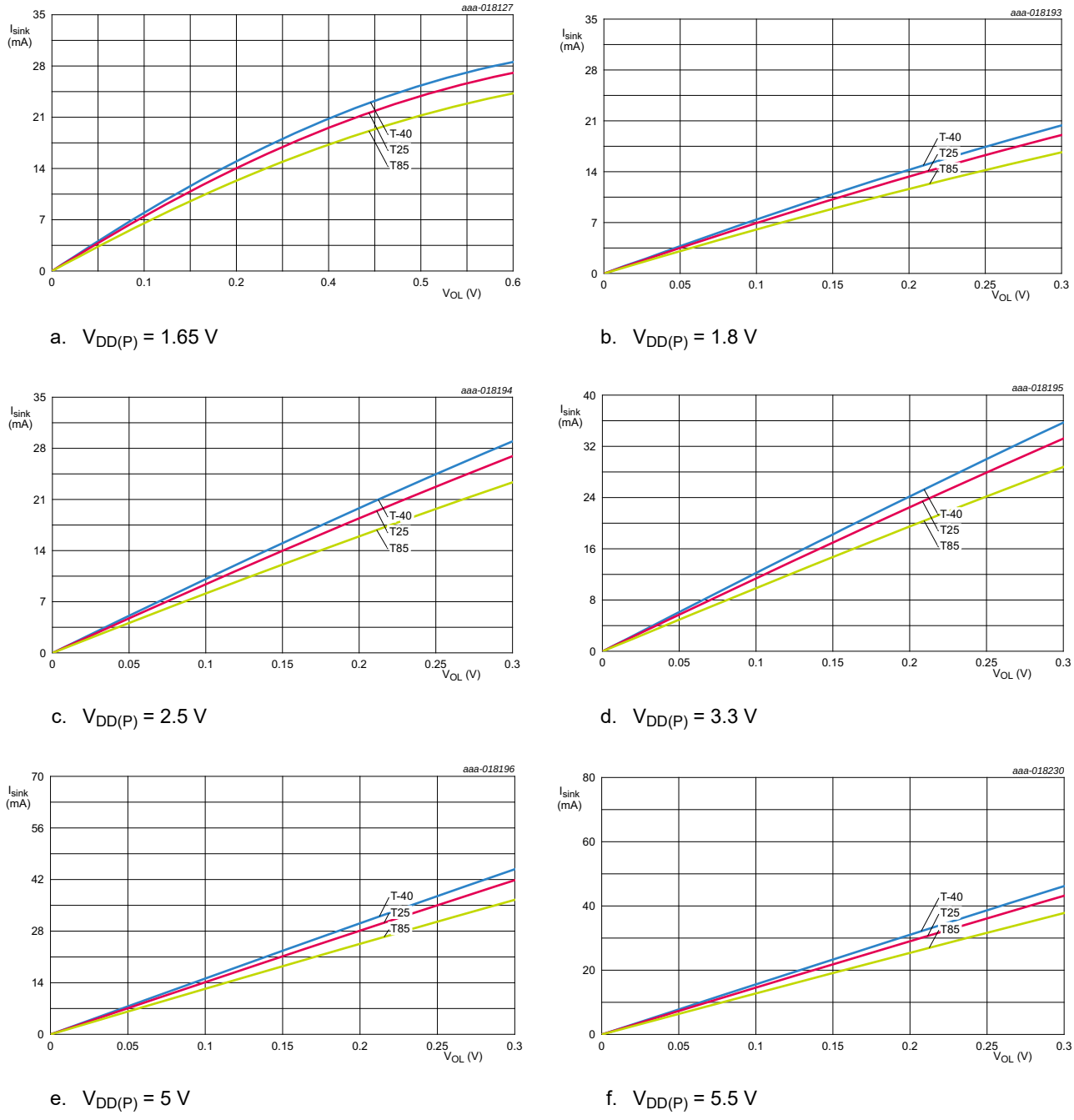


Fig 30. I/O sink current vs LOW-level output voltage

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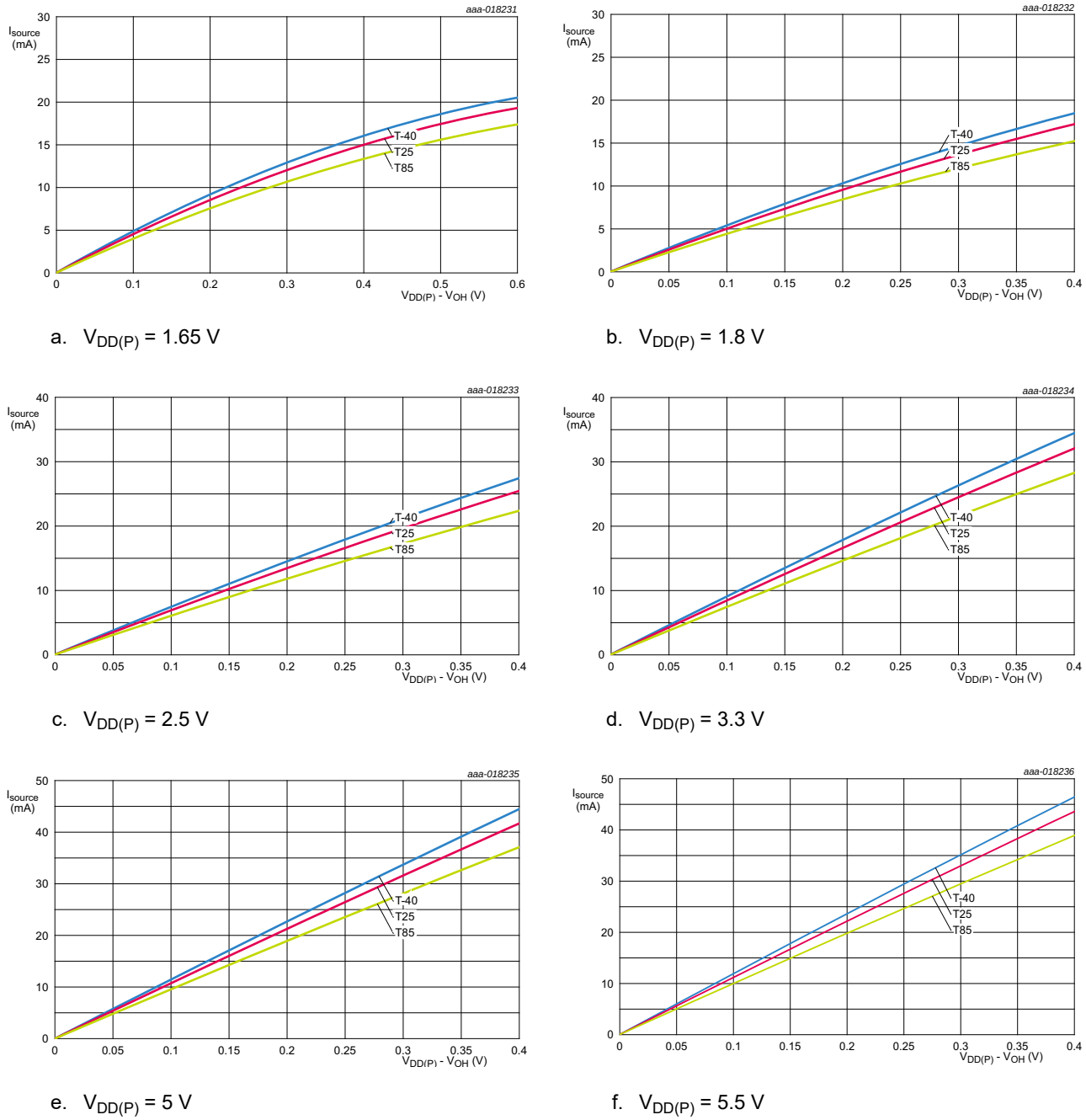


Fig 31. I/O source current vs HIGH-level output voltage

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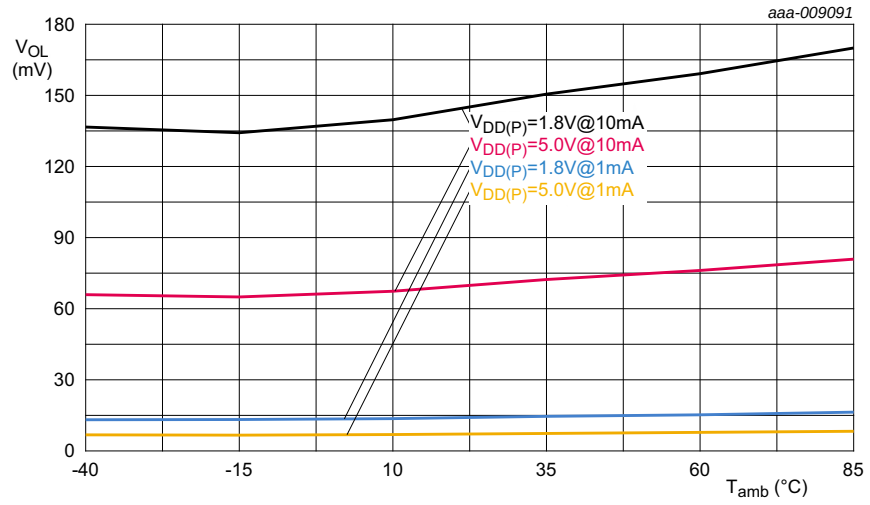


Fig 32. LOW-level output voltage vs temperature

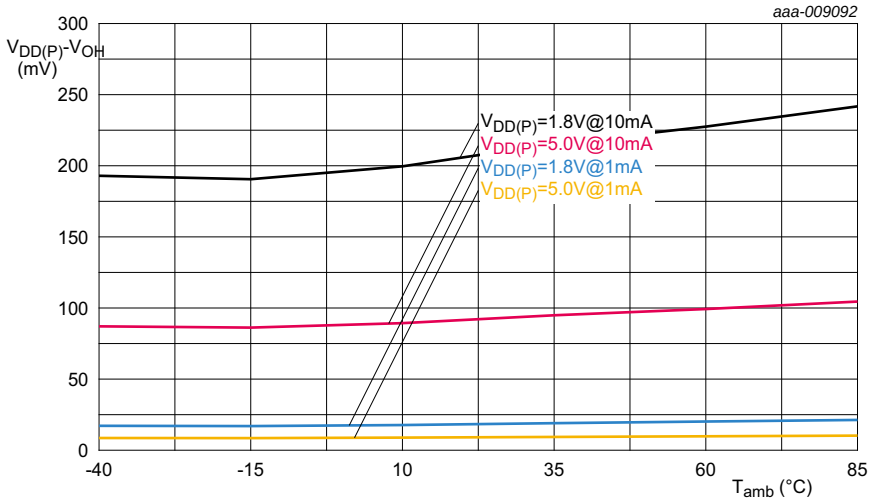


Fig 33. I/O high voltage vs temperature

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13. Dynamic characteristics

Table 95. I²C-bus interface timing requirements

Over recommended operating free air temperature range, unless otherwise specified. See Figure 35.

Symbol	Parameter	Conditions	Standard-mode I²C-bus		Fast-mode I²C-bus		Fast-mode Plus I²C-bus		Unit
			Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	0	1000	kHz
t_{HIGH}	HIGH period of the SCL clock		4	-	0.6	-	0.26	-	µs
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	0.5	-	µs
t_{SP}	pulse width of spikes that must be suppressed by the input filter		0	50	0	50	0	50	ns
$t_{SU;DAT}$	data set-up time		250	-	100	-	50	-	ns
$t_{HD;DAT}$	data hold time		0	-	0	-	0	-	ns
t_r	rise time of both SDA and SCL signals	[1]	-	1000	20	300	-	120	ns
t_f	fall time of both SDA and SCL signals	[1]	-	300	$20 \times (V_{DD} / 5.5\ V)$	300	-	120	ns
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	0.5	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	0.26	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		4	-	0.6	-	0.26	-	µs
$t_{SU;STO}$	set-up time for STOP condition		4	-	0.6	-	0.26	-	µs
$t_{VD;DAT}$	data valid time	SCL LOW to SDA output valid	-	3.45	-	0.9	-	0.45	µs
$t_{VD;ACK}$	data valid acknowledge time	ACK signal from SCL LOW to SDA (out) LOW	-	3.45	-	0.9	-	0.45	µs

[1] Value not tested in production, but guaranteed by design and characterization.

Table 96. Reset timing requirements

Over recommended operating free air temperature range, unless otherwise specified. See Figure 37.

Symbol	Parameter	Conditions	Standard-mode I²C-bus		Fast-mode I²C-bus		Fast-mode Plus I²C-bus		Unit
			Min	Max	Min	Max	Min	Max	
$t_{w(rst)}$	reset pulse width		150	-	150	-	150	-	ns
$t_{rec(rst)}$	reset recovery time		500	-	500	-	500	-	ns
t_{rst}	reset time	[1]	600	-	600	-	600	-	ns

[1] Minimum time for SDA to become HIGH or minimum time to wait before doing a START.

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Table 97. Switching characteristics

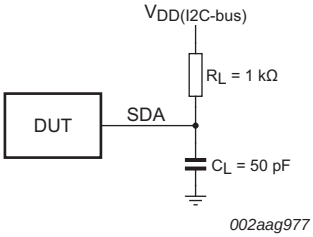
Over recommended operating free air temperature range; $C_L \leq 100$ pF; unless otherwise specified. See Figure 36.

Symbol	Parameter	Conditions	Standard-mode I²C-bus		Fast-mode I²C-bus		Fast-mode Plus I²C-bus		Unit
			Min	Max	Min	Max	Min	Max	
$t_{v(INT)}$	valid time on pin $\overline{INT}$	from P port to $\overline{INT}$	-	1	-	1	-	1	µs
$t_{rst(INT)}$	reset time on pin $\overline{INT}$	from SCL to $\overline{INT}$	-	1	-	1	-	1	µs
$t_{v(Q)}$	data output valid time	from SCL to P port	-	400	-	400	-	400	ns
$t_{su(D)}$	data input set-up time	from P port to SCL	0	-	0	-	0	-	ns
$t_{h(D)}$	data input hold time	from P port to SCL	300	-	300	-	300	-	ns

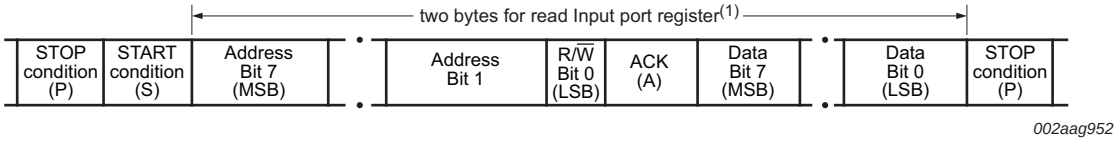
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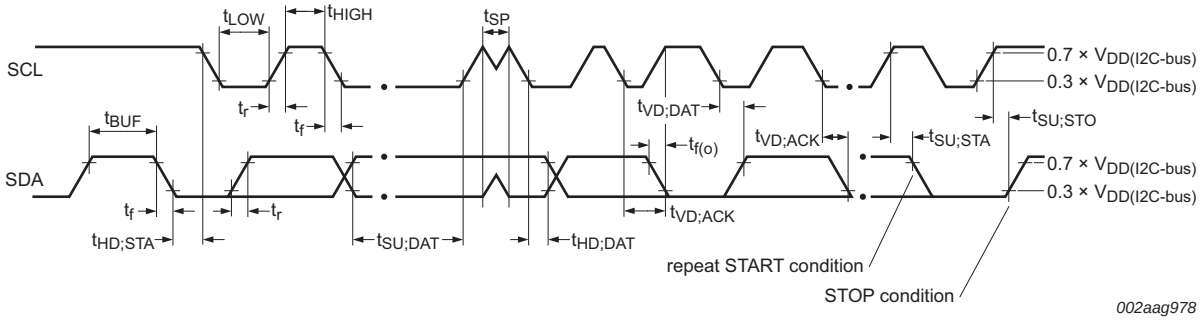
14. Parameter measurement information



a. SDA load configuration



b. Transaction format



c. Voltage waveforms

C_L includes probe and jig capacitance.

All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r/t_f ≤ 30 ns.

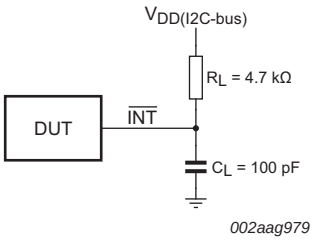
All parameters and waveforms are not applicable to all devices.

Byte 1 = I²C-bus address; Byte 2, byte 3 = P port data.

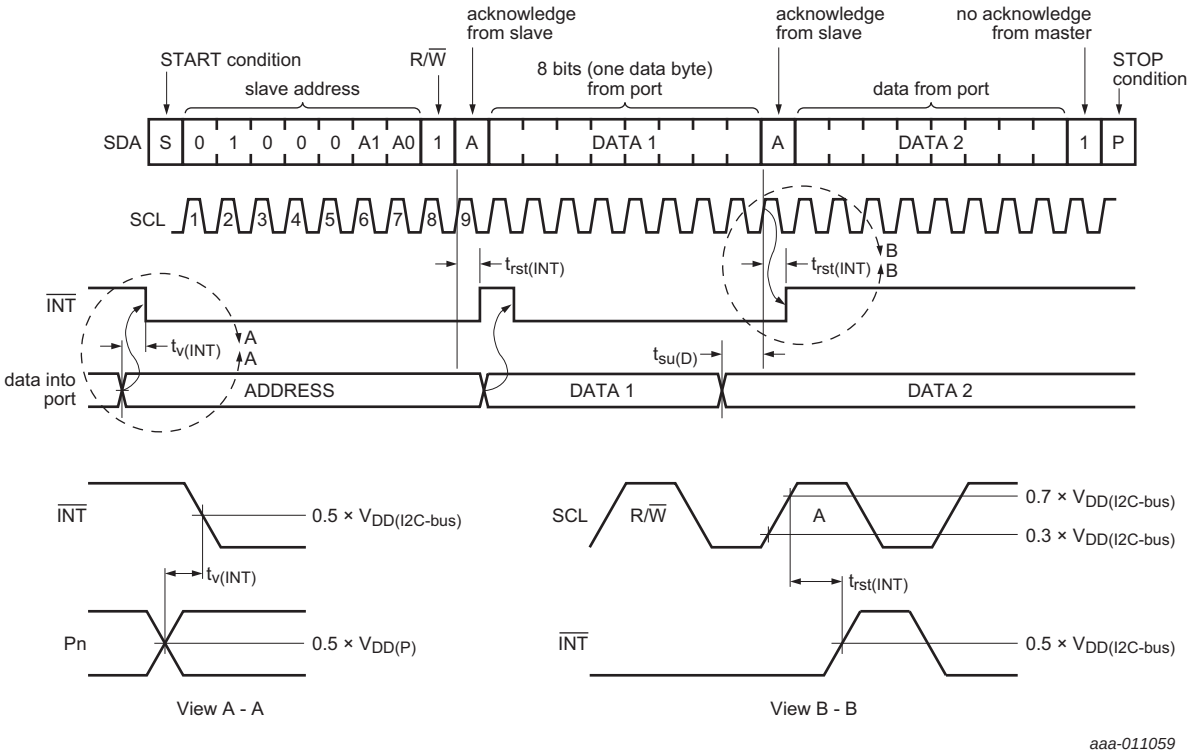
Fig 34. I²C-bus interface load circuit and voltage waveforms

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a. Interrupt load configuration



b. Voltage waveforms

C_L includes probe and jig capacitance.

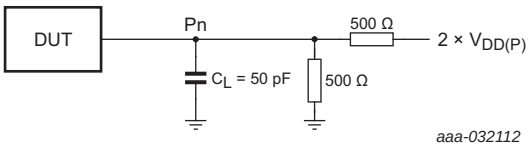
All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r/t_f ≤ 30 ns.

All parameters and waveforms are not applicable to all devices.

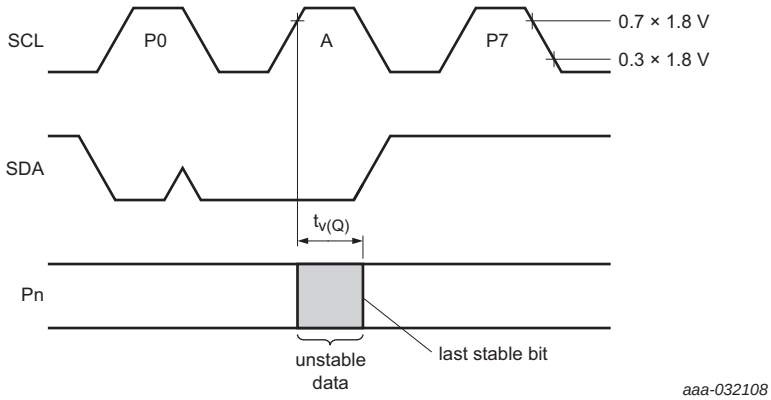
Fig 35. Interrupt load circuit and voltage waveforms

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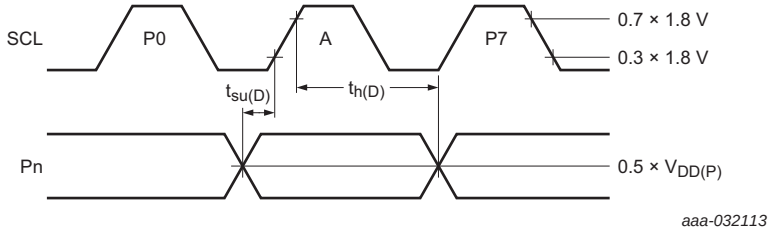
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a. P port load configuration



b. Write mode (R/$\overline{W}$ = 0)



c. Read mode (R/$\overline{W}$ = 1)

C_L includes probe and jig capacitance.

$t_{v(Q)}$ is measured from 0.7 × $V_{DD(I2C\text{-}bus)}$ on SCL to 50 % I/O (Pn) output.

All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r/t_f ≤ 30 ns.

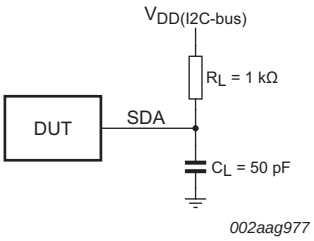
The outputs are measured one at a time, with one transition per measurement.

All parameters and waveforms are not applicable to all devices.

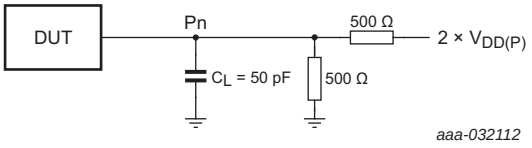
Fig 36. P port load circuit and voltage waveforms

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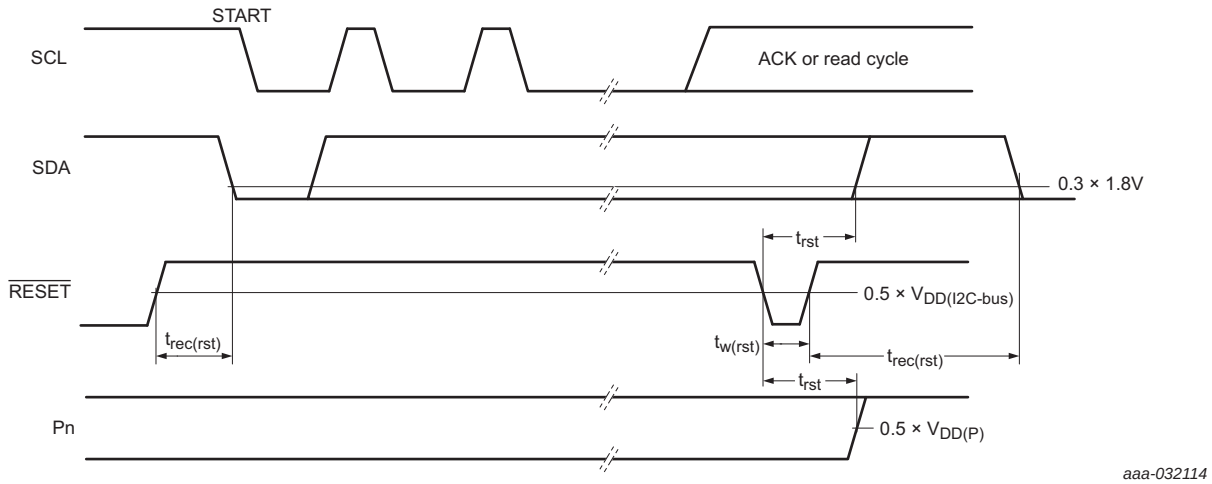
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a. SDA load configuration



b. P port load configuration



c. $\overline{\text{RESET}}$ timing

C_L includes probe and jig capacitance.

All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r/t_f ≤ 30 ns.

The outputs are measured one at a time, with one transition per measurement.

I/Os are configured as inputs.

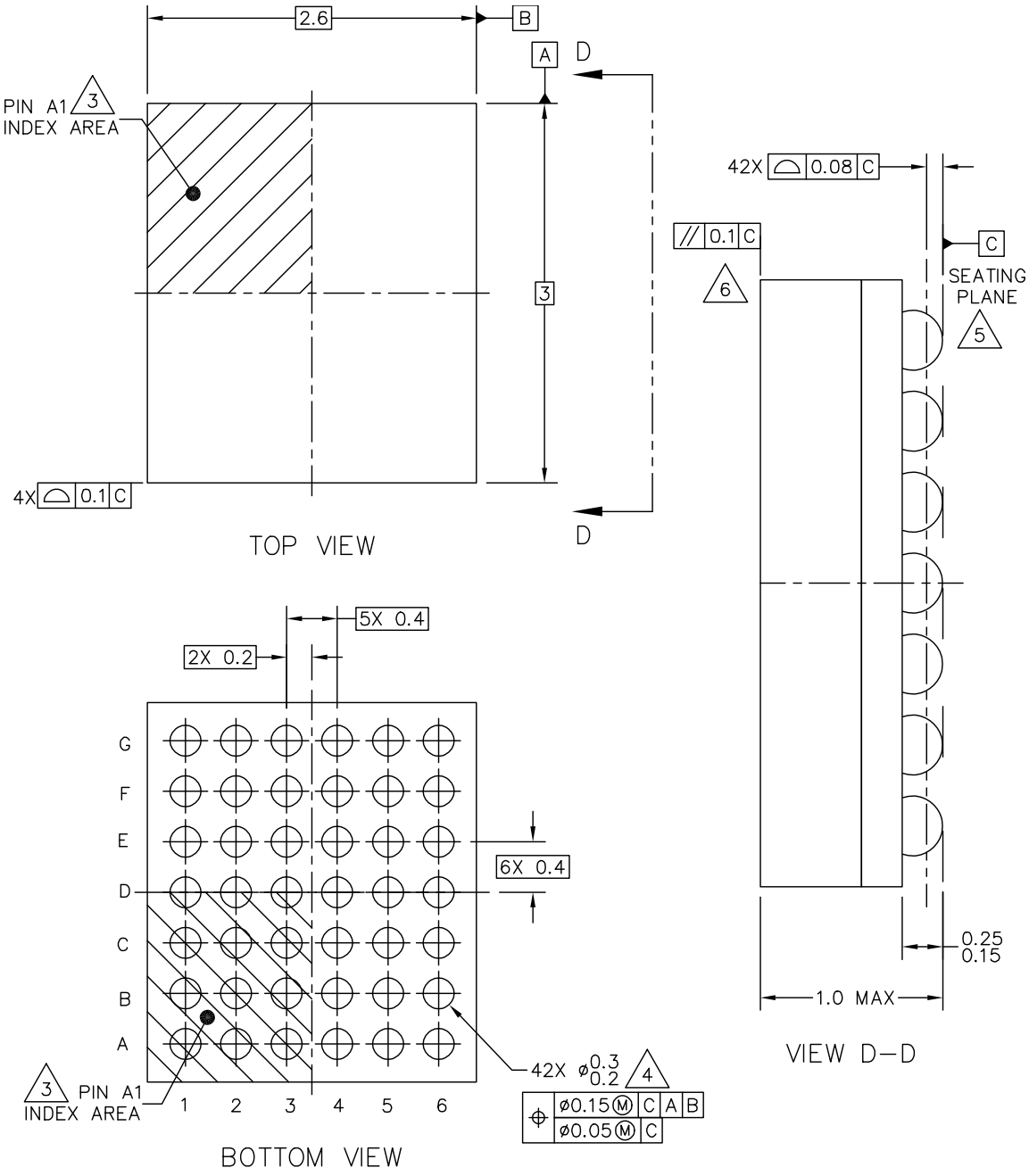
All parameters and waveforms are not applicable to all devices.

Fig 37. Reset load circuits and voltage waveforms

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15. Package outline



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MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: SOT1963–1	REVISION: 0	

Fig 38. Package outline SOT1963-1 (VFBGA42)

16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

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16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 39) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 98 and 99

Table 98. SnPb eutectic process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 99. Lead-free process (from J-STD-020D)

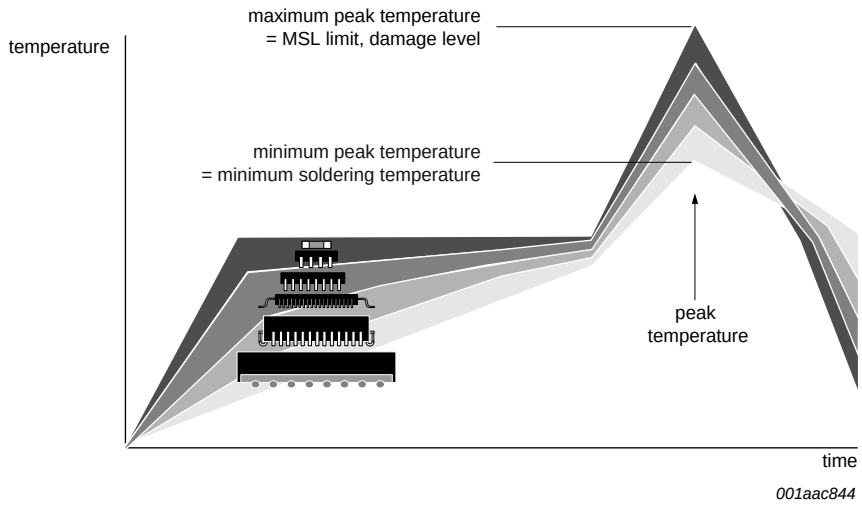
Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 39.

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MSL: Moisture Sensitivity Level

Fig 39. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

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17. Soldering: PCB footprints

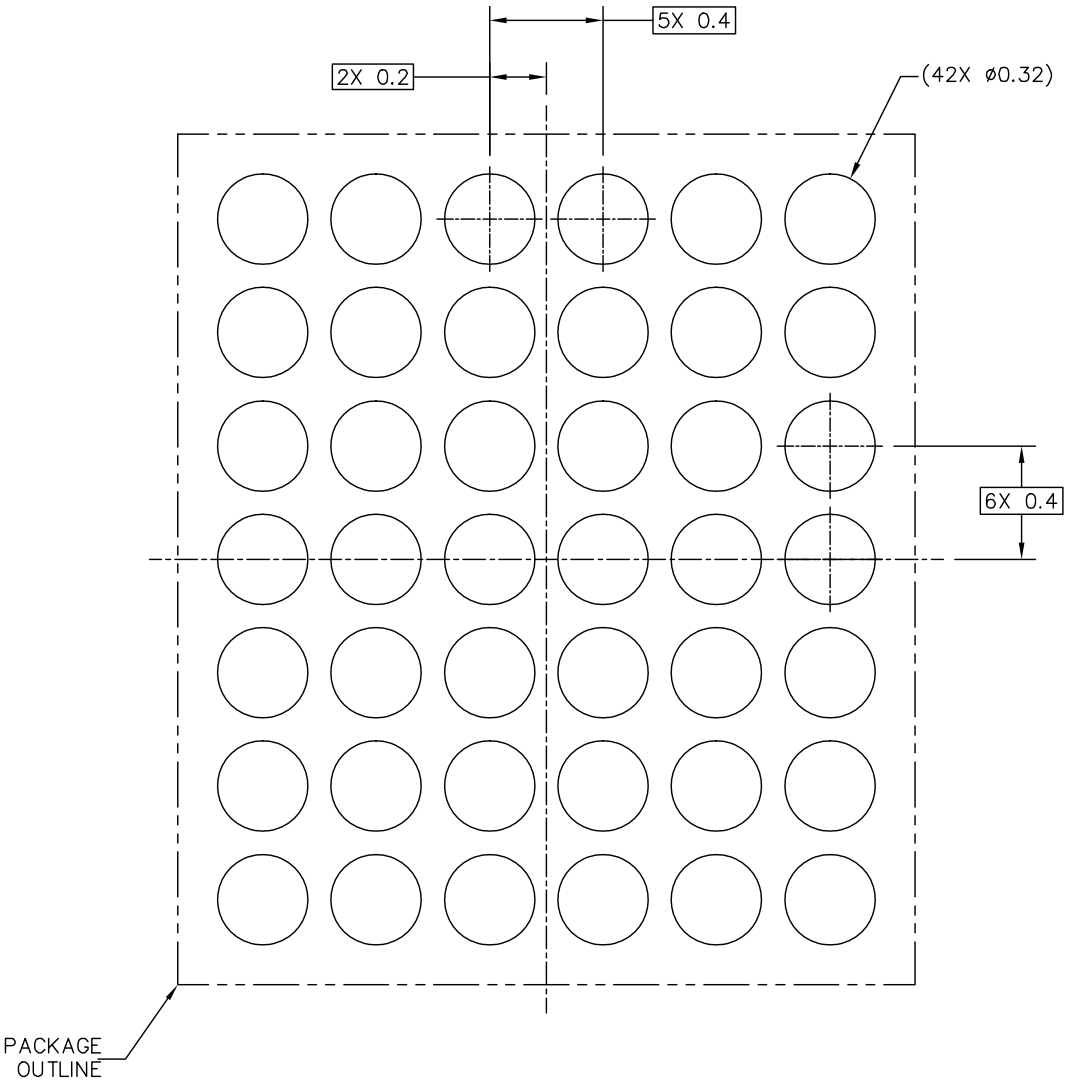
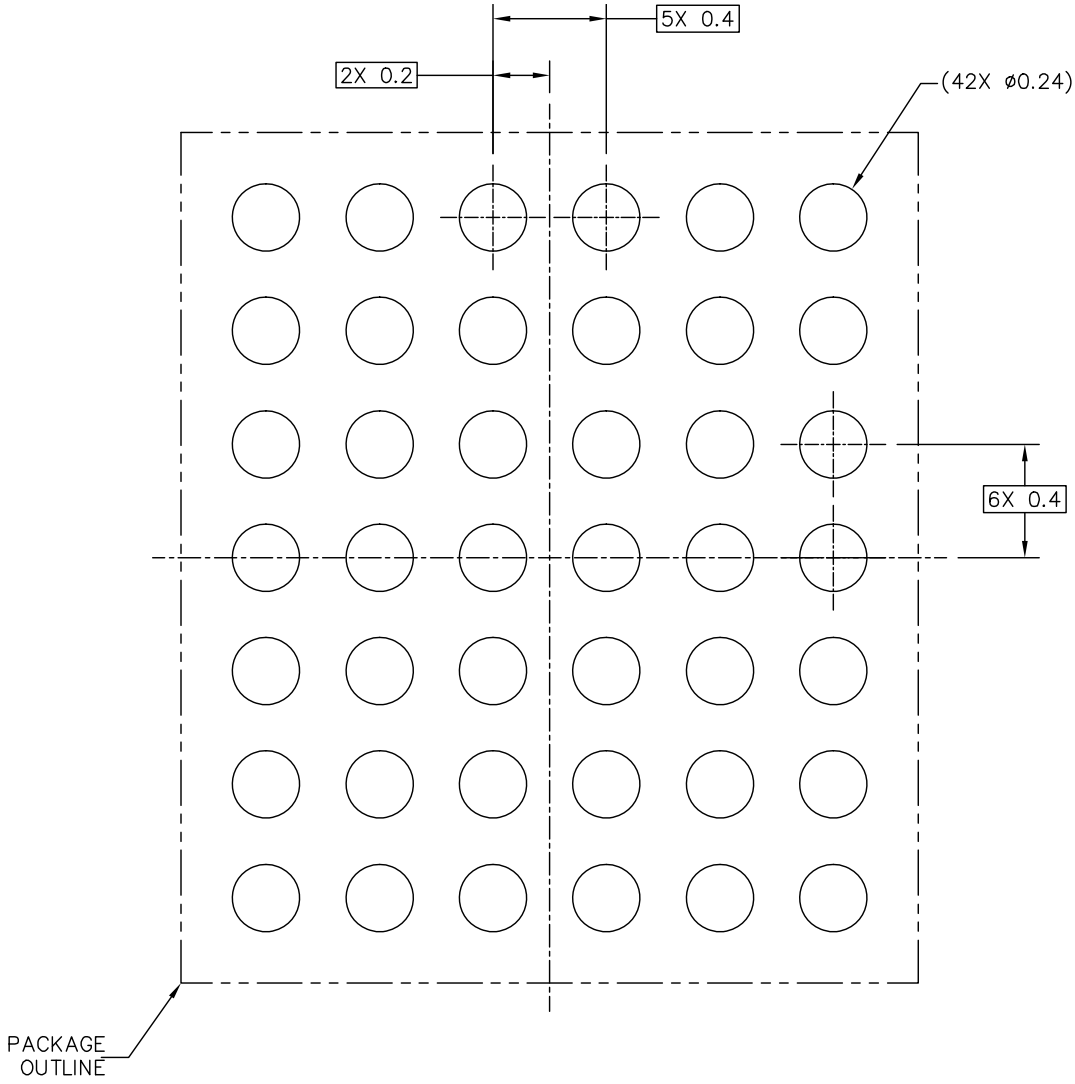


Fig 40. PCB footprint for SOT1963-1 (VFBGA42); reflow soldering (1 of 3)

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PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: SOT1963–1	REVISION: 0	

Fig 41. PCB footprint for SOT1963-1 (VFBGA42); reflow soldering (2 of 3)

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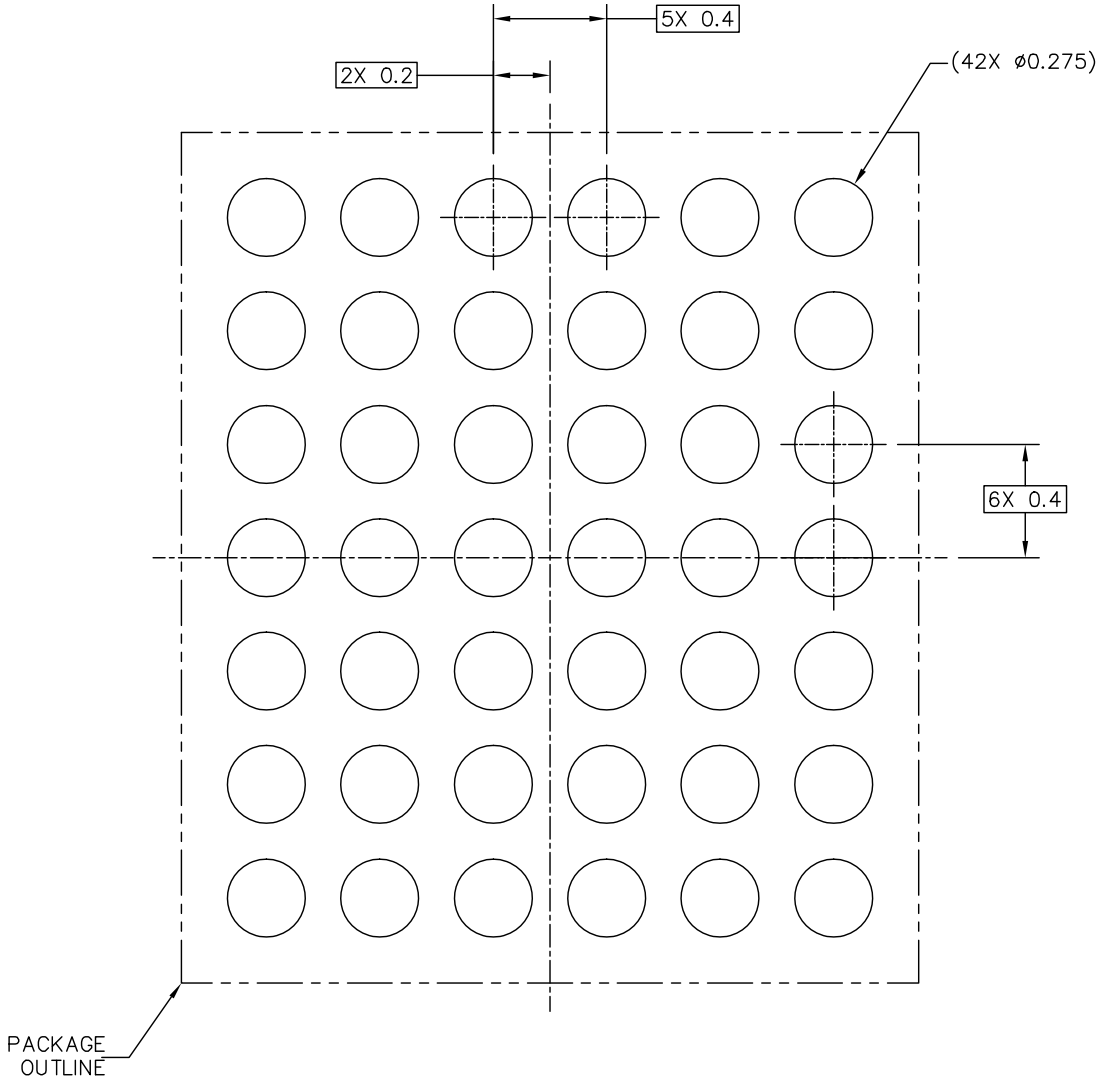


Fig 42. PCB footprint for SOT1963-1 (VFBGA42); reflow soldering (3 of 3)

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18. Abbreviations

Table 100. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
GPIO	General Purpose Input/Output
I^2C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
LED	Light-Emitting Diode
LSB	Least Significant Bit
MSB	Most Significant Bit
NACK	Not ACKnowledge
PCB	Printed-Circuit Board
POR	Power-On Reset
PRR	Pulse Repetition Rate
SMBus	System Management Bus

19. Revision history

Table 101. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCAL6534 v.1	20190111	Product data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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