PCA9922

8-channel constant current LED driver with output error detection

Rev. 2 — 6 April 2011 Product data sheet

1. General description

The PCA9922 is an 8-channel constant current LED driver designed for LED signage and display applications. The output current is adjustable from 15 mA to 60 mA controlled by an external series resistor. The outputs are controlled via a serial interface with a maximum clock frequency of 25 MHz to allow for the system requirement of high volume data transmission. Each of the 8 channel outputs has edge rate control to limit the change in current when the outputs are enabled or disabled.

The device has built-in circuitry for detecting LED open-circuit and output short to ground. After signaling the specified error detect sequence on the input control lines, error status can be read out of the device via the serial data out.

The device is designed such that it may be cascaded with other similar devices. The SDO pin contains the output of the shift register which may be used for cascading to the SDI pin of the next device in the series. SDO changes state on the falling edge of CLK. SDI captures data on the rising edge of CLK.

The PCA9922 is a pin-to-pin functionally equivalent 5 V alternative (exception: **error data is inverted**; see Section 7.2.1, Section 7.2.2 and Section 7.2.7) for the ST2221A and STP08CDC596.

The PCA9922 is available in DIP16, TSSOP16 and HVQFN20 packages and is specified over the −40 °C to +85 °C industrial temperature range.

2. Features and benefits

- 25 MHz serial interface
- 3.3 V to 5.5 V operation
- 8 LED low side constant current outputs
- Global control for the 8 LED outputs variable between 15 mA to 60 mA
- 15 mA to 60 mA maximum current for all 8 output channels set by an external resistor
- Constant current matching at 25 °C, V_{DD} = 5.0 V
- Bit-to-bit: ±6 %
- Chip-to-chip: ±10 %
- Gradual turn-on/turn-off output to limit EMI
- Error detection mode for line open, output short to ground, LED open and LED short
- −40 °C to +85 °C operation
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA

- Packages offered: DIP16, TSSOP16, HVQFN20

3. Applications

- Full color, multi-color, monochrome LED signs
- LED billboard displays
- Traffic display signs
- Transportation and commercial LED signs

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCA9922N	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
PCA9922PW	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
PCA9922BS	HVQFN20	plastic thermal enhanced very thin quad flat package; no leads; 20 terminals; body 5 × 5 × 0.85 mm	SOT662-1

4.1 Ordering options

Table 2. Ordering options

Type number	Topside mark	Temperature range
PCA9922N	PCA9922N	T_{amb} = −40 °C to +85 °C
PCA9922PW	PCA9922	T_{amb} = −40 °C to +85 °C
PCA9922BS	P9922	T_{amb} = −40 °C to +85 °C

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5. Block diagram

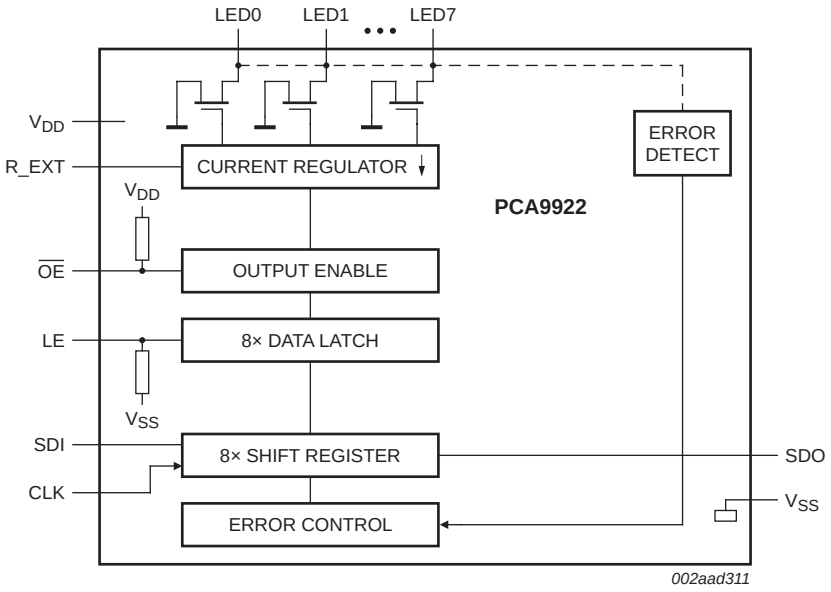


Fig 1. Block diagram of PCA9922

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6. Pinning information

6.1 Pinning

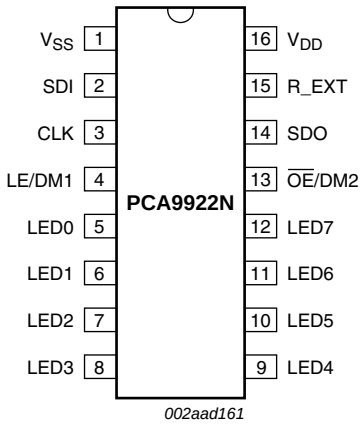


Fig 2. Pin configuration for DIP16

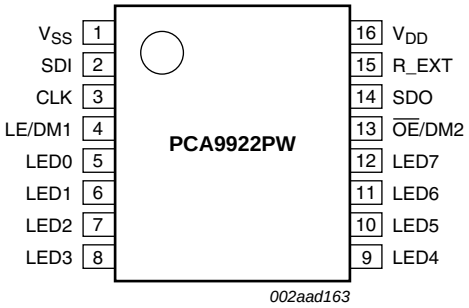


Fig 3. Pin configuration for TSSOP16

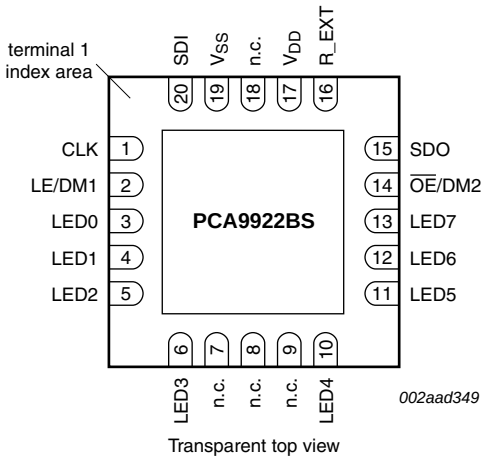


Fig 4. Pin configuration for HVQFN20

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6.2 Pin description

Table 3. Pin description

I = input; O = output.

Symbol	Pin		Type	Description
	DIP16, TSSOP16	HVQFN20		
V_{SS}	1	19[1]	power supply	supply ground
SDI	2	20	I	serial data in
CLK	3	1	I	serial data clock used to shift data on SDI into the shift register
LE/DM1	4	2	I	latch enable with internal pull-down resistor; active HIGH signal used to capture data in the shift register to present to the outputs Detection Mode 1
LED0	5	3	O	constant current LED output driver 0
LED1	6	4	O	constant current LED output driver 1
LED2	7	5	O	constant current LED output driver 2
LED3	8	6	O	constant current LED output driver 3
LED4	9	10	O	constant current LED output driver 4
LED5	10	11	O	constant current LED output driver 5
LED6	11	12	O	constant current LED output driver 6
LED7	12	13	O	constant current LED output driver 7
$\overline{OE}$/DM2	13	14	I	output enable with internal pull-up resistor; active LOW signal used to allow data captured in the latch to be presented to the constant current outputs Detection Mode 2
SDO	14	15	O	serial data output
R_EXT	15	16	analog input	external resistor input
V_{DD}	16	17	power supply	supply voltage
n.c.	-	7, 8, 9, 18	-	not connected

[1] HVQFN20 package die supply ground is connected to both V_{SS} pin and exposed center pad. V_{SS} pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the PCB in the thermal pad region.

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7. Functional description

The PCA9922 is an 8-channel constant current LED driver with built-in LED output error detection. The PCA9922 contains an 8-bit shift register and data latches, which convert serial input data into parallel output data.

At the output stage, 8 regulated current sinks are designed to provide constant and uniform current through LEDs with different forward voltages (V_F).

Refer to Figure 1 “Block diagram of PCA9922”.

7.1 System interface

During normal operation, serial data can be transferred into the PCA9922 through SDI, shifted into the shift register, and out through the SDO. Data shifts from the SDI pin into the next sequential bit in the shift register on each rising edge of the CLK input. The MSB is the first bit to be clocked in. Data shifts out of the shift register and is presented on the SDO pin on the falling edge of CLK. The exception to this is during the error detect sequence, at which time the error status is loaded in a parallel fashion into the shift register. The shift register is never disabled. It is either shifting or it is loading the error status on every rising edge of CLK. Additionally, the device is designed such that it may be cascaded with other similar devices. The SDO pin contains the output of the shift register which may be used for cascading to the SDI pin of the next device in the series.

Data is parallel loaded from the serial shift register to an output control register when LE (Latch Enable) is asserted HIGH (serial-to-parallel conversion). The output control register will continue to reflect the shift register data, even if changes occur in the shift register data, as long as LE is HIGH. When LE is LOW the latch is closed and changes in the shift register data no longer effect the output control register. Applications where the latches are bypassed (LE tied HIGH) will require that the $\overline{OE}$ input be HIGH during serial data entry.

The data in the output control register is then used to drive the constant current output drivers when the outputs are enabled. The outputs are globally enabled or disabled through the $\overline{OE}$. A LOW level on the $\overline{OE}$ will enable the output drivers, LED0 to LED7, to reflect the data contained in the output control register.

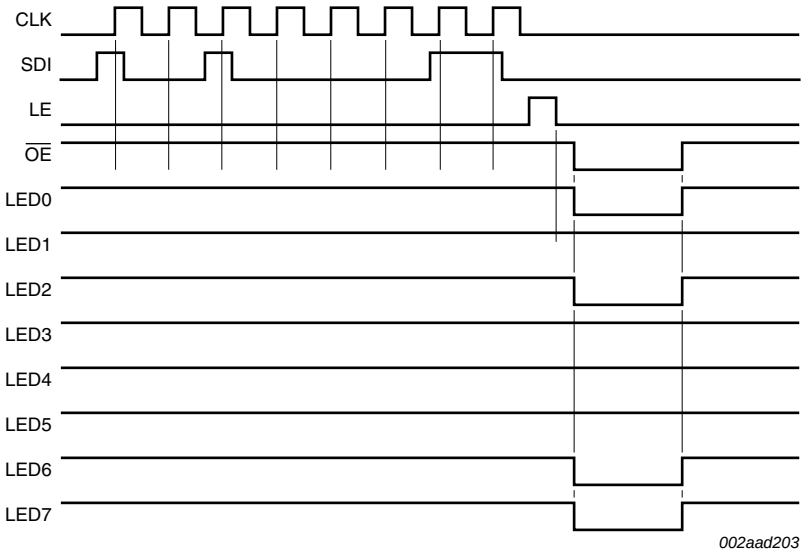
An example timing diagram of expected normal operation of the device is shown in Figure 5.

Remark: It is recommended that $\overline{OE}$ and LE pulse widths be at least two clocks wide when CLK is running to avoid inadvertent entry into the error detect modes.

There is no synchronization logic in the design between CLK, LE and $\overline{OE}$. It is the user’s responsibility to meet the timing presented in Table 10 in order to guarantee proper operation.

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For each LEDn 0 is on, 1 is off.

Fig 5. Normal function timing diagram

7.2 LED output error detection

The PCA9922 has built-in circuitry for detecting LED open-circuit and output short conditions. A predefined set of signal sequence on the input control lines must be initiated to perform the output error detection. Once the error data is captured by this sequence, error status can be read out of the device via the serial interface.

The error detection mode is entered by the user via specific timing sequences presented on the CLK, $\overline{OE}$ and LE pins. There are three key sequences to be generated by the user: enter error detect, capture faults, and exit error detect. It is the responsibility of the user to enable all outputs that the user wants to test during the error detect sequence.

Performing an error mode detection sequence consists of several operations:

1. Entering error detect mode.
2. Setting all bits that you want to test by enabling all outputs to logical 1s in the output latch.
3. Capture fault data.
4. Exit error detect.

7.2.1 Open-circuit detection principle

The LED open-circuit detection compares the effective current level I_O with the open load detection threshold current $I_{th(det)}$. If I_O is below $I_{th(det)}$, the PCA9922 detects an open-load condition. This error status can be read as an error status code in the error detect mode. For open-circuit error detection, a channel must be on.

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Table 4. Open-circuit detection

State of output port	Condition of output current	Error status code	Meaning
off	I_O = 0 mA	0	detection not possible
on	$I_O < I_{th(det)}$[1]	1	open circuit
	$I_O \geq I_{th(det)}$[1]	channel n error status bit 0	normal

[1] $I_{th(det)} = 0.5 \times I_O$ (target) (typical).

7.2.2 Short-circuit detection principle

The LED short-circuit detection compares the effective voltage level (V_O) with the shorted-load detection threshold voltages $V_{th(det)sc}$ and $V_{th(norm)}$. If V_O is above the $V_{th(det)sc}$ threshold, the PCA9922 detects a shorted-load condition. If V_O is below the $V_{th(norm)}$ threshold, no error is detected or error bit is reset. This error status can be read as an error status code in the Special mode. For short-circuit error detection, a channel must be on.

Table 5. Shorted-load detection

State of output port	Condition of output voltage	Error status code	Meaning
off	I_O = 0 mA	0	detection not possible
on	$V_O \geq V_{th(det)sc}$	1	short circuit
	$V_O < V_{th(norm)}$	channel n error status bit 0	normal

7.2.3 Entering error detect mode

Entering the error detect mode consists of a 5-clock sequence involving CLK, $\overline{OE}$ and LE as shown in Figure 6. The user must meet the set-up and hold times for $\overline{OE}$ and LE as detailed inTable 10 to guarantee proper operation of the error detect circuitry. It should be noted that the act of driving LE HIGH around the rising edge of clock 4 opens the latch in the current control register block and data captured in the shift register at that point in time is moved into the output control register. It should also be noted that the output logic was enabled for a brief period of time while $\overline{OE}$ is LOW around the rising edge of clock 2. The outputs LED[7:0] will glitch during this period.

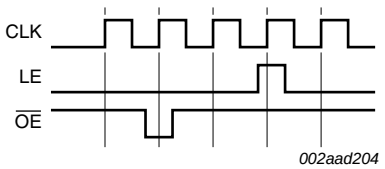


Fig 6. Timing for ‘Enter Error Detect Mode’ command

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7.2.4 Setting the outputs to test

Before the Capture Fault sequence may be performed, the outputs must be set up. A logic HIGH must be sent to the output control register for all eight bits. This is done after the Enter Error Detect sequence is performed as a normal data load sequence as seen in Figure 5. Please note that this process is completely destructive to the data that is stored in the output control register (and the LED[7:0] pins). The output control register will have to be restored to its proper values by the user after the error detect sequence has been completed.

7.2.5 Capturing the fault/output error data

The Capture Fault/Error Data sequence can only follow the Enter Error Detect sequence. If the Error Detect sequence has not occurred, this sequence will be treated as a normal operational sequence. Once the Capture Fault sequence has occurred, an Exit Error Detect sequence should be performed. There can be no more Capture Sequences until another Enter Error Detect sequence has occurred.

The Capture Fault Sequence consists of holding $\overline{OE}$ LOW for no less than 3 clocks (CLK) and for a minimum of 2 μs, whichever is longer. During this period of time, the shift register is being loaded with the fault status. As such, data presented to the device via SDI will not be captured. Bit 7 of the fault data will be present on SDO by the first falling edge CLK after the user de-asserts $\overline{OE}$ for this cycle. An error condition is output as a 1 (HIGH bit), and a 0 (LOW bit) designates a normal status. Timing for this sequence is shown in Figure 7.

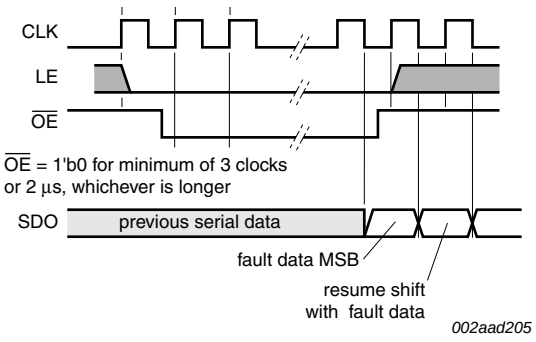


Fig 7. Timing for 'Capture Fault Mode' command

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7.2.6 Exit error detect mode

The ‘Exit error detect mode’ sequence is used to exit the error detect mode of operation and resume normal mode. This is a 5-clock timing sequence using CLK, $\overline{OE}$ and LE. This sequence consists of LE being held inactive for all five clocks. $\overline{OE}$ is active in the second clock for one and only one clock. Figure 8 shows the timing for this sequence.

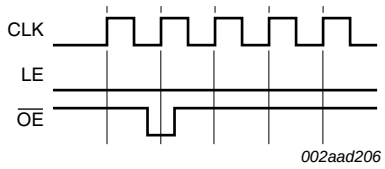


Fig 8. Timing for ‘Exit Error Detect Mode’ command

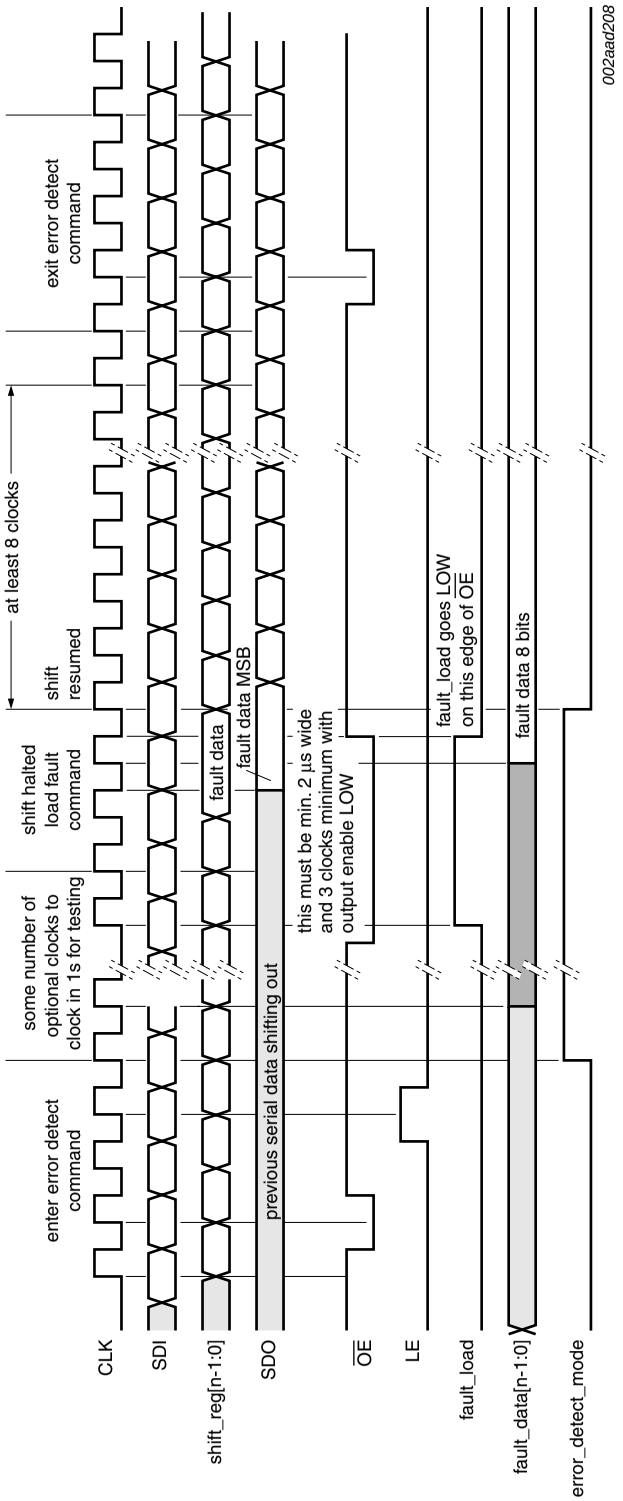
7.2.7 Error detection data

The PCA9922 will return a logical 1 for each output pin that has an error condition detected as described in Table 4 and Table 5. An error condition may be either an open circuit or short-circuit at the output pin. Once the Capture Fault sequence has completed, the resultant fault/output error data may be shifted out of the device by issuing 8 clocks and reading the data at the SDO pin. If more than one device is connected in series, then more than 8 clocks will be needed to shift all of the data from all of the devices through to the last SDO pin in the chain.

Figure 9 shows a complete error detection sequence.

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Lower-case signal names are internal signals shown to aid understanding of timing.

Fig 9. Timing for a complete error detection sequence

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8. Application design-in information

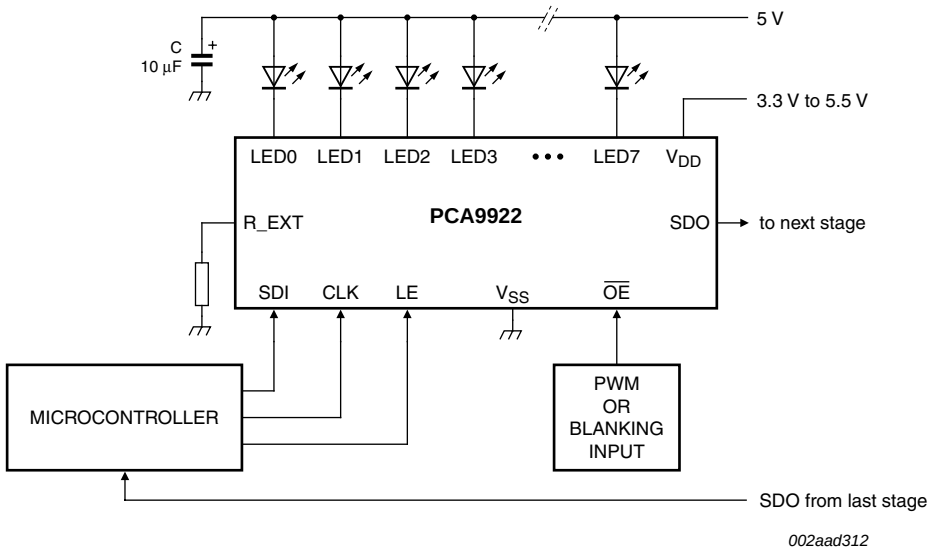


Fig 10. Typical application

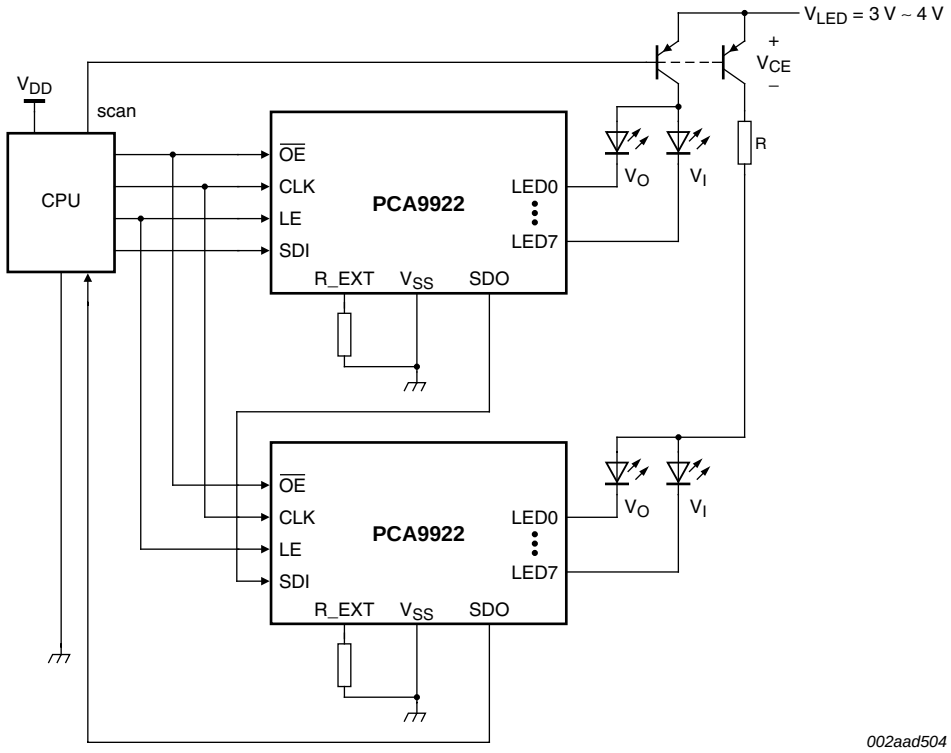


Fig 11. The PCA9922 in a typical multi-device architecture

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9. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+6.0	V
$V_{O(LED)}$	LED output voltage	pins LED0 to LED7	–0.5	+6.0	V
$V_{O(SDO)}$	output voltage on pin SDO		–0.5	+6.0	V
V_I	input voltage		–0.4	V_{DD} + 0.4	V
I_{SS}	ground supply current		-	485	mA
$I_{O(LEDn)}$	output current on pin LEDn		-	60	mA
f_{clk}	clock frequency	operating	-	25	MHz
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–40	+125	°C
P_{tot}	total power dissipation	T_{amb} = 25 °C			
		DIP16	-	1.12	W
		TSSOP16	-	0.625	W
		HVQFN20	-	3.125	W

10. Recommended operating conditions

Table 7. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		3.3	5.5	V
$V_{O(LED)}$	LED output voltage	pins LED0 to LED7			
		inactive	-	5.5	V
		output active	-	2.2	V
$I_{O(LEDn)}$	output current on pin LEDn		15	60	mA
$V_{O(SDO)}$	output voltage on pin SDO		-	5.5	V
P_{tot}	total power dissipation	T_{amb} = 85 °C			
		DIP16	-	0.44	W
		TSSOP16	-	0.25	W
		HVQFN20	-	1.25	W
T_{oper}	operating temperature		–40	+85	°C

11. Thermal characteristics

Table 8. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	DIP16	89	°C/W
		TSSOP16	160	°C/W
		HVQFN20	32	°C/W

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12. Static characteristics

Table 9. Static characteristics

V_{DD} = 5.0 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{th(det)sc}$	short-circuit detection threshold voltage	for short-error detection; I_O (target) = 5 mA to 120 mA		2.4	2.5	2.6	V
$V_{th(norm)}$	normal mode threshold voltage	for short-error detection; I_O (target) = 5 mA to 120 mA		2.3	-	-	V
Control interface ($\overline{OE}$, LE, CLK, SDI, SDO)							
V_{IH}	HIGH-level input voltage		[1]	$0.7V_{DD}$	-	V_{DD} + 0.3	V
V_{IL}	LOW-level input voltage			−0.3	-	$0.3V_{DD}$	V
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA		-	-	0.4	V
V_{OH}	HIGH-level output voltage	I_{OL} = −1 mA		V_{DD} − 0.4	-	-	V
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS} (CLK, SDI)		−1	-	+1	μA
C_i	input capacitance	$V_I = V_{DD}$ or 0 V		-	1.5	5	pF
R_{PU}	pull-up resistance	$\overline{OE}$ pin		150	300	600	kΩ
R_{pd}	pull-down resistance	LE pin		100	200	400	kΩ
Current controlled outputs (LED[7:0])							
I_{OL}	LOW-level output current	V_O = 0.7 V; R_{ext} = 910 Ω		17.5	19.5	21.7	mA
		V_O = 0.7 V; R_{ext} = 470 Ω		35.4	38.1	40.8	mA
ΔI_{OL}	LOW-level output current variation	between bits					
		V_O = 0.7 V; R_{ext} = 910 Ω		-	±3.0	±7	%
		V_O = 0.7 V; R_{ext} = 470 Ω		-	±1.5	±4	%
I_{DD}	supply current	R_{ext} = open; LED[7:0] = off		-	0.7	1.05	mA
		R_{ext} = 910 Ω; LED[7:0] = off		-	3.6	6.0	mA
		R_{ext} = 470 Ω; LED[7:0] = off		-	6.2	9.0	mA
		R_{ext} = 910 Ω; LED[7:0] = on		-	3.6	6.0	mA
		R_{ext} = 470 Ω; LED[7:0] = on		-	6.2	9.0	mA

[1] $\overline{OE}$ must be held active LOW for at least the duration of the rise/fall time of the LEDn pins. This pulse width does not apply to active LOW times for executing error detect sequences.

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13. Dynamic characteristics

Table 10. Dynamic characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{w(LE)}$	LE pulse width	V_{DD} = 3.3 V	[1]	10	-	-	ns
$t_{w(OE)}$	$\overline{OE}$ pulse width		[2]	200	-	-	ns
$t_{su(SDI)}$	SDI set-up time	from SDI to CLK		5	-	-	ns
$t_{h(SDI)}$	SDI hold time	from CLK to SDI		5	-	-	ns
f_{CLK}	frequency on pin CLK			0	-	25	MHz
δ	clock duty cycle			-	50 to 50	60 to 40	%
$t_{w(CLKH)}$	CLK HIGH pulse width			16	-	-	ns
$t_{w(CLKL)}$	CLK LOW pulse width			16	-	-	ns
$t_{PD(CLK-SDO)}$	propagation delay from CLK to SDO			-	-	10	ns
$t_{su(LE)}$	LE set-up time	from LE to CLK	[3]	20	-	-	ns
$t_{su(OE)}$	$\overline{OE}$ set-up time	from $\overline{OE}$ to CLK	[3]	20	-	-	ns
$t_{h(LE)}$	LE hold time	from CLK to LE	[3]	5	-	-	ns
$t_{h(OE)}$	$\overline{OE}$ hold time	from CLK to $\overline{OE}$	[3]	5	-	-	ns
$t_{PD(OE-LEDH)}$	propagation delay from $\overline{OE}$ to LED HIGH	pins LED0 to LED7; V_{DD} = 5.0 V; C_L = 30 pF; R_L = 15 Ω; V_L = 1.9 V; I_O = 20.7 mA; R_{ext} = 910 Ω		-	210	-	ns
$t_{PD(OE-LEDL)}$	propagation delay from $\overline{OE}$ to LED LOW	pins LED0 to LED7; V_{DD} = 5.0 V; C_L = 30 pF; R_L = 15 Ω; V_L = 1.9 V; I_O = 20.7 mA; R_{ext} = 910 Ω		-	210	-	ns
$t_{PD(LEH-LEDH)}$	propagation delay from LE HIGH to LED HIGH	pins LED0 to LED7; V_{DD} = 5.0 V; C_L = 30 pF; R_L = 15 Ω; V_L = 1.9 V; I_O = 20.7 mA; R_{ext} = 910 Ω; $\overline{OE}$ = logic 0		-	210	-	ns
$t_{PD(LEH-LEDL)}$	propagation delay from LE HIGH to LED LOW	pins LED0 to LED7; V_{DD} = 5.0 V; C_L = 30 pF; R_L = 15 Ω; V_L = 1.9 V; I_O = 20.7 mA; R_{ext} = 910 Ω; $\overline{OE}$ = logic 0		-	210	-	ns
$t_{PD(CLKH-LEDH)}$	propagation delay from CLK HIGH to LED HIGH	pins LED0 to LED7; V_{DD} = 5.0 V; C_L = 30 pF; R_L = 15 Ω; V_L = 1.9 V; I_O = 20.7 mA; R_{ext} = 910 Ω; $\overline{OE}$ = logic 0; LE = logic 1		-	210	-	ns
$t_{PD(CLKH-LEDL)}$	propagation delay from CLK HIGH to LED LOW	pins LED0 to LED7; V_{DD} = 5.0 V; C_L = 30 pF; R_L = 15 Ω; V_L = 1.9 V; I_O = 20.7 mA; R_{ext} = 910 Ω; $\overline{OE}$ = logic 0; LE = logic 1		-	210	-	ns
t_r	rise time	pins LED0 to LED7; V_{DD} = 5.0 V; C_L = 30 pF; R_L = 15 Ω; V_L = 1.9 V; I_O = 20.7 mA; R_{ext} = 910 Ω		-	175	-	ns
t_f	fall time	pins LED0 to LED7; V_{DD} = 5.0 V; C_L = 30 pF; R_L = 15 Ω; V_L = 1.9 V; I_O = 20.7 mA; R_{ext} = 910 Ω; $\overline{OE}$ = logic 0		-	190	-	ns

[1] Applies to normal device operation. This pulse width does not apply to active HIGH times for executing error detect sequences.

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[2] $\overline{OE}$ must be held active LOW for at least the duration of the rise/fall time of the LEDn pins. This pulse width does not apply to active LOW times for executing error detect sequences.

[3] Timing required for signaling of error detection sequences. Not necessary for 'normal' operation.

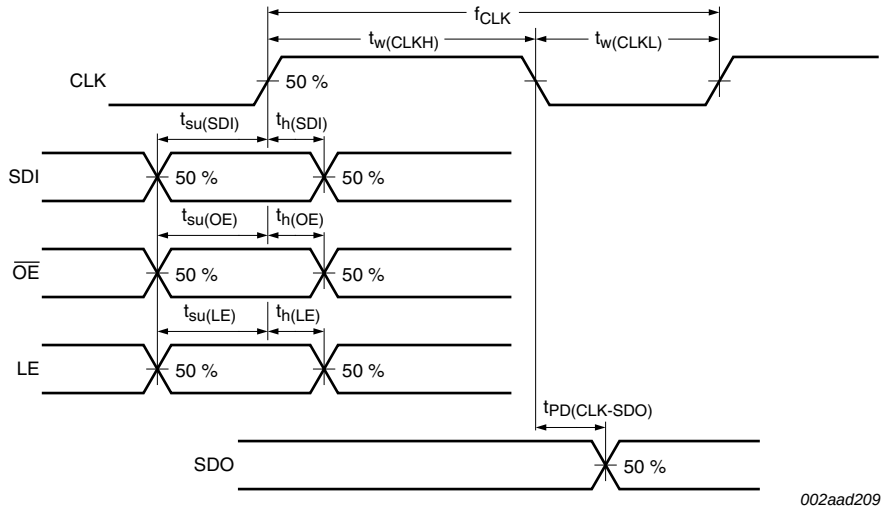


Fig 12. Timing 1

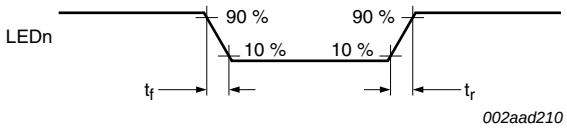


Fig 13. LED[7:0] rise/fall timing

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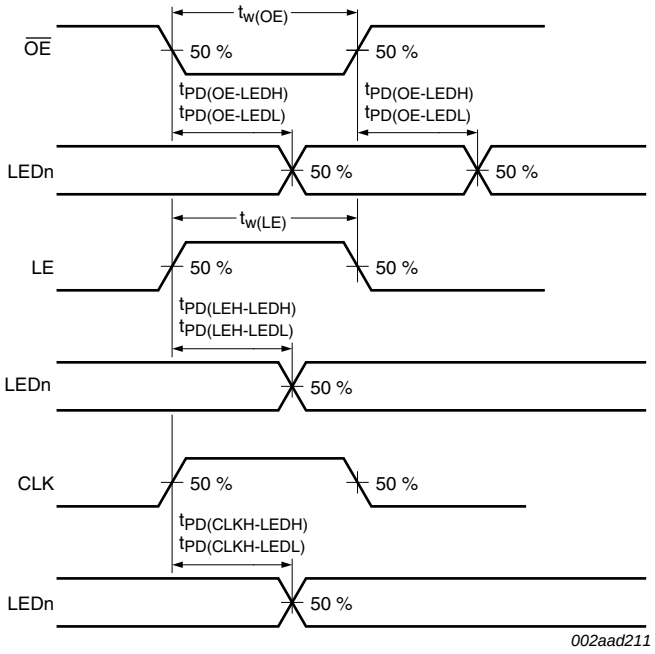


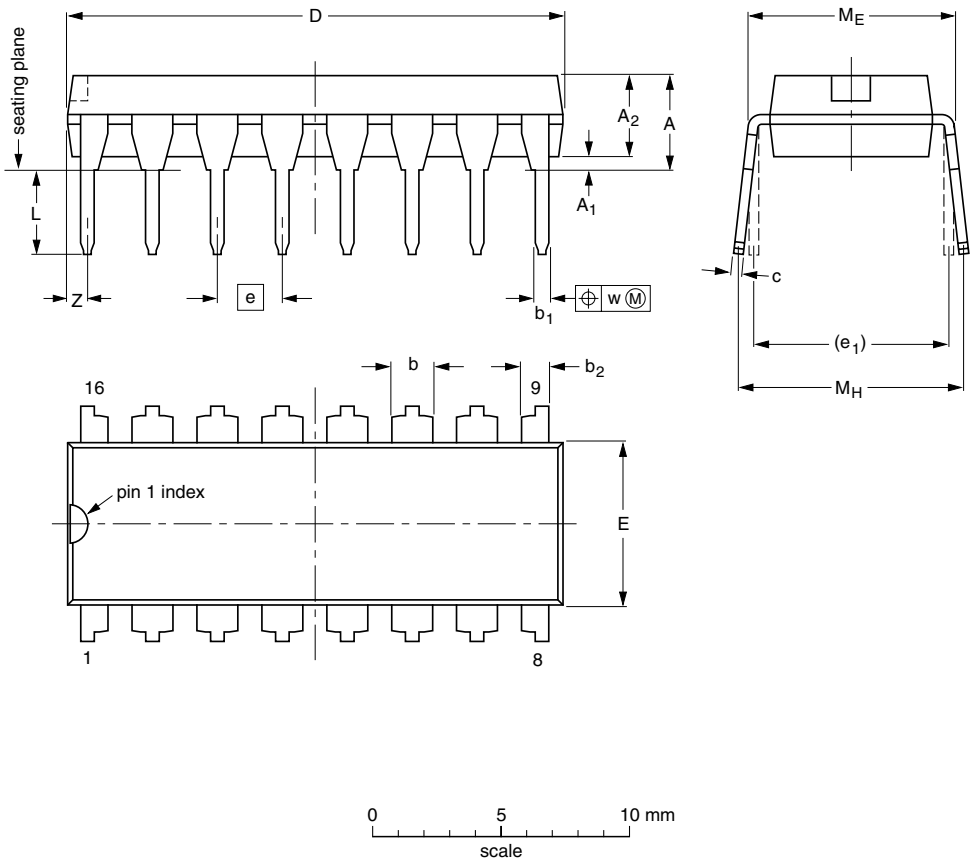
Fig 14. Timing 2

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14. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

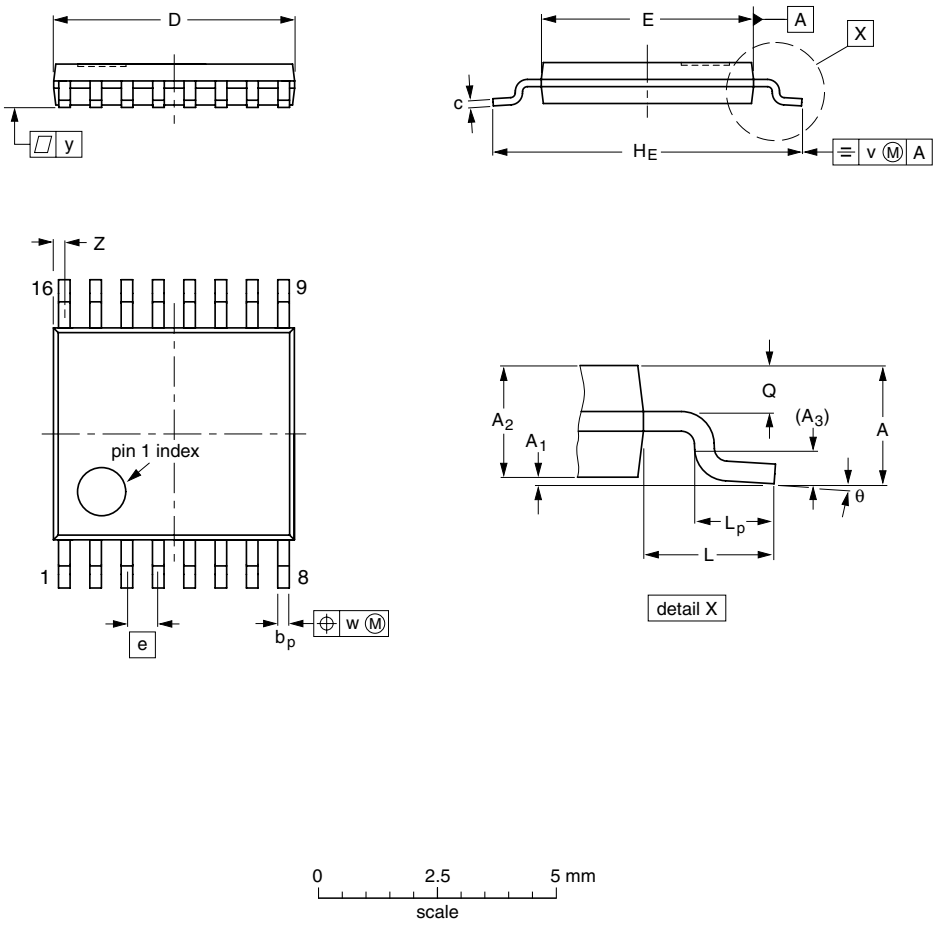
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						~~95-01-14~~ 03-02-13

Fig 15. Package outline SOT38-4 (DIP16)

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TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

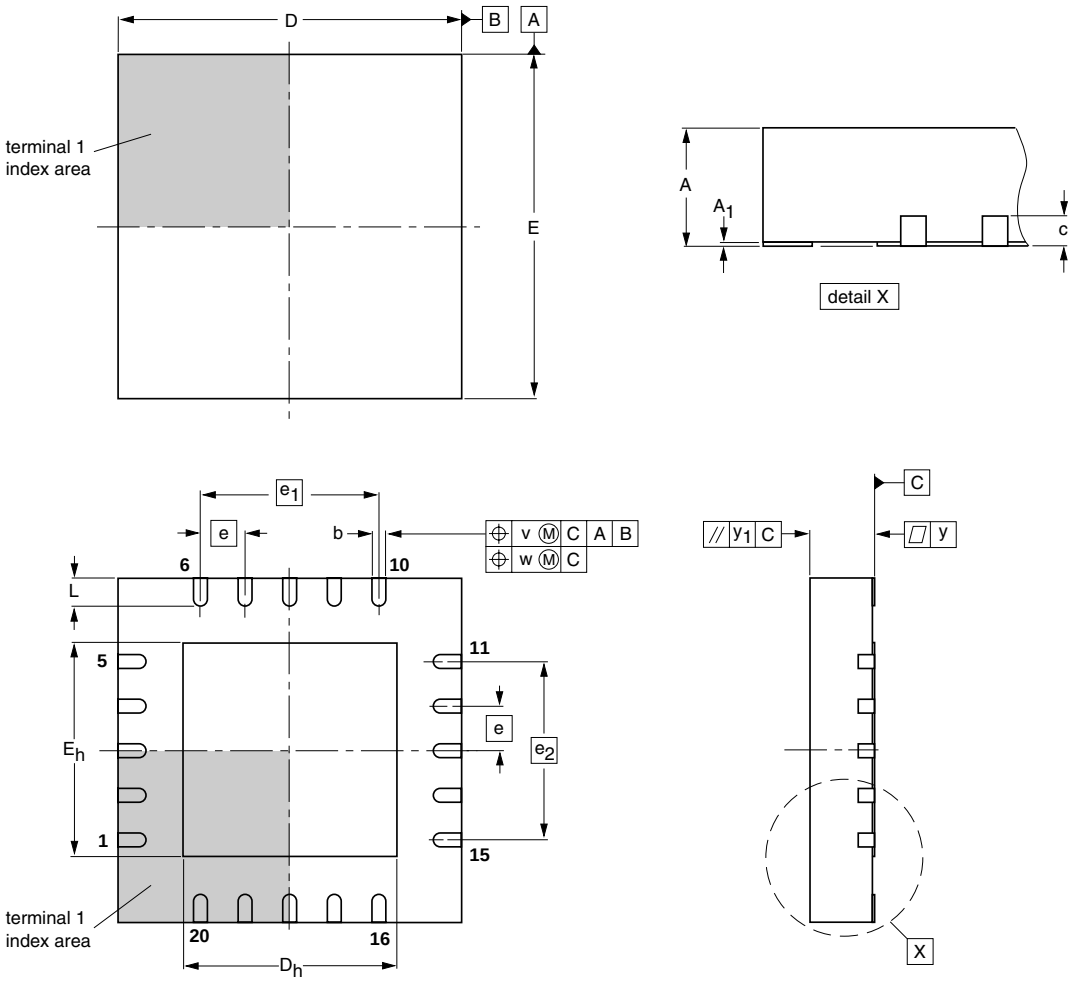
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 16. Package outline SOT403-1 (TSSOP16)

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HVQFN20: plastic thermal enhanced very thin quad flat package; no leads; 20 terminals; body 5 x 5 x 0.85 mm **SOT662-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.38 0.23	0.2	5.1 4.9	3.25 2.95	5.1 4.9	3.25 2.95	0.65	2.6	2.6	0.75 0.50	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT662-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-22

Fig 17. Package outline SOT662-1 (HVQFN20)

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15. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

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- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 18) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 11 and 12

Table 11. SnPb eutectic process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 12. Lead-free process (from J-STD-020C)

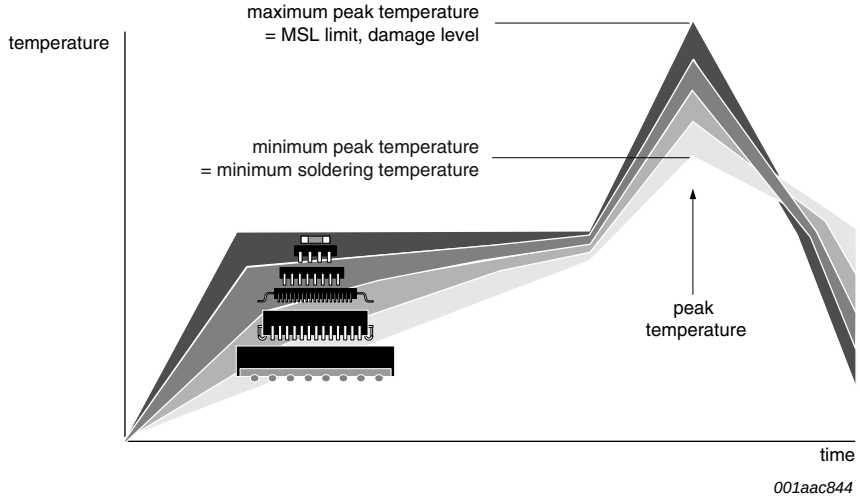
Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 18.

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MSL: Moisture Sensitivity Level

Fig 18. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

17. Soldering of through-hole mount packages

17.1 Introduction to soldering through-hole mount packages

This text gives a very brief insight into wave, dip and manual soldering.

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

17.2 Soldering by dipping or by solder wave

Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing. Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

17.3 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 °C and 400 °C, contact may be up to 5 seconds.

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17.4 Package related soldering information

Table 13. Suitability of through-hole mount IC packages for dipping and wave soldering

Package	Soldering method	
	Dipping	Wave
CPGA, HCPGA	-	suitable
DBS, DIP, HDIP, RDBS, SDIP, SIL	suitable	suitable[1]
PMFP[2]	-	not suitable

[1] For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

[2] For PMFP packages hot bar soldering or manual soldering is suitable.

18. Abbreviations

Table 14. Abbreviations

Acronym	Description
CDM	Charged-Device Model
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
HBM	Human Body Model
LED	Light Emitting Diode
MM	Machine Model
MSB	Most Significant Bit
PCB	Printed-Circuit Board
PWM	Pulse Width Modulator

19. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9922 v.2	20110406	Product data sheet	-	PCA9922 v.1
Modifications:	• Figure 1 “Block diagram of PCA9922”: removed block “auto shutdown and auto power-up”			
PCA9922 v.1	20090115	Product data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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