PCA85232

LCD driver for low multiplex rates

Rev. 4 — 8 April 2015 Product data sheet

1. General description

The PCA85232 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD)[1] with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 160 segments. It can easily be cascaded for larger LCD applications. The PCA85232 is compatible with most microcontrollers and communicates via the two-line bidirectional I^2C-bus. Communication overheads are minimized by a display RAM with auto-incremental addressing, by hardware subaddressing, and by display memory switching (static and duplex drive modes).

For a selection of NXP LCD segment drivers, see Table 29 on page 56.

2. Features and benefits

- AEC-Q100 compliant for automotive applications
- Single-chip LCD controller and driver for up to 640 elements
- Selectable backplane drive configuration: static, 2, 3, or 4 backplane multiplexing
- 160 segment drives:
  - Up to 80 7-segment numeric characters
  - Up to 40 14-segment alphanumeric characters
  - Any graphics of up to 640 elements
- May be cascaded for large LCD applications (up to 5120 elements possible)
- 160 × 4-bit RAM for display data storage
- Software programmable frame frequency in the range of 117 Hz to 176 Hz; factory calibrated
- Wide LCD supply range: from 1.8 V for low threshold LCDs and up to 8.0 V for guest-host LCDs and high threshold (automobile) twisted nematic LCDs
- Internal LCD bias generation with voltage-follower buffers
- Selectable display bias configuration: static, ½, or ⅓
- Wide power supply range: from 1.8 V to 5.5 V
- LCD and logic supplies may be separated
- Low power consumption, typical: I_{DD} = 4 μA, $I_{DD(LCD)}$ = 65 μA
- 400 kHz I^2C-bus interface
- Auto-incremental display data loading across device subaddress boundaries
- Versatile blinking modes
- Compatible with Chip-On-Glass (COG) technology
- No external components required

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 19 on page 58.

- Two sets of backplane outputs for optimal COG configurations of the application

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCA85232U	bare die	197 bumps; 6.5 × 1.16 × 0.40 mm	PCA85232U

3.1 Ordering options

Table 2. Ordering options

Product type number	Orderable part number	Sales item (12NC)	Delivery form	IC revision
PCA85232U/2DA/Q1	PCA85232U/2DA/Q1,0	935291553026	chips with bumps in tray	1

4. Marking

Table 3. Marking codes

Product type number	Marking code
PCA85232U	PC85132/232-1

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5. Block diagram

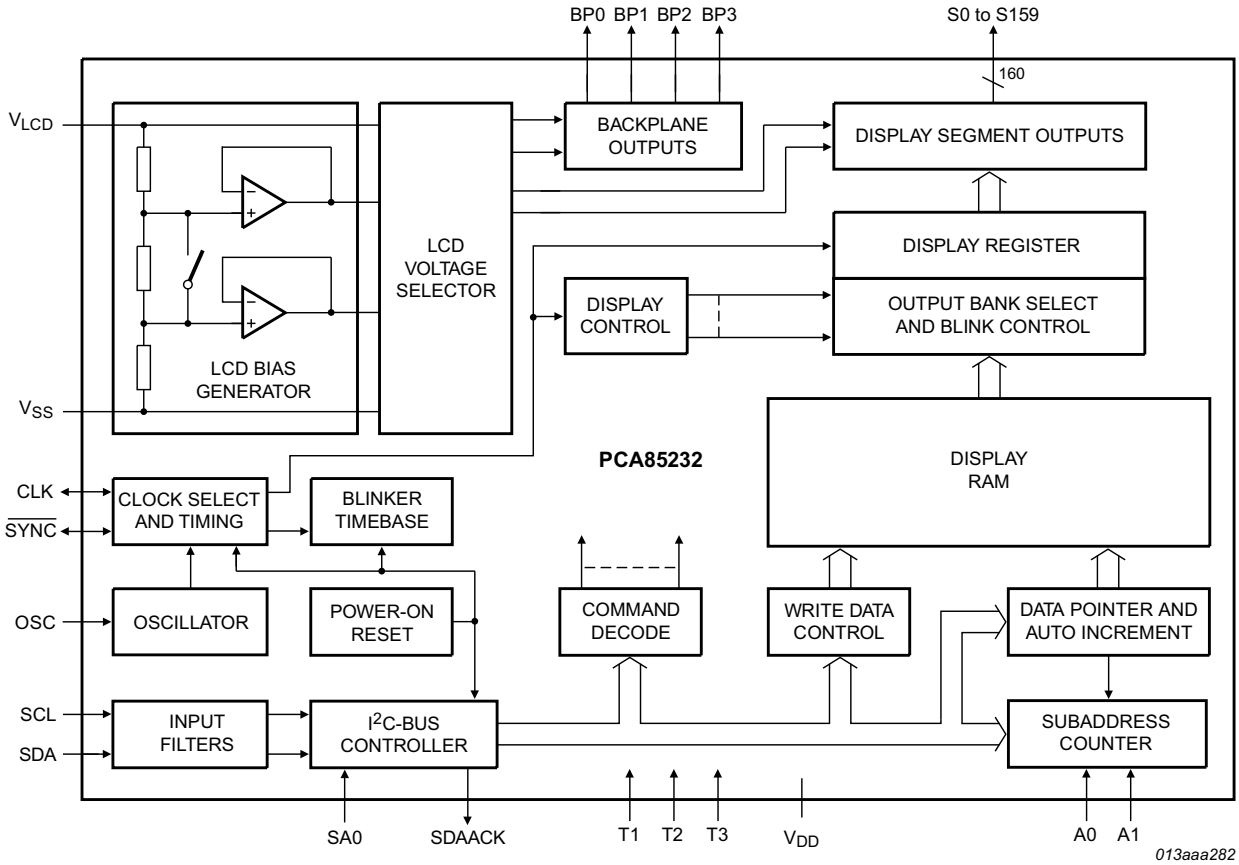


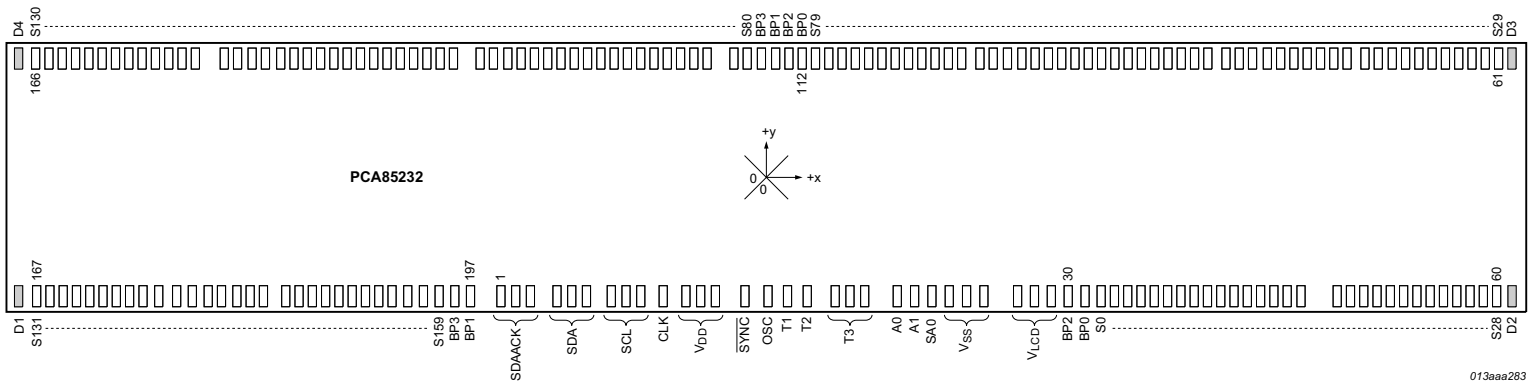
Fig 1. Block diagram of PCA85232

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6. Pinning information

6.1 Pinning



Viewed from active side. For mechanical details, see Figure 37 on page 49.

Fig 2. Pinning diagram of PCA85232

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6.2 Pin description

Table 4. Pin description

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Pin	Description
SDAACK[1]	1 to 3	I^2C-bus acknowledge output
SDA[1]	4 to 6	I^2C-bus serial data input
SCL	7 to 9	I^2C-bus serial clock input
CLK	10	clock input and output
V_{DD}	11 to 13	supply voltage
$\overline{SYNC}$	14	cascade synchronization input and output
OSC	15	selection of internal or external clock
T1, T2, and T3	16, 17, and 18 to 20	dedicated testing pins; to be tied to V_{SS} in application mode
A0 and A1	21, 22	subaddress inputs
SA0	23	I^2C-bus slave address input
V_{SS}[2]	24 to 26	ground supply voltage
V_{LCD}	27 to 29	LCD supply voltage
BP2 and BP0	30, 31	LCD backplane outputs
S0 to S79	32 to 111	LCD segment outputs
BP0, BP2, BP1, and BP3	112 to 115	LCD backplane outputs
S80 to S159	116 to 195	LCD segment outputs
BP3 and BP1	196, 197	LCD backplane outputs

[1] For most applications SDA and SDAACK are shorted together (see Section 14.3 on page 44).

[2] The substrate (rear side of the die) is connected to V_{SS} and should be electrically isolated.

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7. Functional description

The PCA85232 is a versatile peripheral device designed to interface between any microcontroller to a wide variety of LCD segment or dot matrix displays. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 160 segments.

7.1 Commands of PCA85232

The commands available to the PCA85232 are defined in Table 5.

Table 5. Definition of PCA85232 commands

Command	Operation code								Reference
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	
mode-set	1	1	0	0	E	B	M[1:0]		Table 6
load-data-pointer-MSB	0	0	0	0	P[7:4]				Table 7
load-data-pointer-LSB	0	1	0	0	P[3:0]				Table 8
device-select	1	1	1	0	0	0	A[1:0]		Table 9
bank-select	1	1	1	1	1	0	I	O	Table 10
blink-select	1	1	1	1	0	AB	BF[1:0]		Table 11
frequency-ctrl	1	1	1	0	1	F[2:0]			Table 12

7.1.1 Command: mode-set

The mode-set command allows configuring the multiplex mode, the bias levels and enabling or disabling the display.

Table 6. Mode-set - command bit description

Bit	Symbol	Value	Description
7 to 4	-	1100	fixed value
3	E		**display status**[1]
		0[2]	disabled (blank)[3]
		1	enabled
2	B		**LCD bias configuration**[4]
		0[2]	1/3 bias
		1	1/2 bias
1 to 0	M[1:0]		**LCD drive mode selection**
		01	static; BP0
		10	1:2 multiplex; BP0, BP1
		11	1:3 multiplex; BP0, BP1, BP2
		00[2]	1:4 multiplex; BP0, BP1, BP2, BP3

[1] The possibility to disable the display allows implementation of blinking under external control. The enable bit determines also whether the internal clock signal is available at the CLK pin (see Section 7.1.6.2 on page 9).

[2] Default value.

[3] The display is disabled by setting all backplane and segment outputs to V_{LCD}.

[4] Not applicable for static drive mode.

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7.1.2 Command: load-data-pointer

The load-data-pointer command defines the display RAM address where the following display data will be sent to.

Table 7. Load-data-pointer-MSB - command bit description
See Section 7.5.1 on page 24.

Bit	Symbol	Value	Description
7 to 4	-	0000	fixed value
3 to 0	P[7:4]	0000[1] to 1001	**defines the first 4 (most significant) bits of the data-pointer** the data-pointer indicates one of the 160 display RAM addresses

[1] Default value.

Table 8. Load-data-pointer-LSB - command bit description
See Section 7.5.1 on page 24.

Bit	Symbol	Value	Description
7 to 4	-	0100	fixed value
3 to 0	P[3:0]	0000[1] to 1111	**defines the last 4 (least significant) bits of the data-pointer** the data-pointer indicates one of the 160 display RAM addresses

[1] Default value.

7.1.3 Command: device-select

The device-select command allows defining the subaddress counter value.

Table 9. Device-select - command bit description
See Section 7.5.2 on page 24.

Bit	Symbol	Value	Description
7 to 2	-	111000	fixed value
1 to 0	A[1:0]	00[1] to 11	**defines one of four hardware subaddresses** (see Table 23 on page 44)

[1] Default value.

7.1.4 Command: bank-select

The bank-select command controls where data is written to RAM and where it is displayed from.

Table 10. Bank-select - command bit description
See Section 7.5.4 on page 25.

Bit	Symbol	Value	Description	
			Static	**1:2 multiplex[1]**
7 to 2	-	111110	fixed value	
1	I		**input bank selection**; storage of arriving display data	
		0[2]	RAM row 0	RAM rows 0 and 1
		1	RAM row 2	RAM rows 2 and 3

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Table 10. Bank-select - command bit description *...continued*
See Section 7.5.4 on page 25.

Bit	Symbol	Value	Description	
			Static	**1:2 multiplex[1]**
0	O		**output bank selection**; retrieval of LCD display data	
		0[2]	RAM row 0	RAM rows 0 and 1
		1	RAM row 2	RAM rows 2 and 3

[1] The bank-select command has no effect in 1:3 and 1:4 multiplex drive modes.

[2] Default value.

7.1.5 Command: blink-select

The blink-select command allows configuring the blink mode and the blink frequency.

Table 11. Blink-select - command bit description
See Section 7.1.6.6 on page 10.

Bit	Symbol	Value	Description
7 to 3	-	11110	fixed value
2	AB		**blink mode selection**
		0[1]	normal blinking[2]
		1	alternate RAM bank blinking[3]
1 to 0	BF[1:0]		**blink frequency selection**
		00[1]	off
		01	1
		10	2
		11	3

[1] Default value.

[2] Normal blinking is assumed when the LCD multiplex drive modes 1:3 or 1:4 are selected.

[3] Alternate RAM bank blinking does not apply in 1:3 and 1:4 multiplex drive modes.

7.1.6 Clock frequency and timing

The timing of the PCA85232 organizes the internal data flow of the device. The timing includes the transfer of display data from the display RAM to the display segment outputs and therefore the frame frequency.

7.1.6.1 Clock source selection

The PCA85232 can be configured to use either the built-in oscillator or an external clock as clock source:

Internal clock — To enable the internal oscillator, pin OSC has to be connected to V_{SS}. Pin CLK then becomes an output. For further information on the internal clock, see Section 7.1.6.2.

External clock — To enable the use of an external clock, pin OSC has to be connected to V_{DD}. Pin CLK then becomes an input for the external clock frequency $f_{clk(ext)}$. For further information on the external clock, see Section 7.1.6.3.

Figure 3 illustrates the frequency generation of the PCA85232.

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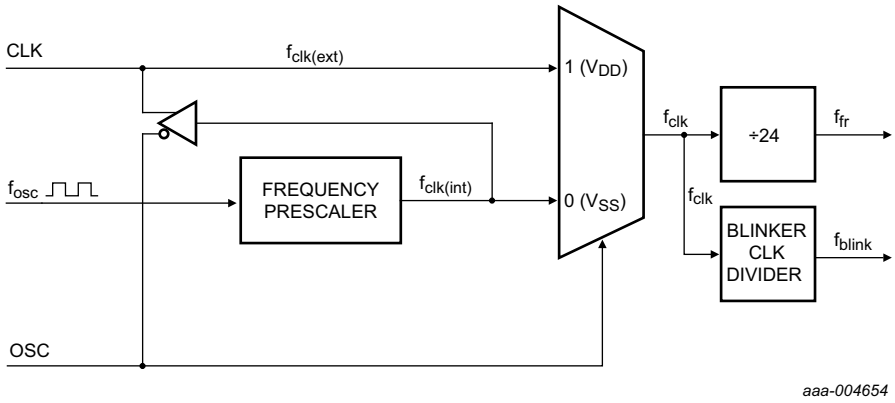


Fig 3. Frequency generation of the PCA85232

Remark: A clock signal must always be supplied to the device. Removing the clock may freeze the LCD in a DC state, which is not suitable for the liquid crystal.

7.1.6.2 Internal clock

If the internal oscillator is used, the timing of the PCA85232 is derived from the built-in oscillator by a pre-scaler which can be configured with the frequency-ctrl command (see Table 12).

The internal oscillator is calibrated within an accuracy of ±5.1 % (at V_{DD} = 5.0 V; T_{amb} = 30 °C).

The frequency-ctrl command determines the division factor between the oscillator frequency f_{osc} and the internal clock frequency $f_{clk(int)}$. If the internal oscillator is used, the frame frequency is derived from the internal clock frequency $f_{clk(int)}$ by the fixed division shown in Equation 1 on page 9.

If the display is enabled (see bit E in Table 6), $f_{clk(int)}$ on pin CLK provides the clock signal for cascaded LCD drivers in the system. For further information about cascading, see Section 14.4 on page 44. The value range of f_{osc} is specified in Table 22 on page 38.

7.1.6.3 External clock

If the external clock source is selected, the timing frequency of the PCA85232 is the external clock frequency. In this case, the frequency-ctrl command has no influence on the clock frequency nor the frame frequency. The frame frequency is derived from the external clock frequency $f_{clk(ext)}$ by the fixed division as shown in Equation 1.

7.1.6.4 Frame frequency

Sourced by the internal oscillator or an external clock, the frame frequency is derived from the clock frequency f_{clk} by Equation 1.

$$f_{fr} = \frac{f_{clk}}{24} \quad (1)$$

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7.1.6.5 Command: frequency-ctrl

Table 12. Frequency-ctrl - command bit description

Bit	Symbol	Value	Description		
			Equation	Nominal clock frequency[1]	Nominal frame frequency[1]
7 to 4	-	11101	fixed value		
3 to 0	F[2:0]		**defines the division factor**		
		000	$f_{clk(int)} = \frac{64}{80} \times f_{osc}$	2800 Hz	117 Hz
		001	$f_{clk(int)} = \frac{64}{74} \times f_{osc}$	3027 Hz	126 Hz
		010	$f_{clk(int)} = \frac{64}{68} \times f_{osc}$	3294 Hz	137 Hz
		011[2], 111	$f_{clk(int)} = f_{osc}$	3500 Hz	146 Hz
		100	$f_{clk(int)} = \frac{64}{60} \times f_{osc}$	3733 Hz	156 Hz
		101	$f_{clk(int)} = \frac{64}{56} \times f_{osc}$	4000 Hz	167 Hz
		110	$f_{clk(int)} = \frac{64}{53} \times f_{osc}$	4226 Hz	176 Hz

[1] Calculated with the oscillator frequency of f_{osc} = 3.500 Hz. The frame frequency is derived from the internal clock frequency by Equation 1.

[2] Default value.

7.1.6.6 Blinking

The display blinking capabilities of the PCA85232 are very versatile. The whole display can blink at frequencies selected by the blink-select command (see Table 11). The blink frequencies are derived from the clock frequency (f_{clk}). The ratios between the clock and blink frequencies depend on the blink mode in which the device is operating (see Table 13).

Table 13. Blink frequencies

Assuming that f_{clk} = 3.500 kHz.

Blink mode	Operating mode ratio	Blink frequency
off	-	blinking off
1	$f_{blink} = \frac{f_{clk}}{768}$	~4.56 Hz
2	$f_{blink} = \frac{f_{clk}}{1536}$	~2.28 Hz
3	$f_{blink} = \frac{f_{clk}}{3072}$	~1.14 Hz

An additional feature is for an arbitrary selection of LCD elements to blink. This applies to the static and 1:2 multiplex drive modes and can be implemented without any communication overheads: With the output bank selector, the displayed RAM banks are

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exchanged (see Section 7.5.4 on page 25) with alternate RAM banks at the blink frequency. This mode can also be specified by the blink-select command (see Table 11 on page 8).

In the 1:3 and 1:4 multiplex modes, where no alternate RAM bank is available, groups of LCD elements can blink selectively by changing the display RAM data at fixed time intervals.

The entire display can blink at a frequency other than the nominal blinking frequency. This can be effectively performed by resetting and setting the display enable bit E at the required rate using the mode-set command (see Table 6).

7.2 Power-On Reset (POR)

At power-on, the PCA85232 resets to the following starting conditions:

- All backplane and segment outputs are set to V_{LCD}
- The selected drive mode is 1:4 multiplex with $\frac{1}{3}$ bias
- Blinking is switched off
- Input and output bank selectors are reset
- The I^2C-bus interface is initialized
- The data pointer and the subaddress counter are cleared (set to logic 0)
- The display is disabled (bit E = 0, see Table 6 on page 6)
- If internal oscillator is selected (pin OSC connected to V_{SS}), then there is no clock signal on pin CLK

Remark: Do not transfer data on the I^2C-bus for at least 1 ms after a power-on to allow the reset action to complete.

7.3 Possible display configurations

The display configurations possible with the PCA85232 depend on the required number of active backplane outputs. A selection of display configurations is given in Table 14.

All of the display configurations given in Table 14 can be implemented in a typical system as shown in Figure 5.

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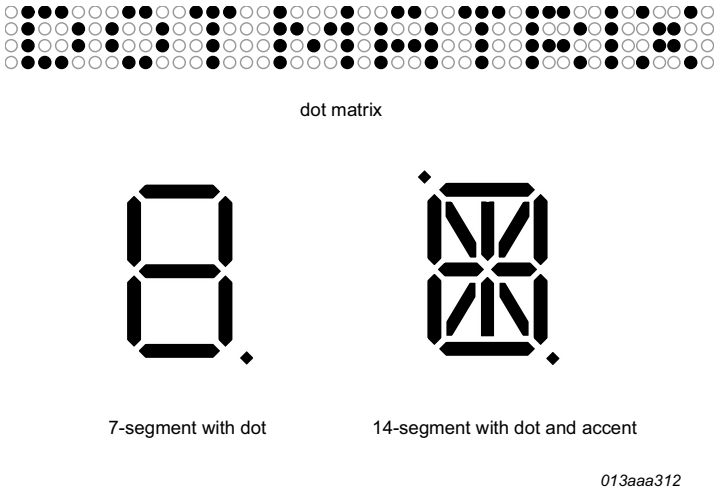


Fig 4. Example of displays suitable for PCA85232

Table 14. Selection of possible display configurations

Number of				
Backplanes	**Icons**	**Digits/Characters**		**Dot matrix/ Elements**
		7-segment	**14-segment**	
4	640	80	40	640 dots (4 × 160)
3	480	60	30	480 dots (3 × 160)
2	320	40	20	320 dots (2 × 160)
1	160	20	10	160 dots (1 × 160)

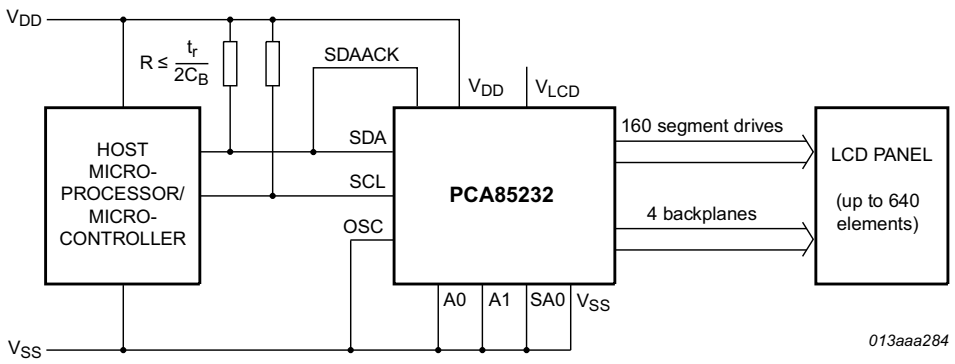


Fig 5. Typical system configuration

The host microcontroller maintains the 2-line I²C-bus communication channel with the PCA85232.

Biasing voltages for the multiplexed LCD waveforms are generated internally, removing the need for an external bias generator. The internal oscillator is selected by connecting pin OSC to V_{SS}. The only other connections required to complete the system are the power supplies (V_{DD}, V_{SS}, and V_{LCD}) and the LCD panel selected for the application.

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7.3.1 LCD bias generator

Fractional LCD biasing voltages are obtained from an internal voltage divider of three impedances connected between pins V_{LCD} and V_{SS}. The center impedance is bypassed by switch if the ½ bias voltage level for the 1:2 multiplex drive mode configuration is selected.

7.3.2 Display register

The display register holds the display data while the corresponding multiplex signals are generated.

7.3.3 LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by the mode-set command. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of V_{LCD} and the resulting discrimination ratios (D) are given in Table 15.

Discrimination is a term which is defined as the ratio of the on and off RMS voltage across a segment. It can be thought of as a measurement of contrast.

Table 15. Biasing characteristics

LCD drive mode	Number of:		LCD bias configuration	$\frac{V_{off(RMS)}}{V_{LCD}}$	$\frac{V_{on(RMS)}}{V_{LCD}}$	$D = \frac{V_{on(RMS)}}{V_{off(RMS)}}$
	Backplanes	Levels				
static	1	2	static	0	1	∞
1:2 multiplex	2	3	½	0.354	0.791	2.236
1:2 multiplex	2	4	⅓	0.333	0.745	2.236
1:3 multiplex	3	4	⅓	0.333	0.638	1.915
1:4 multiplex	4	4	⅓	0.333	0.577	1.732

A practical value for V_{LCD} is determined by equating $V_{off(RMS)}$ with a defined LCD threshold voltage ($V_{th(off)}$), typically when the LCD exhibits approximately 10 % contrast. In the static drive mode, a suitable choice is $V_{LCD} > 3V_{th(off)}$.

Multiplex drive modes of 1:3 and 1:4 with ½ bias are possible but the discrimination and hence the contrast ratios are smaller.

Bias is calculated by $\frac{1}{1+a}$, where the values for a are

a = 1 for ½ bias

a = 2 for ⅓ bias

The RMS on-state voltage ($V_{on(RMS)}$) for the LCD is calculated with Equation 2:

$$V_{on(RMS)} = V_{LCD}\sqrt{\frac{a^2 + 2a + n}{n \times (1+a)^2}} \quad (2)$$

where the values for n are

n = 1 for static drive mode

n = 2 for 1:2 multiplex drive mode

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n = 3 for 1:3 multiplex drive mode

n = 4 for 1:4 multiplex drive mode

The RMS off-state voltage ($V_{off(RMS)}$) for the LCD is calculated with Equation 3:

$$V_{off(RMS)} = V_{LCD}\sqrt{\frac{a^2 - 2a + n}{n \times (1 + a)^2}} \quad (3)$$

Discrimination is the ratio of $V_{on(RMS)}$ to $V_{off(RMS)}$ and is determined from Equation 4:

$$D = \frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{a^2 + 2a + n}{a^2 - 2a + n}} \quad (4)$$

Using Equation 4, the discrimination for an LCD drive mode of 1:3 multiplex with $\frac{1}{2}$ bias is $\sqrt{3} = 1.732$ and the discrimination for an LCD drive mode of 1:4 multiplex with $\frac{1}{2}$ bias is $\frac{\sqrt{21}}{3} = 1.528$.

The advantage of these LCD drive modes is a reduction of the LCD full scale voltage V_{LCD} as follows:

- 1:3 multiplex ($\frac{1}{2}$ bias): $V_{LCD} = \sqrt{6} \times V_{off(RMS)} = 2.449 V_{off(RMS)}$
- 1:4 multiplex ($\frac{1}{2}$ bias): $V_{LCD} = \left[\frac{(4 \times \sqrt{3})}{3}\right] = 2.309 V_{off(RMS)}$

These compare with $V_{LCD} = 3V_{off(RMS)}$ when $\frac{1}{3}$ bias is used.

V_{LCD} is sometimes referred as the LCD operating voltage.

7.3.3.1 Electro-optical performance

Suitable values for $V_{on(RMS)}$ and $V_{off(RMS)}$ are dependent on the LCD liquid used. The RMS voltages, at which a pixel is switched on or off, determine the transmissibility of the pixel.

For any given liquid, there are two threshold values defined. One point is at 10 % relative transmission (at $V_{th(off)}$) and the other at 90 % relative transmission (at $V_{th(on)}$), see Figure 6. For a good contrast performance, the following rules should be followed:

$$V_{on(RMS)} \geq V_{th(on)} \quad (5)$$

$$V_{off(RMS)} \leq V_{th(off)} \quad (6)$$

$V_{on(RMS)}$ and $V_{off(RMS)}$ are properties of the display driver and are affected by the selection of a (see Equation 2), n (see Equation 4), and the V_{LCD} voltage.

$V_{th(off)}$ and $V_{th(on)}$ are properties of the LCD liquid and can be provided by the module manufacturer. $V_{th(off)}$ is sometimes named V_{th}. $V_{th(on)}$ is sometimes named saturation voltage V_{sat}.

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It is important to match the module properties to those of the driver in order to achieve optimum performance.

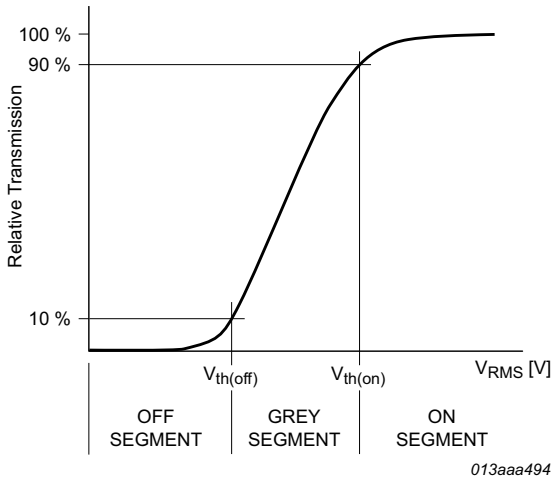


Fig 6. Electro-optical characteristic: relative transmission curve of the liquid

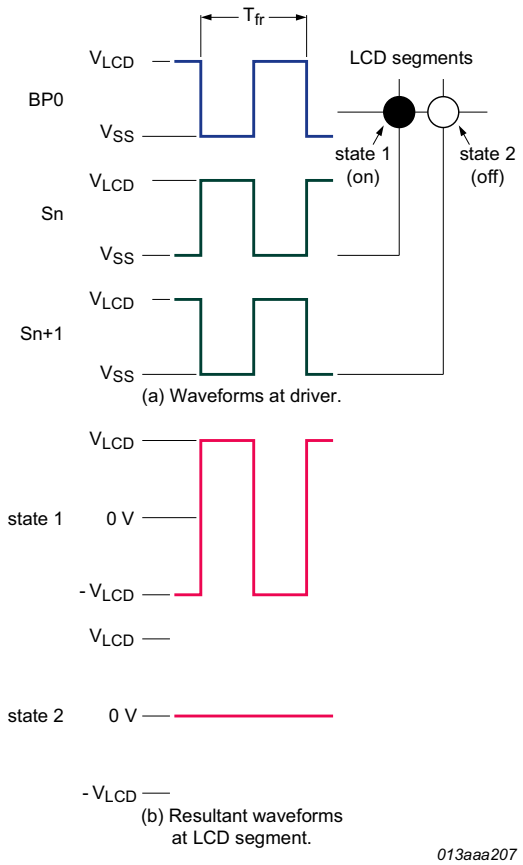
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7.3.4 LCD drive mode waveforms

7.3.4.1 Static drive mode

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Figure 7.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = V_{LCD}$.

$V_{state2}(t) = V_{(Sn+1)}(t) - V_{BP0}(t)$.

$V_{off(RMS)} = 0$ V.

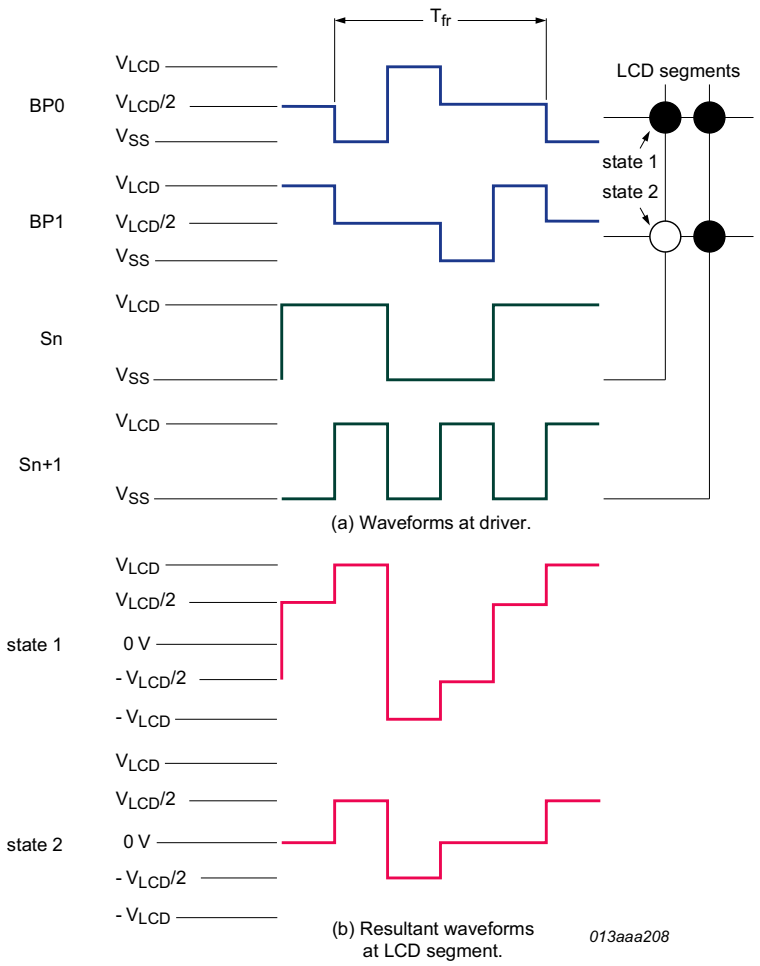
Fig 7. Static drive mode waveforms

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7.3.4.2 1:2 multiplex drive mode

When two backplanes are provided in the LCD, the 1:2 multiplex mode applies. The PCA85232 allows the use of ½ bias or ⅓ bias in this mode as shown in Figure 8 and Figure 9.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.791V_{LCD}$.

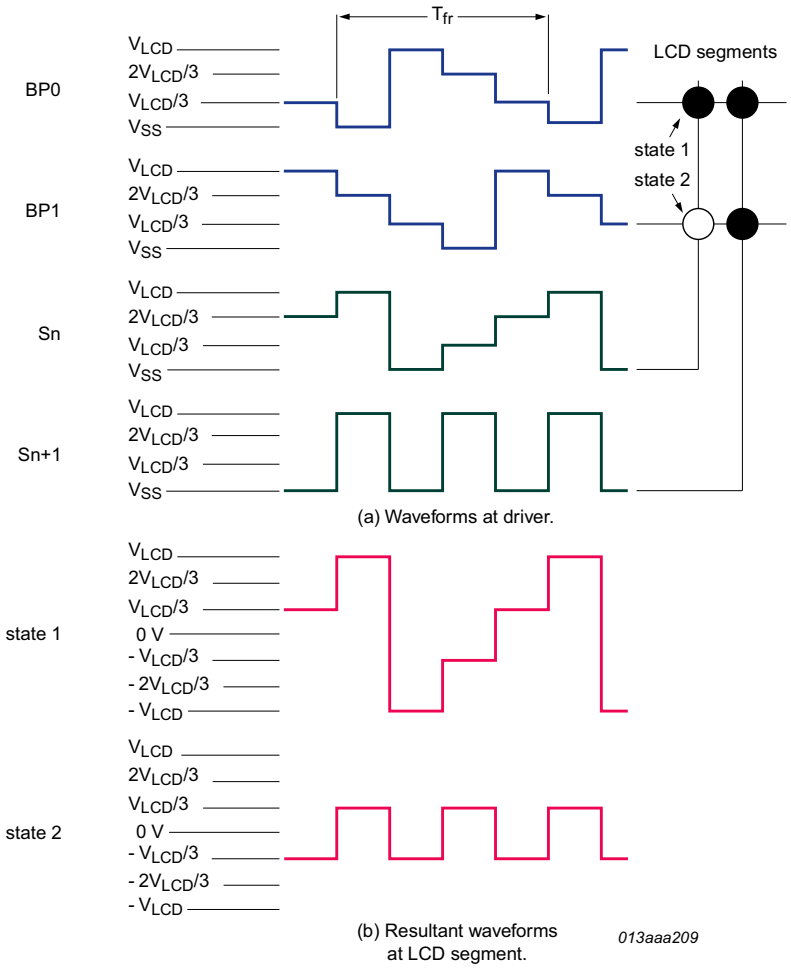
$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.354V_{LCD}$.

Fig 8. Waveforms for the 1:2 multiplex drive mode with ½ bias

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$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.745V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

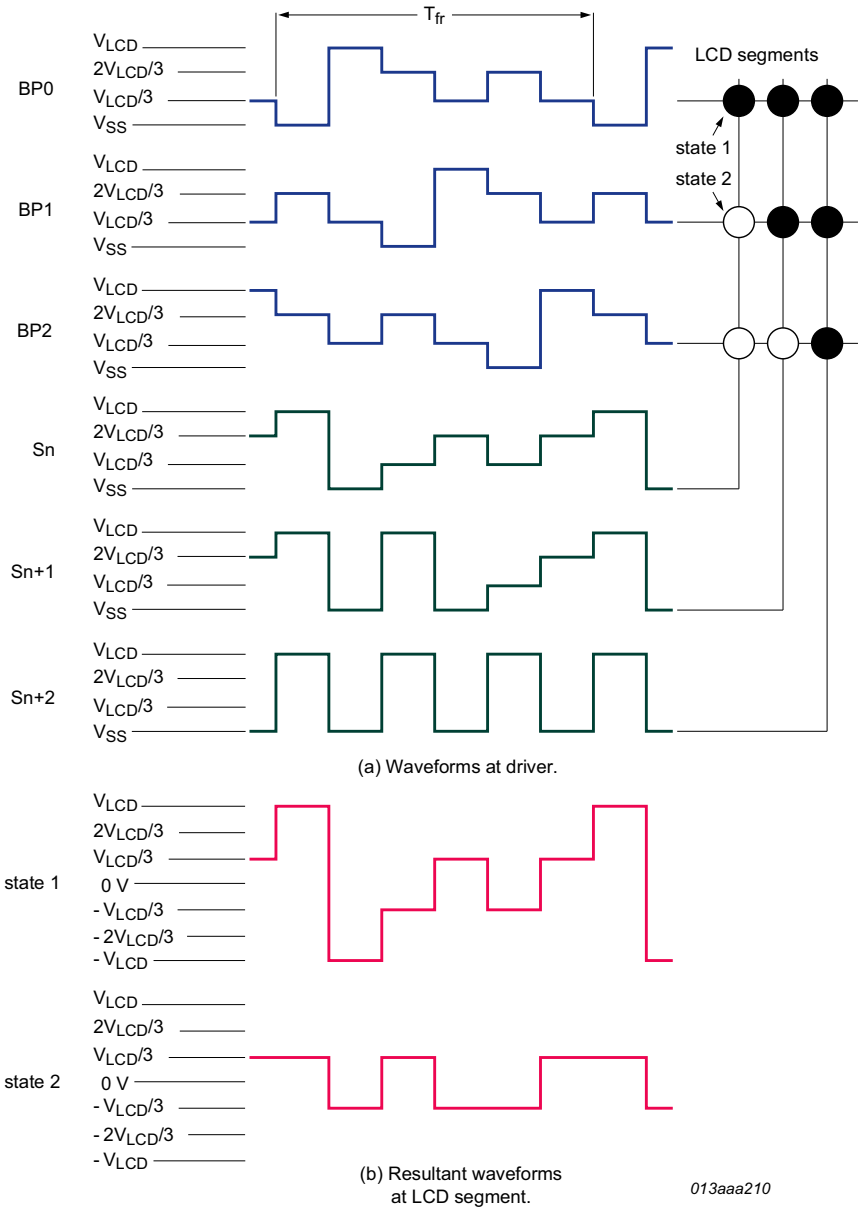
Fig 9. Waveforms for the 1:2 multiplex drive mode with ⅓ bias

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7.3.4.3 1:3 multiplex drive mode

When three backplanes are provided in the LCD, the 1:3 multiplex drive mode applies as shown in Figure 10.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.638V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

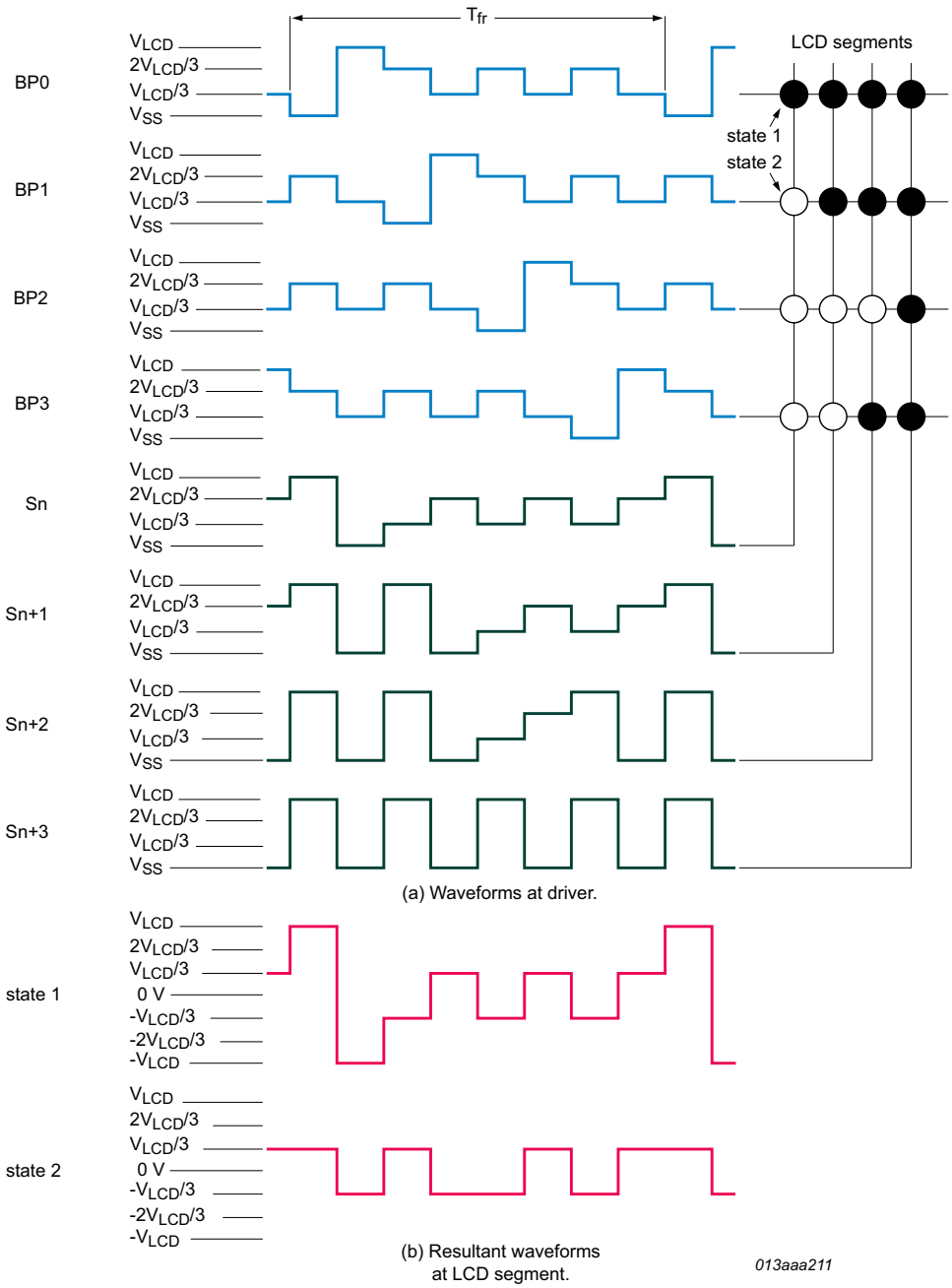
Fig 10. Waveforms for the 1:3 multiplex drive mode with ⅓ bias

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7.3.4.4 1:4 multiplex drive mode

When four backplanes are provided in the LCD, the 1:4 multiplex drive mode applies as shown in Figure 11.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.577V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 11. Waveforms for the 1:4 multiplex drive mode with ⅓ bias

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7.4 Backplane and segment outputs

7.4.1 Backplane outputs

The LCD drive section includes four backplane outputs: BP0 to BP3. The backplane output signals are generated in accordance with the selected LCD drive mode.

- In the 1:4 multiplex drive mode BP0 to BP3 must be connected directly to the LCD.

If less than four backplane outputs are required, the unused outputs can be left open-circuit.

- In 1:3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities.
- In 1:2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities.
- In static drive mode, the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

The pins for the four backplanes BP0 to BP3 are available on both pin bars of the chip. In applications, it is possible to use either the pins for the backplanes

- on the top pin bar
- on the bottom pin bar
- or both of them to increase the driving strength of the device.

When using all backplanes available they may be connected to the respective sibling (BP0 on the top pin bar with BP0 on the bottom pin bar, and so on).

7.4.2 Segment outputs

The LCD drive section includes 160 segment outputs (S0 to S159) which must be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with data resident in the display register. When less than 160 segment outputs are required, the unused segment outputs must be left open-circuit.

7.5 Display RAM

The display RAM is a static 160 $\times$ 4 bit RAM which stores LCD data. There is a one-to-one correspondence between

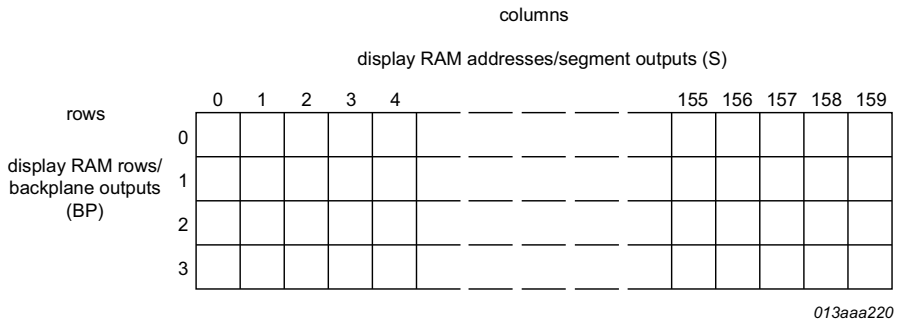
- the bits in the RAM bitmap and the LCD elements
- the RAM columns and the segment outputs
- the RAM rows and the backplane outputs.

A logic 1 in the RAM bitmap indicates the on-state of the corresponding LCD element; similarly, a logic 0 indicates the off-state.

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The display RAM bitmap, Figure 12, shows the rows 0 to 3 which correspond with the backplane outputs BP0 to BP3, and the columns 0 to 159 which correspond with the segment outputs S0 to S159. In multiplexed LCD applications the segment data of the first, second, third, and fourth row of the display RAM are time-multiplexed with BP0, BP1, BP2, and BP3 respectively.



The display RAM bitmap shows the direct relationship between the display RAM addresses and the segment outputs; and between the bits in a RAM word and the backplane outputs.

Fig 12. Display RAM bitmap

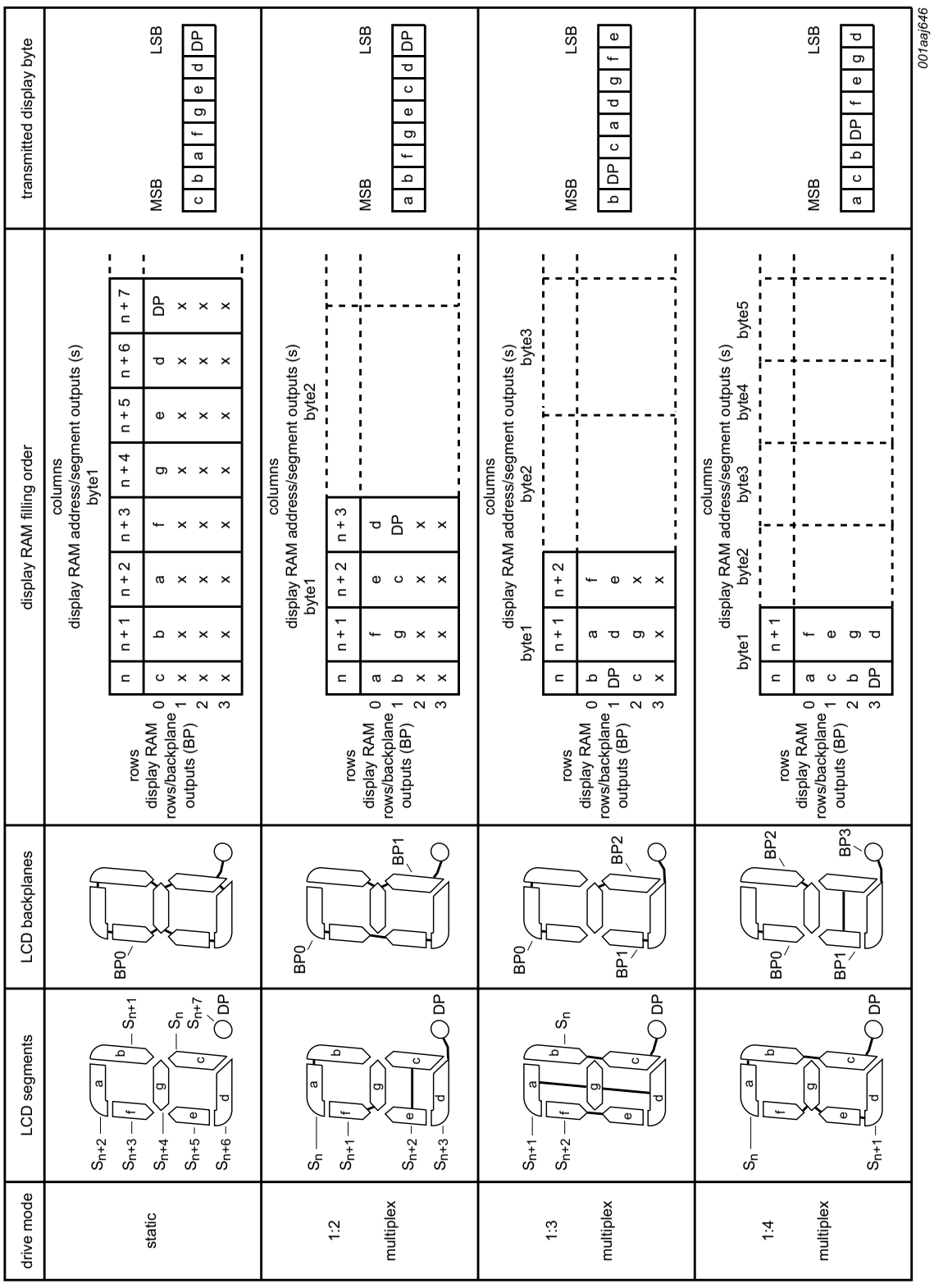
When display data is transmitted to the PCA85232, the received display bytes are stored in the display RAM in accordance with the selected LCD drive mode. The data is stored as it arrives and does not wait for the acknowledge cycle as with the commands. Depending on the current multiplex drive mode, data is stored singularly, in pairs, triples, or quadruples. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Figure 13. The RAM filling organization depicted applies equally to other LCD types.

The following applies to Figure 13:

- In static drive mode the eight transmitted data bits are placed in row 0 as 1 byte.
- In 1:2 multiplex drive mode the eight transmitted data bits are placed in pairs into row 0 and 1 as four successive 2-bit RAM words.
- In 1:3 multiplex drive mode the 8 bits are placed in triples into row 0, 1, and 2 as 3 successive 3-bit RAM words, with bit 3 of the third address left unchanged. It is not recommended to use this bit in a display because of the difficult addressing. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overwriting adjacent data because always full bytes are transmitted (see Section 7.5.3 on page 24).
- In 1:4 multiplex drive mode, the eight transmitted data bits are placed in quadruples into row 0, 1, 2, and 3 as 2 successive 4-bit RAM words.

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x = data bit unchanged

Fig 13. Relationships between LCD layout, drive mode, display RAM filling order, and display data transmitted over the I²C-bus

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7.5.1 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the load-data-pointer command (see Table 7 on page 7 and Table 8 on page 7). Following this command, an arriving data byte is stored at the display RAM address indicated by the data pointer. The filling order is shown in Figure 13.

After each byte is stored, the content of the data pointer is automatically incremented by a value dependent on the selected LCD drive mode:

- In static drive mode by eight
- In 1:2 multiplex drive mode by four
- In 1:3 multiplex drive mode by three
- In 1:4 multiplex drive mode by two

If an I^2C-bus data access is terminated early, then the state of the data pointer is unknown. The data pointer should be re-written before further RAM accesses.

7.5.2 Subaddress counter

The storage of display data is conditioned by the content of the subaddress counter. Storage is allowed only when the content of the subaddress counter matches with the hardware subaddress applied to A0 and A1. The subaddress counter value is defined by the device-select command (see Table 9 on page 7). If the content of the subaddress counter and the hardware subaddress do not match then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are sent to the display RAM, automatic wrap-over to the next PCA85232 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character.

The hardware subaddress must not be changed while the device is being accessed on the I^2C-bus interface.

7.5.3 RAM writing in 1:3 multiplex drive mode

In 1:3 multiplex drive mode, the RAM is written as shown in Table 16 (see Figure 13 as well).

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Table 16. Standard RAM filling in 1:3 multiplex drive mode

*Assumption: BP2/S2, BP2/S5, BP2/S8 etc. **are not connected** to any elements on the display.*

Display RAM bits (rows)/ backplane outputs (BPn)	Display RAM addresses (columns)/segment outputs (Sn)										
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**:**
0	a7	a4	a1	b7	b4	b1	c7	c4	c1	d7	:
1	a6	a3	a0	b6	b3	b0	c6	c3	c0	d6	:
2	a5	a2	-	b5	b2	-	c5	c2	-	d5	:
3	-	-	-	-	-	-	-	-	-	-	:

If the bit at position BP2/S2 would be written by a second byte transmitted, then the mapping of the segment bits would change as illustrated in Table 17.

Table 17. Entire RAM filling by rewriting in 1:3 multiplex drive mode

*Assumption: BP2/S2, BP2/S5, BP2/S8 etc. **are connected** to elements on the display.*

Display RAM bits (rows)/ backplane outputs (BPn)	Display RAM addresses (columns)/segment outputs (Sn)										
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**:**
0	a7	a4	a1/b7	b4	b1/c7	c4	c1/d7	d4	d1/e7	e4	:
1	a6	a3	a0/b6	b3	b0/c6	c3	c0/d6	d3	d0/e6	e3	:
2	a5	a2	b5	b2	c5	c2	d5	d2	e5	e2	:
3	-	-	-	-	-	-	-	-	-	-	:

In the case described in Table 17 the RAM has to be written entirely and BP2/S2, BP2/S5, BP2/S8, and so on, have to be connected to elements on the display. This can be achieved by a combination of writing and rewriting the RAM like follows:

- In the first write to the RAM, bits a7 to a0 are written
- The data-pointer (see Section 7.1.2 on page 7) has to be set to the address of bit a1
- In the second write, bits b7 to b0 are written, overwriting bits a1 and a0 with bits b7 and b6
- The data-pointer has to be set to the address of bit b1
- In the third write, bits c7 to c0 are written, overwriting bits b1 and b0 with bits c7 and c6

Depending on the method of writing to the RAM (standard or entire filling by rewriting), some elements remain unused or can be used, but it has to be considered in the module layout process as well as in the driver software design.

7.5.4 Bank selection

7.5.4.1 Output bank selector

The output bank selector (see Table 10 on page 7) selects one of the four rows per display RAM address for transfer to the display register. The actual row selected depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence.

- In 1:4 multiplex mode, all RAM addresses of row 0 are selected, followed by the contents of row 1, row 2, and then row 3
- In 1:3 multiplex mode, rows 0, 1, and 2 are selected sequentially

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- In 1:2 multiplex mode, rows 0 and 1 are selected
- In static mode, row 0 is selected

7.5.4.2 Input bank selector

The input bank selector loads display data into the display RAM in accordance with the selected LCD drive configuration. Display data can be loaded by using the bank-select command (see Table 10). The input bank selector functions independently to the output bank selector.

7.5.4.3 RAM bank switching

The PCA85232 includes a RAM bank switching feature in the static and 1:2 multiplex drive modes. A bank can be thought of as one RAM row or a collection of RAM rows (see Figure 14). The RAM bank switching gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is complete.

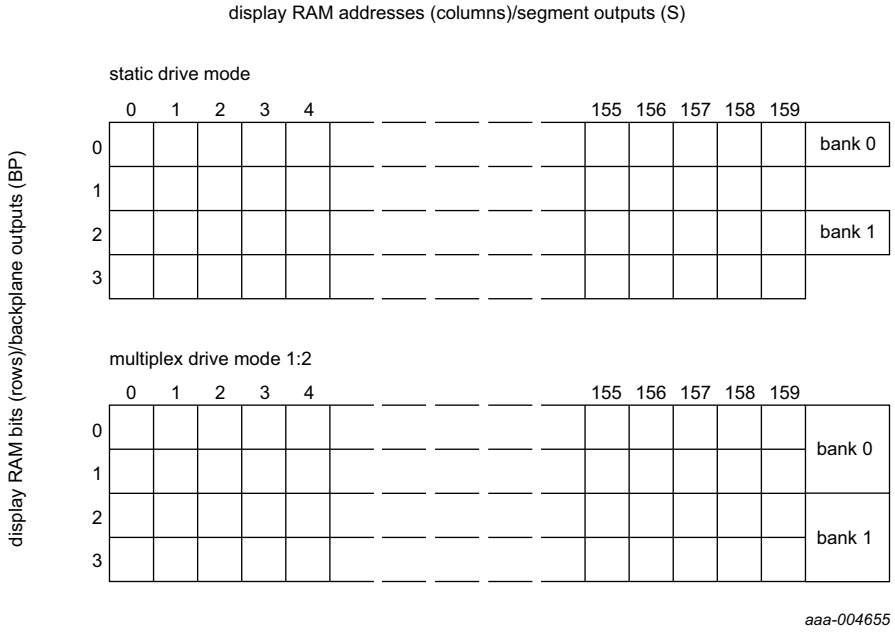


Fig 14. RAM banks in static and multiplex driving mode 1:2

There are two banks; bank 0 and bank 1. Figure 14 shows the location of these banks relative to the RAM map. Input and output banks can be set independently from one another with the Bank-select command (see Table 10 on page 7). Figure 15 shows the concept.

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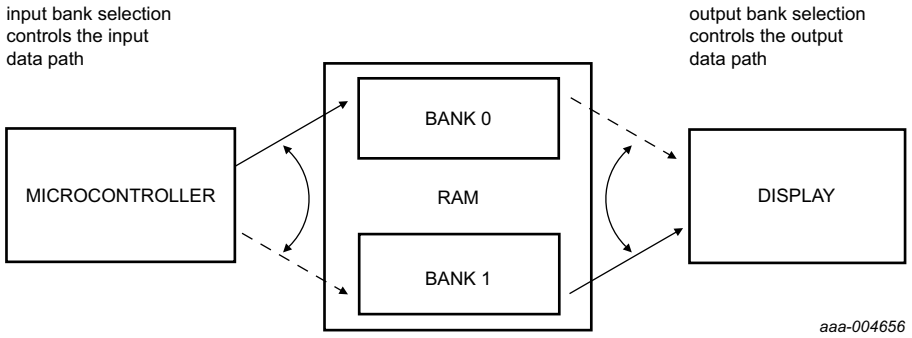


Fig 15. Bank selection

In the static drive mode, the bank-select command may request the contents of row 2 to be selected for display instead of the contents of row 0. In the 1:2 multiplex mode, the contents of rows 2 and 3 may be selected instead of rows 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

In Figure 16 an example is shown for 1:2 multiplex drive mode where the displayed data is read from the first two rows of the memory (bank 0), while the transmitted data is stored in the second two rows of the memory (bank 1).

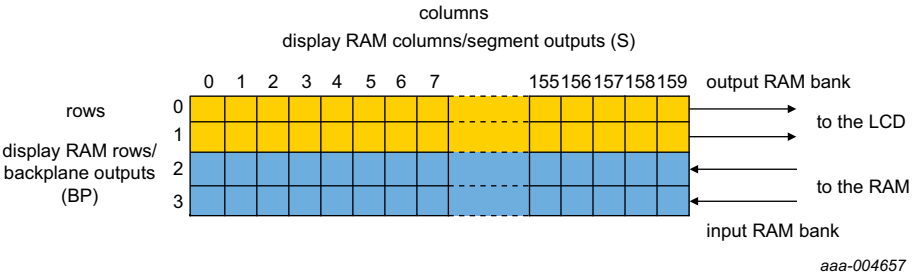


Fig 16. Example of the Bank-select command with multiplex drive mode 1:2

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8. Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial DAta line (SDA) and a Serial CLock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

By connecting pin SDAACK to pin SDA on the PCA85232, the SDA line becomes fully I²C-bus compatible. In COG applications where the track resistance from the SDAACK pin to the system SDA line can be significant, possibly a voltage divider is generated by the bus pull-up resistor and the Indium Tin Oxide (ITO) track resistance. As a consequence, it may be possible that the acknowledge generated by the PCA85232 cannot be interpreted as logic 0 by the master. In COG applications where the acknowledge cycle is required, it is therefore necessary to minimize the track resistance from the SDAACK pin to the system SDA line to guarantee a valid LOW level (see Section 14.2 on page 42).

By separating the acknowledge output from the serial data line (having the SDAACK open circuit) design efforts to generate a valid acknowledge level can be avoided. However, in that case the I²C-bus master has to be set up in such a way that it ignores the acknowledge cycle.[2]

The following definition assumes that SDA and SDAACK are connected and refers to the pair as SDA.

8.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time are interpreted as a control signal (see Figure 17).

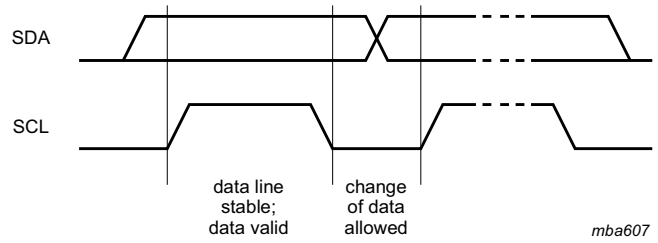


Fig 17. Bit transfer

8.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW change of the data line, while the clock is HIGH is defined as the START condition (S).
A LOW-to-HIGH change of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are shown in Figure 18.

2. For further information, please consider the NXP application note: Ref. 1 “AN10170”.

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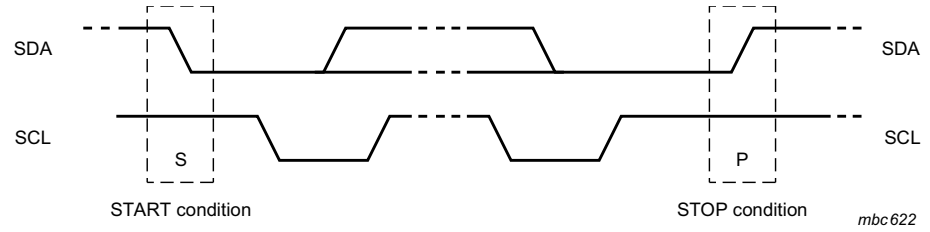


Fig 18. Definition of START and STOP conditions

8.2 System configuration

A device generating a message is a transmitter; a device receiving a message is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves. The system configuration is shown in Figure 19.

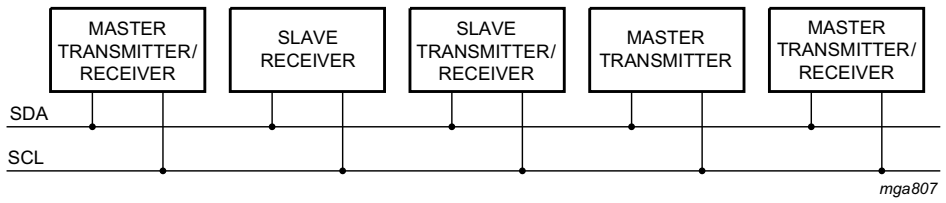


Fig 19. System configuration

8.3 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of 8 bits is followed by an acknowledge cycle.

- A slave receiver which is addressed must generate an acknowledge after the reception of each byte.
- Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be considered).
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the I^2C-bus is shown in Figure 20.

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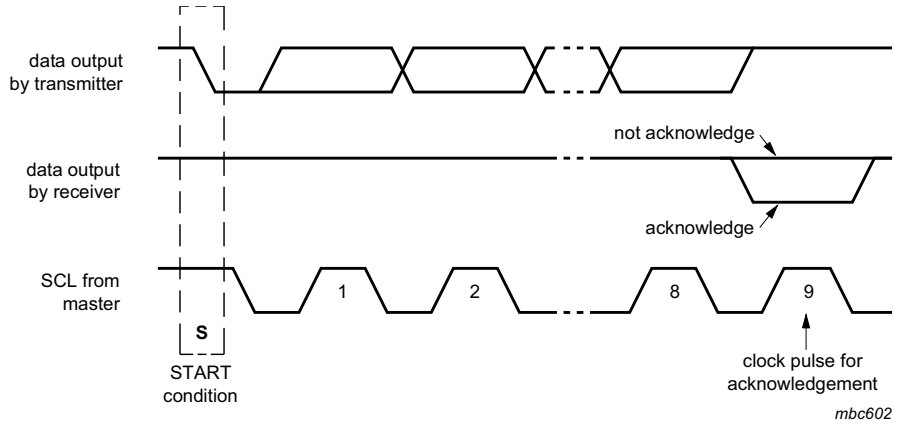


Fig 20. Acknowledgement on the I²C-bus

8.4 I²C-bus controller

The PCA85232 acts as an I²C-bus slave receiver. It does not initiate I²C-bus transfers or transmit data to an I²C-bus master receiver. The only data output from the PCA85232 is the acknowledge signal. Device selection depends on the I²C-bus slave address, on the transferred command data, and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0 and A1 are normally tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0 and A1 are tied to V_{SS} or V_{DD} in accordance with a binary coding scheme. No two devices with a common I²C-bus slave address must have the same hardware subaddress.

8.5 Input filters

To enhance noise immunity in electrical adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

8.6 I²C-bus protocol

Two I²C-bus slave addresses (0111 000 and 0111 001) are reserved for the PCA85232.The entire I²C-bus slave address byte is shown in Table 18.

Table 18. I²C slave address byte

	Slave address							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	MSB							**LSB**
	0	1	1	1	0	0	SA0	R/$\overline{W}$

The PCA85232 is a write-only device and does not respond to a read access, therefore bit 0 should always be logic 0. Bit 1 of the slave address byte, that a PCA85232 responds to, is defined by the level tied to its SA0 input (V_{SS} for logic 0 and V_{DD} for logic 1).

Having two reserved slave addresses allows the following on the same I²C-bus:

- Up to 8 PCA85232 on the same I²C-bus for very large LCD applications

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- The use of two types of LCD multiplex drive modes on the same I²C-bus

The I²C-bus protocol is shown in Figure 21. The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by one of two possible PCA85232 slave addresses available. All PCA85232 with the corresponding SA0 level acknowledge in parallel to the slave address, but all PCA85232 with the alternative SA0 level ignore the whole I²C-bus transfer.

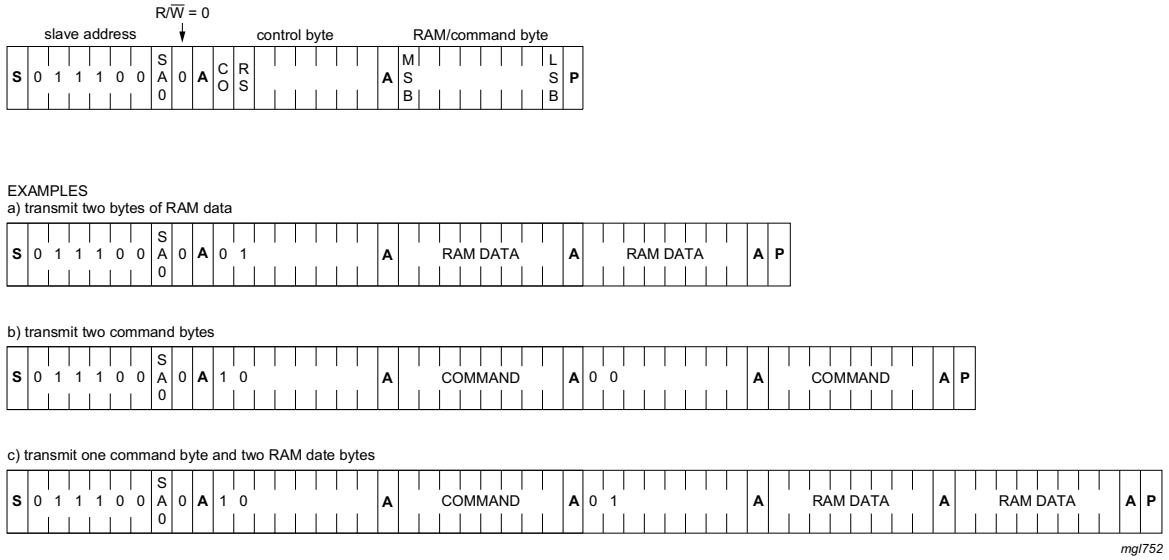


Fig 21. I²C-bus protocol

After acknowledgement, a control byte follows which defines if the next byte is RAM or command information.

Table 19. Control byte description

Bit	Symbol	Value	Description
7	CO		**continue bit**
		0	last control byte
		1	control bytes continue
6	RS		**register selection**
		0	command register
		1	data register
5 to 0	-	-	not relevant

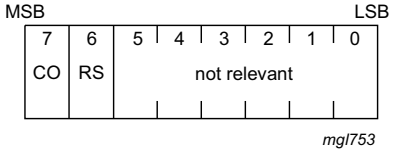


Fig 22. Control byte format

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In this way, it is possible to configure the device and then fill the display RAM with little overhead.

The command bytes and control bytes are also acknowledged by all addressed PCA85232 connected to the bus.

The display bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter; see Section 7.5.1 and Section 7.5.2.

The acknowledgement after each byte is made only by the (A0 and A1) addressed PCA85232. After the last (display) byte, the I^2C-bus master issues a STOP condition (P). Alternatively a repeated START may be asserted to restart an I^2C-bus access.

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9. Internal circuitry

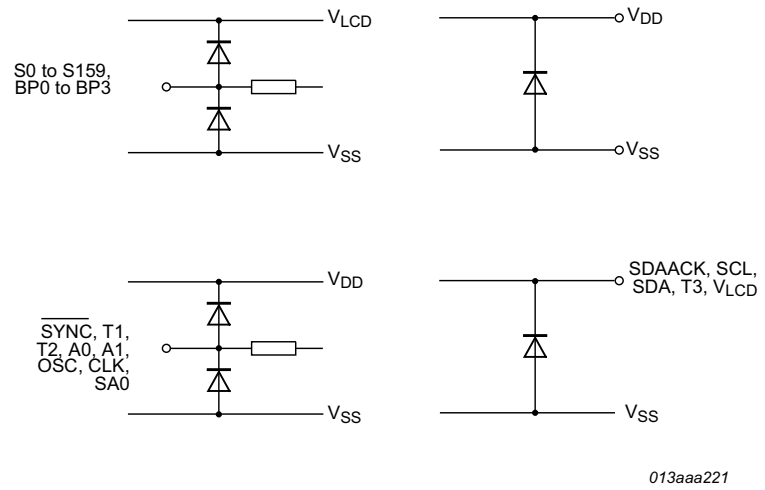


Fig 23. Device protection diagram

10. Safety notes

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

CAUTION



Static voltages across the liquid crystal display can build up when the LCD supply voltage (V_{LCD}) is on while the IC supply voltage (V_{DD}) is off, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts, V_{LCD} and V_{DD} must be applied or removed together.

CAUTION



Semiconductors are light sensitive. Exposure to light sources can cause the IC to malfunction. The IC must be protected against light. The protection must be applied to all sides of the IC.

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11. Limiting values

Table 20. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+6.5	V
I_{DD}	supply current		–50	+50	mA
V_{LCD}	LCD supply voltage		–0.5	+9.0	V
$I_{DD(LCD)}$	LCD supply current		–50	+50	mA
V_I	input voltage	on pins CLK, $\overline{SYNC}$, SA0, OSC, SDA, SCL, A0, A1, T1, T2, and T3	–0.5	+6.5	V
I_I	input current		–10	+10	mA
V_O	output voltage	on pins S0 to S159 and BP0 to BP3	–0.5	+9.0	V
		on pins SDAACK, CLK, $\overline{SYNC}$	–0.5	+6.5	V
I_O	output current		–10	+10	mA
I_{SS}	ground supply current		–50	+50	mA
P_{tot}	total power dissipation		-	400	mW
P/out	power dissipation per output		-	100	mW
V_{ESD}	electrostatic discharge voltage	HBM [2]	-	±4500	V
		MM [3]	-	±300	V
I_{lu}	latch-up current	[4]	-	200	mA
T_{stg}	storage temperature	[5]	–65	+150	°C
T_{amb}	ambient temperature	operating device	–40	+95	°C

[1] Stresses above these values listed may cause permanent damage to the device.

[2] Pass level; Human Body Model (HBM) according to Ref. 6 “JESD22-A114”.

[3] Pass level; Machine Model (MM), according to Ref. 7 “JESD22-A115”.

[4] Pass level; latch-up testing, according to Ref. 8 “JESD78” at maximum ambient temperature ($T_{amb(max)}$).

[5] According to the store and transport requirements (see Ref. 11 “UM10569”) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %.

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12. Static characteristics

Table 21. Static characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 1.8 V to 8.0 V; T_{amb} = −40 °C to +95 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DD}	supply voltage		1.8	-	5.5	V
V_{LCD}	LCD supply voltage		1.8	-	8.0	V
I_{DD}	supply current	$f_{clk(ext)}$ = 3.500 kHz [1][2][3]	-	-	30	µA
		with internal oscillator running [1][3]	-	-	80	µA
$I_{DD(LCD)}$	LCD supply current	$f_{clk(ext)}$ = 3.500 kHz [1][2][4]	-	-	60	µA
		with internal oscillator running [1][4]	-	-	80	µA
Logic[5]						
V_I	input voltage	on pins SDA and SCL	−0.5	-	+5.5	V
		all other input pins	−0.5	-	V_{DD} + 0.5	V
V_{IH}	HIGH-level input voltage	on pins CLK, $\overline{SYNC}$, OSC, A0, A1, SA0, SCL, and SDA	$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage	on pins CLK, $\overline{SYNC}$, OSC, A0, A1, SA0, SCL, and SDA	-	-	$0.3V_{DD}$	V
V_O	output voltage	on pins CLK and $\overline{SYNC}$	−0.5	-	V_{DD} + 0.5	V
		on pin SDAACK	−0.5	-	+5.5	V
V_{OH}	HIGH-level output voltage	on pin $\overline{SYNC}$, CLK	$0.8V_{DD}$	-	V_{DD}	V
V_{OL}	LOW-level output voltage	on pin $\overline{SYNC}$, CLK, SDAACK	V_{SS}	-	$0.2V_{DD}$	V
I_{OH}	HIGH-level output current	output source current; V_{OH} = 4.6 V; V_{DD} = 5 V; on pin CLK	1.5	-	-	mA
I_{OL}	LOW-level output current	output sink current; on pins CLK and $\overline{SYNC}$				
		V_{OL} = 0.4 V; V_{DD} = 5 V	1.5	-	-	mA
		on pin SDAACK				
		$V_{DD} \leq 2$ V; $V_{OL} = 0.2V_{DD}$	3	-	-	mA
		2 V < V_{DD} < 3 V; V_{OL} = 0.4 V	3	-	-	mA
		$V_{DD} \geq 3$ V; V_{OL} = 0.4 V	6	-	-	mA
V_{POR}	power-on reset voltage		1.0	1.3	1.6	V
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}; on pin OSC, CLK, A0, A1, SA0, SDA, and SCL	−1	-	+1	µA

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Table 21. Static characteristics *...continued*

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 1.8 V to 8.0 V; T_{amb} = −40 °C to +95 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LCD outputs						
ΔV_O	output voltage variation	on pins BP0 to BP3 and S0 to S159 [6][7]	−30	-	+30	mV
R_O	output resistance	V_{LCD} = 5 V				
		on pins BP0 to BP3	-	1.5	5	kΩ
		on pins S0 to S159	-	2.0	5	kΩ

[1] LCD outputs are open-circuit; inputs at V_{SS} or V_{DD}; I^2C-bus inactive; V_{LCD} = 8.0 V, V_{DD} = 5.0 V and RAM written with all logic 1.

[2] External clock with 50 % duty factor.

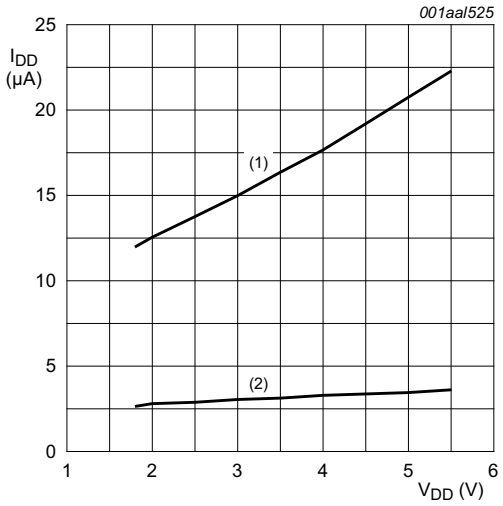
[3] For typical values, see Figure 24.

[4] For typical values, see Figure 25.

[5] The I^2C-bus interface of PCA85232 is 5 V tolerant.

[6] Variation between any 2 backplanes on a given voltage level; static measured.

[7] Variation between any 2 segments on a given voltage level; static measured.



(1) I_{DD} internal is measured with the internal oscillator.

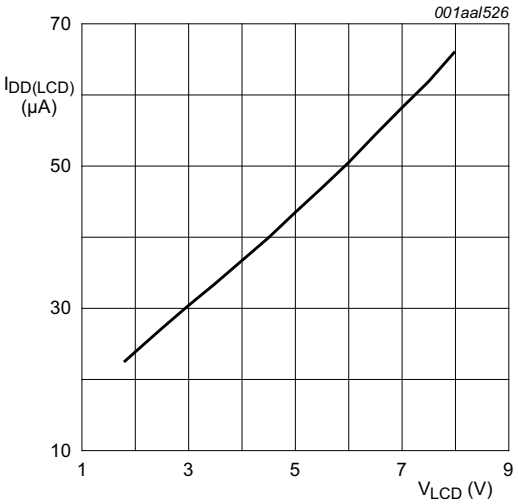
(2) I_{DD} external is measured with an external clock.

T_{amb} = 30 °C; 1:4 multiplex; V_{LCD} = 8 V; all RAM written with logic 1; no display connected.

Fig 24. I_{DD} with respect to V_{DD}

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T_{amb} = 30 °C; 1:4 multiplex; all RAM written with logic 1; no display connected; f_{clk} = 3.5 kHz or $f_{clk(ext)}$ = 3.500 kHz.

Fig 25. $I_{DD(LCD)}$ with respect to V_{LCD}

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13. Dynamic characteristics

Table 22. Dynamic characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 1.8 V to 8.0 V; T_{amb} = −40 °C to +95 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{clk(int)}$	internal clock frequency	on pin CLK; V_{DD} = 5 V ± 0.5 V [1][2][3]	3050	3500	4052	Hz
$f_{clk(ext)}$	external clock frequency	[4]	700	-	5000	Hz
$t_{clk(H)}$	HIGH-level clock time	external clock source used	100	-	-	µs
$t_{clk(L)}$	LOW-level clock time	external clock source used	100	-	-	µs
Δf_{fr}	frame frequency variation	V_{DD} = 5 V ± 0.5 V				
		f_{fr} = 146 Hz; T_{amb} = 30 °C	−5.1	-	+5.1	%
		f_{fr} = 135 Hz; T_{amb} = 95 °C	−6.2	-	+6.9	%
		f_{fr} = 157 Hz; T_{amb} = −40 °C	−7.8	-	+7.6	%
$t_{PD(SYNC_N)}$	$\overline{SYNC}$ propagation delay		-	30	-	ns
t_{SYNC_NL}	$\overline{SYNC}$ LOW time		100	-	-	µs
$t_{PD(drv)}$	driver propagation delay	V_{LCD} = 5 V	-	10	-	µs
Timing characteristics: I²C-bus[5]						
f_{SCL}	SCL clock frequency		-	-	400	kHz
t_{BUF}	bus free time between a STOP and START condition		1.3	-	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		0.6	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	-	-	µs
$t_{VD;ACK}$	data valid acknowledge time		-	-	0.9	µs
t_{LOW}	LOW period of the SCL clock		1.3	-	-	µs
t_{HIGH}	HIGH period of the SCL clock		0.6	-	-	µs
t_f	fall time	of both SDA and SCL signals	-	-	0.3	µs
t_r	rise time	of both SDA and SCL signals	-	-	0.3	µs
C_b	capacitive load for each bus line		-	-	400	pF
$t_{SU;DAT}$	data set-up time		200	-	-	ns
$t_{HD;DAT}$	data hold time		0	-	-	ns
$t_{SU;STO}$	set-up time for STOP condition		0.6	-	-	µs
t_{SP}	pulse width of spikes that must be suppressed by the input filter		-	-	50	ns

[1] Typical output duty factor: 50 % measured at the CLK output pin.

[2] For the respective frame frequency f_{fr}, see Table 12.

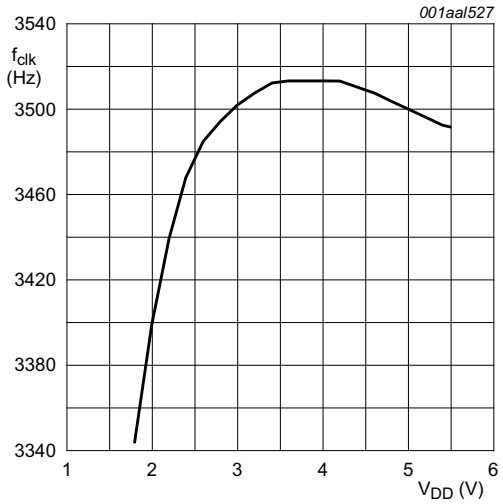
[3] For the characteristics of V_{DD} at a fixed temperature or of the temperature at a fixed V_{DD}, see Figure 26 and Figure 27.

[4] For $f_{clk(ext)}$ > 4 kHz, it is recommended to use an external pull-up resistor between pin $\overline{SYNC}$ and pin V_{DD}. The value of the resistor should be between 100 kΩ and 1 MΩ.

[5] All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

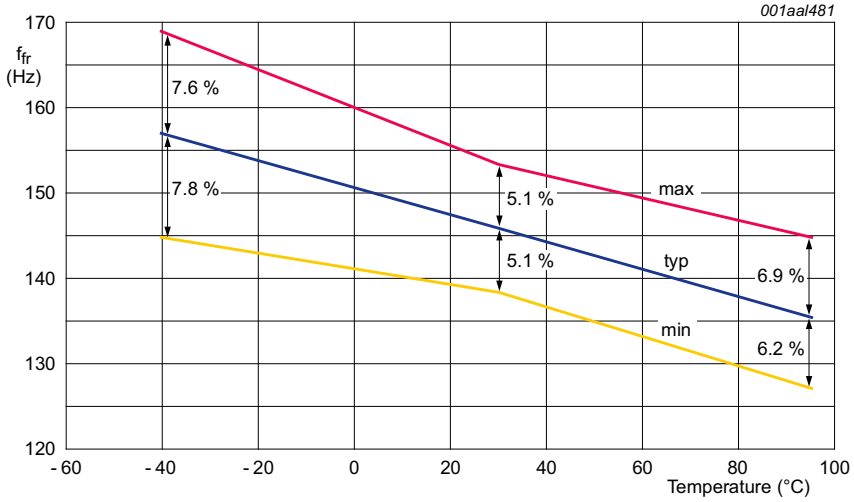
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T_{amb} = 30 °C.

Fig 26. Typical clock frequency (f_{clk}) with respect to V_{DD}



Condition: V_{DD} = 5 V ± 0.5 V; frame frequency prescaler = 011; 146 Hz typical.

The frame frequency is derived from the internal or external clock frequency by Equation 1.

Fig 27. Frame frequency variation

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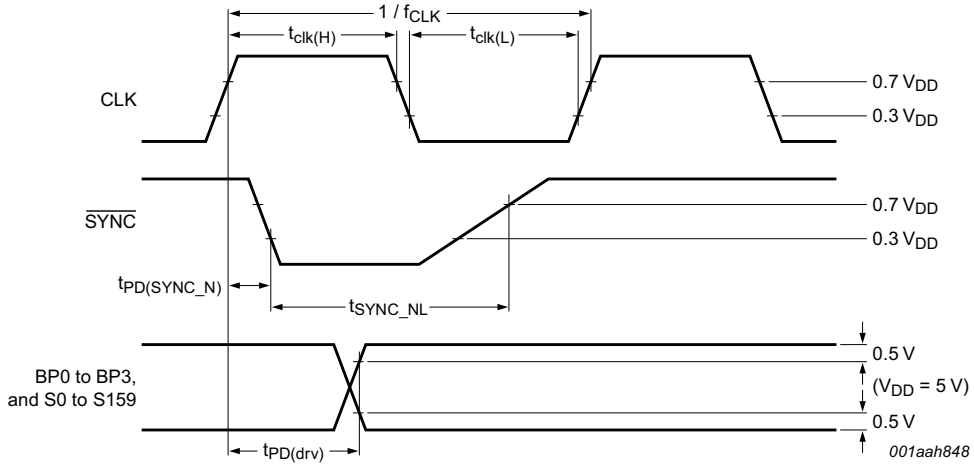


Fig 28. Driver timing waveforms

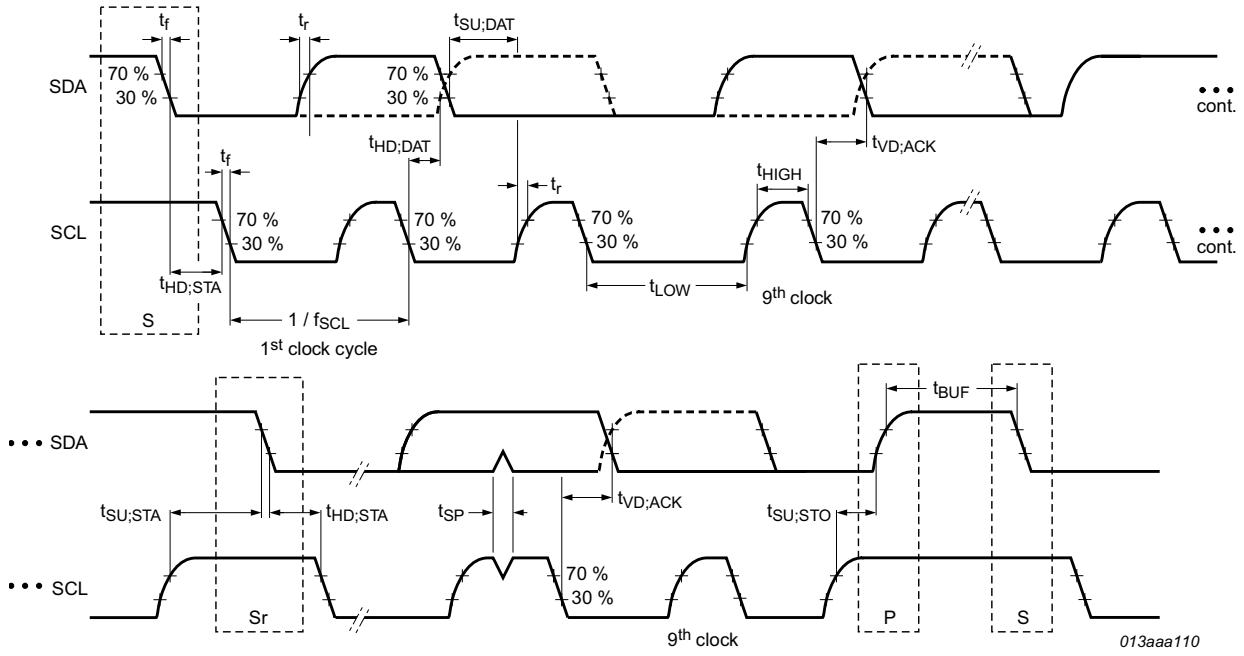


Fig 29. I²C-bus timing waveforms when SDA and SDAACK are connected

14. Application information

14.1 Pull-up resistor sizing on I²C-bus

14.1.1 Max value of pull-up resistor

The bus capacitance (C_b) is the total capacitance of wire, connections, and pins. This capacitance on pin SDA limits the maximum value of the pull-up resistor (R_{PU}) due to the specified rise time.

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According to the I²C-bus specification the rise time (t_r) is defined between the V_{DD}-related input threshold of $V_{IL} = 0.3V_{DD}$ and $V_{IH} = 0.7V_{DD}$. The value for $t_{r(max)}$ is 300 ns.

t_r is calculated with Equation 7:

$$t_r = t2 - t1 \tag{7}$$

whereas t1 and t2 are the time since the charging started. The values for t1 and t2 are derivatives of the functions V(t1) and V(t2):

$$V(t1) = 0.3V_{DD} = V_{DD}(1 - e^{-t1/R_{PU}C_b}) \tag{8}$$

$$V(t2) = 0.7V_{DD} = V_{DD}(1 - e^{-t2/R_{PU}C_b}) \tag{9}$$

with the results of

$$t1 = -R_{PU}C_b \times \ln(0.7) \tag{10}$$

$$t2 = -R_{PU}C_b \times \ln(0.3) \tag{11}$$

$$t_r = -R_{PU}C_b \times \ln(0.3) + R_{PU}C_b \times \ln(0.7) \tag{12}$$

$R_{PU(max)}$ is a function of the rise time (t_r) and the bus capacitance (C_b) and is calculated with Equation 13:

$$R_{PU(max)} = \frac{t_r}{0.8473C_b} = \frac{300 \times 10^{-9}}{0.8473C_b} \tag{13}$$

14.1.2 Min value of pull-up resistor

The supply voltage limits the minimum value of resistor R_{PU} due to the specified minimum sink current (see value of I_{OL} on pin SDAACK in Table 21 on page 35). $R_{PU(min)}$ as a function of V_{DD} is calculated with Equation 14:

$$R_{PU(min)} = \frac{V_{DD} - V_{OL}}{I_{OL}} \tag{14}$$

The designer now has the minimum and maximum value of R_{PU}. The values for $R_{PU(max)}$ and $R_{PU(min)}$ are shown in Figure 30 and Figure 31.

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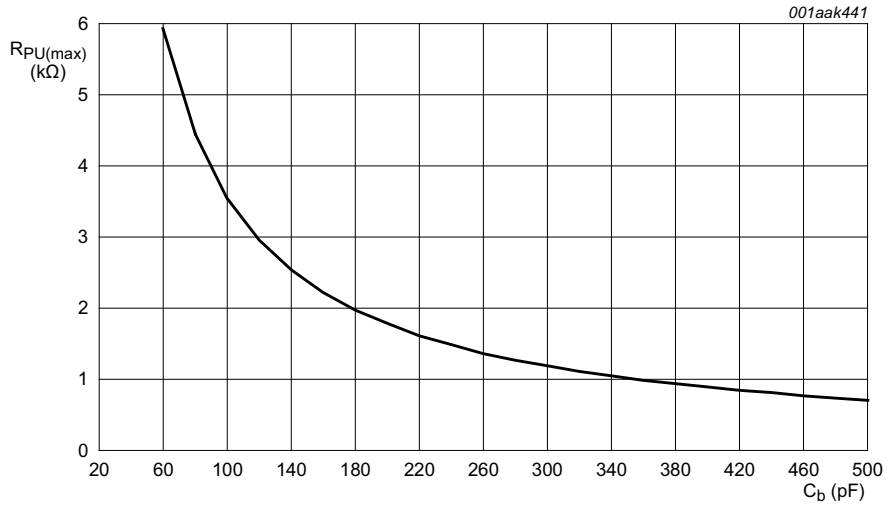


Fig 30. Values for $R_{PU(max)}$

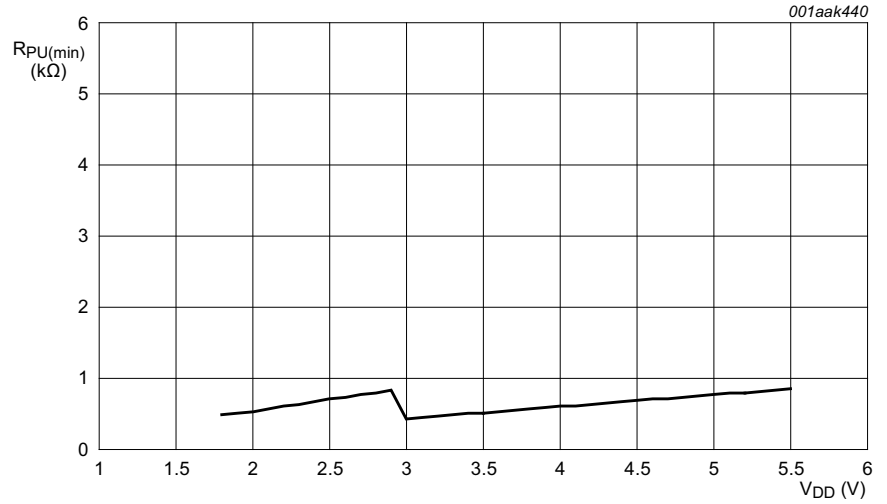


Fig 31. Values for $R_{PU(min)}$

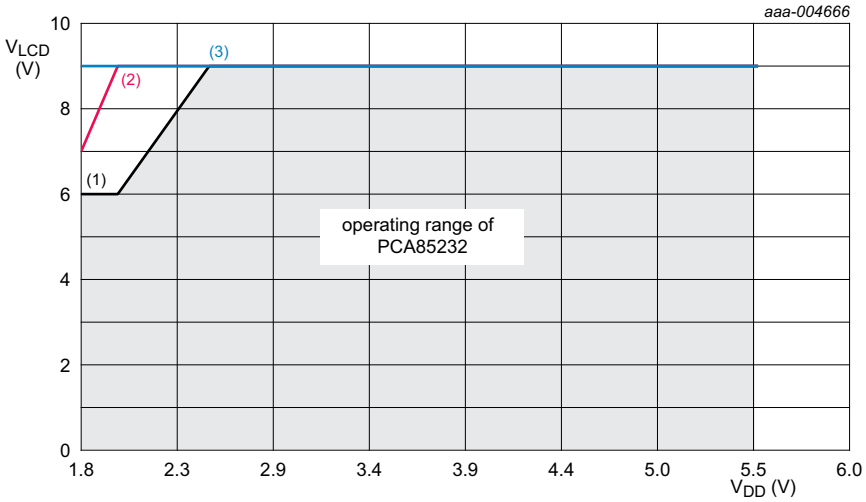
14.2 ITO track resistance

If an application requires to have a low V_{DD} supply voltage compared to the V_{LCD} supply voltage, it is recommended to increase the ITO resistance on the V_{LCD} supply track in order to reduce the noise induced on the V_{SS} line when display is enabled. A low V_{DD} voltage supply and noise peaks on V_{SS} induced by display activities may introduce disturbances into the I^2C communication with the microcontroller.

Figure 32 shows that, when the ITO resistance of the V_{SS} pin has a certain value, it is indicated to have a higher ITO resistance on the V_{LCD} track, especially if V_{LCD} (for example, 9 V) is sharply higher than V_{DD} (for example, 1.8 V). With a higher ITO resistance on the V_{LCD} track, the noise spikes induced to the V_{SS} of the PCA85232 are getting smaller and the functionality is less affected.

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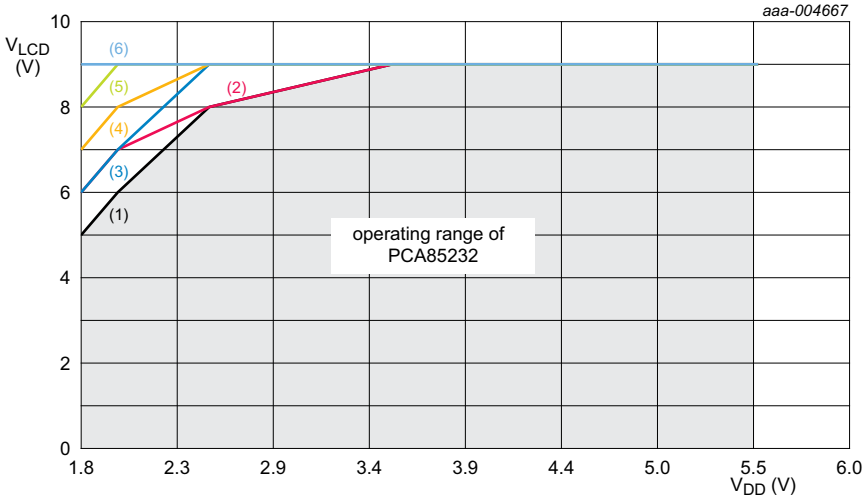
T_{amb} = 25 °C; $R_{ITO(VSS)}$ = 25 Ω; $R_{ITO(VDD)}$ = 50 Ω.

(1) $R_{ITO(VLCD)}$ = 50 Ω.

(2) $R_{ITO(VLCD)}$ = 100 Ω.

(3) $R_{ITO(VLCD)}$ = 150 Ω.

a. Operating range of the PCA85232 with $R_{ITO(VSS)}$ = 25 Ω



T_{amb} = 25 °C; $R_{ITO(VSS)}$ = 50 Ω; $R_{ITO(VDD)}$ = 50 Ω.

(1) $R_{ITO(VLCD)}$ = 50 Ω.

(2) $R_{ITO(VLCD)}$ = 75 Ω.

(3) $R_{ITO(VLCD)}$ = 100 Ω.

(4) $R_{ITO(VLCD)}$ = 150 Ω.

(5) $R_{ITO(VLCD)}$ = 200 Ω.

(6) $R_{ITO(VLCD)}$ = 300 Ω.

b. Operating range of the PCA85232 with $R_{ITO(VSS)}$ = 50 Ω

Fig 32. Operating range of the PCA85232 with respect to the ITO track resistance

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14.3 SDA and SDAACK configuration

The Serial DAta line (SDA) and the I²C-bus acknowledge line (SDAACK) are split. Both lines can be connected together to facilitate a single-line SDA.

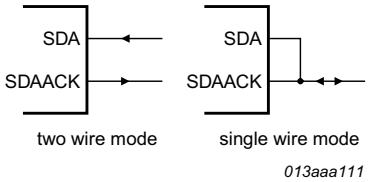


Fig 33. SDA, SDAACK configurations

14.4 Cascaded operation

In large display configurations, up to 8 PCA85232 can be distinguished on the same I²C-bus by using the 2-bit hardware subaddress (A0 and A1) and the programmable I²C-bus slave address (SA0).

Table 23. Addressing cascaded PCA85232

Cluster	Bit SA0	Pin A1	Pin A0	Device
1	0	0	0	0
		0	1	1
		1	0	2
		1	1	3
2	1	0	0	4
		0	1	5
		1	0	6
		1	1	7

When cascaded PCA85232 are synchronized, they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCA85232 of the cascade contributes additional segment outputs.The backplanes can be left open-circuit (as shown in the examples of Figure 34 and Figure 35) or tied together to give enhanced drive capabilities (see Section 7.4.1 on page 21).

For display sizes that are not multiple of 640 elements, a mixed cascaded system can be considered containing only devices like PCA85232 and PCA85133. Depending on the application, one must take care of the software commands compatibility and pin connection compatibility.

The $\overline{\text{SYNC}}$ line is provided to maintain the correct synchronization between all cascaded PCA85232. This synchronization is guaranteed after the Power-On Reset (POR). The only time that $\overline{\text{SYNC}}$ is likely to be needed is if synchronization is accidentally lost (for example, by noise in adverse electrical environments, or by the definition of a multiplex mode when PCA85232 with different SA0 levels are cascaded). $\overline{\text{SYNC}}$ is organized as an input/output pin; the output selection being realized as an open-drain driver with an internal pull-up resistor. A PCA85232 asserts the $\overline{\text{SYNC}}$ line at the onset of its last active

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backplane signal and monitors the $\overline{SYNC}$ line at all other times. Should synchronization in the cascade be lost, it is restored by the first PCA85232 to assert $\overline{SYNC}$. The timing relationship between the backplane waveforms and the $\overline{SYNC}$ signal for the various drive modes of the PCA85232 are shown in Figure 36 on page 48.

When using an external clock signal with high frequencies ($f_{clk(ext)}$ > 4 kHz), it is recommended to have an external pull-up resistor between pin $\overline{SYNC}$ and pin V_{DD} (see Table 22 on page 38). This resistor should be present even when no cascading configuration is used! When using it in a cascaded configuration, care must be taken not to route the $\overline{SYNC}$ signal to close to noisy signals.

The contact resistance between the $\overline{SYNC}$ pads of cascaded devices must be controlled. If the resistance is too high, the device is not able to synchronize properly. This is particularly applicable to COG applications. Table 24 shows the limiting values for contact resistance.

Table 24. $\overline{SYNC}$ contact resistance

Number of devices	Maximum contact resistance
2	6000 Ω
3 to 5	2200 Ω
6 to 8	1200 Ω

In the cascaded applications, the OSC pin of the PCA85232 with subaddress 0 is connected to V_{SS} so that this device uses its internal clock to generate a clock signal at the CLK pin. The other PCA85232 devices are having the OSC pin connected to V_{DD}, meaning that these devices are ready to receive external clock, the signal being provided by the device with subaddress 0.

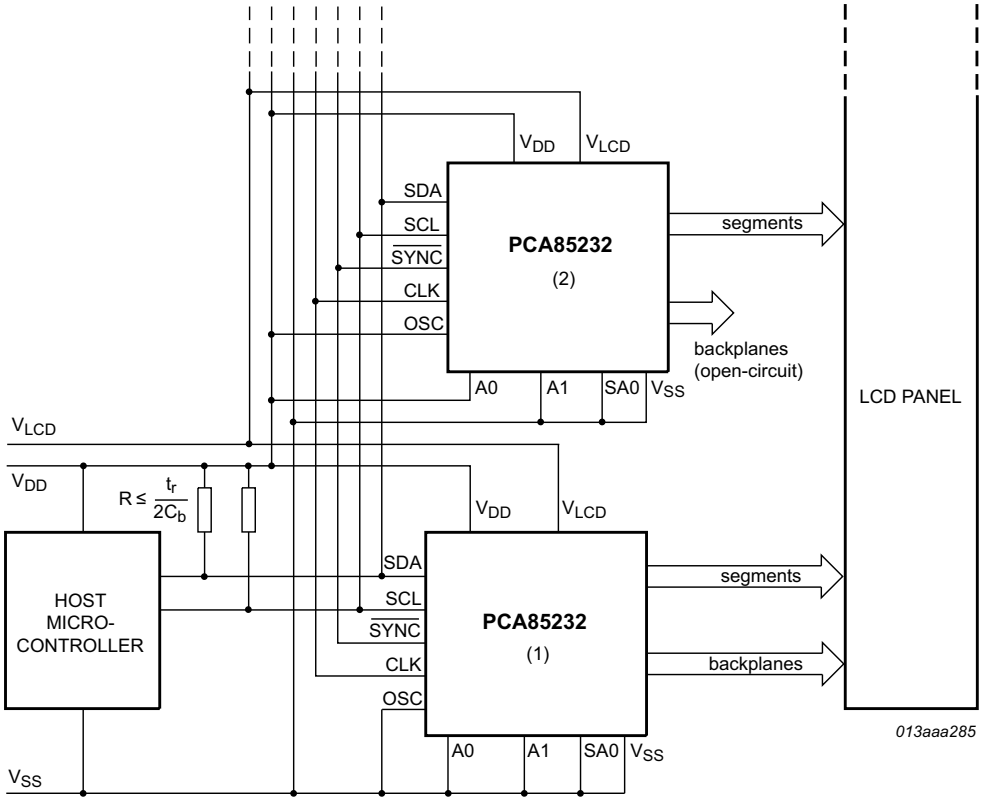
If the master is providing the clock signal to the slave devices, care must be taken that the sending of display enable or disable is received by both, the master and the slaves at the same time. When the display is disabled, the output from pin CLK is disabled too. The disconnection of the clock may result in a DC component for the display.

Alternatively, the schematic can be also constructed such that all the devices have OSC pin connected to V_{DD} and thus an external CLK being provided for the system (all devices connected to the same external CLK).

A configuration where $\overline{SYNC}$ is connected but all PCA85232 are using their internal clock (OSC pin tied to V_{SS}) should not be used and may lead to display artifacts!

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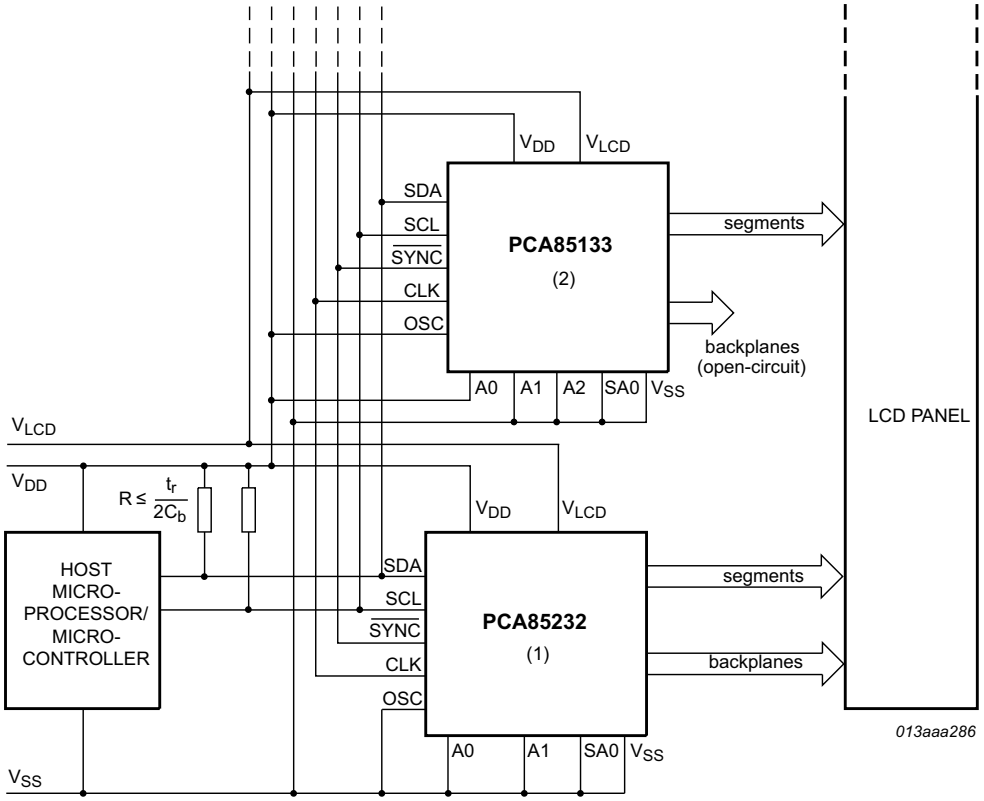
(1) Is master (OSC connected to V_{SS}).

(2) Is slave (OSC connected to V_{DD}).

Fig 34. Cascaded configuration with two PCA85232 using the internal clock of the master

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(1) Is master (OSC connected to V_{SS}).

(2) Is slave (OSC connected to V_{DD}).

Fig 35. Cascaded configuration with one PCA85232 and one PCA85133 using the internal clock of the master

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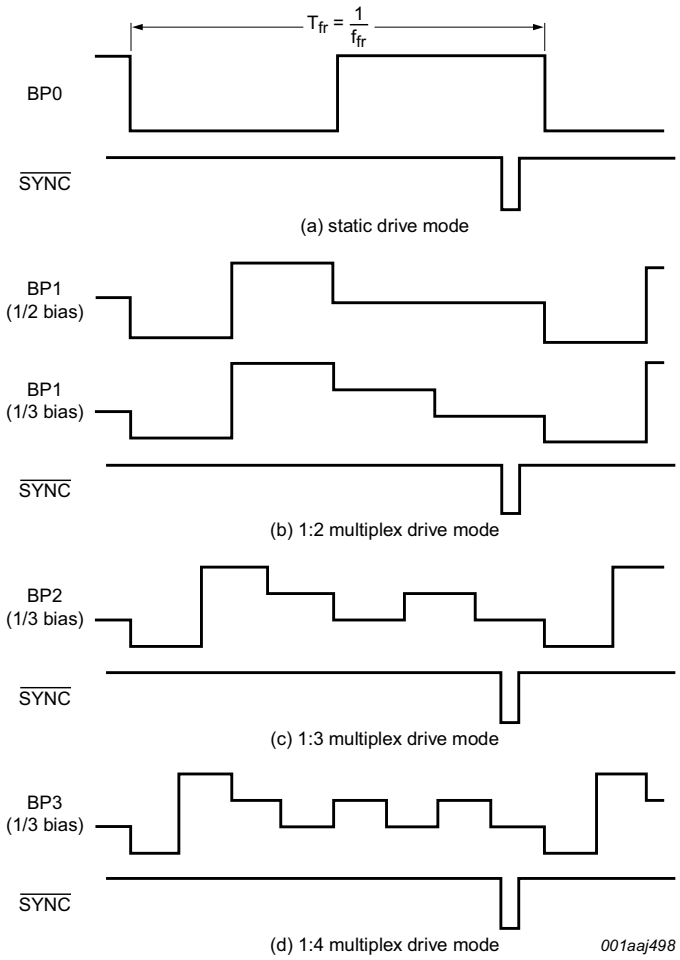


Fig 36. Synchronization of the cascade for the various PCA85232 drive modes

15. Test information

15.1 Quality information

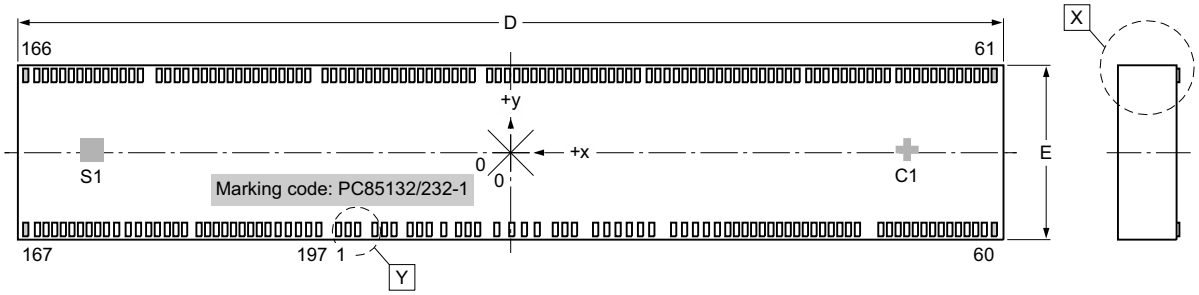
This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

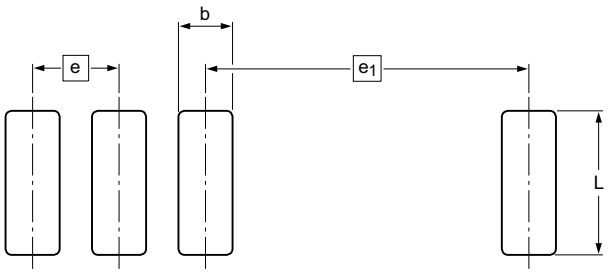
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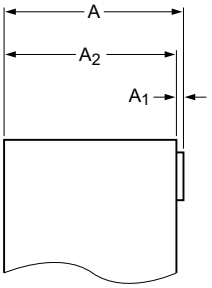
16. Bare die outline

Bare die; 197 bumps; 6.5 x 1.16 x 0.40 mm **PCA85232U**

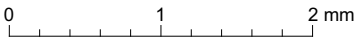




detail Y



detail X



Dimensions

Unit		$A^{(1)}$	$A_1{}^{(1)}$	$A_2{}^{(1)}$	$b^{(1)}$	D	E	$e^{(1)}$	$e_1{}^{(1)}$	$L^{(1)}$
mm	max		0.018							
	nom	0.40	0.015	0.380	0.0338	6.5	1.16	0.054	0.2025	0.090
	min		0.012							

Note
1. Dimension not drawn to scale.

pca85232_do

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
PCA85232U						~~11-09-19~~ 12-03-22

Fig 37. Bare die outline of PCA85232

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Table 25. Bump locations

All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip; see Figure 37.

Symbol	Bump	X (μm)	Y (μm)	Symbol	Bump	X (μm)	Y (μm)
SDAACK	1	−1165.3	−481.5	S68	100	750.2	481.5
SDAACK	2	−1111.3	−481.5	S69	101	696.2	481.5
SDAACK	3	−1057.3	−481.5	S70	102	642.2	481.5
SDA	4	−854.8	−481.5	S71	103	588.2	481.5
SDA	5	−800.8	−481.5	S72	104	534.2	481.5
SDA	6	−746.8	−481.5	S73	105	480.2	481.5
SCL	7	−575.8	−481.5	S74	106	426.2	481.5
SCL	8	−521.8	−481.5	S75	107	372.2	481.5
SCL	9	−467.8	−481.5	S76	108	318.2	481.5
CLK	10	−316.2	−481.5	S77	109	264.2	481.5
V_{DD}	11	−204.1	−481.5	S78	110	210.2	481.5
V_{DD}	12	−150.1	−481.5	S79	111	156.2	481.5
V_{DD}	13	−96.1	−481.5	BP0	112	86.8	481.5
$\overline{SYNC}$	14	6.9	−481.5	BP2	113	32.8	481.5
OSC	15	119.4	−481.5	BP1	114	−21.2	481.5
T1	16	203.1	−481.5	BP3	115	−75.2	481.5
T2	17	286.8	−481.5	S80	116	−190.7	481.5
T3	18	389.9	−481.5	S81	117	−244.7	481.5
T3	19	443.9	−481.5	S82	118	−298.7	481.5
T3	20	497.9	−481.5	S83	119	−352.7	481.5
A0	21	640.5	−481.5	S84	120	−406.7	481.5
A1	22	724.2	−481.5	S85	121	−460.7	481.5
SA0	23	807.9	−481.5	S86	122	−514.7	481.5
V_{SS}	24	893.0	−481.5	S87	123	−568.7	481.5
V_{SS}	25	947.0	−481.5	S88	124	−622.7	481.5
V_{SS}	26	1001.0	−481.5	S89	125	−676.7	481.5
V_{LCD}	27	1107.2	−481.5	S90	126	−730.7	481.5
V_{LCD}	28	1161.2	−481.5	S91	127	−784.7	481.5
V_{LCD}	29	1215.2	−481.5	S92	128	−838.7	481.5
BP2	30	1303.4	−481.5	S93	129	−892.7	481.5
BP0	31	1357.4	−481.5	S94	130	−946.7	481.5
S0	32	1411.4	−481.5	S95	131	−1000.7	481.5
S1	33	1465.4	−481.5	S96	132	−1054.7	481.5
S2	34	1519.4	−481.5	S97	133	−1108.7	481.5
S3	35	1573.4	−481.5	S98	134	−1224.2	481.5
S4	36	1627.4	−481.5	S99	135	−1278.2	481.5
S5	37	1681.4	−481.5	S100	136	−1332.2	481.5
S6	38	1735.4	−481.5	S101	137	−1386.2	481.5
S7	39	1789.4	−481.5	S102	138	−1440.2	481.5

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Table 25. Bump locations *...continued*

All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip; see Figure 37.

Symbol	Bump	X (μm)	Y (μm)	Symbol	Bump	X (μm)	Y (μm)
S8	40	1843.4	−481.5	S103	139	−1494.2	481.5
S9	41	1897.4	−481.5	S104	140	−1548.2	481.5
S10	42	1951.4	−481.5	S105	141	−1602.2	481.5
S11	43	2005.4	−481.5	S106	142	−1656.2	481.5
S12	44	2059.4	−481.5	S107	143	−1710.2	481.5
S13	45	2113.4	−481.5	S108	144	−1764.2	481.5
S14	46	2167.4	−481.5	S109	145	−1818.2	481.5
S15	47	2221.4	−481.5	S110	146	−1872.2	481.5
S16	48	2363.9	−481.5	S111	147	−1926.2	481.5
S17	49	2417.9	−481.5	S112	148	−1980.2	481.5
S18	50	2471.9	−481.5	S113	149	−2034.2	481.5
S19	51	2525.9	−481.5	S114	150	−2088.2	481.5
S20	52	2579.9	−481.5	S115	151	−2142.2	481.5
S21	53	2633.9	−481.5	S116	152	−2284.7	481.5
S22	54	2687.9	−481.5	S117	153	−2338.7	481.5
S23	55	2741.9	−481.5	S118	154	−2392.7	481.5
S24	56	2795.9	−481.5	S119	155	−2446.7	481.5
S25	57	2849.9	−481.5	S120	156	−2500.7	481.5
S26	58	2903.9	−481.5	S121	157	−2554.7	481.5
S27	59	2957.9	−481.5	S122	158	−2608.7	481.5
S28	60	3011.9	−481.5	S123	159	−2662.7	481.5
S29	61	3067.7	481.5	S124	160	−2716.7	481.5
S30	62	3013.7	481.5	S125	161	−2770.7	481.5
S31	63	2959.7	481.5	S126	162	−2824.7	481.5
S32	64	2905.7	481.5	S127	163	−2878.7	481.5
S33	65	2851.7	481.5	S128	164	−2932.7	481.5
S34	66	2797.7	481.5	S129	165	−2986.7	481.5
S35	67	2743.7	481.5	S130	166	−3040.7	481.5
S36	68	2689.7	481.5	S131	167	−3025.2	−481.5
S37	69	2635.7	481.5	S132	168	−2971.2	−481.5
S38	70	2520.2	481.5	S133	169	−2917.2	−481.5
S39	71	2466.2	481.5	S134	170	−2863.2	−481.5
S40	72	2412.2	481.5	S135	171	−2809.2	−481.5
S41	73	2358.2	481.5	S136	172	−2755.2	−481.5
S42	74	2304.2	481.5	S137	173	−2701.2	−481.5
S43	75	2250.2	481.5	S138	174	−2647.2	−481.5
S44	76	2196.2	481.5	S139	175	−2593.2	−481.5
S45	77	2142.2	481.5	S140	176	−2539.2	−481.5
S46	78	2088.2	481.5	S141	177	−2485.2	−481.5

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Table 25. Bump locations *...continued*

All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip; see Figure 37.

Symbol	Bump	X (μm)	Y (μm)	Symbol	Bump	X (μm)	Y (μm)
S47	79	2034.2	481.5	S142	178	−2431.2	−481.5
S48	80	1891.7	481.5	S143	179	−2377.2	−481.5
S49	81	1837.7	481.5	S144	180	−2234.7	−481.5
S50	82	1783.7	481.5	S145	181	−2180.7	−481.5
S51	83	1729.7	481.5	S146	182	−2126.7	−481.5
S52	84	1675.7	481.5	S147	183	−2072.7	−481.5
S53	85	1621.7	481.5	S148	184	−2018.7	−481.5
S54	86	1567.7	481.5	S149	185	−1964.7	−481.5
S55	87	1513.7	481.5	S150	186	−1910.7	−481.5
S56	88	1459.7	481.5	S151	187	−1856.7	−481.5
S57	89	1405.7	481.5	S152	188	−1802.7	−481.5
S58	90	1351.7	481.5	S153	189	−1748.7	−481.5
S59	91	1297.7	481.5	S154	190	−1694.7	−481.5
S60	92	1243.7	481.5	S155	191	−1640.7	−481.5
S61	93	1189.7	481.5	S156	192	−1586.7	−481.5
S62	94	1135.7	481.5	S157	193	−1532.7	−481.5
S63	95	1081.7	481.5	S158	194	−1478.7	−481.5
S64	96	1027.7	481.5	S159	195	−1424.7	−481.5
S65	97	973.7	481.5	BP3	196	−1370.7	−481.5
S66	98	858.2	481.5	BP1	197	−1316.7	−481.5
S67	99	804.2	481.5				

The dummy pins are connected to the segments shown (see Table 26) but are not tested.

Table 26. Dummy bumps

All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip; see Figure 37 on page 49.

Symbol	Connected to pin	X (μm)	Y (μm)
D1	S131	−3079.2	−481.5
D2	S28	3065.9	−481.5
D3	S29	3121.7	481.5
D4	S130	−3094.7	481.5

The alignment marks are shown in Table 27.

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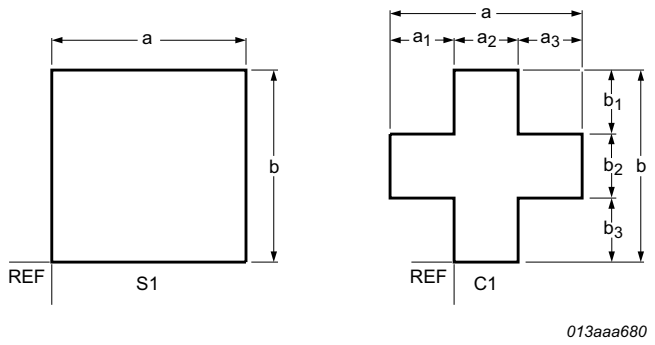


Fig 38. Alignment marks

Table 27. Alignment marks

All x/y coordinates represent the position of the REF point (see Figure 38) with respect to the center (x/y = 0) of the chip; see Figure 37 on page 49.

a	a_1	a_2	a_3	b	b_1	b_2	b_3	Coordinates		Unit
								X	Y	
Alignment mark S1										
121.5	-	-	-	121.5	-	-	-	–2733.75	–47.25	µm
Alignment mark C1										
121.5	36.45	48.6	36.45	121.5	36.45	48.6	36.45	2603.7	–47.25	µm

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17. Packing information

17.1 Tray information

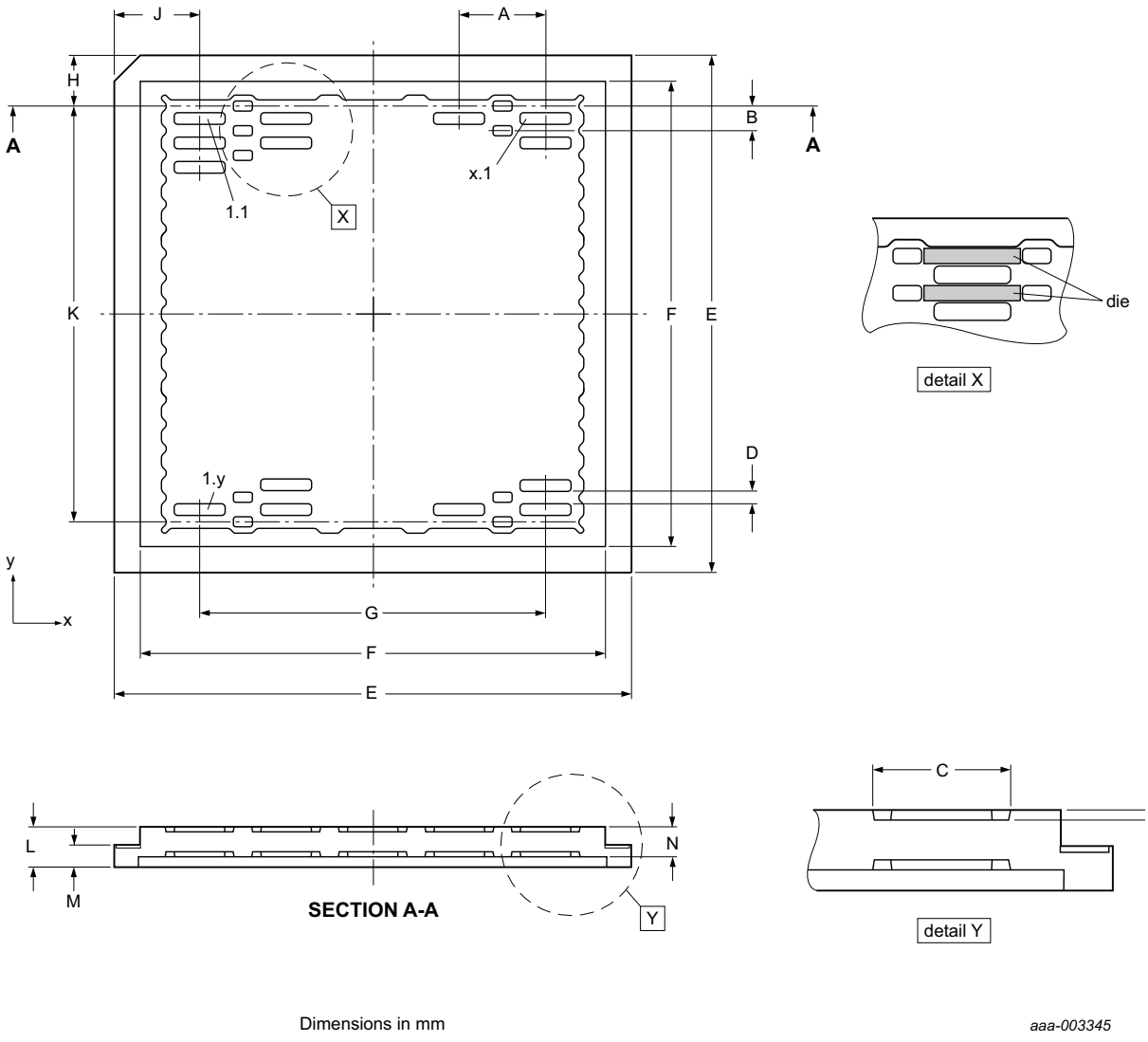


Fig 39. Tray details

Table 28. Description of tray details

Tray details are shown in Figure 39.

Tray details														
Dimensions														
A	B	C	D	E	F	G	H	J	K	L	M	N	O	Unit
8.50	2.40	6.596	1.259	50.8	45.72	34.0	5.0	8.40	40.80	3.96	2.18	2.49	0.5	mm
Number of pockets														
x direction							y direction							
5							18							

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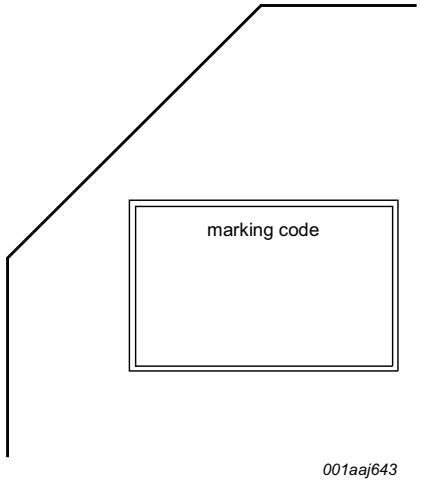


Fig 40. Tray alignment

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18. Appendix

18.1 LCD segment driver selection

Table 29. Selection of LCD segment drivers

Type name	Number of elements at MUX							V_{DD} (V)	V_{LCD} (V)	f_{fr} (Hz)	V_{LCD} (V) charge pump	V_{LCD} (V) temperature compensat.	T_{amb} (°C)	Interface	Package	AEC-Q100
	1:1	1:2	1:3	1:4	1:6	1:8	1:9									
PCA8553DTT	40	80	120	160	-	-	-	1.8 to 5.5	1.8 to 5.5	32 to 256[1]	N	N	–40 to 105	I^2C / SPI	TSSOP56	Y
PCA8546ATT	-	-	-	176	-	-	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	–40 to 95	I^2C	TSSOP56	Y
PCA8546BTT	-	-	-	176	-	-	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	–40 to 95	SPI	TSSOP56	Y
PCA8547AHT	44	88	-	176	-	-	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	–40 to 95	I^2C	TQFP64	Y
PCA8547BHT	44	88	-	176	-	-	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	–40 to 95	SPI	TQFP64	Y
PCF85134HL	60	120	180	240	-	-	-	1.8 to 5.5	2.5 to 6.5	82	N	N	–40 to 85	I^2C	LQFP80	N
PCA85134H	60	120	180	240	-	-	-	1.8 to 5.5	2.5 to 8	82	N	N	–40 to 95	I^2C	LQFP80	Y
PCA8543AHL	60	120	-	240	-	-	-	2.5 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	–40 to 105	I^2C	LQFP80	Y
PCF8545ATT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 5.5	60 to 300[1]	N	N	–40 to 85	I^2C	TSSOP56	N
PCF8545BTT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 5.5	60 to 300[1]	N	N	–40 to 85	SPI	TSSOP56	N
PCF8536AT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	–40 to 85	I^2C	TSSOP56	N
PCF8536BT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	–40 to 85	SPI	TSSOP56	N
PCA8536AT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	–40 to 95	I^2C	TSSOP56	Y
PCA8536BT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	–40 to 95	SPI	TSSOP56	Y
PCF8537AH	44	88	-	176	276	352	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	–40 to 85	I^2C	TQFP64	N
PCF8537BH	44	88	-	176	276	352	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	–40 to 85	SPI	TQFP64	N
PCA8537AH	44	88	-	176	276	352	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	–40 to 95	I^2C	TQFP64	Y
PCA8537BH	44	88	-	176	276	352	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	–40 to 95	SPI	TQFP64	Y
PCA9620H	60	120	-	240	320	480	-	2.5 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	–40 to 105	I^2C	LQFP80	Y
PCA9620U	60	120	-	240	320	480	-	2.5 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	–40 to 105	I^2C	Bare die	Y
PCF8576DU	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 6.5	77	N	N	–40 to 85	I^2C	Bare die	N
PCF8576EUG	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 6.5	77	N	N	–40 to 85	I^2C	Bare die	N
PCA8576FUG	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 8	200	N	N	–40 to 105	I^2C	Bare die	Y
PCF85133U	80	160	240	320	-	-	-	1.8 to 5.5	2.5 to 6.5	82, 110[2]	N	N	–40 to 85	I^2C	Bare die	N
PCA85133U	80	160	240	320	-	-	-	1.8 to 5.5	2.5 to 8	82, 110[2]	N	N	–40 to 95	I^2C	Bare die	Y

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Table 29. Selection of LCD segment drivers *...continued*

Type name	Number of elements at MUX							V_{DD} (V)	V_{LCD} (V)	f_{fr} (Hz)	V_{LCD} (V) charge pump	V_{LCD} (V) temperature compensat.	T_{amb} (°C)	Interface	Package	AEC-Q100
	1:1	1:2	1:3	1:4	1:6	1:8	1:9									
PCA85233UG	80	160	240	320	-	-	-	1.8 to 5.5	2.5 to 8	150, 220[2]	N	N	–40 to 105	I^2C	Bare die	Y
PCF85132U	160	320	480	640	-	-	-	1.8 to 5.5	1.8 to 8	60 to 90[1]	N	N	–40 to 85	I^2C	Bare die	N
PCA8530DUG	102	204	-	408	-	-	-	2.5 to 5.5	4 to 12	45 to 300[1]	Y	Y	–40 to 105	I^2C / SPI	Bare die	Y
PCA85132U	160	320	480	640	-	-	-	1.8 to 5.5	1.8 to 8	60 to 90[1]	N	N	–40 to 95	I^2C	Bare die	Y
PCA85232U	160	320	480	640	-	-	-	1.8 to 5.5	1.8 to 8	117 to 176[1]	N	N	–40 to 95	I^2C	Bare die	Y
PCF8538UG	102	204	-	408	612	816	918	2.5 to 5.5	4 to 12	45 to 300[1]	Y	Y	–40 to 85	I^2C / SPI	Bare die	N
PCA8538UG	102	204	-	408	612	816	918	2.5 to 5.5	4 to 12	45 to 300[1]	Y	Y	–40 to 105	I^2C / SPI	Bare die	Y

[1] Software programmable.

[2] Hardware selectable.

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19. Abbreviations

Table 30. Abbreviations

Acronym	Description
AEC	Automotive Electronics Council
COG	Chip-On-Glass
DC	Direct Current
HBM	Human Body Model
I^2C	Inter-Integrated Circuit
IC	Integrated Circuit
ITO	Indium Tin Oxide
LCD	Liquid Crystal Display
LSB	Least Significant Bit
MM	Machine Model
MSB	Most Significant Bit
POR	Power-On Reset
RC	Resistance and Capacitance
RAM	Random Access Memory
RMS	Root Mean Square
SCL	Serial CLock line
SDA	Serial DAta line

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20. References

[1] **AN10170 —** Design guidelines for COG modules with NXP monochrome LCD drivers

[2] **AN10706 —** Handling bare die

[3] **AN11267 —** EMC and system level ESD design guidelines for LCD drivers

[4] **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[5] **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

[6] **JESD22-A114 —** Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[7] **JESD22-A115 —** Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)

[8] **JESD78 —** IC Latch-Up Test

[9] **JESD625-A —** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

[10] **UM10204 —** I^2C-bus specification and user manual

[11] **UM10569 —** Store and transport requirements

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21. Revision history

Table 31. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA85232 v.4	20150408	Product data sheet	-	PCA85232 v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Changed description of backplane connections when cascading			
PCA85232 v.3	20130711	Product data sheet	-	PCA85232 v.2
PCA85232 v.2	20120905	Product data sheet	-	PCA85232 v.1
PCA85232 v.1	20101208	Product data sheet	-	-

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22. Legal information

22.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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