PCA6408A

Low-voltage, 8-bit I²C-bus and SMBus I/O expander with interrupt output, reset, and configuration registers

Rev. 1 — 27 September 2012 Product data sheet

1. General description

The PCA6408A is an 8-bit general purpose I/O expander that provides remote I/O expansion for most microcontroller families via the I²C-bus interface.

NXP I/O expanders provide a simple solution when additional I/Os are needed while keeping interconnections to a minimum, for example, in battery-powered mobile applications for interfacing to sensors, push buttons, keypad, etc. In addition to providing a flexible set of GPIOs, it simplifies interconnection of a processor running at one voltage level to I/O devices operating at a different (usually higher) voltage level. The PCA6408A has built-in level shifting feature that makes these devices extremely flexible in mixed signal environments where communication between incompatible I/O voltages is required. Its wide V_{DD} range of 1.65 V to 5.5 V on the dual power rail allows seamless communications with next-generation low voltage microprocessors and microcontrollers on the interface side (SDA/SCL) and peripherals at a higher voltage on the port side.

There are two supply voltages for PCA6408A: $V_{DD(I2C\text{-}bus)}$ and $V_{DD(P)}$. $V_{DD(I2C\text{-}bus)}$ provides the supply voltage for the interface at the master side (for example, a microcontroller) and the $V_{DD(P)}$ provides the supply for core circuits and Port P. The bidirectional voltage level translation in the PCA6408A is provided through $V_{DD(I2C\text{-}bus)}$. $V_{DD(I2C\text{-}bus)}$ should be connected to the V_{DD} of the external SCL/SDA lines. This indicates the V_{DD} level of the I²C-bus to the PCA6408A. The voltage level on Port P of the PCA6408A is determined by the $V_{DD(P)}$.

The PCA6408A consists of one 8-bit Configuration (input or output selection), Input, Output, and Polarity Inversion (active HIGH) register. At power-on, the I/Os are configured as inputs. However, the system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input or Output register. The polarity of the Input port register can be inverted with the Polarity Inversion register, saving interrupts.

The system master can reset the PCA6408A in the event of a time-out or other improper operation by asserting a LOW in the $\overline{\text{RESET}}$ input. The power-on reset puts the registers in their default state and initializes the I²C-bus/SMBus state machine. The $\overline{\text{RESET}}$ pin causes the same reset/initialization to occur without de-powering the part.

The PCA6408A open-drain interrupt ($\overline{\text{INT}}$) output is activated when any input state differs from its corresponding Input port register state and is used to indicate to the system master that an input state has changed.

$\overline{\text{INT}}$ can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I²C-bus. Thus, the PCA6408A can remain a simple slave device.

The device Port P outputs have 25 mA sink capabilities for directly driving LEDs while consuming low device current.

One hardware pin (ADDR) can be used to program and vary the fixed I²C-bus address and allow up to two devices to share the same I²C-bus or SMBus.

2. Features and benefits

- I²C-bus to parallel port expander
- Operating power supply voltage range of 1.65 V to 5.5 V
- Allows bidirectional voltage-level translation and GPIO expansion between:
  - 1.8 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V or 5 V Port P
  - 2.5 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V or 5 V Port P
  - 3.3 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V or 5 V Port P
  - 5 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V or 5 V Port P
- Low standby current consumption of 1 μA
- Schmitt-trigger action allows slow input transition and better switching noise immunity at the SCL and SDA inputs
  - V_{hys} = 0.18 V (typical) at 1.8 V
  - V_{hys} = 0.25 V (typical) at 2.5 V
  - V_{hys} = 0.33 V (typical) at 3.3 V
  - V_{hys} = 0.5 V (typical) at 5 V
- 5 V tolerant I/O ports
- Active LOW reset input ($\overline{RESET}$)
- Open-drain active LOW interrupt output ($\overline{INT}$)
- 400 kHz Fast-mode I²C-bus
- Input/Output Configuration register
- Polarity Inversion register
- Internal power-on reset
- Power-up with all channels configured as inputs
- No glitch on power-up
- Noise filter on SCL/SDA inputs
- Latched outputs with 25 mA drive maximum capability for directly driving LEDs
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD protection exceeds JESD 22
  - 2000 V Human-Body Model (A114-A)
  - 1000 V Charged-Device Model (C101)
- Packages offered: HVQFN16, TSSOP16, XQFN16

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3. Ordering information

Table 1. Ordering information

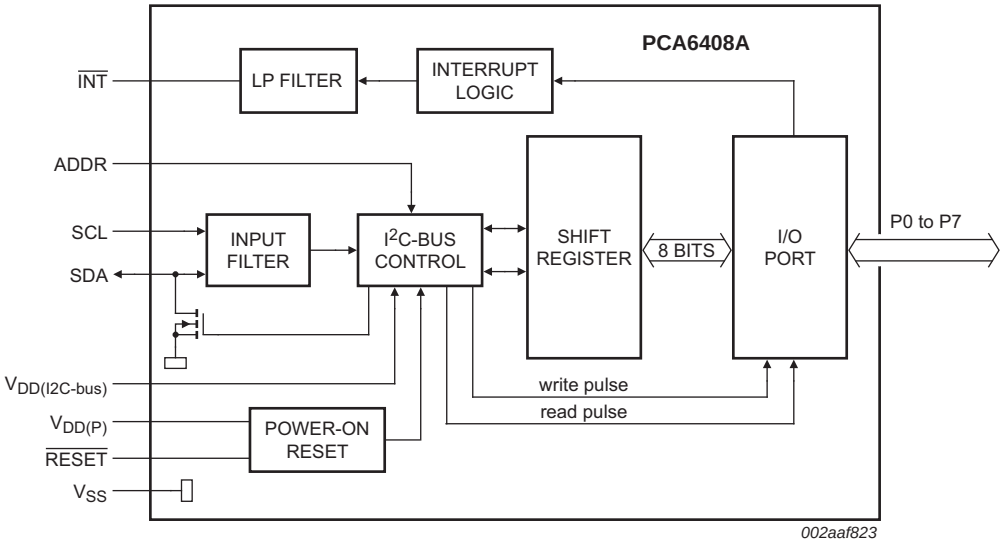
Type number	Topside mark	Package		
		Name	Description	Version
PCA6408ABS	P8A	HVQFN16	plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 × 3 × 0.85 mm	SOT758-1
PCA6408APW	PA6408A	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
PCA6408AHK	P8	XQFN16	plastic, extremely thin quad flat package; no leads; 16 terminals; body 1.80 × 2.60 × 0.50 mm	SOT1161-1

3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCA6408ABS	PCA6408ABSHP	HVQFN16	Reel pack, SMD, 13-inch, Turned	6000	T_{amb} = −40 °C to +85 °C
PCA6408APW	PCA6408APW,118	TSSOP16	Reel pack, SMD, 13-inch	2500	T_{amb} = −40 °C to +85 °C
PCA6408AHK	PCA6408AHKX	XQFN16	Reel pack, SMD	4000	T_{amb} = −40 °C to +85 °C

4. Block diagram



All I/Os are set to inputs at reset.

Fig 1. Block diagram (positive logic)

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5. Pinning information

5.1 Pinning

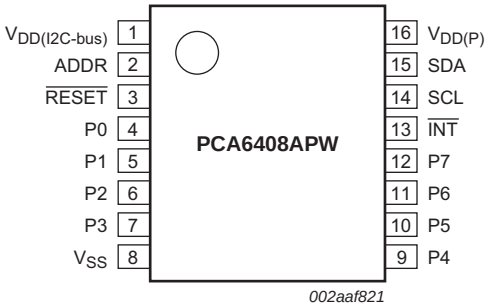
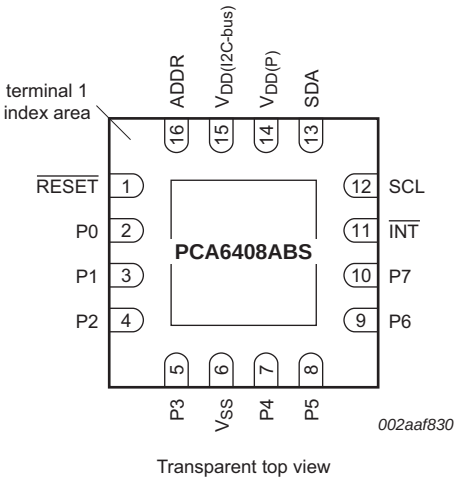


Fig 2. Pin configuration for TSSOP16



The exposed center pad, if used, must be connected only as a secondary V_{SS} or must be left electrically open.

Fig 3. Pin configuration for HVQFN16

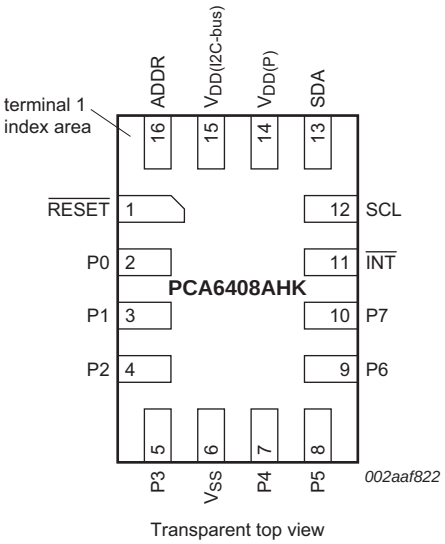


Fig 4. Pin configuration for XQFN16

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5.2 Pin description

Table 3. Pin description

Symbol	Pin			Description
	TSSOP16	HVQFN16	XQFN16	
$V_{DD(I2C\text{-}bus)}$	1	15	15	Supply voltage of I²C-bus. Connect directly to the V_{DD} of the external I²C master. Provides voltage-level translation.
ADDR	2	16	16	Address input. Connect directly to $V_{DD(P)}$ or ground.
$\overline{RESET}$	3	1	1	Active LOW reset input. Connect to $V_{DD(I2C\text{-}bus)}$ through a pull-up resistor if no active connection is used.
P0[1]	4	2	2	Port P input/output 0.
P1[1]	5	3	3	Port P input/output 1.
P2[1]	6	4	4	Port P input/output 2.
P3[1]	7	5	5	Port P input/output 3.
V_{SS}	8	6	6	Ground.
P4[1]	9	7	7	Port P input/output 4.
P5[1]	10	8	8	Port P input/output 5.
P6[1]	11	9	9	Port P input/output 6.
P7[1]	12	10	10	Port P input/output 7.
$\overline{INT}$	13	11	11	Interrupt output. Connect to $V_{DD(I2C\text{-}bus)}$ through a pull-up resistor.
SCL	14	12	12	Serial clock bus. Connect to $V_{DD(I2C\text{-}bus)}$ through a pull-up resistor.
SDA	15	13	13	Serial data bus. Connect to $V_{DD(I2C\text{-}bus)}$ through a pull-up resistor.
$V_{DD(P)}$	16	14	14	Supply voltage of PCA6408A for Port P.

[1] All I/O are configured as input at power-on.

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6. Voltage translation

Table 4 shows how to set up V_{DD} levels for the necessary voltage translation between the I²C-bus and the PCA6408A.

Table 4. Voltage translation

$V_{DD(I2C-bus)}$ (SDA and SCL of I²C master)	$V_{DD(P)}$ (Port P)
1.8 V	1.8 V
1.8 V	2.5 V
1.8 V	3.3 V
1.8 V	5 V
2.5 V	1.8 V
2.5 V	2.5 V
2.5 V	3.3 V
2.5 V	5 V
3.3 V	1.8 V
3.3 V	2.5 V
3.3 V	3.3 V
3.3 V	5 V
5 V	1.8 V
5 V	2.5 V
5 V	3.3 V
5 V	5 V

7. Functional description

Refer to Figure 1 “Block diagram (positive logic)”.

7.1 Device address

The address of the PCA6408A is shown in Figure 5.

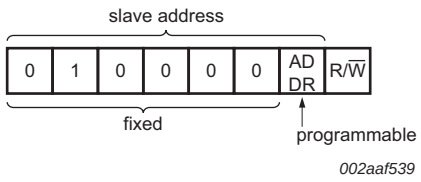


Fig 5. PCA6408A address

ADDR is the hardware address package pin and is held to either HIGH (logic 1) or LOW (logic 0) to assign one of the two possible slave addresses. The last bit of the slave address defines the operation (read or write) to be performed. A HIGH (logic 1) selects a read operation, while a LOW (logic 0) selects a write operation.

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7.2 Interface definition

Table 5. Interface definition

Byte	Bit							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I²C-bus slave address	L	H	L	L	L	L	ADDR	R/$\overline{W}$
I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

7.3 Pointer register and command byte

Following the successful acknowledgement of the address byte, the bus master sends a command byte, which is stored in the Pointer register in the PCA6408A. Two bits of this data byte state the operation (read or write) and the internal registers (Input, Output, Polarity Inversion, or Configuration) that will be affected. This register is write only.

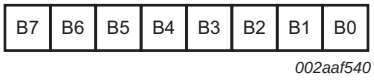


Fig 6. Pointer register bits

Table 6. Command byte

Pointer register bits								Command byte (hexadecimal)	Register	Protocol	Power-up default
B7	B6	B5	B4	B3	B2	B1	B0				
0	0	0	0	0	0	0	0	00h	Input port	read byte	xxxx xxxx[1]
0	0	0	0	0	0	0	1	01h	Output port	read/write byte	1111 1111
0	0	0	0	0	0	1	0	02h	Polarity Inversion	read/write byte	0000 0000
0	0	0	0	0	0	1	1	03h	Configuration	read/write byte	1111 1111

[1] Undefined.

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7.4 Register descriptions

7.4.1 Input port register (00h)

The Input port register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. The Input port register is read only; writes to this register have no effect. The default value 'X' is determined by the externally applied logic level. An Input port register read operation is performed as described in Section 8.2 "Read commands".

Table 7. Input port register (address 00h)

Bit	7	6	5	4	3	2	1	0
Symbol	I7	I6	I5	I4	I3	I2	I1	I0
Default	X	X	X	X	X	X	X	X

7.4.2 Output port register (01h)

The Output port register (register 1) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in these registers have no effect on pins defined as inputs. In turn, reads from this register reflect the value that was written to this register, **not** the actual pin value.

Table 8. Output port register (address 01h)

Bit	7	6	5	4	3	2	1	0
Symbol	O7	O6	O5	O4	O3	O2	O1	O0
Default	1	1	1	1	1	1	1	1

7.4.3 Polarity inversion register (02h)

The Polarity inversion register (register 2) allows polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with '1'), the corresponding port pin's polarity is inverted. If a bit in this register is cleared (written with a '0'), the corresponding port pin's original polarity is retained.

Table 9. Register 2: Polarity inversion register (address 02h)

Bit	7	6	5	4	3	2	1	0
Symbol	N7	N6	N5	N4	N3	N2	N1	N0
Default	0	0	0	0	0	0	0	0

7.4.4 Configuration register (03h)

The Configuration register (register 3) configures the direction of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as a high-impedance input. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

Table 10. Register 3: Configuration register (address 03h)

Bit	7	6	5	4	3	2	1	0
Symbol	C7	C6	C5	C4	C3	C2	C1	C0
Default	1	1	1	1	1	1	1	1

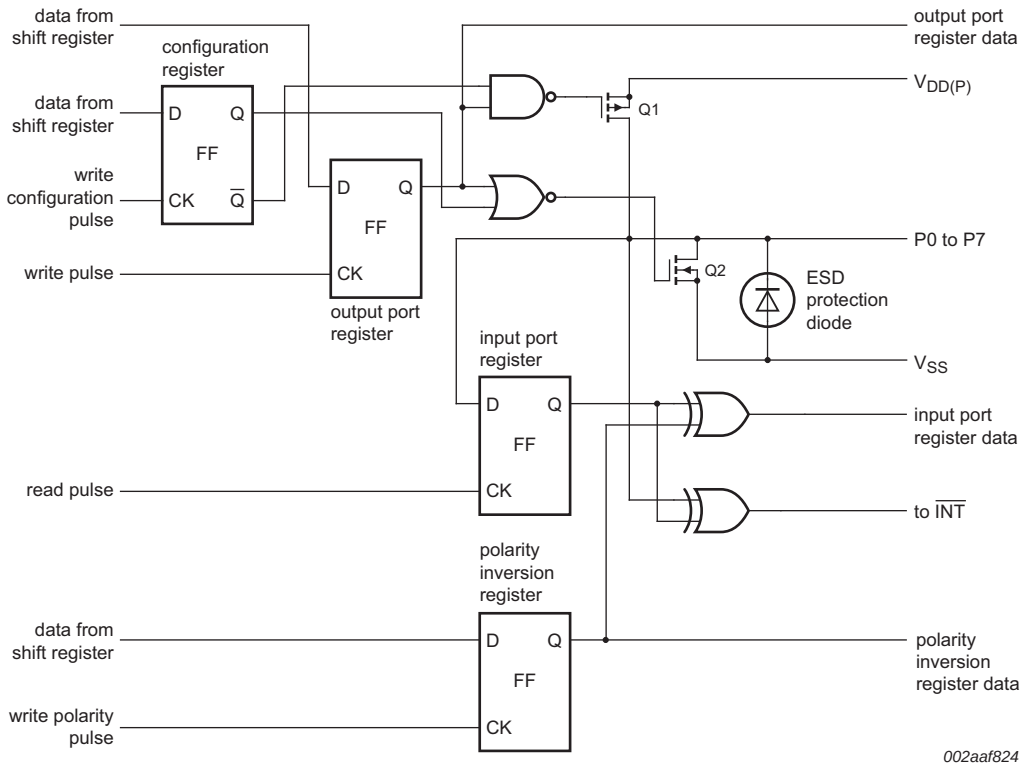
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7.5 I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, which creates a high-impedance input. The input voltage may be raised above V_{DD} to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the Output port register. In this case, there are low-impedance paths between the I/O pin and either $V_{DD(P)}$ or V_{SS}. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.



On power-up or reset, all registers return to default values.

Fig 7. Simplified schematic of P0 to P7

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7.6 Power-on reset

When power (from 0 V) is applied to $V_{DD(P)}$, an internal power-on reset holds the PCA6408A in a reset condition until $V_{DD(P)}$ has reached V_{POR}. At that time, the reset condition is released and the PCA6408A registers and I²C-bus/SMBus state machine initialize to their default states. After that, $V_{DD(P)}$ must be lowered to below V_{PORF} and back up to the operating voltage for a power-reset cycle. See Section 9.2 “Power-on reset requirements”.

7.7 Reset input ($\overline{\text{RESET}}$)

The $\overline{\text{RESET}}$ input can be asserted to initialize the system while keeping the $V_{DD(P)}$ at its operating level. A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin LOW for a minimum of $t_{w(rst)}$. The PCA6408A registers and I²C-bus/SMBus state machine are changed to their default state once $\overline{\text{RESET}}$ is LOW (0). When $\overline{\text{RESET}}$ is HIGH (1), the I/O levels at the P port can be changed externally or through the master. This input requires a pull-up resistor to $V_{DD(I2C\text{-}bus)}$ if no active connection is used.

7.8 Interrupt output ($\overline{\text{INT}}$)

An interrupt is generated by any rising or falling edge of the port inputs in the Input mode. After time $t_{v(INT)}$, the signal $\overline{\text{INT}}$ is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting or when data is read from the port that generated the interrupt (see Figure 11). Resetting occurs in the Read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{\text{INT}}$.

A pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the Input port register.

The $\overline{\text{INT}}$ output has an open-drain structure and requires a pull-up resistor to $V_{DD(P)}$ or $V_{DD(I2C\text{-}bus)}$ depending on the application. $\overline{\text{INT}}$ should be connected to the voltage source of the device that requires the interrupt information.

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8. Bus transactions

The PCA6408A is an I²C-bus slave device. Data is exchanged between the master and PCA6408A through write and read commands using I²C-bus. The two communication lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

8.1 Write commands

Data is transmitted to the PCA6408A by sending the device address and setting the Least Significant Bit (LSB) to a logic 0 (see Figure 5 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte. There is no limitation on the number of data bytes sent in one write transmission.

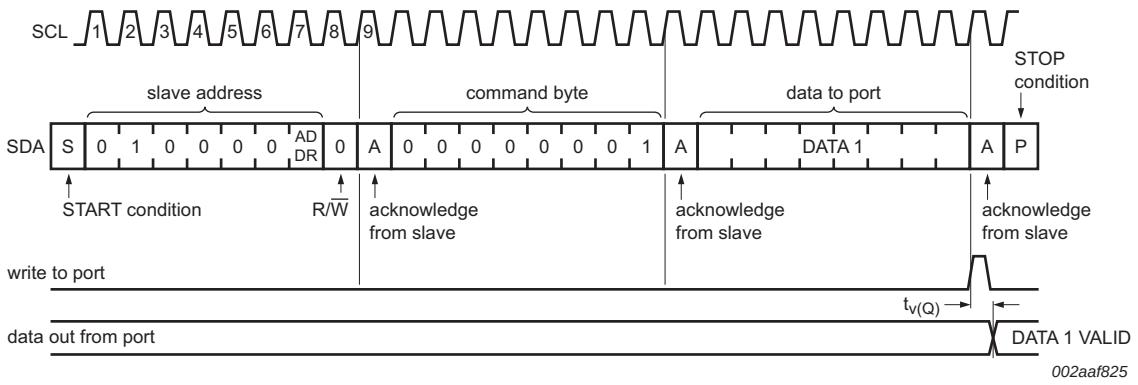


Fig 8. Write to Output port register

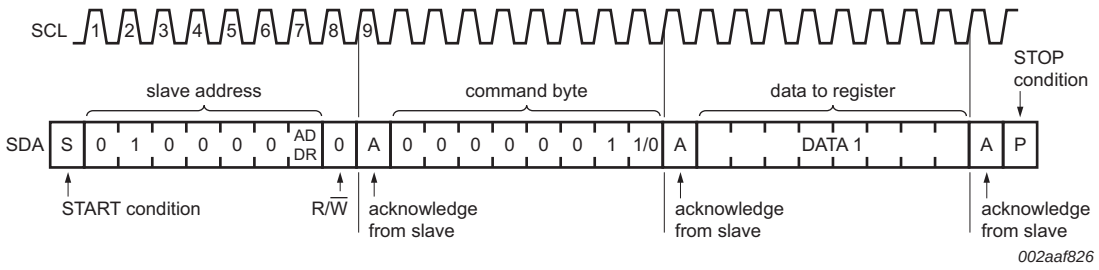


Fig 9. Write to Configuration or Polarity inversion registers

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8.2 Read commands

To read data from the PCA6408A, the bus master must first send the PCA6408A address with the least significant bit set to a logic 0 (see Figure 5 for device address). The command byte is sent after the address and determines which register is to be accessed.

After a restart the device address is sent again, but this time the LSB is set to a logic 1. Data from the register defined by the command byte then is sent by the PCA6408A (see Figure 10 and Figure 11).

Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limit on the number of data bytes received in one read transmission, but on the final byte received the bus master must not acknowledge the data.

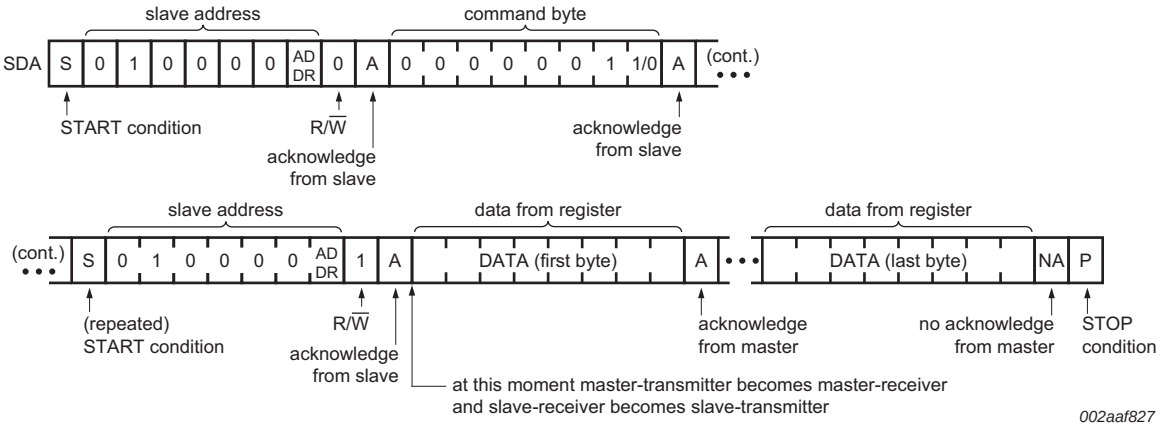
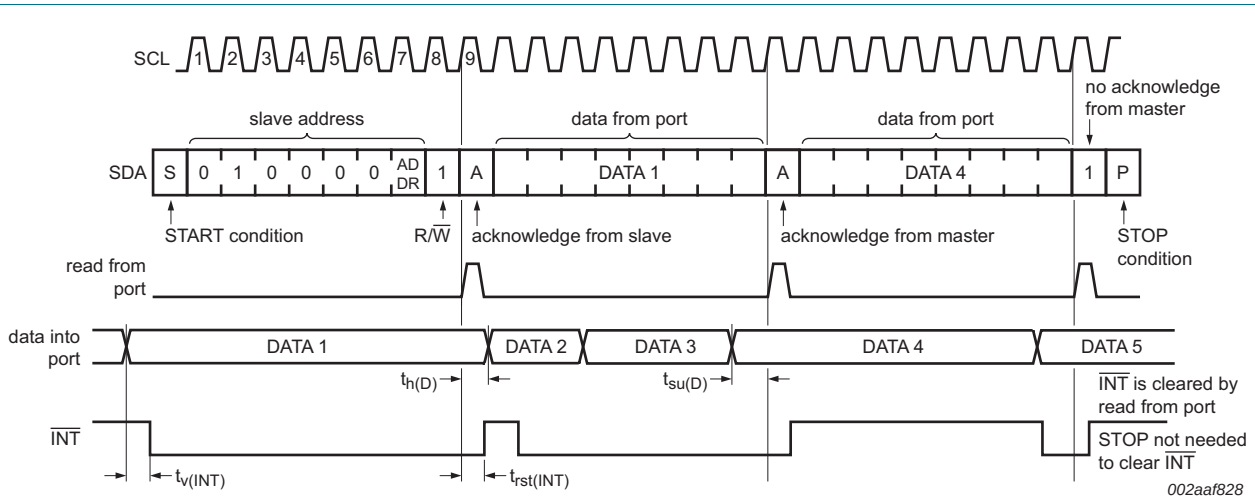


Fig 10. Read from register



Transfer of data can be stopped at any time by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been programmed with 00h (read Input port register).

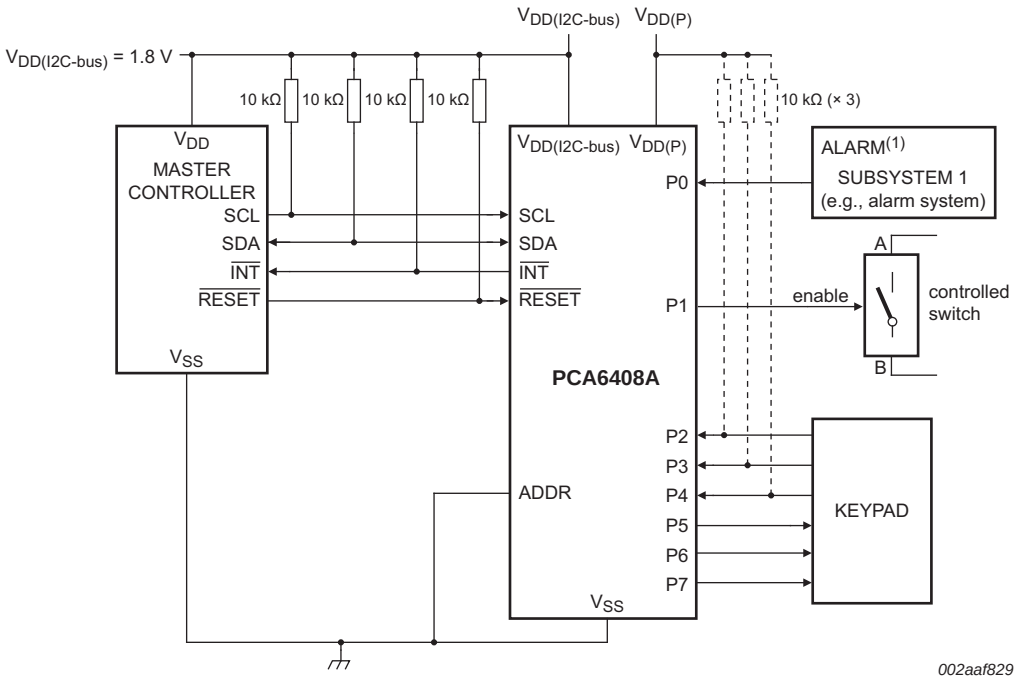
This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from P port (see Figure 10).

Fig 11. Read Input port register

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9. Application design-in information



Device address configured as 0100 000x for this example.

P0 and P2 through P4 are configured as inputs.

P1 and P5 through P7 are configured as outputs.

(1) Resistors are required for inputs (on P port) that may float. If a driver to an input will never let the input float, a resistor is not needed. Outputs (in the P port) do not need pull-up resistors.

Fig 12. Typical application

9.1 Minimizing I_{DD} when I/Os control LEDs

When the I/Os are used to control LEDs, normally they are connected to $V_{DD(P)}$ through a resistor as shown in Figure 12. The LED acts as a diode, so when the LED is off, the I/O V_I is about 1.2 V less than $V_{DD(P)}$. The ΔI_{DD} parameter in Table 15 “Static characteristics” shows how $I_{DD(P)}$ increases as V_I becomes lower than $V_{DD(P)}$. Designs that must minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to $V_{DD(P)}$ when the LED is off.

Figure 13 shows a high-value resistor in parallel with the LED. Figure 14 shows $V_{DD(P)}$ less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_I at or above $V_{DD(P)}$ and prevent additional supply current consumption when the LED is off.

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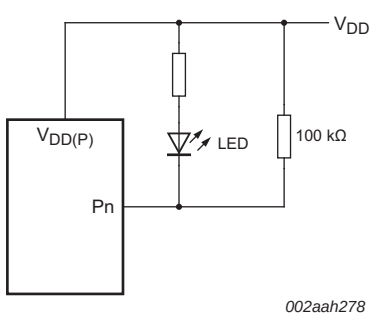


Fig 13. High-value resistor in parallel with the LED

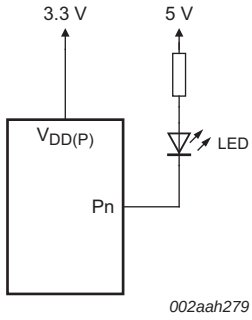


Fig 14. Device supplied by a lower voltage

9.2 Power-on reset requirements

In the event of a glitch or data corruption, PCA6408A can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in Figure 15 and Figure 16.

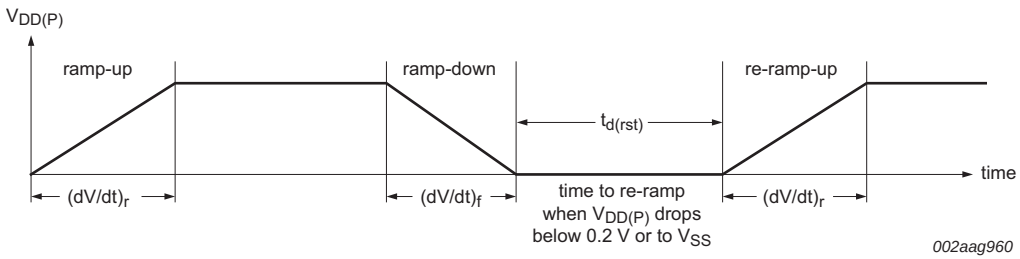


Fig 15. $V_{DD(P)}$ is lowered below 0.2 V or 0 V and then ramped up to $V_{DD(P)}$

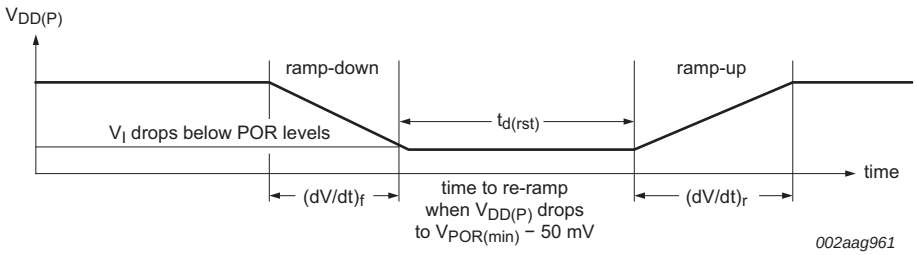


Fig 16. $V_{DD(P)}$ is lowered below the POR threshold, then ramped back up to $V_{DD(P)}$

Table 11 specifies the performance of the power-on reset feature for PCA6408A for both types of power-on reset.

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Table 11. Recommended supply sequencing and ramp rates

T_{amb} = 25 °C (unless otherwise noted). Not tested; specified by design.

Symbol	Parameter	Condition		Min	Typ	Max	Unit
$(dV/dt)_f$	fall rate of change of voltage	Figure 15		0.1	-	2000	ms
$(dV/dt)_r$	rise rate of change of voltage	Figure 15		0.1	-	2000	ms
$t_{d(rst)}$	reset delay time	Figure 15; re-ramp time when $V_{DD(P)}$ drops to V_{SS}		1	-	-	µs
		Figure 16; re-ramp time when $V_{DD(P)}$ drops to $V_{POR(min)}$ − 50 mV		1	-	-	µs
$\Delta V_{DD(gl)}$	glitch supply voltage difference	Figure 17	[1]	-	-	1.0	V
$t_{w(gl)VDD}$	supply voltage glitch pulse width	Figure 17	[2]	-	-	10	µs
$V_{POR(trip)}$	power-on reset trip voltage	falling $V_{DD(P)}$		0.7	-	-	V
		rising $V_{DD(P)}$		-	-	1.4	V

[1] Level that $V_{DD(P)}$ can glitch down to with a ramp rate of 0.4 µs/V, but not cause a functional disruption when $t_{w(gl)VDD}$ < 1 µs.

[2] Glitch width that will not cause a functional disruption when $\Delta V_{DD(gl)} = 0.5 \times V_{DD(P)}$.

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ($t_{w(gl)VDD}$) and glitch height ($\Delta V_{DD(gl)}$) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 17 and Table 11 provide more information on how to measure these specifications.

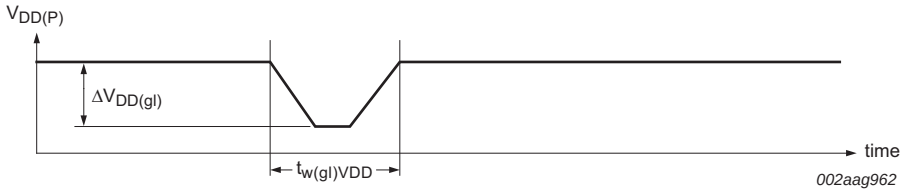


Fig 17. Glitch width and glitch height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I²C-bus/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the $V_{DD(P)}$ being lowered to or from 0 V. Figure 18 and Table 11 provide more details on this specification.

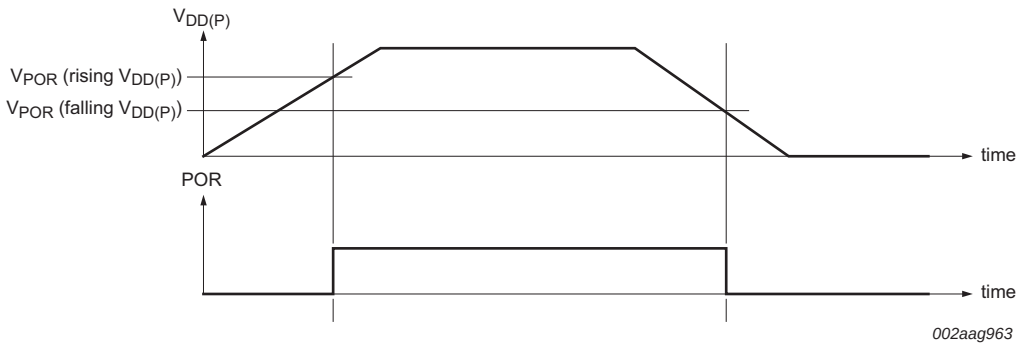


Fig 18. Power-on reset voltage (V_{POR})

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10. Limiting values

Table 12. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(I2C\text{-}bus)}$	I²C-bus supply voltage			–0.5	+6.5	V
$V_{DD(P)}$	supply voltage port P			–0.5	+6.5	V
V_I	input voltage		[1]	–0.5	+6.5	V
V_O	output voltage		[1]	–0.5	+6.5	V
I_{IK}	input clamping current	ADDR, $\overline{RESET}$, SCL; $V_I < 0$ V		-	±20	mA
I_{OK}	output clamping current	$\overline{INT}$; $V_O < 0$ V		-	±20	mA
I_{IOK}	input/output clamping current	P port; $V_O < 0$ V or $V_O > V_{DD(P)}$		-	±20	mA
		SDA; $V_O < 0$ V or $V_O > V_{DD(I2C\text{-}bus)}$		-	±20	mA
I_{OL}	LOW-level output current	continuous; P port; $V_O = 0$ V to $V_{DD(P)}$		-	50	mA
		continuous; SDA, $\overline{INT}$; $V_O = 0$ V to $V_{DD(I2C\text{-}bus)}$		-	25	mA
I_{OH}	HIGH-level output current	continuous; P port; $V_O = 0$ V to $V_{DD(P)}$		-	25	mA
I_{DD}	supply current	continuous through V_{SS}		-	200	mA
$I_{DD(P)}$	supply current port P	continuous through $V_{DD(P)}$		-	160	mA
$I_{DD(I2C\text{-}bus)}$	I²C-bus supply current	continuous through $V_{DD(I2C\text{-}bus)}$		-	10	mA
T_{stg}	storage temperature			–65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	125	°C

[1] The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

11. Recommended operating conditions

Table 13. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD(I2C\text{-}bus)}$	I²C-bus supply voltage		1.65	5.5	V
$V_{DD(P)}$	supply voltage port P		1.65	5.5	V
V_{IH}	HIGH-level input voltage	SCL, SDA, $\overline{RESET}$	$0.7 \times V_{DD(I2C\text{-}bus)}$	5.5	V
		ADDR, P7 to P0	$0.7 \times V_{DD(P)}$	5.5	V
V_{IL}	LOW-level input voltage	SCL, SDA, $\overline{RESET}$	–0.5	$0.3 \times V_{DD(I2C\text{-}bus)}$	V
		ADDR, P7 to P0	–0.5	$0.3 \times V_{DD(P)}$	V
I_{OH}	HIGH-level output current	P7 to P0	-	10	mA
I_{OL}	LOW-level output current	P7 to P0	-	25	mA
T_{amb}	ambient temperature	operating in free air	–40	+85	°C

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12. Thermal characteristics

Table 14. Thermal characteristics

Symbol	Parameter	Conditions		Max	Unit
$Z_{th(j-a)}$	transient thermal impedance from junction to ambient	TSSOP16 package	[1]	108	K/W
		HVQFN16 package	[1]	53	K/W
		XQFN16 package	[1]	184	K/W

[1] The package thermal impedance is calculated in accordance with JESD 51-7.

13. Static characteristics

Table 15. Static characteristics

T_{amb} = −40 °C to +85 °C; $V_{DD(I2C-bus)}$ = 1.65 V to 5.5 V; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{IK}	input clamping voltage	I_I = −18 mA		−1.2	-	-	V
V_{POR}	power-on reset voltage	$V_I = V_{DD(P)}$ or V_{SS}; I_O = 0 mA		-	1.1	1.4	V
V_{OH}	HIGH-level output voltage	P port					
		I_{OH} = −8 mA; $V_{DD(P)}$ = 1.65 V	[2]	1.2	-	-	V
		I_{OH} = −10 mA; $V_{DD(P)}$ = 1.65 V	[2]	1.1	-	-	V
		I_{OH} = −8 mA; $V_{DD(P)}$ = 2.3 V	[2]	1.8	-	-	V
		I_{OH} = −10 mA; $V_{DD(P)}$ = 2.3 V	[2]	1.7	-	-	V
		I_{OH} = −8 mA; $V_{DD(P)}$ = 3.0 V	[2]	2.6	-	-	V
		I_{OH} = −10 mA; $V_{DD(P)}$ = 3.0 V	[2]	2.5	-	-	V
		I_{OH} = −8 mA; $V_{DD(P)}$ = 4.5 V	[2]	4.1	-	-	V
		I_{OH} = −10 mA; $V_{DD(P)}$ = 4.5 V	[2]	4.0	-	-	V
V_{OL}	LOW-level output voltage	P port; I_{OL} = 8 mA					
		$V_{DD(P)}$ = 1.65 V	[2]	-	-	0.45	V
		$V_{DD(P)}$ = 2.3 V	[2]	-	-	0.25	V
		$V_{DD(P)}$ = 3 V	[2]	-	-	0.25	V
		$V_{DD(P)}$ = 4.5 V	[2]	-	-	0.2	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; $V_{DD(P)}$ = 1.65 V to 5.5 V					
		SDA	[3]	3	-	-	mA
		$\overline{INT}$	[3]	3	15[4]	-	mA
		P port					
		V_{OL} = 0.5 V; $V_{DD(P)}$ = 1.65 V	[3]	8	10	-	mA
		V_{OL} = 0.7 V; $V_{DD(P)}$ = 1.65 V	[3]	10	13	-	mA
		V_{OL} = 0.5 V; $V_{DD(P)}$ = 2.3 V	[3]	8	10	-	mA
		V_{OL} = 0.7 V; $V_{DD(P)}$ = 2.3 V	[3]	10	13	-	mA
		V_{OL} = 0.5 V; $V_{DD(P)}$ = 3.0 V	[3]	8	14	-	mA
		V_{OL} = 0.7 V; $V_{DD(P)}$ = 3.0 V	[3]	10	19	-	mA
		V_{OL} = 0.5 V; $V_{DD(P)}$ = 4.5 V	[3]	8	17	-	mA
		V_{OL} = 0.7 V; $V_{DD(P)}$ = 4.5 V	[3]	10	24	-	mA

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Table 15. Static characteristics *...continued*

T_{amb} = −40 °C to +85 °C; $V_{DD(I2C\text{-}bus)}$ = 1.65 V to 5.5 V; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I_I	input current	$V_{DD(P)}$ = 1.65 V to 5.5 V				
		SCL, SDA, $\overline{RESET}$; $V_I = V_{DD(I2C\text{-}bus)}$ or V_{SS}	-	-	±1	µA
		ADDR; $V_I = V_{DD(P)}$ or V_{SS}	-	-	±1	µA
I_{IH}	HIGH-level input current	P port; $V_I = V_{DD(P)}$; $V_{DD(P)}$ = 1.65 V to 5.5 V	-	-	1	µA
I_{IL}	LOW-level input current	P port; $V_I = V_{SS}$; $V_{DD(P)}$ = 1.65 V to 5.5 V	-	-	1	µA
I_{DD}	supply current	$I_{DD(I2C\text{-}bus)} + I_{DD(P)}$; SDA, P port, ADDR, $\overline{RESET}$; V_I on SDA and $\overline{RESET} = V_{DD(I2C\text{-}bus)}$ or V_{SS}; V_I on P port and ADDR = $V_{DD(P)}$; I_O = 0 mA; I/O = inputs; f_{SCL} = 400 kHz				
		$V_{DD(P)}$ = 3.6 V to 5.5 V	-	10	25	µA
		$V_{DD(P)}$ = 2.3 V to 3.6 V	-	6.5	15	µA
		$V_{DD(P)}$ = 1.65 V to 2.3 V	-	4	9	µA
		$I_{DD(I2C\text{-}bus)} + I_{DD(P)}$; SCL, SDA, P port, ADDR, $\overline{RESET}$; V_I on SCL, SDA and $\overline{RESET} = V_{DD(I2C\text{-}bus)}$ or V_{SS}; V_I on P port and ADDR = $V_{DD(P)}$; I_O = 0 mA; I/O = inputs; f_{SCL} = 0 kHz				
		$V_{DD(P)}$ = 3.6 V to 5.5 V	-	1.5	7	µA
		$V_{DD(P)}$ = 2.3 V to 3.6 V	-	1	3.2	µA
		$V_{DD(P)}$ = 1.65 V to 2.3 V	-	0.5	1.7	µA
		Active mode; $I_{DD(I2C\text{-}bus)} + I_{DD(P)}$; P port, ADDR, $\overline{RESET}$; V_I on $\overline{RESET} = V_{DD(I2C\text{-}bus)}$; V_I on P port and ADDR = $V_{DD(P)}$; I_O = 0 mA; I/O = inputs; f_{SCL} = 400 kHz, continuous register read				
		$V_{DD(P)}$ = 3.6 V to 5.5 V	-	60	125	µA
		$V_{DD(P)}$ = 2.3 V to 3.6 V	-	40	75	µA
		$V_{DD(P)}$ = 1.65 V to 2.3 V	-	20	45	µA
ΔI_{DD}	additional quiescent supply current	SCL, SDA, $\overline{RESET}$; one input at $V_{DD(I2C\text{-}bus)}$ − 0.6 V, other inputs at $V_{DD(I2C\text{-}bus)}$ or V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V	-	-	25	µA
		P port, ADDR; one input at $V_{DD(P)}$ − 0.6 V, other inputs at $V_{DD(P)}$ or V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V	-	-	80	µA
C_i	input capacitance	$V_I = V_{DD(I2C\text{-}bus)}$ or V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V	-	6	7	pF
C_{io}	input/output capacitance	$V_{I/O} = V_{DD(I2C\text{-}bus)}$ or V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V	-	7	8	pF
		$V_{I/O} = V_{DD(P)}$ or V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V	-	7.5	8.5	pF

[1] For I_{DD}, all typical values are at nominal supply voltage (1.8 V, 2.5 V, 3.3 V, 3.6 V or 5 V V_{DD}) and T_{amb} = 25 °C. Except for I_{DD}, the typical values are at $V_{DD(P)} = V_{DD(I2C\text{-}bus)}$ = 3.3 V and T_{amb} = 25 °C.

[2] The total current sourced by all I/Os must be limited to 80 mA.

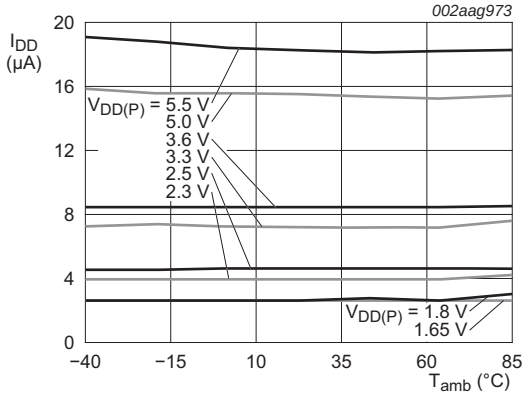
[3] Each I/O must be externally limited to a maximum of 25 mA, for a device total of 200 mA.

[4] Typical value for T_{amb} = 25 °C. V_{OL} = 0.4 V and V_{DD} = 3.3 V. Typical value for V_{DD} < 2.5 V, V_{OL} = 0.6 V.

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13.1 Typical characteristics



$I_{DD} = I_{DD(I2C\text{-}bus)} + I_{DD(P)}$

Fig 19. Supply current versus ambient temperature

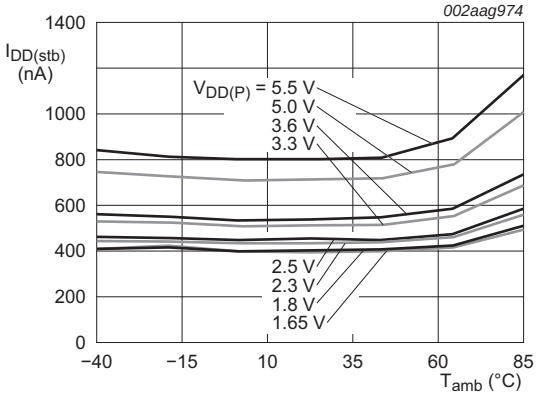
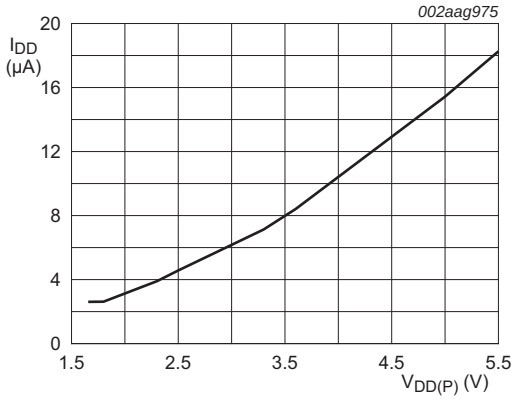


Fig 20. Standby supply current versus ambient temperature



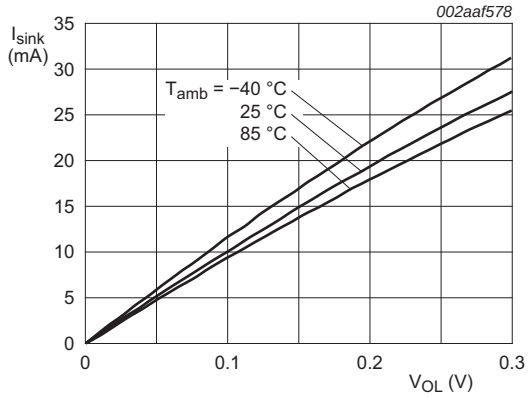
T_{amb} = 25 °C

$I_{DD} = I_{DD(I2C\text{-}bus)} + I_{DD(P)}$

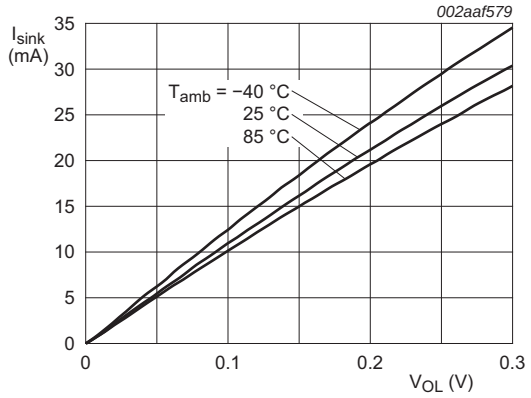
Fig 21. Supply current versus supply voltage

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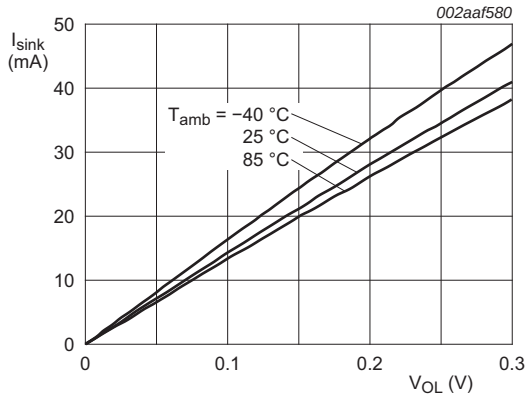
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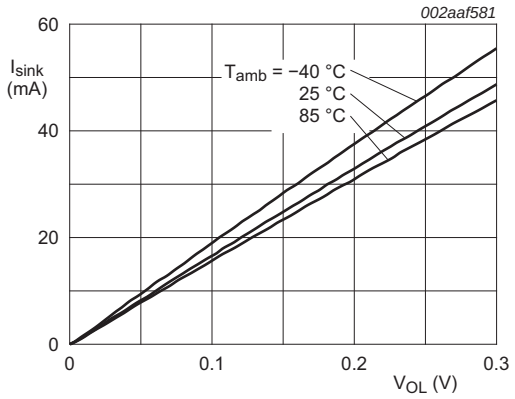
a. $V_{DD(P)}$ = 1.65 V



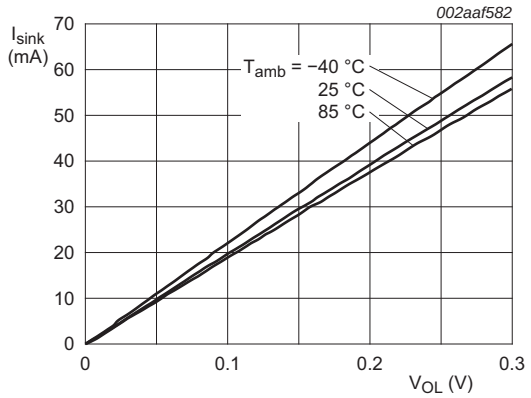
b. $V_{DD(P)}$ = 1.8 V



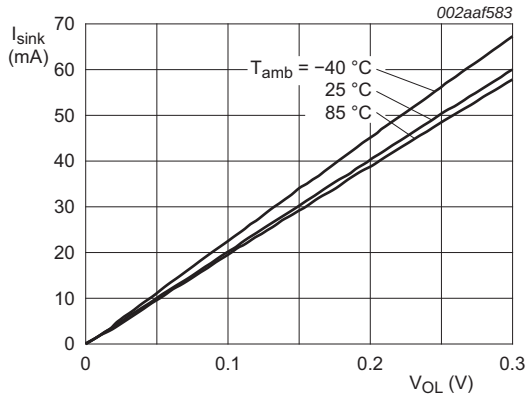
c. $V_{DD(P)}$ = 2.5 V



d. $V_{DD(P)}$ = 3.3 V



e. $V_{DD(P)}$ = 5.0 V

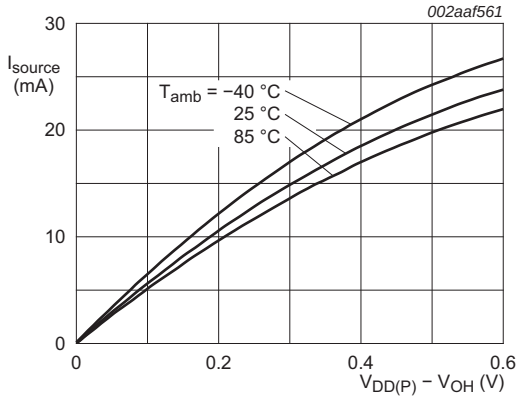


f. $V_{DD(P)}$ = 5.5 V

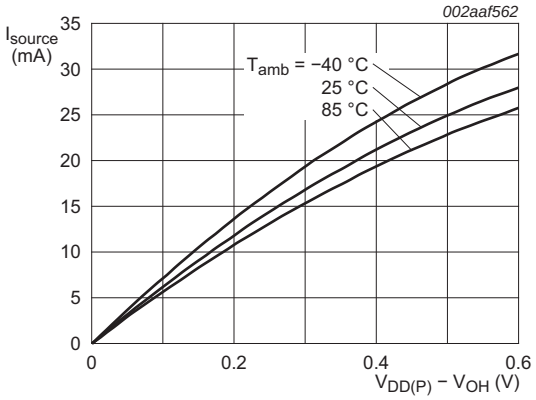
Fig 22. I/O sink current versus LOW-level output voltage

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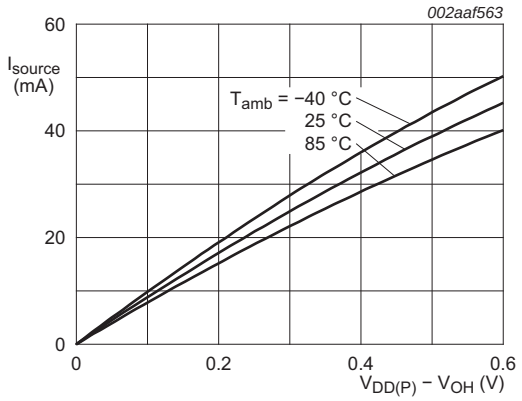
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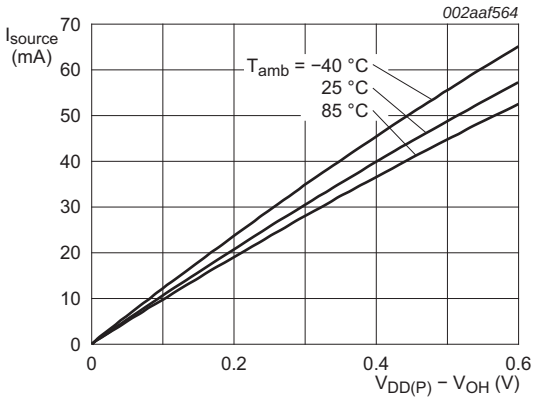
a. $V_{DD(P)}$ = 1.65 V



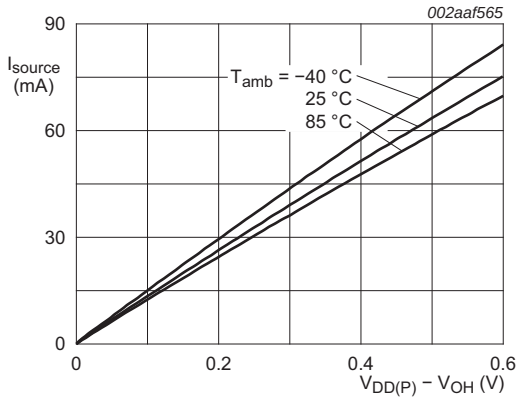
b. $V_{DD(P)}$ = 1.8 V



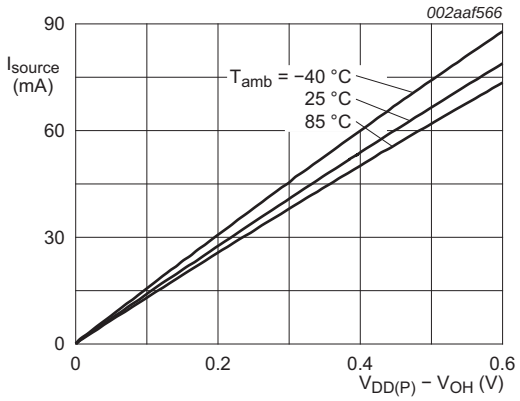
c. $V_{DD(P)}$ = 2.5 V



d. $V_{DD(P)}$ = 3.3 V



e. $V_{DD(P)}$ = 5.0 V

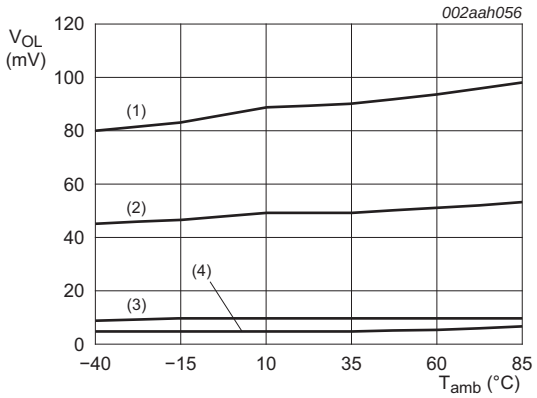


f. $V_{DD(P)}$ = 5.5 V

Fig 23. I/O source current versus HIGH-level output voltage

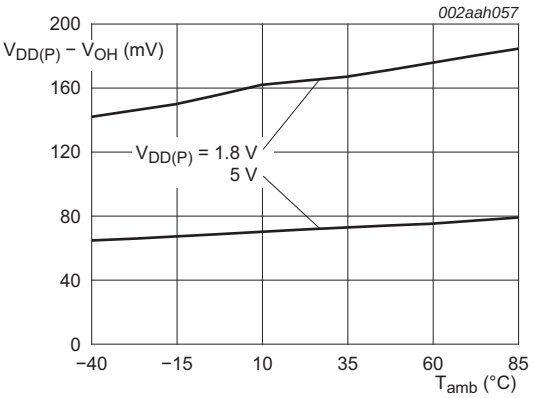
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(1) $V_{DD(P)}$ = 1.8 V; I_{sink} = 10 mA
(2) $V_{DD(P)}$ = 5 V; I_{sink} = 10 mA
(3) $V_{DD(P)}$ = 1.8 V; I_{sink} = 1 mA
(4) $V_{DD(P)}$ = 5 V; I_{sink} = 1 mA

Fig 24. LOW-level output voltage versus temperature



I_{source} = −10 mA

Fig 25. I/O high voltage versus temperature

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14. Dynamic characteristics

Table 16. I²C-bus interface timing requirements

Over recommended operating free air temperature range, unless otherwise specified. See Figure 26.

Symbol	Parameter	Conditions	Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	kHz
t_{HIGH}	HIGH period of the SCL clock		4	-	0.6	-	µs
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	µs
t_{SP}	pulse width of spikes that must be suppressed by the input filter		0	50	0	50	ns
$t_{SU;DAT}$	data set-up time		250	-	100	-	ns
$t_{HD;DAT}$	data hold time		0	-	0	-	ns
t_r	rise time of both SDA and SCL signals		-	1000	20	300	ns
t_f	fall time of both SDA and SCL signals		-	300	$20 \times (V_{DD} / 5.5\ V)$	300	ns
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		4	-	0.6	-	µs
$t_{SU;STO}$	set-up time for STOP condition		4	-	0.6	-	µs
$t_{VD;DAT}$	data valid time	SCL LOW to SDA output valid	-	3.45	-	0.9	µs
$t_{VD;ACK}$	data valid acknowledge time	ACK signal from SCL LOW to SDA (out) LOW	-	3.45	-	0.9	µs

Table 17. Reset timing requirements

Over recommended operating free air temperature range, unless otherwise specified. See Figure 29.

Symbol	Parameter	Conditions	Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
			Min	Max	Min	Max	
$t_{w(rst)}$	reset pulse width		30	-	30	-	ns
$t_{rec(rst)}$	reset recovery time		200	-	200	-	ns
t_{rst}	reset time		600	-	600	-	ns

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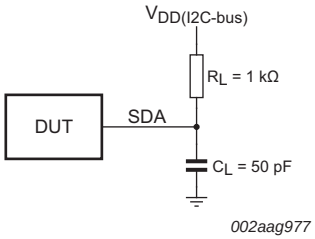
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Table 18. Switching characteristics

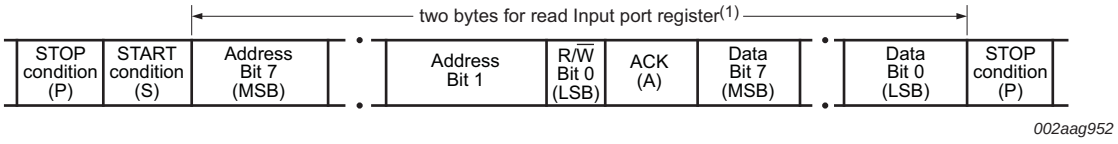
Over recommended operating free air temperature range; $C_L \leq 100$ pF; unless otherwise specified. See Figure 28.

Symbol	Parameter	Conditions	Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
			Min	Max	Min	Max	
$t_{v(INT)}$	valid time on pin $\overline{INT}$	from P port to $\overline{INT}$	-	1	-	1	µs
$t_{rst(INT)}$	reset time on pin $\overline{INT}$	from SCL to $\overline{INT}$	-	1	-	1	µs
$t_{v(Q)}$	data output valid time	from SCL to P port	-	400	-	400	ns
$t_{su(D)}$	data input set-up time	from P port to SCL	0	-	0	-	ns
$t_{h(D)}$	data input hold time	from P port to SCL	300	-	300	-	ns

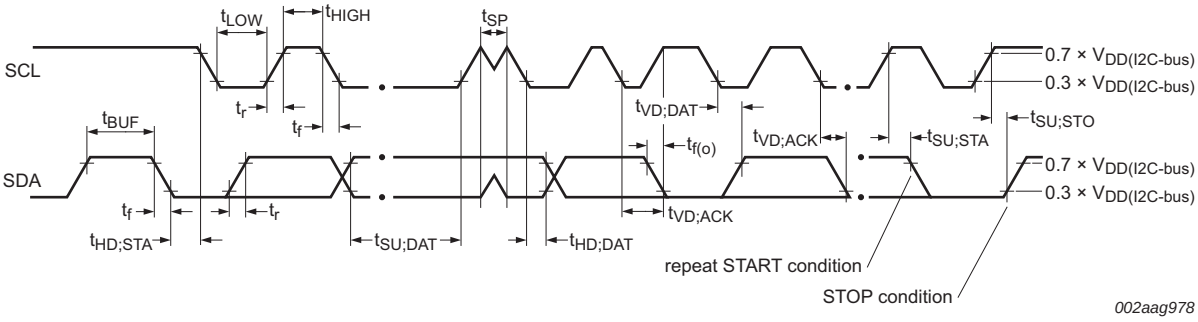
15. Parameter measurement information



a. SDA load configuration



b. Transaction format



c. Voltage waveforms

C_L includes probe and jig capacitance. $t_{f(o)}$ is measured with C_L of 10 pF or 400 pF.

All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; $t_r/t_f \leq 30$ ns.

All parameters and waveforms are not applicable to all devices.

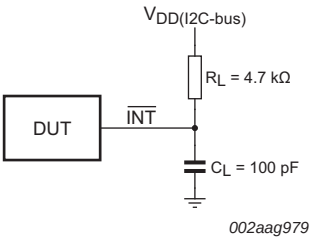
Byte 1 = I²C-bus address; Byte 2 = Input register port data.

(1) See Figure 11.

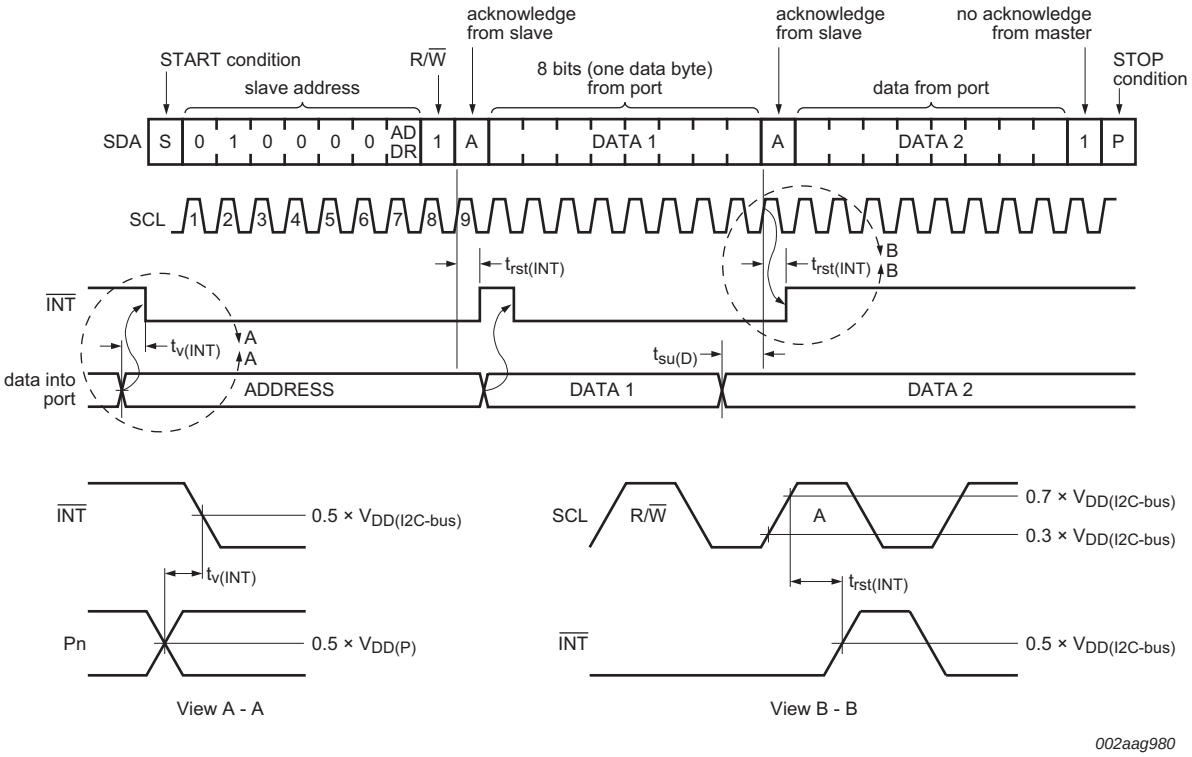
Fig 26. I²C-bus interface load circuit and voltage waveforms

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a. Interrupt load configuration



b. Voltage waveforms

C_L includes probe and jig capacitance.

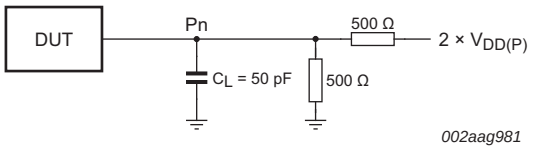
All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r/t_f ≤ 30 ns.

All parameters and waveforms are not applicable to all devices.

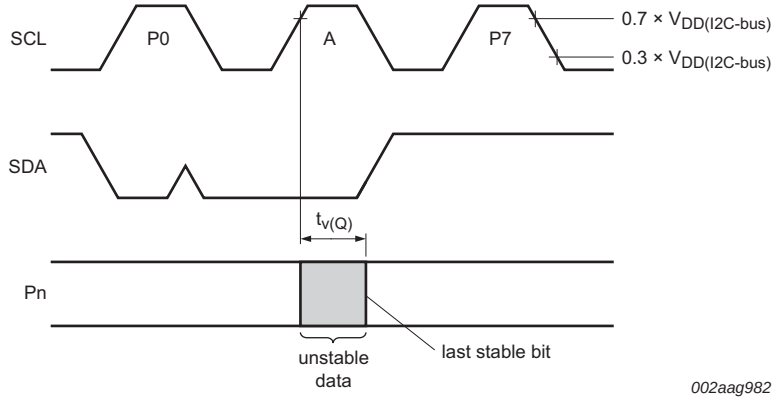
Fig 27. Interrupt load circuit and voltage waveforms

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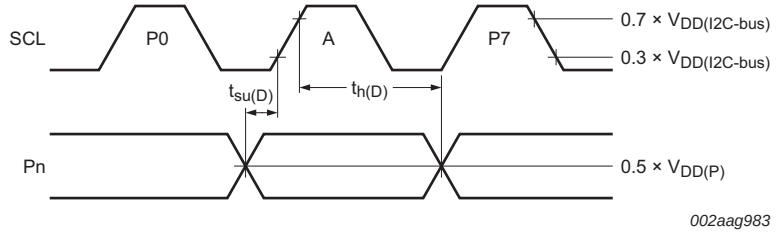
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a. P port load configuration



b. Write mode (R/$\overline{W}$ = 0)



c. Read mode (R/$\overline{W}$ = 1)

C_L includes probe and jig capacitance.

$t_{v(Q)}$ is measured from $0.7 \times V_{DD}$ on SCL to 50 % I/O (Pn) output.

All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r/t_f ≤ 30 ns.

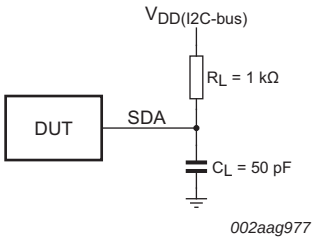
The outputs are measured one at a time, with one transition per measurement.

All parameters and waveforms are not applicable to all devices.

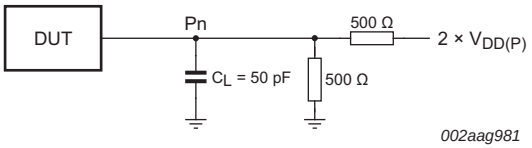
Fig 28. P port load circuit and voltage waveforms

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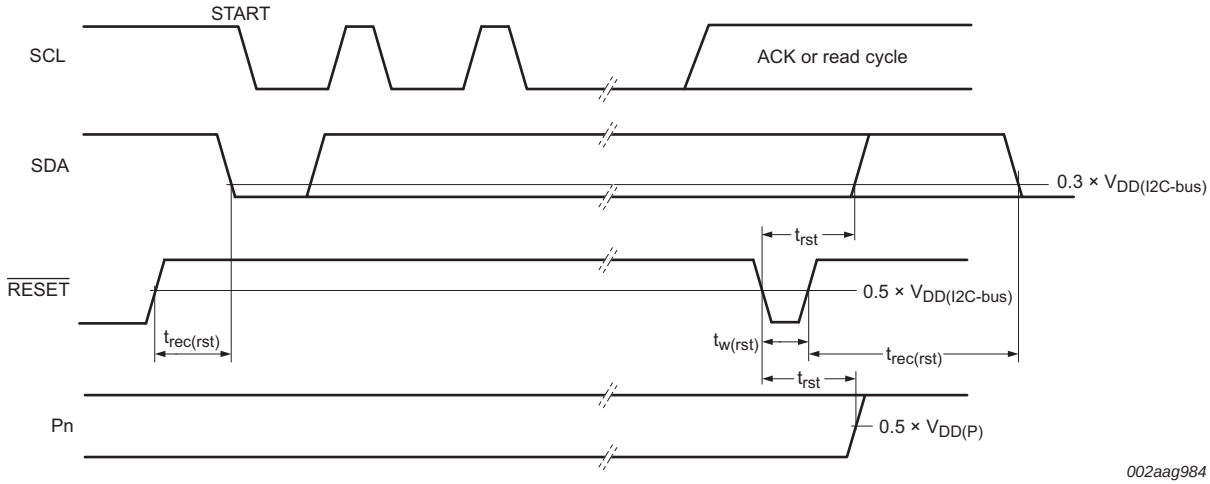
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a. SDA load configuration



b. P port load configuration



c. $\overline{\text{RESET}}$ timing

C_L includes probe and jig capacitance.

All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r/t_f ≤ 30 ns.

The outputs are measured one at a time, with one transition per measurement.

I/Os are configured as inputs.

All parameters and waveforms are not applicable to all devices.

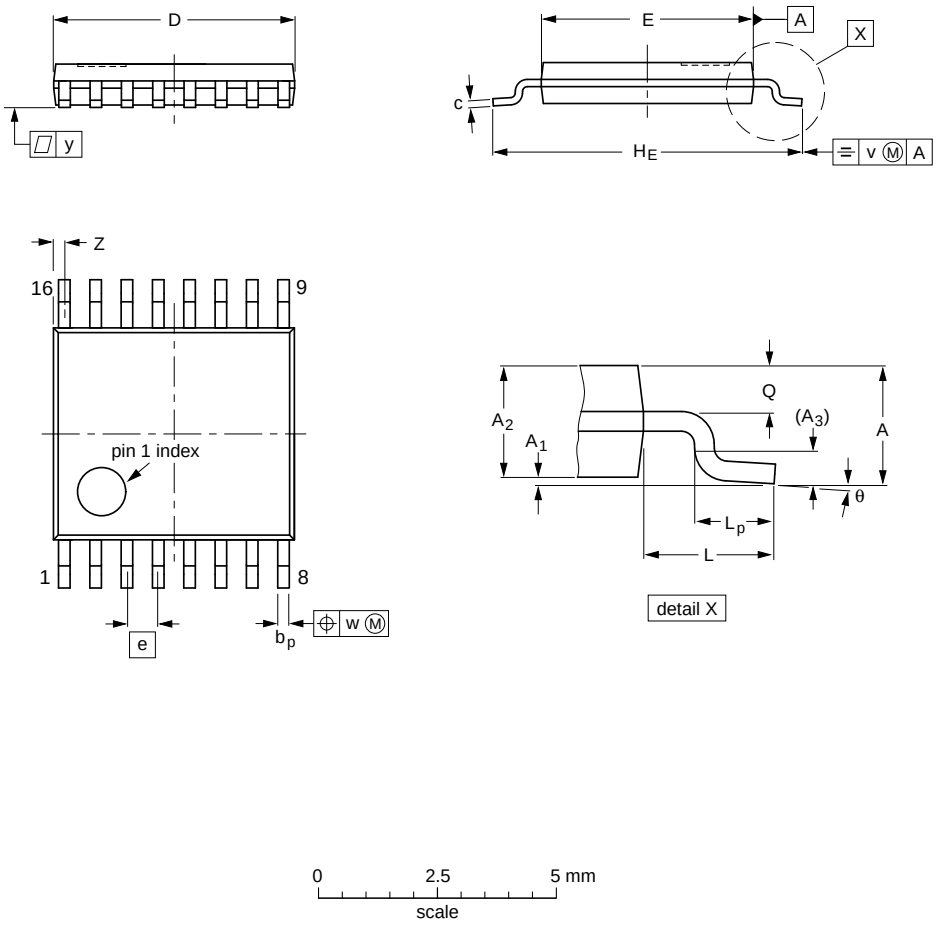
Fig 29. Reset load circuits and voltage waveforms

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16. Package outline

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

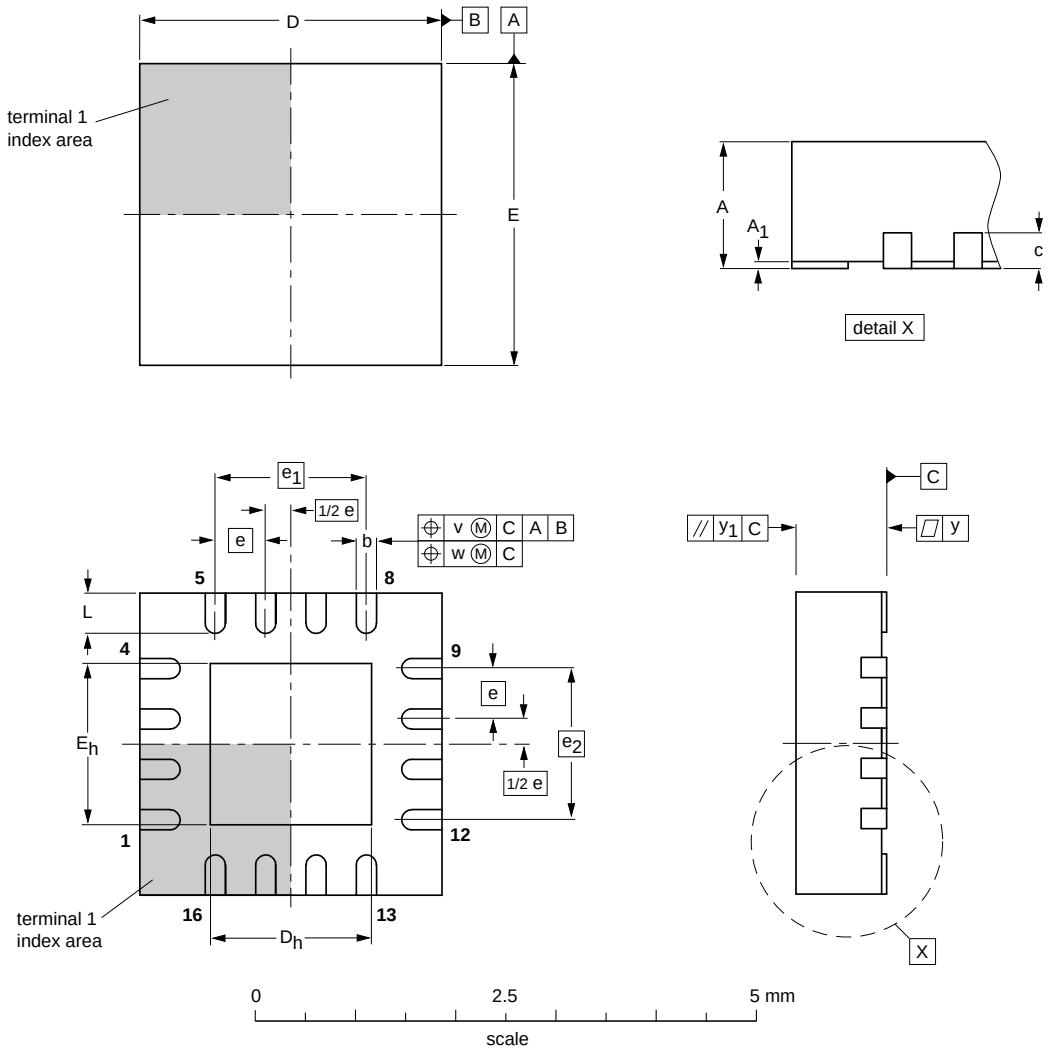
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 30. Package outline SOT403-1 (TSSOP16)

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HVQFN16: plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 x 3 x 0.85 mm **SOT758-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.75 1.45	3.1 2.9	1.75 1.45	0.5	1.5	1.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

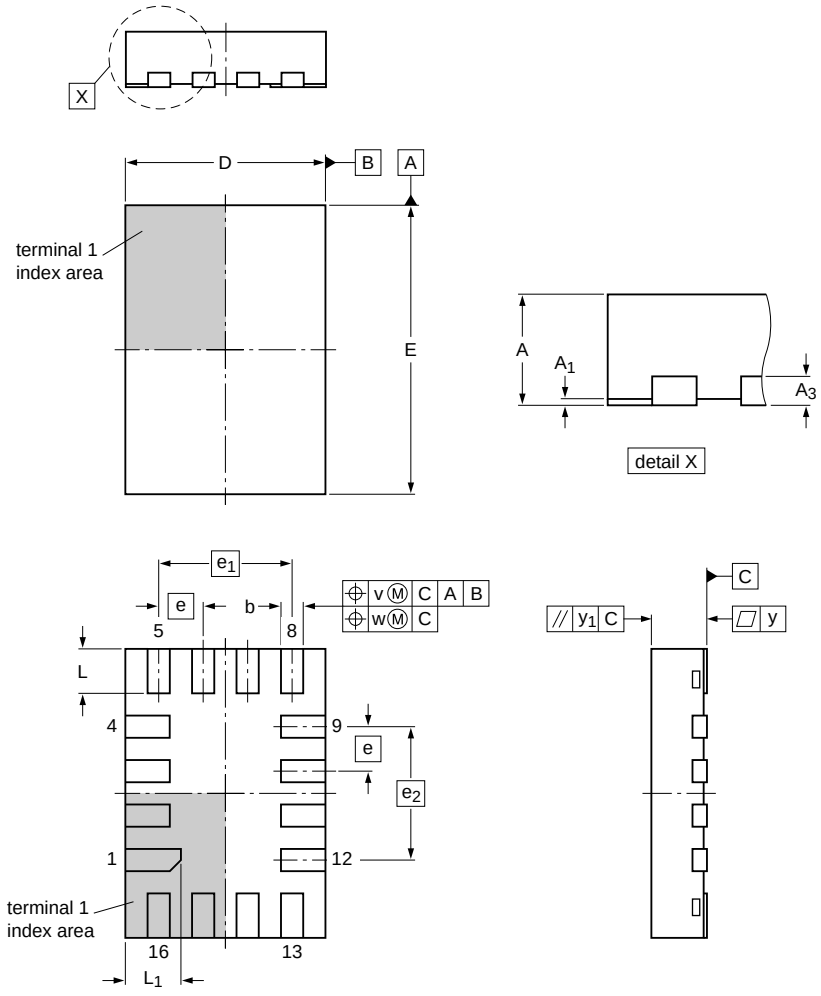
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT758-1	- - -	MO-220	- - -			~~02-03-25~~ 02-10-21

Fig 31. Package outline SOT758-1 (HVQFN16)

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XQFN16: plastic, extremely thin quad flat package; no leads; 16 terminals; body 1.80 x 2.60 x 0.50 mm **SOT1161-1**



Dimensions

Unit(1)		A	A_1	A_3	b	D	E	e	e_1	e_2	L	L_1	v	w	y	y_1
	max	0.5	0.05		0.25	1.9	2.7				0.45	0.55				
mm	nom			0.127	0.20	1.8	2.6	0.4	1.2	1.2	0.40	0.50	0.1	0.05	0.05	0.05
	min		0.00		0.15	1.7	2.5				0.35	0.45				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1161-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1161-1	- - -	- - -	- - -			~~09-12-28~~ 09-12-29

Fig 32. Package outline SOT1161-1 (XQFN16)

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17. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

17.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

17.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

17.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

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17.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 33) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 19 and 20

Table 19. SnPb eutectic process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 20. Lead-free process (from J-STD-020C)

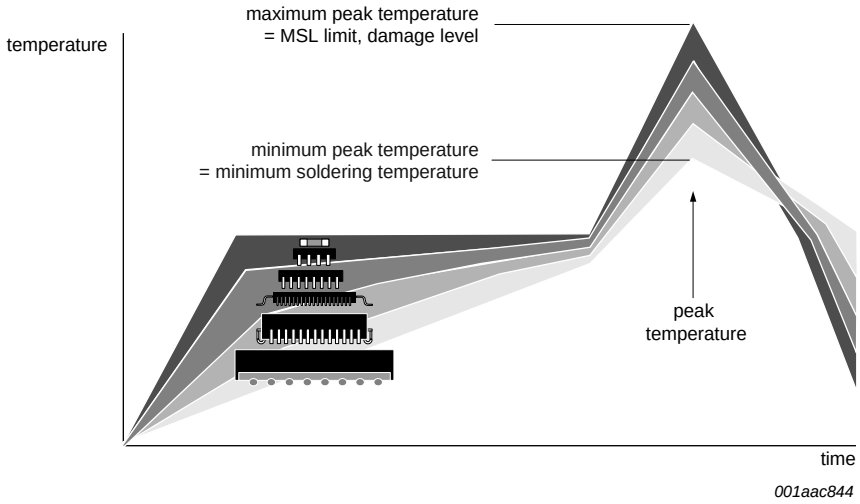
Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 33.

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MSL: Moisture Sensitivity Level

Fig 33. Temperature profiles for large and small components

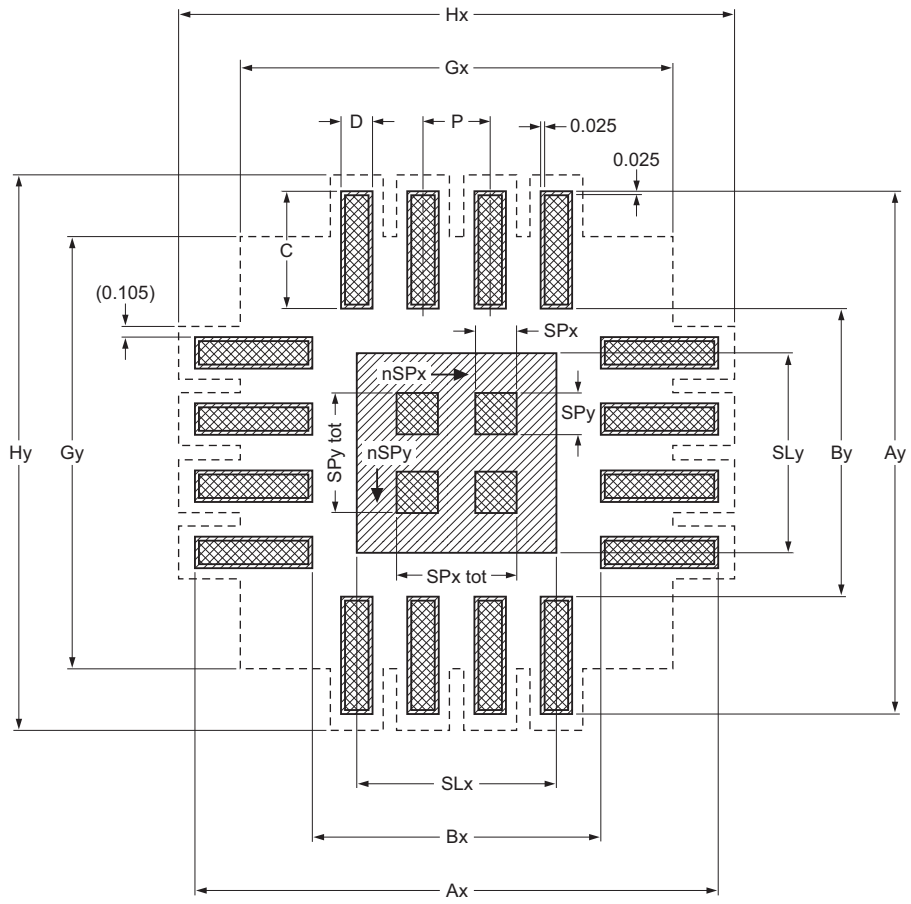
For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

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18. Soldering: PCB footprints

Footprint information for reflow soldering of HVQFN16 package **SOT758-1**



solder land

solder paste deposit

solder land plus solder paste

occupied area

nSPx	nSPy
2	2

Dimensions in mm

P	Ax	Ay	Bx	By	C	D	SLx	SLy	SPx tot	SPy tot	SPx	SPy	Gx	Gy	Hx	Hy
0.50	4.00	4.00	2.20	2.20	0.90	0.24	1.50	1.50	0.90	0.90	0.30	0.30	3.30	3.30	4.25	4.25

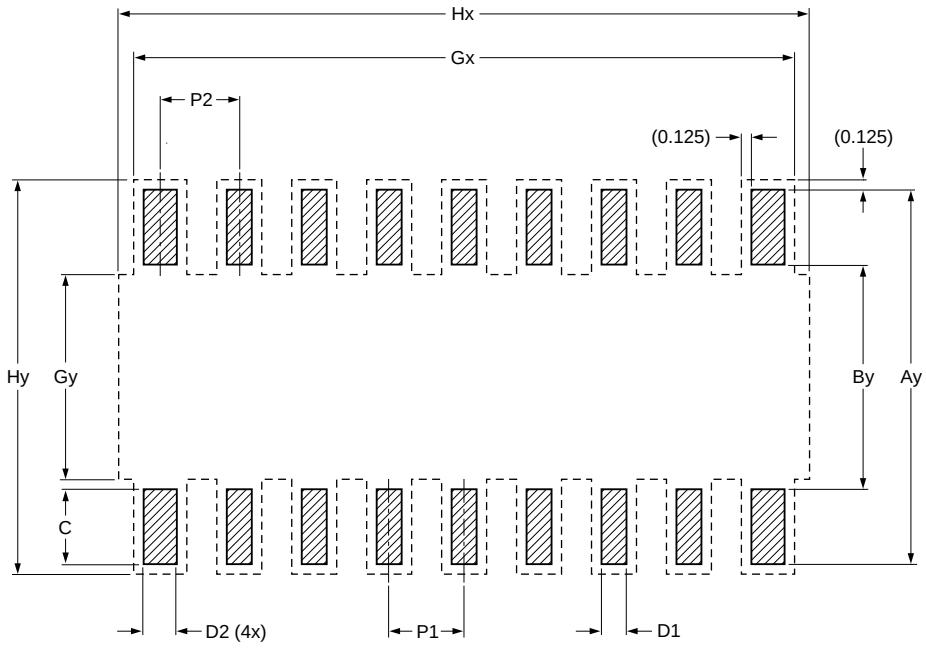
Issue date ~~12-03-07~~ 12-03-08 *sot758-1_fr*

Fig 34. PCB footprint for SOT758-1 (HVQFN16); reflow soldering

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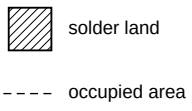
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Footprint information for reflow soldering of TSSOP16 package **SOT403-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout



DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.650	0.750	7.200	4.500	1.350	0.400	0.600	5.600	5.300	5.800	7.450

sot403-1_fr

Fig 35. PCB footprint for SOT403-1 (TSSOP16); reflow soldering

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Footprint information for reflow soldering of XQFN16 package **SOT1161-1**

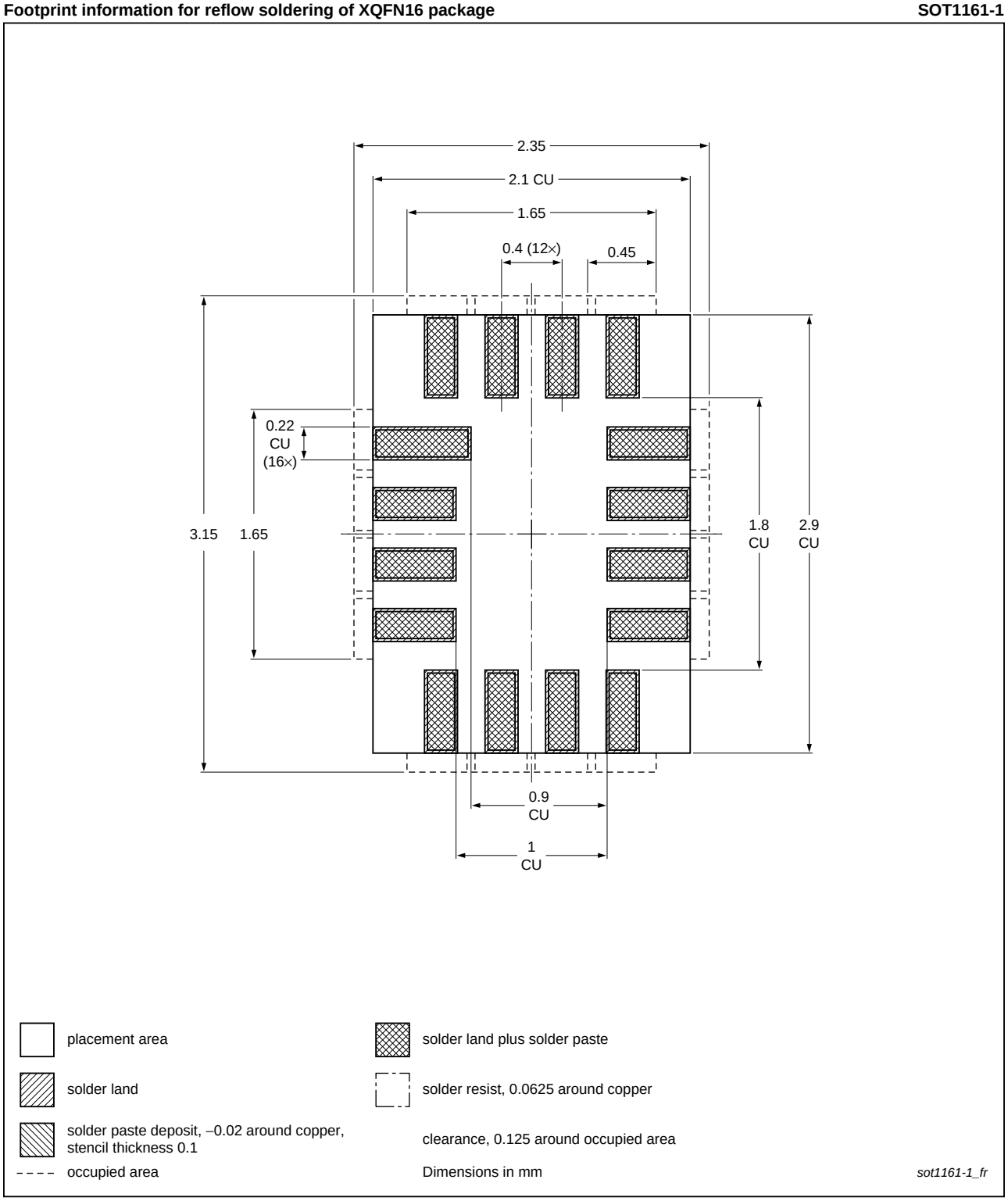


Fig 36. PCB footprint for SOT1161-1 (XQFN16); reflow soldering

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19. Abbreviations

Table 21. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
GPIO	General Purpose Input/Output
I²C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
LED	Light-Emitting Diode
LSB	Least Significant Bit
MSB	Most Significant Bit
PCB	Printed-Circuit Board
POR	Power-On Reset
SMBus	System Management Bus

20. Revision history

Table 22. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA6408A v.1	20120927	Product data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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