National Semiconductor

PRELIMINARY
May 1998

PC87351 PC98 and ACPI Compliant SuperI/O with System Wake-Up Control

Highlights

General Description

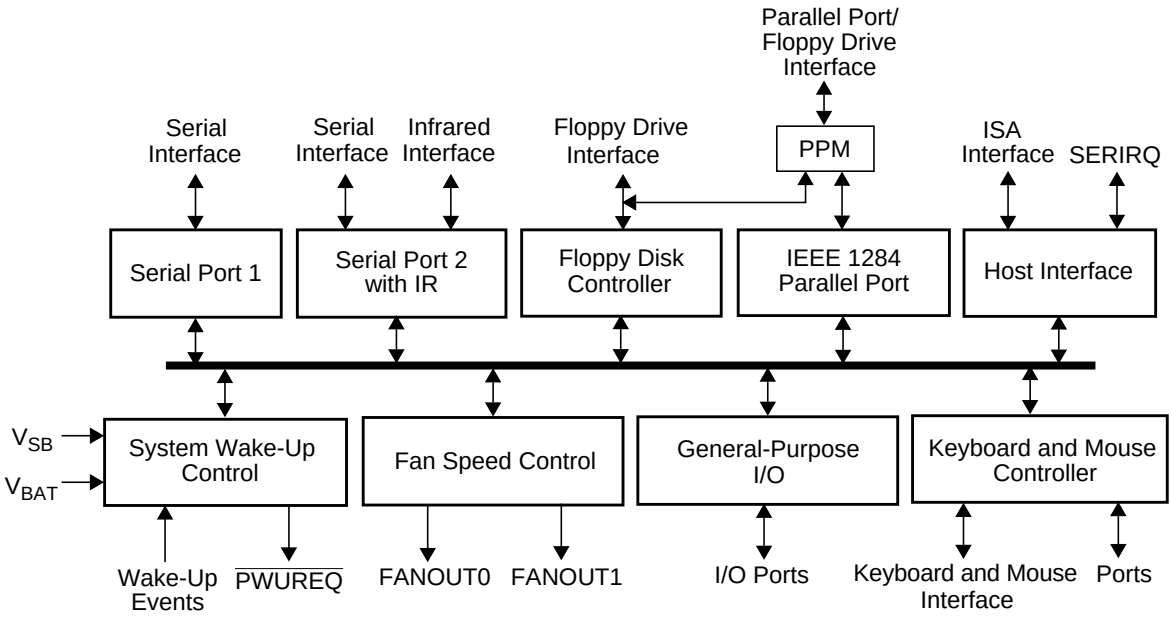
The PC87351, a member of National Semiconductor's SuperI/O family of integrated PC peripherals, is a 128-pin, PC98 and ACPI compliant SuperI/O that offers a single-chip solution to the most commonly used ISA peripherals.

The PC87351 incorporates: a Floppy Disk Controller (FDC) which is available also on the Parallel Port pins as a multiplexed option (PPM), two enhanced Serial Ports, Infrared Comunication Port (HP-SIR, Sharp-IR, and Consumer Electronics-IR), a full IEEE 1284 Parallel Port, a Keyboard and Mouse Controller (KBC), System Wake-Up Control (SWC), General-Purpose Input/Output (GPIO) Ports with assert interrupt capability, and Fan Speed Control (FSC).

Outstanding Features

- Fan Speed Control for two fans
- 11 General-Purpose I/O Ports, bi-directional, with interrupt assertion capability
- System Wake-Up Control powered by V_{SB}, generates power-up request in response to preprogrammed keyboard or mouse sequence, modem, telephone ring, and two general-purpose events without an external clock
- Serial or parallel IRQ support
- Programmable write protect for Floppy Disk Controller
- Power-fail recovery support

Block Diagram



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Highlights (Continued)

Features

- PC98 and ACPI Compliant
  - — PnP Configuration Register structure
  - — Flexible resource allocation for all logical devices
    - ❑ Relocatable base address
    - ❑ 9 Parallel IRQ or 15 Serial IRQ routing options
    - ❑ 3 optional 8-bit DMA channels (where applicable)
- Floppy Disk Controller (FDC)
  - — Software compatible with the PC8477, which contains a superset of the FDC functions in the µDP8473, the NEC µPD765A and the N82077
  - — 16-byte FIFO
  - — Burst and non-burst modes
  - — High-performance, digital data separator that does not require any external filter components
  - — Standard 5.25" and 3.5" Floppy Disk Drive (FDD) support
  - — Perpendicular recording drive support
  - — Three-mode FDD support
  - — Full support for IBM Tape Drive Register (TDR) implementation of AT and PS/2 drive types
  - — Programmable write protect
- Parallel Port
  - — Software or hardware control
  - — Enhanced Parallel Port (EPP) compatible with new version EPP 1.9 and IEEE 1284 compliant
  - — EPP support for version EPP 1.7 of the Xircom specification
  - — EPP support as mode 4 of the Extended Capabilities Port (ECP)
  - — IEEE 1284 compliant ECP, including level 2
  - — Selection of internal pull-up or pull-down resistor for Paper End (PE) pin
  - — PCI bus utilization reduction by supporting a demand DMA mode mechanism and a DMA fairness mechanism
  - — Protection circuit that prevents damage to the parallel port when a printer connected to it powers up or is operated at high voltages, even if the device is in power-down
  - — Output buffers that can sink and source 14 mA
- Parallel Port Multiplexer (PPM)
  - — Additional set of FDC signals multiplexed on Parallel Port pins
  - — Optional connection of additional, external FDD on Parallel Port connector
- Serial Port 1
  - — Software compatible with the 16550A and the 16450
  - — Shadow register support for write-only bit monitoring
  - — UART data rates up to 1.5 Mbaud
- Serial Port 2 with Infrared
  - — Software compatible with the 16550A and the 16450
  - — Shadow register support for write-only bit monitoring
  - — UART data rates up to 1.5 Mbaud
  - — HP-SIR
  - — ASK-IR option of SHARP-IR
  - — DASK-IR option of SHARP-IR
  - — Consumer Remote Control supports RC-5, RC-6, NEC, RCA and RECS 80
  - — Non-standard DMA support – 1 or 2 channels
- Keyboard and Mouse Controller (KBC)
  - — 8-bit microcontroller
  - — Software compatible with the 8042AH and PC87911 microcontrollers
  - — 2 KB custom-designed program ROM
  - — 256 bytes RAM for data
  - — Four programmable dedicated open-drain I/O lines
  - — Asynchronous access to two data registers and one status register during normal operation
  - — Support for both interrupt and polling
  - — 93 instructions
  - — 8-bit timer/counter
  - — Support for binary and BCD arithmetic
  - — Operation at 8 MHz,12 MHz or 16 MHz (programmable option)
  - — Can be customized by using the PC87323, which includes a RAM-based KBC as a development platform for KBC code
- 11 General-Purpose Bi-Directional I/O (GPIO) Ports
  - — 11 GPIO pins with interrupt assertion capability
  - — Programmable drive type for each output pin (open-drain, push-pull or output disable)
  - — Programmable option for internal pull-up resistor on each input pin
  - — Output lock option
  - — Back-drive protection circuit
- System Wake-Up Control (SWC)
  - — Power-up request upon detection of Keyboard, Mouse, $\overline{RI1}$, $\overline{RI2}$, $\overline{RING}$, PME1 and PME2 activity, as follows:
    - ❑ Preprogrammed Keyboard or Mouse sequence
    - ❑ External modem ring on serial ports
    - ❑ Ring pulse or pulse train on the $\overline{RING}$ input
    - ❑ General purpose events, PME1 and PME2
  - — Optional routing of power-up request on IRQ line
  - — Powered by V_{SB}
  - — Battery-backed wake-up setup
  - — Power-fail recovery support

Highlights (Continued)

- Fan Speed Control
  - Supports different fan types
  - Two speed control lines with Pulse Width Modulation (PWM)
    - Output signal in the range of 6 Hz to 93.75 KHz
    - Duty cycle resolution of 1/256
- Clock Sources
  - 48 MHz clock input
  - On-chip low frequency clock generator for wake-up
  - 33 MHz PCI clock input for Serial IRQ

Datasheet Revision Record

Revision Date	Status	Comments
January 1998	Advanced Information	First pass with pin assignment
March 1998	Preliminary	Implemented: Item 1, Important Notice, pin reassignment
May 1998	Preliminary	Implemented: Items 2-31 below Paginated Datasheet Revision Record in datasheet body

Item	Topic	Change/Correction	Location
2	Pin description	Table describing KBCLK, KBDAT, MCLK and MDAT signals enhanced to identify pin drivers	Section 1.4.7
3	PPM power save mode	All references deleted	Chapter 2
4	Device architecture	9 logical devices	Section 2.1
5	Index 74h, 75h DMA Channel Select 0, 1	Modified	Section 2.2.3, Table 2-7
6	VSB Power-Up Reset	Hardware reset explanation modified	Section 2.2.5
7	New section added	REGISTER TYPE ABBREVIATIONS added before the existing section; all subsequent numbering changed	Section 2.3
8	SuperI/O Configuration 1 Register Bit 3	Reserved	Section 2.4.3
9	SuperI/O Configuration 2 Register	**Bits 6 5 — Function** 0 0 — GPIO17 0 1 — KBRST (default) 1 0 — P12 1 1 — PNF (PPM mode enabled) **Bits 2 1 0 — Function** 0 0 X — GPIO14 (default) 0 1 1 — GPIO14 0 1 0 — IRQ9 1 0 X — IRRX2/IRSL0 1 1 X — P17	Section 2.4.4
10	SuperI/O Revision ID Register	Location and Type added	Section 2.4.7
11	Keyboard and Mouse Controller	All references to TEST0 and TEST1 changed to T0 and T1, respectively.	Section 2.11.1
12	Implementation	Ports 1 and 2 description deleted	Section 2.12.2
13	GPIO Configuration Registers' Access	Drawing modified	Figure 2-6
14	GPIO Pin Configuration Select Register Bits 5-4	01, 10: Binary value of the port number, 1-2 respectively 11: Reserved	Section 2.12.4
15	Fan Speed Control	General Description modified; nomenclature of Fan Control Duty Cycle and Fan Control Pre-Scale registers changed; references to Fan Speed Monitor deleted; configuration parameters (Reset and Type) modified	Section 2.13
16	System events	Number of events changed to seven	Section 3.2

Datasheet Revision Record (Continued)

Item	Topic	Change/Correction	Location
17	Keyboard Data Shift Register	Description modified	Section 3.4.6
18	Mouse Data Shift Register	Description modified	Section 3.4.7
19	Ports with fewer than 8 bits	Implementation description	Chapter 4
20	Interrupt Assertion and Handling	Bit nomenclature modified	Section 4.3
21	GPIO Pin Configuration Access Register	Bit nomenclature and descriptions changed	Section 4.4.1
22	GPIO Data Out Register	Bitmap and Reset values added	Section 4.4.3
23	GPIO Data In Register	Bitmap and Reset values added	Section 4.4.4
24	GPIO Interrupt Enable Register	Bitmap and Reset values added	Section 4.4.5
25	GPIO Status Register	Bitmap and Reset values added	Section 4.4.6
26	Functional Description	Corrected and enhanced	Section 5.2
27	Fan Control Duty Cycle Register Bits 7-0	00h: PWM output is continuously low 01h-FEh: PWM output is high for [Duty Cycle Value] clock cycles and low for [256-Duty Cycle Value] clock cycles FFh: PWM output is continuously high	Section 5.3.3
28	Device Specifications	Timing diagrams drawn more precisely	Chapter 11
29	V_{BAT} Battery Supply Current	Conditions and Max modified	Section 11.1.4
30	Host Interface I/O Cycle Timing	t_{RDYA}, t_{RDYI} and t_{RWI} added to table; footnote 2 added to table; IOCHRDY timing diagram added	Section 11.2.3
31	Serial IRQ Timing	Output timing diagram modified	Section 11.2.6

Contents at a Glance

This datasheet is organized to reflect two major topics: device specific issues (Highlights through Chapter 2), and proprietary functional blocks (Chapters 3 through 10). Chapter 11 summarizes the AC/DC device characteristics.

Highlights 1

This chapter provides a description and block diagram of the PC87351 major functional blocks, the features that make this device outstanding as compared with comparable devices, and the features of each functional block.

Datasheet Revision Record 4

This chapter serves two functions: it provides a record of the datasheet revisions; it documents the major changes of this revision as compared with the previous one. Each change is cross-referenced and linked to the change location within the datasheet.

1 Signal/Pin Connection and Description 11

This chapter includes four major sections: a connection diagram that shows all pins and their related signals; an alphabetical directory of all signals/pins linked to a table where more detailed information is provided; a summary of all multiplexed signals and how to configure them for default and alternate settings, and functionally grouped tables that describe each signal/pin in detail.

2 Device Architecture and Configuration 24

This chapter presents all PC87351 device specific information on the relevant functional blocks, as well as hardware and software configuration procedures and the related configuration registers.

3 System Wake-Up Control (SWC) 51

This chapter describes the system wake-up capabilities of the PC87351, designed to maximize device functionality while minimizing power consumption.

4 General-Purpose Input/Output (GPIO) Port 57

This chapter describes a single 8-bit GPIO port, whose operation is associated with two register sets. Refer to the Device Architecture and Configuration chapter for the specific implementation in this device.

5 Fan Speed Control 64

This chapter describes the Fan Speed Control, a programmable Pulse Width Modulation (PWM) generator whose output is used to control the fan's power voltage. Refer to the *Device Architecture and Configuration* chapter for the specific implementation in this device.

6-10 Legacy Functional Blocks

Please refer to the PC87307, PC87309 or PC87317 Datasheet for information on the Keyboard and Mouse Controller (KBC), Serial Port 1, Serial Port 2 with IR, Parallel Port and Floppy Disk Controller (FDC).

11 Device Characteristics 72

This chapter provides DC electrical characteristics, both general and of all device pins, as well as AC electrical characteristics.

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6.0 Floppy Disk Controller (FDC)
Refer to PC87307, PC87309 or PC87317 datasheet.

7.0 Parallel Port
Refer to PC87307, PC87309 or PC87317 datasheet.

8.0 Serial Port 2 with IR
Refer to PC87307, PC87309 or PC87317 datasheet.

9.0 Serial Port 1
Refer to PC87307, PC87309 or PC87317 datasheet.

10.0 Keyboard and Mouse Controller (KBC)
Refer to PC87307, PC87309 or PC87317 datasheet.

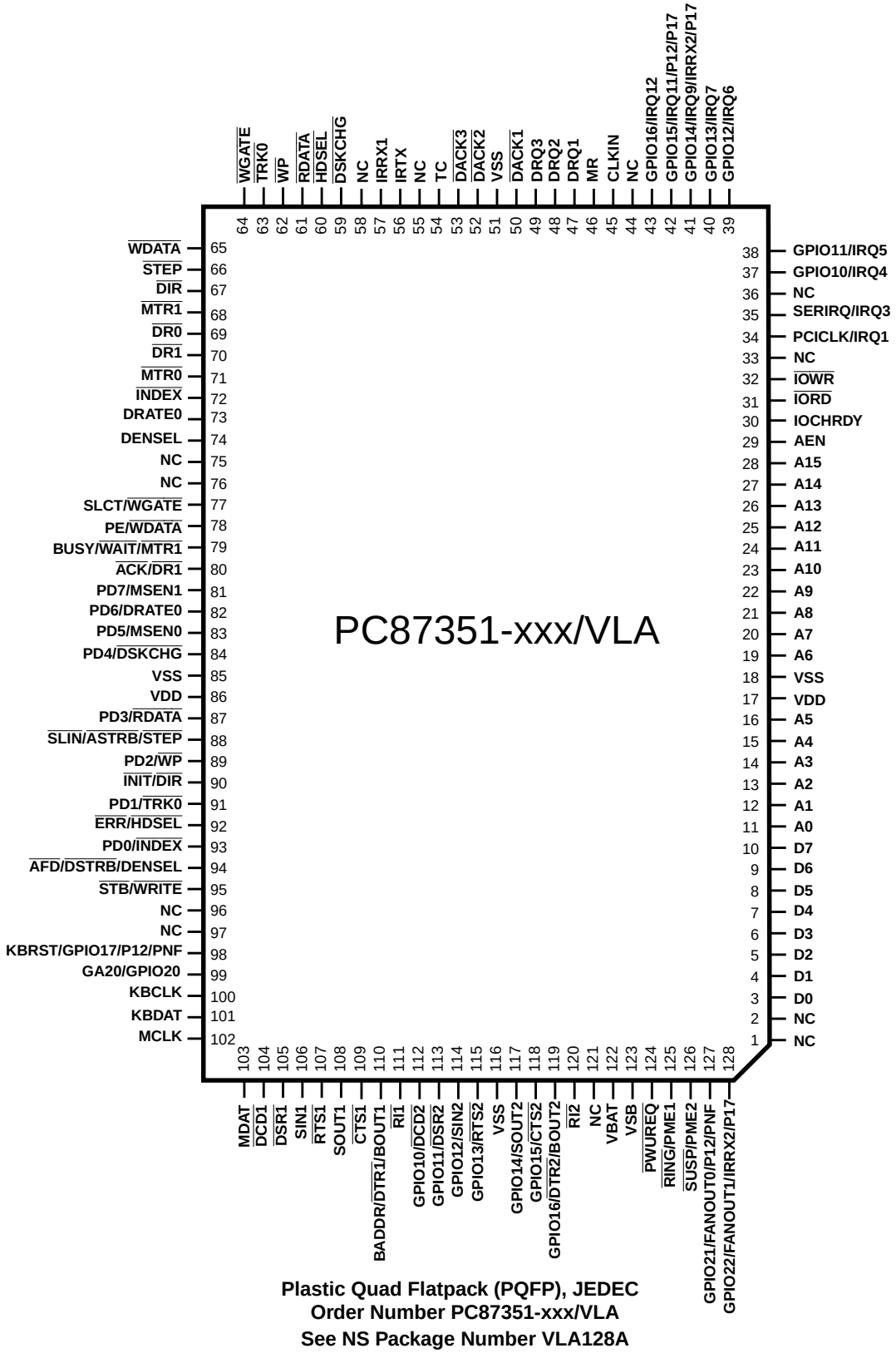
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1.0 Signal/Pin Connection and Description

1.1 CONNECTION DIAGRAM



Plastic Quad Flatpack (PQFP), JEDEC
Order Number PC87351-xxx/VLA
See NS Package Number VLA128A

xxx = Three character identifier for National data, and keyboard ROM and/or customer identification code

1.0 Signal/Pin Connection and Description (Continued)

1.2 SIGNAL/PIN DIRECTORY

See Table 1-2 for an alphabetical listing of all signals, cross-referenced to additional information for detailed functional descriptions, electrical DC characteristics, and pin multiplexing. The DC characteristics are denoted by a buffer type symbol, described briefly in Table 1-1 and in detail in Sections 11.1.6 to 11.1.10. The pin multiplexing information refers to three different types of multiplexing:

- MUX - Multiplexed functions. Pins are shared between two different functions. Each function is associated with different board connectivity, and normally, the function selection is determined by the board design and cannot be changed dynamically. The multiplexing options must be configured by the BIOS upon power-up, in order to comply with the board implementation.
- MM - Multiple Mode. Pins have two or more modes of operation within the same function. These modes are associated with the same external (board) connectivity. Mode selection may be controlled by the device driver, through the registers of the functional block, and do not require a special BIOS setup upon power-up. These pins are not considered multiplexed pins from the SuperI/O configuration perspective. The mode selection method (registers and bits) as well as the signal specification in each mode, are described within the functional description of the relevant functional blocks.
- PPM - Parallel Port MUX. This special multiplexing of the FDC signals on the Parallel Port pins allows connection of the external FDC through the Parallel Port connector. This multiplexing is dynamic, controlled by hardware, and does not require any special BIOS setup except for enabling the PPM function. The PPM functionality and a listing of the pins that are multiplexed are described in Section 2.5.

Table 1-1. Buffer Types

Name	Description	Section
GND	Ground pin	N/A
IN_{PCI}	Input, PCI 5V	11.1.5
IN_{STRP}	Input, Strap pin (min VIH is 0.6VDD) with weak pull-down during strap time	11.1.6
IN_{T}	Input, TTL compatible	11.1.7
IN_{TS}	Input, TTL compatible with Schmitt trigger	11.1.8
IN_{ULR}	Input, with serial UL Resistor	N/A
$O_{p/n}$	Output, Totem-Pole buffer that is capable of sourcing *p* mA and sinking *n* mA	11.1.9
OD_{n}	Output, Open-Drain output buffer that is capable of sinking *n* mA	11.1.10
PWR	Power pin	N/A

Table 1-2. Signal/Pin Directory

Signal	Pin/s	Functional Group		DC Characteristics		Multiplexed
		Name	Section	Buffer Type	Section	
A15-0	28-19, 16-11	Host Interface	1.4.5	IN_{T}	11.1.7	
$\overline{ACK}$	80	Parallel Port	1.4.8	IN_{T}	11.1.7	PPM
AEN	29	Host Interface	1.4.5	IN_{T}	11.1.7	
$\overline{AFD}/\overline{DSTRB}$	94	Parallel Port	1.4.8	OD_{14}, $O_{14/14}$	11.1.10, 11.1.9	MM/PPM
$\overline{ASTRB}$	See $\overline{SLIN}/\overline{ASTRB}$					
BADDR	110	Strapping	1.4.11	IN_{STRP}	11.1.6	MUX
BOUT1	See $\overline{DTR1}$/BOUT1					
BOUT2	See $\overline{DTR2}$/BOUT2					
BUSY/$\overline{WAIT}$	79	Parallel Port	1.4.8	IN_{T}	11.1.7	MM/PPM
CLKIN	45	Clock	1.4.1	IN_{T}	11.1.7	

1.0 Signal/Pin Connection and Description (Continued)

Table 1-2. Signal/Pin Directory (Continued)

Signal	Pin/s	Functional Group		DC Characteristics		Multiplexed
		Name	Section	Buffer Type	Section	
$\overline{CTS1}$	109	Serial Port 1	1.4.10	IN_{TS}	11.1.8	
$\overline{CTS2}$	118	Serial Port 2	1.4.10	IN_{TS}	11.1.8	MUX
D7-0	10-3	Host Interface	1.4.5	IN_T $O_{15/24}$	11.1.7 11.1.9	
$\overline{DACK1\text{-}3}$	50, 52-53	Host Interface	1.4.5	IN_T	11.1.7	
$\overline{DCD1}$	104	Serial Port 1	1.4.10	IN_{TS}	11.1.8	
$\overline{DCD2}$	112	Serial Port 2	1.4.10	IN_{TS}	11.1.8	MUX
DENSEL	74	FDC	1.4.3	OD_{24}, $O_{4/24}$	11.1.10, 11.1.9	
	94					PPM
$\overline{DIR}$	67	FDC	1.4.3	OD_{24}, $O_{4/24}$	11.1.10, 11.1.9	
	90					PPM
$\overline{DR0}$	69	FDC	1.4.3	OD_{24}, $O_{4/24}$	11.1.10, 11.1.9	
$\overline{DR1}$	70	FDC	1.4.3	OD_{24}, $O_{4/24}$	11.1.10, 11.1.9	
	80					PPM
DRATE0	73	FDC	1.4.3	$O_{6/12}$	11.1.9	
	82					PPM
DRQ1-3	47-49	Host Interface	1.4.5	$O_{15/24}$	11.1.9	
$\overline{DSKCHG}$	59	FDC	1.4.3	IN_T	11.1.7	
	84					PPM
$\overline{DSR1}$	105	Serial Port 1	1.4.10	IN_{TS}	11.1.8	
$\overline{DSR2}$	113	Serial Port 2	1.4.10	IN_{TS}	11.1.8	MUX
$\overline{DSTRB}$	See AFD/DSTRB					
$\overline{DTR1}$/BOUT1	110	Serial Port 1	1.4.10	$O_{6/12}$	11.1.9	MM
$\overline{DTR2}$/BOUT2	119	Serial Port 2	1.4.10	$O_{6/12}$	11.1.9	MM/MUX
$\overline{ERR}$	92	Parallel Port	1.4.8	IN_T	11.1.7	PPM
FANOUT0	127	Fan Speed Control	1.4.2	$O_{2/20}$	11.1.9	MUX
FANOUT1	128	Fan Speed Control	1.4.2	$O_{2/20}$	11.1.9	MUX
GPIO17-10	98, 37-43 or 112-5, 117-9	GPIO Port 1	1.4.4	IN_{TS} OD_{12}, $O_{6/12}$	11.1.8 11.1.10, 11.1.9	MUX
GPIO22-20	127-128, 99	GPIO Port 2	1.4.4	IN_{TS} OD_{12}, $O_{6/12}$	11.1.8 11.1.10, 11.1.9	MUX
$\overline{HDSEL}$	60	FDC	1.4.3	OD_{24}, $O_{4/24}$	11.1.10, 11.1.9	
	92					PPM
$\overline{INDEX}$	72	FDC	1.4.3	IN_T	11.1.7	
	93					PPM

1.0 Signal/Pin Connection and Description (Continued)

Table 1-2. Signal/Pin Directory (Continued)

Signal	Pin/s	Functional Group		DC Characteristics		Multiplexed
		Name	Section	Buffer Type	Section	
GA20	99	KBC	1.4.7	OD_4	11.1.10	MUX
$\overline{INIT}$	90	Parallel Port	1.4.8	OD_{14}, $O_{14/14}$	11.1.10, 11.1.9	PPM
IOCHRDY	30	Host Interface	1.4.5	OD_{24}	11.1.10	
$\overline{IORD}$	31	Host Interface	1.4.5	IN_T	11.1.7	
$\overline{IOWR}$	32	Host Interface	1.4.5	IN_T	11.1.7	
IRQ1, 3-7, 9, 11-12	34, 35, 37-43	Host Interface	1.4.5	IN_T OD_{24}, $O_{15/24}$	11.1.7 11.1.10, 11.1.9	MUX
IRRX1	57	Infrared	1.4.5	IN_T	11.1.7	
IRRX2/IRSL0	41, 128	Infrared	1.4.5	IN_T $O_{6/12}$	11.1.7 11.1.9	MM/MUX
IRRX2	See IRRX2/IRSL0					
IRSL0	See IRRX2/IRSL0					
IRTX	56	Infrared	1.4.5	$O_{6/12}$	11.1.9	
KBCLK	100	Wake-Up KBC	1.4.12 1.4.7	IN_T OD_4	11.1.7 11.1.10	
KBDAT	101	Wake-Up KBC	1.4.12 1.4.7	IN_T OD_4	11.1.7 11.1.10	
KBRST	98	KBC	1.4.7	OD_4	11.1.10	MUX
MCLK	102	Wake-Up KBC	1.4.12 1.4.7	IN_T OD_4	11.1.7 11.1.10	
MDAT	103	Wake-Up KBC	1.4.12 1.4.7	IN_T OD_4	11.1.7 11.1.10	
MR	46	Host Interface	1.4.5	IN_{TS}	11.1.8	
MSEN0	83	FDC	1.4.3	IN_T	11.1.7	PPM
MSEN1	81	FDC	1.4.3	IN_T	11.1.7	PPM
$\overline{MTR0}$	71	FDC	1.4.3	OD_{24}, $O_{4/24}$	11.1.10, 11.1.9	
$\overline{MTR1}$	68	FDC	1.4.3	OD_{24}, $O_{4/24}$	11.1.10, 11.1.9	
	79					PPM
P12	42, 98, 127	KBC	1.4.7	OD_4	11.1.10	MUX
P17	41, 42, 128	KBC	1.4.7	OD_4	11.1.10	MUX
PCICLK	34	Host Interface	1.4.5	IN_T	11.1.7	MUX
PD7-0	81-84, 87, 89, 91, 93	Parallel Port	1.4.8	IN_T OD_{14}, $O_{14/14}$	11.1.7 11.1.10, 11.1.9	PPM
PE	78	Parallel Port	1.4.8	IN_T	11.1.7	PPM
PME1	125	Wake-Up	1.4.12	IN_{TS}	11.1.8	MUX
PME2	126	Wake-Up	1.4.12	IN_{TS}	11.1.8	MUX

1.0 Signal/Pin Connection and Description (Continued)

Table 1-2. Signal/Pin Directory (Continued)

Signal	Pin/s	Functional Group		DC Characteristics		Multiplexed
		Name	Section	Buffer Type	Section	
PNF	98, 127	Parallel Port	1.4.8	IN_T	11.1.7	MUX
$\overline{PWUREQ}$	124	Wake-Up	1.4.12	OD_{12}	11.1.10	
$\overline{RDATA}$	61	FDC	1.4.3	IN_T	11.1.7	
	87					PPM
$\overline{RI1}$	111	Wake-Up Serial Port 1	1.4.12 1.4.10	IN_{TS}	11.1.8	
$\overline{RI2}$	120	Wake-Up Serial Port 2	1.4.12 1.4.10	IN_{TS}	11.1.8	
$\overline{RING}$	125	Wake-Up	1.4.12	IN_{TS}	11.1.8	MUX
$\overline{RTS1}$	107	Serial Port 1	1.4.10	$O_{6/12}$	11.1.9	
$\overline{RTS2}$	115	Serial Port 2	1.4.10	$O_{6/12}$	11.1.9	MUX
SERIRQ	35	Host Interface	1.4.5	IN_{TS} $O_{15/24}$	11.1.8 11.1.9	MUX
SIN1	106	Serial Port 1	1.4.10	IN_{TS}	11.1.8	
SIN2	114	Serial Port 2	1.4.10	IN_{TS}	11.1.8	MUX
SLCT	77	Parallel Port	1.4.8	IN_T	11.1.7	PPM
$\overline{SLIN}$/$\overline{ASTRB}$	88	Parallel Port	1.4.8	OD_{14}, $O_{14/14}$	11.1.10, 11.1.9	MM/PPM
SOUT1	108	Serial Port 1	1.4.10	$O_{6/12}$	11.1.9	
SOUT2	117	Serial Port 2	1.4.10	$O_{6/12}$	11.1.9	MUX
$\overline{STEP}$	66	FDC	1.4.3	OD_{24}, $O_{4/24}$	11.1.10, 11.1.9	
	88					PPM
$\overline{STB}$/$\overline{WRITE}$	95	Parallel Port	1.4.8	OD_{14}, $O_{14/14}$	11.1.10, 11.1.9	MM
$\overline{SUSP}$	126	Wake-Up	1.4.12	IN_{TS}	11.1.8	MUX
TC	54	Host Interface	1.4.5	IN_T	11.1.7	
$\overline{TRK0}$	63	FDC	1.4.3	IN_T	11.1.7	
	91					PPM
V_{BAT}	122	Power and Ground	1.4.11	IN_{ULR}	N/A	
V_{DD}	17, 86	Power and Ground	1.4.9	PWR	N/A	
V_{SB}	123	Power and Ground	1.4.12	PWR	N/A	
V_{SS}	18, 51, 85, 116	Power and Ground	1.4.12	GND	N/A	
$\overline{WAIT}$	See BUSY/$\overline{WAIT}$					
$\overline{WDATA}$	65	FDC	1.4.3	OD_{24}, $O_{4/24}$	11.1.10, 11.1.9	
	78					PPM

1.0 Signal/Pin Connection and Description (Continued)

Table 1-2. Signal/Pin Directory (Continued)

Signal	Pin/s	Functional Group		DC Characteristics		Multiplexed
		Name	Section	Buffer Type	Section	
$\overline{WGATE}$	64	FDC	1.4.3	OD_{24}, $O_{4/24}$	11.1.10, 11.1.9	
	77					PPM
$\overline{WP}$	62	FDC	1.4.3	IN_T	11.1.7	
	89					PPM
$\overline{WRITE}$	See $\overline{STB}/\overline{WRITE}$					

1.3 PIN MULTIPLEXING

There are three categories of pins with multiple names: Multiplexed (MUX), Multiple Mode (MM) and Parallel Port MUX (PPM). See Section 1.2 for descriptions of these categories. All the multiplexing options in the MUX category and their associated setup configuration are described in Table 1-3. A multiplexing option may be chosen on one pin only per group.

Table 1-3. Pin Multiplexing Configuration

Pin	Default			Alternate		
	Signal	I/O	Configuration	Signal	I/O	Configuration
34	PCICLK	I	SIOCF2, Bit 0 = 0	IRQ1	I/O	SIOCF2, Bit 0 = 1
35	SERIRQ	I/O	SIOCF2, Bit 0 = 0	IRQ3	I/O	SIOCF2, Bit 0 = 1
37	GPIO10	I/O	SIOCF2, Bit 0 = 0	IRQ4	I/O	SIOCF2, Bit 0 = 1
38	GPIO11			IRQ5		
39	GPIO12			IRQ6		
40	GPIO13			IRQ7		
43	GPIO16			IRQ12		
41	GPIO14	I/O	SIOCF2, Bits 2-1 = 00 or Bits 2-0 = 011	IRQ9	I/O	SIOCF2, Bits 2-0 = 010
				IRRX2/IRSL0	I/O	SIOCF2, Bits 2-1 = 10
				P17	I/O	SIOCF2, Bits 2-1 = 11
42	GPIO15	I/O	SIOCF2, Bits 4-3 = 00 or Bits 4-3, 0 = 011	IRQ11	O	SIOCF2, Bits 4-3, 0 = 010
				P12	I/O	SIOCF2, Bits 4-3 = 10
				P17	I/O	SIOCF2, Bits 4-3 = 11
98	KBRST	I/O	SIOCF2, Bits 6-5 = 01	GPIO17	I/O	SIOCF2, Bits 6-5 = 00
				P12	I/O	SIOCF2, Bits 6-5 = 10
				PNF	I/O	SIOCF2, Bits 6-5 = 11
99	GA20	I/O	SIOCF2, Bit 7 = 1	GPIO20	I/O	SIOCF2, Bit 7 = 0

1.0 Signal/Pin Connection and Description (Continued)

Table 1-3. Pin Multiplexing Configuration (Continued)

Pin	Default			Alternate		
	Signal	I/O	Configuration	Signal	I/O	Configuration
112	GPIO10	I/O	SIOCF3, Bit 0 = 0	$\overline{DCD2}$	I	SIOCF3, Bit 0 = 1
113	GPIO11			$\overline{DSR2}$	I	
114	GPIO12			SIN2	I	
115	GPIO13			$\overline{RTS2}$	O	
117	GPIO14			SOUT2	O	
118	GPIO15			$\overline{CTS2}$	I	
119	GPIO16			$\overline{DTR2}$/BOUT2	O	
125	$\overline{RING}$	I	SIOCF4, Bit 0 = 0	PME1	I	SIOCF4, Bit 0 = 1
126	$\overline{SUSP}$	I	SIOCF4, Bit 2 = 0	PME2	I	SIOCF4, Bit 2 = 1
127	GPIO21	I/O	SIOCF3, Bits 2-1 = 00	FANOUT0	I/O	SIOCF3, Bits 2-1 = 01
				P12	I/O	SIOCF3, Bits 2-1 = 10
				PNF	I/O	SIOCF3, Bits 2-1 = 11
128	GPIO22	I/O	SIOCF3, Bits 4-3 = 00	FANOUT1	I/O	SIOCF3, Bits 4-3 = 01
				IRRX2/IRSL0	I/O	SIOCF3, Bits 4-3 = 10
				P17	I/O	SIOCF3, Bits 4-3 = 11

1.4 DETAILED SIGNAL/PIN DESCRIPTIONS

1.4.1 Clock

Signal	Pin/s	I/O	Buffer Type	Description
CLKIN	45	I	IN_T	**Clock In.** A 48MHz clock input.

1.4.2 Fan Speed Control

Signal	Pin/s	I/O	Buffer Type	Description
FANOUT0 FANOUT1	127, 128	O	$O_{2/20}$	**Fan Output 0, 1.** Pulse Width Modulation (PWM) signals, that are used to control the speed of cooling fans by controlling the voltage supplied to the fan's motor.

1.4.3 FDC (Including PPM)

The Parallel-Port/FDC MUX (PPM) provides a means to connect an external FDD on the Parallel Port connector, in addition to the internal FDD on the FDC header. This is done by physically connecting internally each FDC pin to a corresponding Parallel Port pin while isolating it from the Parallel Port logic. The Parallel Port becomes an additional connecting point to the FDC interface as long as the PPM is in active mode. The functional descriptions in this table apply to both the FDC pin and to the corresponding PPM pin. For a detailed description of PPM functionality, see Section 2.5.

1.0 Signal/Pin Connection and Description (Continued)

Signal	Pin/s	I/O	Buffer Type	Description
DENSEL	74	O	$O_{4/24}$	**Density Select.** Indicates that a high FDC density data rate (500 Kbps or 1 Mbps) or a low density data rate (250 or 300 Kbps) is selected. DENSEL polarity is controlled by bit 5 of the FDC Configuration Register.
	94			This pin provides an additional density select signal in PPM mode when PNF = 0.
$\overline{DIR}$	67	O	OD_{24}-$O_{4/24}$	**Direction.** Determines the direction of the Floppy Disk Drive (FDD) head movement (active = step in, inactive = step out) during a seek operation. During reads or writes, $\overline{DIR}$ is inactive.
	90			This pin provides an additional direction signal in PPM mode when PNF = 0.
$\overline{DR0}$	69	O	OD_{24}-$O_{4/24}$	**Drive Select 0.** Decoded drive select output signal. $\overline{DR0}$ is controlled by Digital Output Register (DOR) bit 0.
$\overline{DR1}$	70	O	OD_{24}-$O_{4/24}$	**Drive Select 1.** Decoded drive select output signal. $\overline{DR1}$ is controlled by Digital Output Register (DOR) bit 1.
	80			This pin provides an additional drive select 1 signal in PPM mode when PNF = 0.
DRATE0	73	O	$O_{6/12}$	**Data Rate 0.** Reflects the value of bit 0 of the Configuration Control Register (CCR) or the Data Rate Select Register (DSR), whichever was written to last. Output from the pin is totem-pole buffered.
	82			This pin provides an additional FDC data rate signal in PPM mode, when PNF = 0.
$\overline{DSKCHG}$	59	I	IN_T	**Disk Change.** Indicates if the drive door has been opened. The state of this pin is stored in the Digital Input Register (DIR). This pin can also be configured as the RGATE data separator diagnostic input signal via the MODE command.
	84			This pin provides an additional FDC Disk Change signal in PPM Mode when PNF = 0.
$\overline{HDSEL}$	60	O	OD_{24}, $O_{4/24}$	**Head Select.** Determines which side of the FDD is accessed. Active low selects side 1, inactive selects side 0.
	92			This pin provides an additional head select signal in PPM mode when PNF = 0.
$\overline{INDEX}$	72	I	IN_T	**Index.** Indicates the beginning of an FDD track.
	93			This pin provides an additional index signal in PPM mode when PNF = 0.
MSEN0, MSEN1	82, 80	I	IN_T	**Media Sense Signals 0 and 1.** Provide media sense signals only in PPM mode when PNF = 0.
$\overline{MTR0}$	71	O	OD_{24}, $O_{4/24}$	**Motor Select 0.** Active low, motor enable line for drive 0, controlled by bits D7-4 of the Digital Output Register (DOR). This signal is not available on the PPM, assuming that the external FDD is either drive 1 or 3.
$\overline{MTR1}$	68	O	OD_{24}, $O_{4/24}$	**Motor Select 1.** Active low, motor enable line for drive 1, controlled by bits D7-4 of the Digital Output Register (DOR).
	79			This pin provides an additional motor select 1 signal in PPM mode when PNF = 0. This pin is the motor enable line for drive 1 or drive 0, according to the TDR Register.
$\overline{RDATA}$	61	I	IN_T	**Read Data.** Raw serial input data stream read from the FDD.
	87			This pin provides an additional read data signal in PPM mode when PNF = 0.

1.0 Signal/Pin Connection and Description (Continued)

Signal	Pin/s	I/O	Buffer Type	Description
$\overline{STEP}$	66	O	OD_{24}, $O_{4/24}$	**Step.** Issues pulses to the disk drive at a software programmable rate to move the head during a seek operation.
	88			This pin provides an additional step signal in PPM mode when PNF = 0.
$\overline{TRK0}$	63	I	IN_T	**Track 0.** Indicates to the controller that the head of the selected floppy disk drive is at track 0.
	91			This pin provides an additional Track 0 signal in PPM Mode when PNF = 0.
$\overline{WDATA}$	65	O	OD_{24}, $O_{4/24}$	**Write Data.** Carries out the write pre-compensated serial data that is written to the selected floppy disk drive. Pre-compensation is software selectable.
	78			This pin provides an additional $\overline{WDATA}$ signal in PPM mode when PNF = 0.
$\overline{WGATE}$	64	O	OD_{24}, $O_{4/24}$	**Write Gate.** Enables the write circuitry of the selected disk drive. WGATE is designed to prevent glitches during power up and power down. This prevents writing to the disk when power is cycled.
	77			This pin provides an additional $\overline{WGATE}$ signal in PPM mode when PNF = 0.
$\overline{WP}$	62	I	IN_T	**Write Protected.** Indicates that the disk in the selected drive is write protected. A software programmable configuration bit (FDC configuration at Index F0h, Logical Device 0) can force an active write-protect indication to the FDC regardless of the status of this pin.
	89			This pin provides an additional $\overline{WP}$ signal in PPM mode when PNF = 0.

1.4.4 General-Purpose Input/Output (GPIO) Ports

Signal	Pin/s	I/O	Buffer Type	Description
GPIO17 GPIO16-10	98 43-37	I/O	IN_{TS}/ OD_{12}, $O_{6/12}$	**General-Purpose I/O Port 1, bits 0-7.** Each pin is configured independently as input or I/O, with or without static pull-up, and with either open-drain or totem-pole output type. The port support interrupt assertion and each pin can be enabled or masked as interrupt source.
GPIO 16-10	119-117, 115-112			These pins provide alternate GPIO location options.
GPIO22-20	128, 127, 99	I/O	IN_{TS}/ $OD_{12,}$ $O_{6/12}$	**General-Purpose I/O Port 2, bits 0-2.** Same as Port 1.

1.0 Signal/Pin Connection and Description (Continued)

1.4.5 Host Interface

Signal	Pin/s	I/O	Buffer Type	Description
A15-A0	11-16, 19-28	I	IN_T	**Address.** These address lines of the ISA bus determine which internal register is accessed. A15-A0 are don't cares during DMA transfer.
AEN	29	I	IN_T	**Address Enable.** This input disables function selection via A15-A0 when it is high. Access during DMA transfer is NOT affected by this pin.
D7-D0	45	I/O	$IN_T/O_{15/24}$	**Data.** Bi-directional data lines of the ISA bus. D7 is the MSB and D0 is the LSB.
$\overline{DACK1\text{-}3}$	50, 52, 53	I	IN_T	**DMA Acknowledge 1, 2 and 3**. These active low signals acknowledge a request for DMA services and enable the $\overline{IORD}$ and the $\overline{IOWR}$ input signals during DMA transfer.
DRQ1-3	47-49	O	$O_{15/24}$	**DMA Request 1, 2, and 3.** These active high output signals inform the DMA controller that a data transfer is needed.
IOCHRDY	30	O	OD_{24}	**I/O Channel Ready.** This is the I/O channel ready open drain output signal. When IOCHRDY is driven low, the EPP extends the host cycle.
$\overline{IORD}$	31	I	IN_{TS}	**I/O Read.** An active low $\overline{RD}$ input signal indicates that the microprocessor has read data.
$\overline{IOWR}$	32	I	IN_{TS}	**I/O Write.** $\overline{WR}$ is an active low input signal that indicates a write operation from the microprocessor to the controller.
IRQ1,3-7, 9, 11-12	34,35, 37-43	I/O	IN_T/ OD_{24}, $O_{15/24}$	**Interrupt Request 1, 3-7, 9, 11-12.** IRQ polarity and output type selection is software configurable by the logical device mapped to the IRQ line.
MR	46	I	IN_{TS}	**Master Reset.** An active high MR input signal resets the device with its default settings.
PCICLK	34	I	IN_{PCI}	**PCI Clock.** Up to 33 MHz.
SERIRQ	35	I/O	$IN_T/O_{15/24}$	**Serial IRQ.** Encoded interrupts on a serial line.
TC	54	I	IN_T	**DMA Terminal Count.** The DMA controller issues TC to indicate the termination of a DMA transfer. TC is accepted only when a $\overline{DACK}$ signal is active. TC is active high in PC-AT mode, and active low in PS/2 mode.

1.4.6 Infrared (IR)

Signal	Pin/s	I/O	Buffer Type	Description
IRRX1	57	I	IN_T	**IR Reception 1.** Primary input to receive serial data from the IR transceiver module.
IRRX2/ IRSL0	41, 128	I/O	$IN_T/O_{6/12}$	**IRRX2 - IR Reception 2.** Auxiliary IR receiver input to support two transceiver modules. **IRSL0** - **IR Control Signals 0**. Output to control the IR analog front end.
IRTX	56	O	$O_{6/12}$	**IR Transmit.** IR serial output data.

1.0 Signal/Pin Connection and Description (Continued)

1.4.7 Keyboard and Mouse Controller (KBC)

Signal	Pin/s	I/O	Buffer Type	Description
GA20	99	I/O	IN_{TS}/OD_4	**Gate A20.** KBC gate A20 (P21) output.
KBCLK	100	I/O	IN_{TS}/OD_4	**Keyboard Clock.** Transfers the keyboard clock between the SuperI/O chip and the external keyboard using the PS/2 protocol. This pin is driven by the internal, inverted KBC P26 signal, and is connected internally to the T0 signal of the KBC. External pull-up resistor to 5V is required (for PS/2 compliance). The pin is monitored for wake-up event detection. However, to enable the activity during power off, it must be pulled up to Keyboard and Mouse standby voltage.
KBDAT	101	I/O	IN_{TS}/OD_4	**Keyboard Data.** Transfers the keyboard data between the SuperI/O chip and the external keyboard using the PS/2 protocol. This pin is driven by the internal, inverted KBC P27 signal, and is connected internally to KBC P10. External pull-up resistor to 5V is required (for PS/2 compliance). The pin is monitored for wake-up event detection. To enable the activity, it must be pulled up to Keyboard and Mouse standby voltage.
KBRST	98	I/O	IN_{TS}/OD_4	**KBD Reset.** Keyboard Reset (P20) output.
MCLK	102	I/O	IN_{TS}/OD_4	**Mouse Clock.** Transfers the mouse clock between the SuperI/O chip and the external keyboard using the PS/2 protocol. This pin is driven by the internal, inverted KBC P23 signal, and is connected internally to KBC's T1. External pull-up resistor to 5V is required (for PS/2 compliance). The pin is monitored for wake-up event detection. To enable the activity, it must be pulled up to Keyboard and Mouse standby voltage.
MDAT	103	I/O	IN_{TS}/OD_4	**Mouse Data.** Transfers the mouse data between the SuperI/O chip and the external keyboard using the PS/2 protocol. This pin is driven by the internal, inverted KBC P22 signal, and is connected internally to KBC's P11. External pull-up resistor to 5V is required (for PS/2 compliance). The pin is monitored for wake-up event detection. To enable the activity, it must be pulled up to Keyboard and Mouse standby voltage.
P12	42, 98, 127	I/O	IN_{TS}/OD_4	**I/O Port.** KBC open-drain signal for general-purpose input and output, controlled by KBC firmware.
P17	41, 42, 128	I/O	IN_{TS}/OD_4	**I/O Port.** KBC open-drain signal for general-purpose input and output, controlled by KBC firmware.

1.0 Signal/Pin Connection and Description (Continued)

1.4.8 Parallel Port

Signal	Pin/s	I/O	Buffer Type	Description
$\overline{ACK}$	80	I	IN_T	**Acknowledge.** Pulsed low by the printer to indicate that it has received data from the Parallel Port.
$\overline{AFD}$/ $\overline{DSTRB}$	94	O	OD_{14}, $O_{14/14}$	**$\overline{AFD}$ - Automatic Feed.** When low, instructs the printer to automatically feed a line after printing each line. This pin is in TRI-STATE after a 0 is loaded into the corresponding control register bit. An external 4.7 KΩ pull-up resistor should be attached to this pin. **$\overline{DSTRB}$ - Data Strobe (EPP).** Active low, used in EPP mode as a data strobe.
BUSY/$\overline{WAIT}$	79	I	IN_T	**Busy.** Set high by the printer when it cannot accept another character. **Wait.** In EPP mode, the Parallel Port device uses this active low signal to extend its access cycle.
$\overline{ERR}$	92	I	IN_T	**Error.** Set active low by the printer when it detects an error.
$\overline{INIT}$	90	O	OD_{14}-$O_{14/14}$	**Initialize.** When low, initializes the printer. This signal is in TRI-STATE after a 1 is loaded into the corresponding control register bit. Use an external 4.7 KΩ pull-up resistor.
PD7-0	81-84, 87, 89, 91, 93	I/O	IN_T/ OD_{14}, $O_{14/14}$	**Parallel Port Data.** Transfer data to and from the peripheral data bus and the appropriate Parallel Port data register. These signals have a high current drive capability.
PE	78	I	IN_T	**Paper End.** Set high by the printer when it is out of paper. This pin has an internal weak pull-up or pull-down resistor.
PNF	98, 127	I	IN_T	**Printer Not Floppy.** This input from the Parallel Port connector is used to detect that a floppy drive is connected to the Parallel Port, and to activates the PPM. The PNF pin is driven to 1 when a parallel device is connected, and to 0 when external FDD is connected. This pin is functional only when the PPM mode is enabled.
SLCT	77	I	IN_T	**Select.** Set active high by the printer when the printer is selected.
$\overline{SLIN}$/ $\overline{ASTRB}$	88	O	OD_{14}, $O_{14/14}$	**$\overline{SLIN}$ - Select Input.** When low, selects the printer. This signal is in TRI-STATE after a 0 is loaded into the corresponding control register bit. Uses an external 4.7 KΩ pull-up resistor. **$\overline{ASTRB}$ - Address Strobe (EPP).** Active low, used in EPP mode as an address strobe.
$\overline{STB}$/ $\overline{WRITE}$	95	O	OD_{14}, $O_{14/14}$	**$\overline{STB}$ - Data Strobe.** Indicates to the printer that valid data is available at the printer port. This signal is in TRI-STATE after a 0 is loaded into the corresponding control register bit. An external 4.7 KΩ pull-up resistor should be employed. **$\overline{WRITE}$ - Write Strobe.** In EPP mode, this active low signal is a write strobe.

1.4.9 Power and Ground

Signal	Pin/s	Buffer Type	Description
V_{BAT}	122	IN_{ULR}	**Battery Power Supply.** Provides battery back-up to the System Wake-Up Control registers, when V_{SB} is lost (power-fail). The pin is connected to the internal logic through a series resistor for UL protection.
V_{DD}	17, 86	PWR	**Main 5V Power Supply.**
V_{SB}	123	PWR	**Standby Power Supply.** Provides 5V power to the Wake-Up Control circuitry, while the main power supply is turned off.
V_{SS}	18, 51, 85, 116	GND	**Ground.**

1.0 Signal/Pin Connection and Description (Continued)

1.4.10 Serial Ports 1 and 2

Signal	Pin/s	I/O	Buffer Type	Description
$\overline{CTS1}$, $\overline{CTS2}$	109, 118	I	IN_{TS}	**Clear to Send.** When low, indicate that the modem or other data transfer device is ready to exchange data.
$\overline{DCD1}$, $\overline{DCD1}$	3, 94	I	IN_{TS}	**Data Carrier Detected.** When low, indicate that the modem or other data transfer device has detected the data carrier.
$\overline{DSR1}$, $\overline{DSR2}$	105, 113	I	IN_{TS}	**Data Set Ready.** When low, indicate that the data transfer device, e.g., modem, is ready to establish a communications link.
$\overline{DTR1}$/ BOUT1, $\overline{DTR2}$/ BOUT2	110, 119	O	$O_{6/12}$	**Data Terminal Ready.** When low, indicate to the modem or other data transfer device that the Serial Port is ready to establish a communications link. After system reset, these pins provides the $\overline{DTR}$ function, sets these signals to inactive high, and loopback operation holds them inactive. **Baud Output.** Provides the associated serial channel baud rate generator output signal if test mode is selected, i.e., bit 7 of the EXCR1 Register is set. $\overline{DTR1}$/BOUT1 is used also as BADDR.
$\overline{RI1}$, $\overline{RI2}$	111, 120	I	IN_{TS}	**Ring Indicators (Modem).** When low, indicate that a telephone ring signal has been received by the modem. These pins may issue wake-up event.
$\overline{RTS1}$, $\overline{RTS2}$	107, 115	O	$O_{6/12}$	**Request to Send.** When low, indicate to the modem or other data transfer device that the corresponding Serial Port is ready to exchange data. A system reset sets these signals to inactive high, and loopback operation holds them inactive.
SIN1, SIN2	106, 114	I	IN_{TS}	**Serial Input.** Receive composite serial data from the communications link (peripheral device, modem or other data transfer device).
SOUT1, SOUT2	108, 117	O	$O_{6/12}$	**Serial Output.** Send composite serial data to the communications link (peripheral device, modem or other data transfer device). The SOUT2,1 signals are set active high after system reset.

1.4.11 Strapping

Signal	Pin/s	I/O	Buffer Type	Description
BADDR	110	I	IN_{STRP}	**Base Address Strap.** Determines the base address of the Index and Data registers. It is pulled down by an internal 30 Kohm resistor to get base address 2Eh for the Index register, and 2Fh for the Data register. If the respective base addresses are 15Ch and 15Dh, use an external 10 Kohm pull-up resistor (to V_{DD}).

1.4.12 System Wake-Up Control

Signal	Pin/s	I/O	Buffer Type	Description
PME1, PME2	125, 126	I	IN_{TS}	**Power Management Event 1, 2.** Detection of an event on PME1 or PME2 may activate the $\overline{PWUREQ}$ signal (wake-up event).
$\overline{PWUREQ}$	124	O	$OD_{6/12}$	**Power Up Request.** Low level (active) indicates that wake-up event has occurred. This may cause the chipset to turn the power supply on, or to exit its current sleep state. The open-drain output must be pulled up to $V_{SB,}$ in order to function during power-off.
$\overline{RING}$	125	I	IN_{TS}	**Telephone Line Ring.** Detection of a pulse-train on the $\overline{RING}$ pin, is a wake-up event that can activate the power-up request ($\overline{PWUREQ}$).
$\overline{SUSP}$	126	I	IN_{TS}	**Suspend Power.** Power Supply On control signal.

2.0 Device Architecture and Configuration

The SuperI/O device comprises a collection of generic functional blocks. Each functional block is described in a separate chapter in this book. However, some parameters in the implementation of each functional block may vary per SuperI/O device. This chapter describes the PC87351 structure and provides all device specific information, including special implementation of generic blocks, host interface and device configuration.

2.1 OVERVIEW

The PC87351 consists of 9 logical devices, a host interface, and a central configuration register set, all built around a central, internal bus. The internal bus is a replication of an 8-bit ISA bus protocol.

The host interface serves as a bridge between the external ISA interface and the internal bus. It supports 8-bit I/O read, 8-bit I/O write and 8-bit DMA transactions, as defined in *Personal Computer Bus Standard P996*.

The central configuration register set supports ACPI compliant PnP configuration. The configuration registers are structured as a subset of the Plug and Play Standard Registers, defined in Appendix A of the *Plug and Play ISA Specification* Version 1.0a by Intel and Microsoft. All system resources assigned to the functional blocks (I/O address space, DMA channels and IRQ lines) are configured in, and managed by, the central configuration register set. In addition, some function-specific parameters are configurable through this unit and distributed to the functional blocks through special control signals.

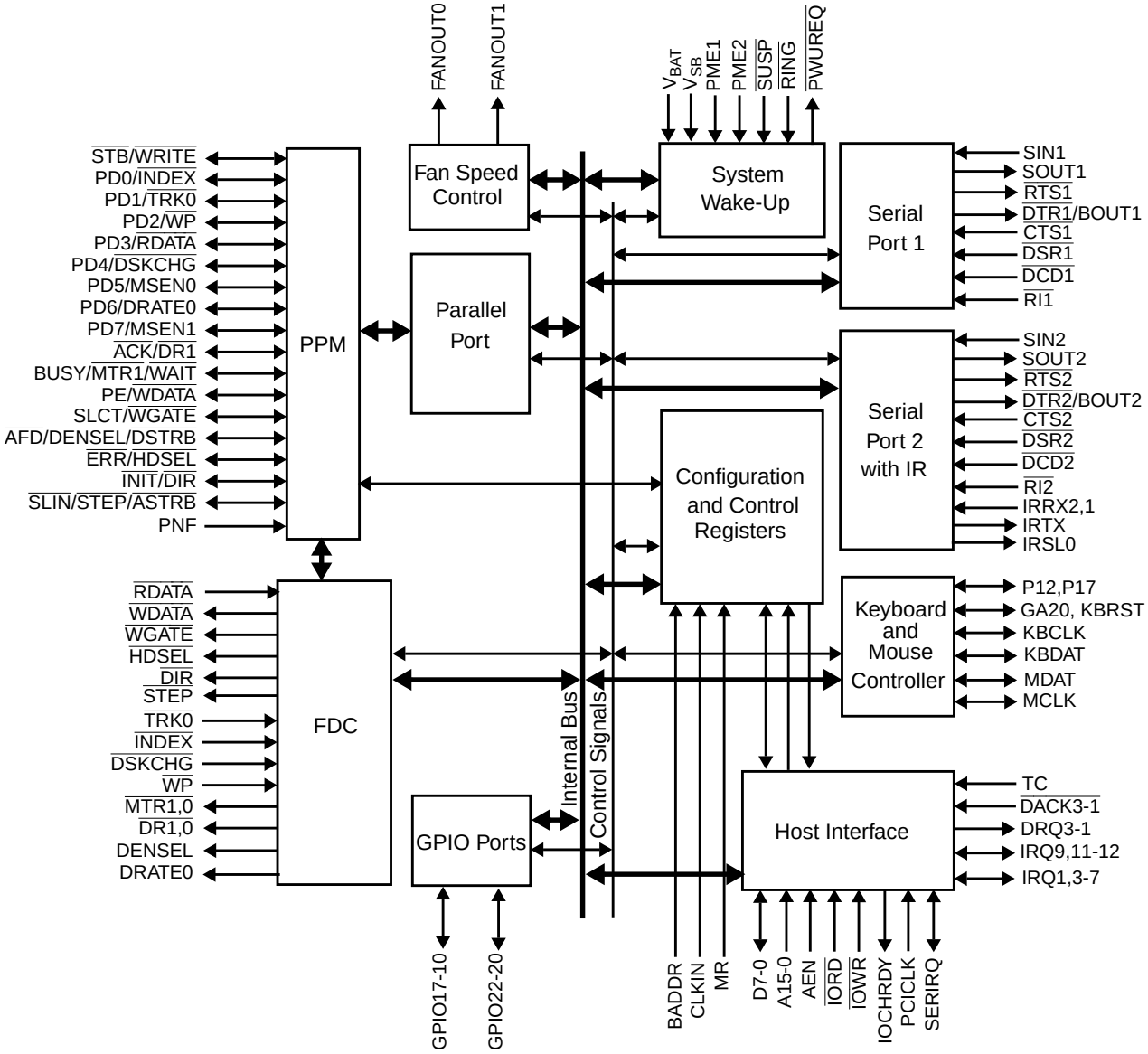


Figure 2-1. Detailed PC87351 Block Diagram

2.0 Device Architecture and Configuration (Continued)

2.2 CONFIGURATION STRUCTURE AND ACCESS

This section describes the structure of the configuration register file, and the method of accessing the configuration registers.

2.2.1 The Index-Data Register Pair

The SuperI/O configuration access is performed via an Index-Data register pair, using only two system I/O byte locations. The base address of this register pair is determined during reset, according to the state of the hardware strapping option on the BADDR pin. Table 2-1 shows the selected base addresses as a function of BADDR.

Table 2-1. BADDR Strapping Options

BADDR	I/O Address	
	Index Register	Data Register
0	002Eh	002Fh
1	015Ch	015Dh

The Index Register is an 8-bit R/W register located at the selected base address (Base+0). It is used as a pointer to the configuration register file, and holds the index of the configuration register that is currently accessible via the Data Register. Reading the Index Register returns the last value written to it (or the default of 00h after reset).

The Data Register is an 8-bit virtual register, used as a data path to any configuration register. Accessing the data register results with physically accessing the configuration register that is currently pointed by the index register.

2.2.2 Banked Logical Device Registers

Each functional block is associated with a Logical Device Number (LDN). The configuration registers are grouped into banks, where each bank holds the standard PnP configuration registers of the corresponding logical device. Table 2-2 shows the LDNs of the device functional blocks.

Figure 2-2 shows the structure of the standard PnP configuration register file. The SIO Control and Configuration registers are not banked and are accessed by the Index-Data register pair only, as described above. However, the device control and device configuration registers are duplicated over 9 banks for 9 logical devices. Therefore, accessing a specific register in a specific bank is performed by two dimensional indexing, where the LDN Register selects the bank (or logical device) and the Index Register selects the register within the bank. Accessing the Data Register while the Index Register holds a value of 30h or higher results in a physical access to the configuration register currently pointed to by the Index Register, within the logical device currently selected by the LDN Register.

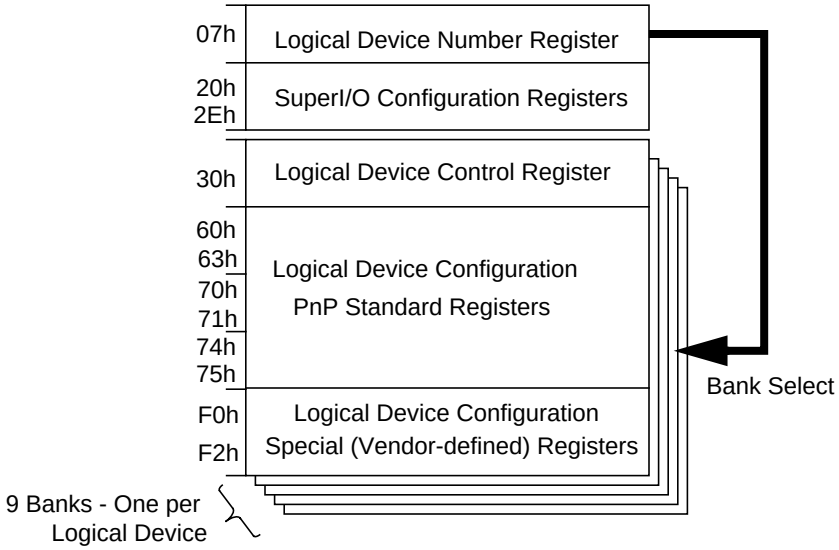


Figure 2-2. Structure of the PnP Standard Registers

2.0 Device Architecture and Configuration (Continued)

Table 2-2. Logical Device Number (LDN) Assignments

LDN	Functional Block
00h	Floppy Disk Controller (FDC)
01h	Parallel Port
02h	Serial Port 2 with IR
03h	Serial Port 1
04h	System Wake-Up Control (SWC)
05h	Keyboard and Mouse Controller (KBC) - Mouse interface
06h	Keyboard and Mouse Controller (KBC) - Keyboard interface
07h	General-Purpose I/O (GPIO)
08h	Fan Speed Control (FSC)

When accessing unimplemented registers (i.e. accessing the Data Register while the Index Register points to a non-existing register or the LDN is higher than 08h), write is ignored and read returns 00h on all addresses except for 74h, 75h (PnP DMA Configuration Registers) which returns 04h (no DMA channel is active). The configuration registers are accessible immediately after reset.

2.2.3 Standard PnP Register Definitions

Tables 2-3 through 2-8 describe the standard PnP registers. For more detailed information on these registers, refer to the *Plug and Play ISA Specification,* Version 1.0a, May 5, 1994.

Unless otherwise noted:

- All registers are read/write.
- All reserved bits return 0 on reads. To prevent unpredictable results, they must not be modified. Using read-modify-write is recommended to prevent the values of reserved bits from being changed during write.
- Write only registers should not use read-modify-write during updates.

Table 2-3. PnP Standard Control Registers

Index	Name	Description
07h	Logical Device Number	This register selects the current logical device.
20h - 2Fh	SuperI/O Configuration Registers	SuperI/O Configuration Registers and ID Registers

Table 2-4. PnP Logical Device Control Registers

Index	Name	Description
30h	Activate	Bit 0 - Logical Device Activation Control 0: Disabled 1: Enabled Bits 7-1 - Reserved

2.0 Device Architecture and Configuration (Continued)

Table 2-5. PnP I/O Space Configuration Registers

Index	Name	Description
60h	I/O Port Base Address Bits (15-8) Descriptor 0	Indicates selected I/O lower limit address bits 15-8 for I/O descriptor 0
61h	I/O Port Base Address Bits (7-0) Descriptor 0	Indicates selected I/O lower limit address bits 7-0 for I/O descriptor 0
62h	I/O Port Base Address Bits (15-8) Descriptor 1	Indicates selected I/O lower limit address bits 15-8 for I/O descriptor 1
63h	I/O Port Base Address Bits (7-0) Descriptor 1	Indicates selected I/O lower limit address bits 7-0 for I/O descriptor 1

Table 2-6. PnP Interrupt Configuration Registers

Index	Name	Description
70h	Interrupt Request Number Select	Indicates selected interrupt number Bits 3-0 select the interrupt number. A value of 1 selects IRQ1, a value of 2 selects IRQ2, etc. (up to IRQ15). IRQ0 is not a valid interrupt selection.
71h	Interrupt Request Type Select	Indicates the type and level of the interrupt request number selected in the previous register Bit 0 - Type of interrupt request selected in previous register 0: Edge 1: Level Bit 1 - Level of interrupt request selected in previous register 0: Low polarity 1: High polarity

Table 2-7. PnP DMA Configuration Registers

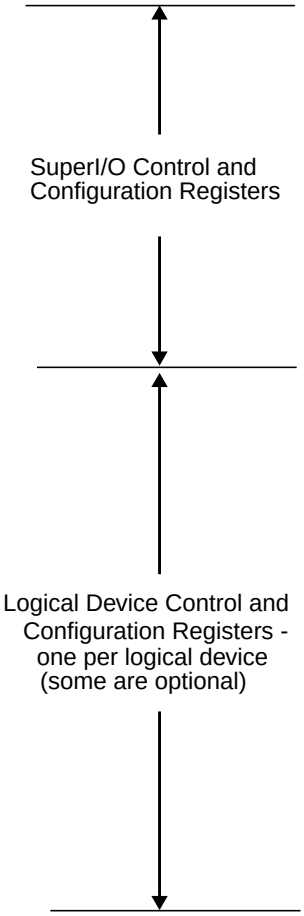
Index	Name	Description
74h	DMA Channel Select 0	Indicates selected DMA channel for DMA 0 Bits 2-0 select the DMA channel for DMA 0. The valid choices are 1-3, where a value of 1 selects DMA channel 1, 2 selects DMA channel 2, etc. A value of 4 indicates that no DMA channel is active. The values 5-7 are reserved.
75h	DMA Channel Select 1	Indicates selected DMA channel for DMA 1 Bits 2-0 select the DMA channel for DMA 1. The valid choices are 1-3, where a value of 1 selects DMA channel 1, 2 selects DMA channel 2, etc. A value of 4 indicates that no DMA channel is active. The values 5-7 are reserved.

Table 2-8. PnP Logical Device Configuration Registers

Index	Name	Description
F0h-FEh	Logical Device Configuration	Vendor-defined

2.0 Device Architecture and Configuration (Continued)

2.2.4 Overview of PnP Standard Registers



Index	Name
07h	Logical Device Number Register
20h	SuperI/O ID Register
21h	SuperI/O Configuration 1 Register
22h	SuperI/O Configuration 2 Register
23h	SuperI/O Configuration 3 Register
24h	SuperI/O Configuration 4 Register
27h	SuperI/O Revision ID Register
2Eh	Reserved exclusively for National use
30h	Logical Device Control Register (Activate)
60h	I/O Base Address Descriptor 0 Bits 15-8
61h	I/O Base Address Descriptor 0 Bits 7-0
62h	I/O Base Address Descriptor 1 Bits 15-8
63h	I/O Base Address Descriptor 1 Bits 7-0
70h	IRQ Number Select
71h	IRQ Type Select
74h	DMA Channel Select 0
75h	DMA Channel Select 1
F0h	Device Specific Logical Device Configuration 1
F1h	Device Specific Logical Device Configuration 2
F2h	Device Specific Logical Device Configuration 3

Figure 2-3. PnP Register Map

SuperI/O Control and Configuration Registers

The only implemented PnP control register in the PC87351 is the Logical Device Number Register at index 07h. All the other standard PnP control registers are associated with PnP protocol for ISA add-in cards, and are not supported by the PC87351.

The SuperI/O Configuration registers at indexes 20h and 27h are mainly used for part identification, global power management and the selection of pin multiplexing options. For details, see Section 2.5.

Logical Device Control and Configuration Registers

A subset of these registers is implemented for each logical device.

Control

The only implemented logical device control register is the activate register at index 30. Bit 0 of the activate register controls the activation of the associated function block. Activation of the block enables access to the block's registers, and attaches its system resources, which are unused as long as the block is not activated. Other effects may apply, on a function-specific basis (such as clock enable and active pinout signaling).

Standard Configuration

The standard configuration registers are used to manage the PnP resource allocation to the functional blocks. The I/O port base address descriptor 0 is a pair of registers at Index 60-61, holding the (first or only) 16-bit base address for the register set of the functional block. An optional second base-address (descriptor 1) at index 62-63 is used for devices with more than one continuous register set. IRQ Number Select (index 70h) and IRQ Type Select (index 71h) allocate an IRQ line to the block and control its type. DMA Channel Select 0 (index 74h) allocates a DMA channel to the block, where applicable. DMA Channel Select 1 (index 75h) allocates a second DMA channel, where applicable.

2.0 Device Architecture and Configuration (Continued)

Special Configuration

The vendor-defined registers, starting at index F0h are used to control function-specific parameters such as operation modes, power saving modes, pin TRI-STATE, clock rate selection, and non-standard extensions to generic functions.

2.2.5 Default Configuration Setup

The device has four reset types, described below. See specific register descriptions for bits affected by each register type.

- **Software Reset**
  This reset is enabled by bit 1 of the SIOCF1 Register, which resets all logical devices. A software reset also resets most bits in the SuperI/O Configuration and Control Registers.
- **Hardware Reset**
  This reset is activated by the assertion of the MR input. It resets all logical devices, with the exception of the SWC. It also resets all SuperI/O Configuration and Control Registers, with the exception of the SIOCF4 Register.
- **V_{PP} Power-Up Reset**
  This reset is activated when either V_{SB} or V_{BAT} is powered on after both have been off. V_{PP} is an internal voltage which is a combination of V_{SB} and V_{BAT}. V_{PP} is taken from V_{SB} if V_{SB} is greater than the minimum (Min) value defined in the *Device Characteristics* chapter; otherwise, V_{BAT} is used as the V_{PP} source. This reset resets all registers whose values are retained by V_{PP}.
- **V_{SB} Power-Up Reset**
  This is an internally generated reset that resets the SWC, excluding those SWC registers whose values are retained by V_{PP}.

The PC87351 wakes up with the default setup, as follows:

- In the event of a hardware reset:
  - The configuration base address is 2Eh or 15Ch, according to the BADDR strap pin value, as shown in Table 2-1.
  - The Keyboard Controller (KBC) is active and all other logical devices are disabled, with the exception of the SWC which remains functional but whose registers cannot be accessed.
  - All the multiplexed GPIO pins, except KBRST/GPIO17/P12/PNF and GA20/GPIO20, are configured as GPIO pins and are in TRI-STATE (default direction is input). KBRST/GPIO17/P12/PNF is configured as KBRST and GA20/GPIO20 is configured as $\overline{GA20}$.
- In the event of either a hardware or a software reset:
  - The legacy devices are assigned with their legacy system resource allocation.
  - The National proprietary functions are not assigned with any default resources and the default values of their base addresses are all 00h.

2.2.6 Address Decoding

A full 16-bit address decoding is applied when accessing the configuration I/O space as well as the registers of the functional blocks. However, the number of configurable bits in the base address registers vary for each device.

The lower 1, 2, 3 or 4 address bits are decoded within the functional block to determine the offset of the accessed register, within the device's I/O range of 2, 4, 8 or 16 bytes, respectively. The rest of the bits are matched with the base address register to decode the entire I/O range allocated to the device. Therefore the lower bits of the base address register are forced to 0 (read-only), and the base address is forced to be 2, 4, 8 or 16 byte aligned, according to the size of the IO range.

The base address of the FDC, Serial Port 1, Serial Port 2 and KBC are limited to the I/O address range of 00h to 7FXh only (bits 11-15 are forced to 0). The Parallel Port base address is limited to the I/O address range of 00h to 3F8h. The addresses of the non-legacy devices are configurable within the full 16-bit address range (up to FFFXh).

In some special cases, other address bits are used for internal decoding (such as bit 2 in the KBC and bit 10 in the PP). The KBC has two I/O descriptors with some implied dependency between them. For more details, please see the detailed description of the base address register for each specific logical device.

2.2.7 The Internal Clocks

The source of the device internal clocks is a 48 MHz clock signal, which is routed through the CLKIN pin. Wake-up on KBD, Mouse and RING pulse train detection operates on internally generated clock.

2.0 Device Architecture and Configuration (Continued)

2.3 REGISTER TYPE ABBREVIATIONS

The register maps in this chapter use the following abbreviations for Type:

- R/W = Read/Write
- R = Read from a specific address returns the value of a specific register. Write to the same address is to a different register.
- W = Write
- RO = Read Only
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.

2.4 SUPERI/O CONFIGURATION AND CONTROL REGISTERS

This section describes the registers with first level indexes in the range 07h - 2Fh.

2.4.1 SuperI/O Register Map

Index	Mnemonic	Name	Type	Section
07h	LDN	Logical Device Number Register	R/W	2.2.2
20h	SID	SuperI/O ID Register	RO	2.4.2
21h	SIOCF1	SuperI/O Configuration 1 Register	R/W	2.4.3
22h	SIOCF2	SuperI/O Configuration 2 Register	R/W	
23h	SIOCF3	SuperI/O Configuration 3 Register	R/W	2.4.5
24h	SIOCF4	SuperI/O Configuration 4 Register	R/W	2.4.6
27h	SRID	SuperI/O Revision ID Register	RO	2.4.7
2Eh	Reserved exclusively for National use			

2.4.2 SuperI/O ID Register (SID)

This register contains the identity number of the chip. The PC87351 is identified by the value E2h.

Location: Index 20h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**Chip ID**							
Reset	1	1	1	0	0	0	1	0

2.0 Device Architecture and Configuration (Continued)

2.4.3 SuperI/O Configuration 1 Register (SIOCF1)

Location: Index 21h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**General Purpose Scratch**		**Lock Scratch**	**PNF Status**	**Reserved**	**Pin Function Lock**	**SW Reset**	**Global Device Enable**
Reset	0	0	0	1	0	0	0	1

Bit	Description
7-6	**General Purpose Scratch**. When bit 5 is set to 1, these bits are read only. After reset, these bits can be read or write. Once changed to read only, the bits can be changed back to read/write only by a hardware reset.
5	**Lock Scratch.** This bit controls bits 7 and 6 of this register. Once this bit is set to 1 by software, it can be cleared to 0 only by a hardware reset. 0: Bits 7 and 6 of this register are read/write bits (default). 1: Bits 7 and 6 of this register are read only bits.
4	**PNF Status**. This read only bit reflects the value of the PNF pin when PPM mode is enabled. If PPM mode is disabled, this bit is 1. Data written to this bit is ignored.
3	**Reserved**
2	**Pin Function Lock.** When this bit is set to 1, all function selection on the associated pins is locked: • All bits of the SIOCF2 Register • Bits 4-0 of the SIOCF3 Register • Bits 3-0 of the SIOCF4 Register. When this bit is set to 1 by software, it can only be cleared to 0 by MR or power-off. 0: No effect (default) 1: Pin function locked
1	**SW Reset**. Read always returns 0. 0: Ignored (default) 1: Resets all the devices that are reset by MR (with the exception of the lock bits) and the registers of the SWC
0	**Global Device Enable.** This bit controls the function enable of all the logical devices in the PC87351, except the SWC. It allows them to be disabled simultaneously by writing to a single bit. 0: All logical devices in the PC87351 disabled, except SWC 1: Each logical device enabled according to its Activate Register at index 30h (default)

2.0 Device Architecture and Configuration (Continued)

2.4.4 SuperI/O Configuration 2 Register (SIOCF2)

This register controls pin multiplexing of pins: 34, 35, 37-43, 98 and 99.

Location: Index 22h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Pin 99 Function Select**	**Pin 98 Function Select**		**Pin 42 Function Select**		**Pin 41 Function Select**		**Select Serial IRQ**
Reset	1	0	1	0	0	0	0	1

Bit	Description
7	**Pin 99 Function Select** 0: GPIO20 1: GA20 (default).
6-5	**Pin 98 Function Select** **Bits 6 5 — Function** 0 0 — GPIO17 0 1 — KBRST (default) 1 0 — P12 1 1 — PNF (PPM mode enabled)
4-3	**Pin 42 Function Select.** The setting of bit 0 of this register effects the function selected, as follows: **Bits 4 3 0 — Function** 0 0 X — GPIO15 (default) 0 1 1 — GPIO15 0 1 0 — IRQ11 1 0 X — P12 1 1 X — P17
2-1	**Pin 41 Function Select.** The setting of bit 0 of this register effects the function selected, as follows: **Bits 2 1 0 — Function** 0 0 X — GPIO14 (default) 0 1 1 — GPIO14 0 1 0 — IRQ9 1 0 X — IRRX2/IRSL0 1 1 X — P17
0	**Select Serial IRQ** 0: Pins 34, 35, 37-40 and 43 function as IRQ1, IRQ3-7 and IRQ12, respectively 1: Pins 34 and 35 function as PCICLK and SERIRQ, respectively. Pins 37-40 and 43 function as GPIO (default).

2.0 Device Architecture and Configuration (Continued)

2.4.5 SuperI/O Configuration 3 Register (SIOCF3)

This register controls multiplexing of pins: 112-115, 117-119 and 127-128.

Location: Index 23h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**			**Pin 128 Function Select**		**Pin 127 Function Select**		**Select Serial Port 2**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-5	**Reserved**
4-3	**Pin 128 Function Select** **Bits 4 3 — Function** 0 0 — GPIO22 (default) 0 1 — FANOUT1 1 0 — IRRX2/IRSL0 1 1 — P17
2-1	**Pin 127 Function Select** **Bits 2 1 — Function** 0 0 — GPIO21 (default) 0 1 — FANOUT0 1 0 — P12 1 1 — PNF (PPM mode enabled)
0	**Select Serial Port 2** 0: Pins 112-115 and 117-119 function as GPIO10-16 (default) 1: Pins 112-115 and 117-119 function as Serial Port 2

2.0 Device Architecture and Configuration (Continued)

2.4.6 SuperI/O Configuration 4 Register (SIOCF4)

This register controls the multiplexing of two pins. Its value is retained by V_{PP}, and is not affected by either hardware or software reset.

Location: Index 24h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**SUSP Value**	**General Purpose Scratch**			**PME2 Debounce Enable**	**Pin 126 Function Select**	**PME1 Debounce Enable**	**Pin 125 Function Select**
Reset	X	0	0	0	1	0	1	0

Bit	Description
7	**SUSP Value.** Last value of SUSP pin prior to V_{SB} loss (power-fail).
6-4	**General Purpose Scratch.** Battery-backed.
3	**PME2 Debounce Enable** 0: Debounce disabled 1: 16mS debounce enabled (V_{PP} power-up default)
2	**Pin 126 Function Select** 0: Pin 126 functions as $\overline{SUSP}$ (V_{PP} power-up default) 1: Pin 126 functions as PME2
1	**PME1 Debounce Enable** 0: Debounce disabled 1: 16mS debounce enabled (V_{PP} power-up default)
0	**Pin 125 Function Select** 0: $\overline{RING}$ (V_{PP} power-up default) 1: PME1

2.4.7 SuperI/O Revision ID Register (SRID)

This read only register contains the identity number of the chip revision. SRID is incremented on each revision.

Location: Index 27h

Type: RO

2.0 Device Architecture and Configuration (Continued)

2.5 PARALLEL PORT MULTIPLEXER (PPM)

The Parallel Port Multiplexer (PPM) logic allows connection of an external Floppy Disk Drive (FDD) through the Parallel Port connector (25-pin DIN), instead of, or in addition to, the internal FDD on the normal FDC header. This is done by turning the Parallel Port pins (normally used by the Parallel Port) into an additional set of FDC pins, while isolating them from the Parallel Port functionality.

A printer (or any other parallel device) may be exchanged with an external FDD, without turning the system off. The PPM logic automatically detects whether a parallel device or the FDD is connected, and routes the Parallel Port pins to either the Parallel Port or the FDC functional blocks, accordingly. See Figure 2-4.

PPM mode is enabled by selecting the PNF pin. When PPM mode is enabled, it is controlled by the PNF input pin, as follows:

- When PNF = 1, PPM is inactive and the Parallel Port pins are assigned Parallel Port functionality.
- When PNF = 0, PPM is active and the Parallel Port pins are assigned FDC functionality.

When PPM mode is disabled, the Parallel Port pins are assigned Parallel Port functionality, regardless of the value of PNF.

The internal FDD (on the normal FDC pins) and the external FDD (on the Parallel Port pins) can be assigned as Drive A and Drive B respectively, or vice versa.

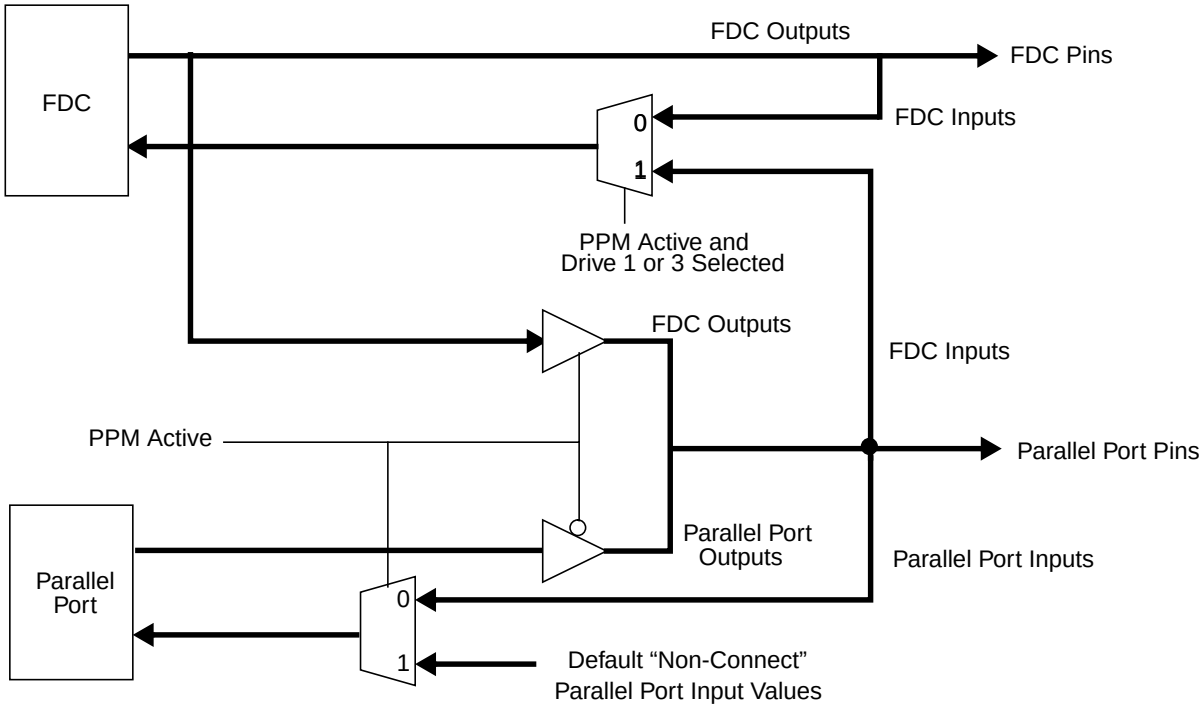


Figure 2-4. PPM Routing

2.5.1 PPM Mode

The Parallel Port pins function as FDD interface for either drive 1 or drive 3. See Figure 2-4 for the internal routing between the PPM and FDC, and the Parallel Port and FDC pin-sets when PPM mode is active. The FDC output signals are driven simultaneously both on the normal FDC pins and on the corresponding Parallel Port pins. The FDC inputs are received from the FDC pins when either drive 0 or drive 2 are selected, and from the corresponding Parallel Port pins when either drive 1 or drive 3 is selected.

The Parallel Port output signals are isolated from the Parallel Port pins. The Parallel Port input signals, as reflected by STR Register, assume their default values ($\overline{BUSY}$ = 1, PE = 0, SLCT = 0, $\overline{ACK}$ = 1), indicating that nothing is connected to the Parallel Port.

2.0 Device Architecture and Configuration (Continued)

2.5.2 TRI-STATE Control of Parallel Port Pins

Normally, the pins of most of the SuperI/O functions can be put in TRI-STATE when the function is disabled. If the TRI-STATE control bit of a logical device (normally bit 0 of the Configuration Register at index F0) is set to 1, and its Activate bit (bit 0 of Activate Register at index 30) is cleared to 0, the output pins of that device are floating. The same is true for the Parallel Port pins, but TRI-STATE control depends on the current functionality of the pins.

When the PPM is disabled or when a parallel device is connected to the port, then the TRI-STATE of the Parallel Port pins is controlled by the Parallel Port Activate bit and TRI-STATE control bit. However, when the PPM is enabled and the external FDD is connected (PNF=0), TRI-STATE is controlled by the corresponding FDC configuration bits.

Table 2-9 shows the standard 25-pin, D-type connector definition for Parallel Port operations in PPM mode.

Table 2-9. Parallel Port Connector Signal Multiplexing

D-Type Connector Pin	PC87351 Pin	Parallel Port		FDC	
		Signal	I/O	Signal	I/O
1	95	$\overline{\text{STB}}$/$\overline{\text{WRITE}}$	I/O	-	I
2	93	PD0	I/O	$\overline{\text{INDEX}}$	I
3	91	PD1	I/O	$\overline{\text{TRK0}}$	I
4	89	PD2	I/O	$\overline{\text{WP}}$	I
5	87	PD3	I/O	$\overline{\text{RDATA}}$	I
6	84	PD4	I/O	$\overline{\text{DSKCHG}}$	I
7	83	PD5	I/O	MSEN0	I
8	82	PD6	I/O	DRATE0	O
9	81	PD7	I/O	MSEN1	I
10	80	$\overline{\text{ACK}}$	I	$\overline{\text{DR1}}$	O
11	79	BUSY/$\overline{\text{WAIT}}$	I	$\overline{\text{MTR1}}$	O
12	78	PE	I	$\overline{\text{WDATA}}$	O
13	77	SLCT	I	$\overline{\text{WGATE}}$	O
14	94	$\overline{\text{AFD}}$/$\overline{\text{DSTRB}}$	I/O	DENSEL	O
15	92	$\overline{\text{ERR}}$	I	$\overline{\text{HDSEL}}$	O
16	90	$\overline{\text{INIT}}$	I/O	$\overline{\text{DIR}}$	O
17	88	$\overline{\text{SLIN}}$/$\overline{\text{ASTRB}}$	I/O	$\overline{\text{STEP}}$	O
18 - 23		GND		GND	
24	98 or 127[1]	$\overline{\text{PNF}}$ = Ground	I	$\overline{\text{PNF}}$ = 1	I
25		GND		GND	

1. The PNF signal is the inverse of pin 24 of the connector ($\overline{\text{PNF}}$).

2.0 Device Architecture and Configuration (Continued)

2.6 FLOPPY DISK CONTROLLER (FDC) - LOGICAL DEVICE 0

2.6.1 General Description

The generic FDC is a standard FDC with a digital data separator, and is DP8473 and N82077 software compatible. The FDC supports 14 of the 17 standard FDC signals on the normal FDD interface pins, as described in Section 2.4.1. Additionally, the FDC supports another 16 pins, multiplexed on the Parallel Port pins, for external FDD support. See Section 2.5.2 for details on these pins in PPM mode and Section 1.4.3 for signal/pin descriptions.

Table 2-10. FDC Registers

Offset	Mnemonic	Name	Type
00h	SRA	Status Register A	RO
01h	SRB	Status Register B	RO
02h	DOR	Digital Output Register	R/W
03h	TDR	Tape Drive Register	R/W
04h	MSR	Main Status Register	R
	DSR	Data Rate Select Register	W
05h	FIFO	Data (FIFO) Register	R/W
06h		N/A	X
07h	DIR	Digital Input Register	R
	CCR	Configuration Control Register	W

The FDC is implemented as follows:

- Automatic media sense is not supported on the standard FDC connector (MSEN0-1 pins are not implemented), but is supported instead on the Parallel Port pins.

2.6.2 Configuration

Index	Configuration Register or Action	Type	Reset
30h	Activate. See also bit 0 of the SIOCF1 Register.	R/W	00h
60h	Base Address MSB Register. Bits 7-3 (for A15-11) are read only, 00000b.	R/W	03h
61h	Base Address LSB Register. Bits 2 and 0 (for A2 and A0) are read only, 00b.	R/W	F2h
70h	Interrupt Number	R/W	06h
71h	Interrupt Type. Bit 1 is read/write; other bits are read only.	R/W	03h
74h	DMA Channel Select	R/W	02h
75h	Report no second DMA assignment	R	04h
F0h	FDC Configuration Register	R/W	24h
F1h	Drive ID Register	R/W	00h

2.0 Device Architecture and Configuration (Continued)

2.6.3 FDC Configuration Register

This register is reset by hardware to 20h.

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Four Drive Control**	**TDR Register Mode**	**DENSEL Polarity Control**	**Reserved**	**Write Protect**	**PC-AT or PS/2 Drive Mode Select**	**Reserved**	**TRI-STATE Control**
Reset	0	0	1	0	0	1	0	0
Required				0				

Bit	Description
7	**Four Drive Control** 0: Two floppy drives directly controlled by $\overline{\text{DR1-0}}$ and $\overline{\text{MTR1-0}}$ (default) 1: Four floppy drives controlled with the aid of external logic
6	**TDR Register Mode** 0: PC-AT compatible drive mode; i.e., bits 7-2 of the TDR are ignored (default) 1: Enhanced drive mode
5	**DENSEL Polarity Control** 0: Active low for 500 Kbps or 1 Mbps data rates 1: Active high for 500 Kbps or 1 Mbps data rates (default)
4	**Reserved.** Must be 0.
3	**Write Protect.** This bit allows forcing of write protect by software. When set, write to the floppy disk drive is disabled. This effect is identical to $\overline{\text{WP}}$ when it is active. 0: Write protected according to $\overline{\text{WP}}$ signal (default) 1: Write protected regardless of value of $\overline{\text{WP}}$ signal
2	**PC-AT or PS/2 Drive Mode Select** 0: PS/2 drive mode 1: PC-AT drive mode (default)
1	**Reserved**
0	**TRI-STATE Control.** When disabled, this bit controls the TRI-STATE status of the logical device output pins. 0: Disabled (default) 1: Enabled when device inactive

2.6.4 Drive ID Register

This read/write register is reset by hardware to 00h. These bits control bits 5 and 4 of the enhanced TDR Register.

Location: Index F1h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**				**Drive 1 ID**		**Drive 0 ID**	
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-4	**Reserved**
3-2	**Drive 1 ID.** These bits are reflected on bits 5 and 4 of the TDR Register, respectively, when drive 1 is accessed.
1-0	**Drive 0 ID.** These bits are reflected on bits 5 and 4 of the TDR Register, respectively, when drive 0 is accessed.

Usage Hints: Some BIOS implementations support automatic media sense FDD, and bit 5 of the TDR is interpreted as valid media sense when it is cleared to 0. If drive 0 and/or drive 1 do not support automatic media sense, bits 1 and/or 3 of the Drive ID Register should be set to 1 respectively, to indicate non-valid media sense, when the corresponding drive is selected and the Drive ID bit is reflected on bit 5 of TDR.

2.0 Device Architecture and Configuration (Continued)

2.7 PARALLEL PORT - LOGICAL DEVICE 1

2.7.1 General Description

The PC87351 Parallel Port device offers a wide range of operational configurations. It utilizes the most advanced protocols in current use, while maintaining full backward compatibility to support existing hardware and software. It supports two Standard Parallel Port (SPP) modes of operation for parallel printer ports, two Enhanced Parallel Port (EPP) modes of operation, and one Extended Capabilities Port (ECP) mode. This versatility is achieved by user software control of the mode in which the device functions. The following table lists the Parallel Port Registers used in each mode of operation.

Note: The Parallel Port does not support zero wait states.

Table 2-11. Parallel Port Registers Classified by Mode

Offset	SPP	EPP	ECP
00h	DTR	DTR	DATAR (modes 0,1) AFIFO (mode 3)
01h	STR	STR	DSR
02h	CTR	CTR	DCR
03h	X	ADDR	X
04h	X	DATA0	X
05h	X	DATA1	X
06h	X	DATA2	X
07h	X	DATA3	X
400h	X	X	CFIFO (mode 2) DFIFO (mode 3) TFIFO (mode 6) CNFGA (mode 7)
401h	X	X	CNFGB
402h	X	X	ECR
403h	X	X	EIR[1]
404h	X	X	EDR[1]
405h	X	X	EAR[1]

1. These registers are extended, and not standard 1284 registers. They are accessible only when enabled by bit 4 of the Parallel Port Configuration Register (see Section 2.7.3).

2.7.2 Configuration

Index	Configuration Register or Action	Type	Reset
30h	Activate. See also bit 0 of the SIOCF1 Register.	R/W	00h
60h	Base Address MSB Register. Bits 7-3 (for A15-11) are read only, 00000b.	R/W	02h
61h	Base Address LSB Register. Bits 1 and 0 (for A1 and A0) are read only, 00b.	R/W	78h
70h	Interrupt Number	R/W	07h
71h	Interrupt Type Bits 7-2 are read only. Bit 1 is a read/write bit. Bit 0 is read only. It reflects the interrupt type dictated by the Parallel Port operation mode and configured by the Parallel Port Configuration Register. This bit is set to 1 (level interrupt) in Extended Mode and cleared (edge interrupt) in all other modes.	R/W	02h
74h	DMA Channel Select	R/W	04h
75h	Report no second DMA assignment	RO	04h
F0h	Parallel Port Configuration Register	R/W	F2h

2.0 Device Architecture and Configuration (Continued)

2.7.3 Parallel Port Configuration Register

This register is reset by hardware to F2h.

Note: For normal operation and to maintain compatibility with future chips, do not change bits 7 through 4.

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Parallel Port Mode Select**			**Extended Register Access**	**Reserved**		**Power Mode Control**	**TRI-STATE Control**
Reset	1	1	1	1	0	0	1	0

Bit	Description
7-5	**Parallel Port Mode Select**. Selection of EPP 1.7 or 1.9 in ECP mode 4 is controlled by bit 4 of the Control2 Configuration Register of the parallel port at offset 02h. **Bits 7 6 5** — **Mode** 0 0 0 — SPP Compatible; PD7-0 always output signals 0 0 1 — SPP Extended; PD7-0 direction controlled by software 0 1 0 — EPP 1.7 0 1 1 — EPP 1.9 1 0 0 — IEEE1284 (selects IEEE1284 register set), without embedded EPP support 1 0 1 — Reserved 1 1 0 — Reserved 1 1 1 — IEEE1284 (selects IEEE1284 register set), with EPP mode selectable as mode 4 (default)
4	**Extended Register Access** 0: Registers at base (address) + 403h, base + 404h and base + 405h are not accessible (reads and writes are ignored). 1: When ECP is selected by bits 7 through 5, the registers at base (address) + 403h, base + 404h and base + 405h are accessible. This option supports run-time configuration within the Parallel Port address space.
3-2	**Reserved**
1	**Power Mode Control.** When the logical device is active: 0: Parallel port clock disabled ECP modes and EPP time-out are not functional when the logical device is active. Registers are maintained. 1: Parallel port clock enabled All operation modes are functional when the logical device is active (default).
0	**TRI-STATE Control.** This bit controls the TRI-STATE status of the logical device output pins when it is inactive (disabled). 0: Disabled (default) 1: Enabled when device inactive

Usage Hints: Parallel Port modes determine which address bits are used for register addresses. In SPP mode, 14 bits are used to decode Parallel Port base addresses. In ECP and EPP modes, 13 address bits are used. Table 2-11 shows which registers and address bits are used in each mode.

The settings of the CTR Register bits listed below control selection of Parallel Port modes, as follows:

- When changing to ECP mode from any other mode, bit 2 must be set to 1, and bits 3 and 4 must be set to 0.
- When changing from SPP to EPP mode, bit 3 must be set to 0.

2.0 Device Architecture and Configuration (Continued)

2.8 SERIAL PORT 2 - LOGICAL DEVICE 2

2.8.1 General Description

Serial Port 2 includes IR functionality as described in the Serial Port 2 with IR chapter.

2.8.2 Configuration

Index	Configuration Register or Action	Type	Reset
30h	Activate. See also bit 0 of the SIOCF1 Register.	R/W	00h
60h	Base Address MSB Register. Bits 7-3 (for A15-11) are read only, 00000b.	R/W	02h
61h	Base Address LSB Register. Bit 2-0 (for A2-0) are read only, 000b.	R/W	F8h
70h	Interrupt Number	R/W	03h
71h	Interrupt Type. Bit 1 is R/W; other bits are read only.	R/W	03h
74h	DMA Channel Select 0 (RX_DMA)	R/W	04h
75h	DMA Channel Select 1 (TX_DMA)	R/W	04h
F0h	Serial Port 2 Configuration Register	R/W	02h

2.8.3 Serial Port 2 Configuration Register

This register is reset by hardware to 02h.

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Bank Select Enable**	**Reserved**				**Busy Indicator**	**Power Mode Control**	**TRI-STATE Control**
Reset	0	0	0	0	0	0	1	0

Bit	Description
7	**Bank Select Enable**. Enables bank switching for Serial Port 2. 0: All attempts to access the extended registers in Serial Port 2 are ignored (default). 1: Enables bank switching for Serial Port 2.
6-3	**Reserved**
2	**Busy Indicator.** This read only bit can be used by power management software to decide when to power-down the Serial Port 2 logical device. 0: No transfer in progress (default). 1: Transfer in progress.
1	**Power Mode Control.** When the logical device is active in: 0: Low power mode Serial Port 2 Clock disabled. The output signals are set to their default states. The $\overline{RI}$ input signal can be programmed to generate an interrupt. Registers are maintained. (Unlike Active bit in Index 30 that also prevents access to Serial Port 2 registers.) 1: Normal power mode Serial Port 2 clock enabled. Serial Port 2 is functional when the logical device is active (default).
0	**TRI-STATE Control**. This bit controls the TRI-STATE status of the device output pins when it is inactive (disabled). One exception is the IRTX pin. It is driven to 0 when Serial Port 2 is inactive, and is not affected by this bit. 0: Disabled (default) 1: Enabled when device inactive

2.0 Device Architecture and Configuration (Continued)

2.9 SERIAL PORT 1 - LOGICAL DEVICE 3

2.9.1 Configuration

Index	Configuration Register or Action	Type	Reset
30h	Activate. See also bit 0 of the SIOCF1 Register.	R/W	00h
60h	Base Address MSB Register. Bits 7-3 (for A15-11) are read only, 00000b.	R/W	03h
61h	Base Address LSB Register. Bit 2-0 (for A2-0) are read only, 000b.	R/W	F8h
70h	Interrupt Number	R/W	04h
71h	Interrupt Type. Bit 1 is R/W; other bits are read only.	R/W	03h
74h	Report no DMA Assignment	R/W	04h
75h	Report no DMA Assignment	R/W	04h
F0h	Serial Port 1 Configuration Register	R/W	02h

2.9.2 Serial Port 1 Configuration Register

This register is reset by hardware to 02h.

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Bank Select Enable**	**Reserved**				**Busy Indicator**	**Power Mode Control**	**TRI-STATE Control**
Reset	0	0	0	0	0	0	1	0

Bit	Description
7	**Bank Select Enable**. Enables bank switching for Serial Port 1. 0: Disabled (default). 1: Enabled
6-3	**Reserved**
2	**Busy Indicator.** This read only bit can be used by power management software to decide when to power-down the Serial Port 1 logical device. 0: No transfer in progress (default). 1: Transfer in progress.
1	**Power Mode Control.** When the logical device is active in: 0: Low power mode Serial Port 1 Clock disabled. The output signals are set to their default states. The $\overline{RI}$ input signal can be programmed to generate an interrupt. Registers are maintained. (Unlike Active bit in Index 30 that also prevents access to Serial Port 1 registers.) 1: Normal power mode Serial Port 1 clock enabled. Serial Port 1 is functional when the logical device is active (default).
0	**TRI-STATE Control**. This bit controls the TRI-STATE status of the device output pins when it is inactive (disabled). One exception is the IRTX pin. It is driven to 0 when Serial Port 1 is inactive, and is not affected by this bit. 0: Disabled (default) 1: Enabled when device inactive

2.0 Device Architecture and Configuration (Continued)

2.10 SYSTEM WAKE-UP CONTROL (SWC) - LOGICAL DEVICE 4

2.10.1 Configuration

Index	Configuration Register or Action	Type	Reset
30h	Activate. When bit 0 is cleared, the registers of this logical device are not accessible.[1]	R/W	00h
60h	Base Address MSB Register	R/W	00h
61h	Base Address LSB Register. Bits 3-0 (for A3-0) are read only, 0000b.	R/W	00h
70h	Interrupt Number (For routing the $\overline{\text{PWUREQ}}$ signal).	R/W	00h
71h	Interrupt Type. Bit 1 is read/write. Other bits are read only.	R/W	03h
74h	Report no DMA assignment	RO	04h
75h	Report no DMA assignment	RO	04h

1. The logical device registers are maintained, and all wake-up detection mechanisms are functional.

2.0 Device Architecture and Configuration (Continued)

2.11 KEYBOARD AND MOUSE CONTROLLER (KBC) - LOGICAL DEVICES 5 AND 6

2.11.1 General Description

The KBC is implemented physically as a single hardware module and houses two separate logical devices: a Mouse controller (logical device 5) and a Keyboard controller (logical device 6).

The hardware KBC module is integrated to provide the following pin functions: P12, P17, KBRST (P20), GA20 (P21), KBDAT, KBCLK, MDAT, and MCLK. P12 and P17 are implemented as quasi bi-directional pins, meaning that they are driven high by the output buffer for a short period, following a low to high transition of the pins, and then left in TRI-STATE. KBRST and GA20 are implemented as bi-directional, open-drain pins. The Keyboard and Mouse interfaces are implemented as bi-directional, open-drain pins. Their internal connections are shown in Figure 2-5.

P10, P11, P13-P16, P22-P27 of the KBC core are not available on dedicated pins; neither are T0 and T1. P10, P11, P22, P23, P26, P27, T0 and T1 are used to implement the Keyboard and Mouse interface.

Internal pull-ups are implemented only on P12 and P17.

The KBC executes a program fetched from an on-chip 2Kbyte ROM. The code programmed in this ROM is user-customizable. The KBC has two interrupt request signals: one for the Keyboard and one for the Mouse. The interrupt requests are implemented using ports P24 and P25 of the KBC core. The interrupt requests are controlled exclusively by the KBC firmware, except for the type and number, which are affected by configuration registers (see Section 2.11.2).

The interrupt requests are implemented as bi-directional signals. When an I/O port is read, all unused bits return the value latched in the output registers of the ports.

For KBC firmware that implements interrupt-on-OBF schemes, it is recommended to implement it as follows:

1. Put the data in DBBOUT.
2. Set the appropriate port bit to issue an interrupt request.

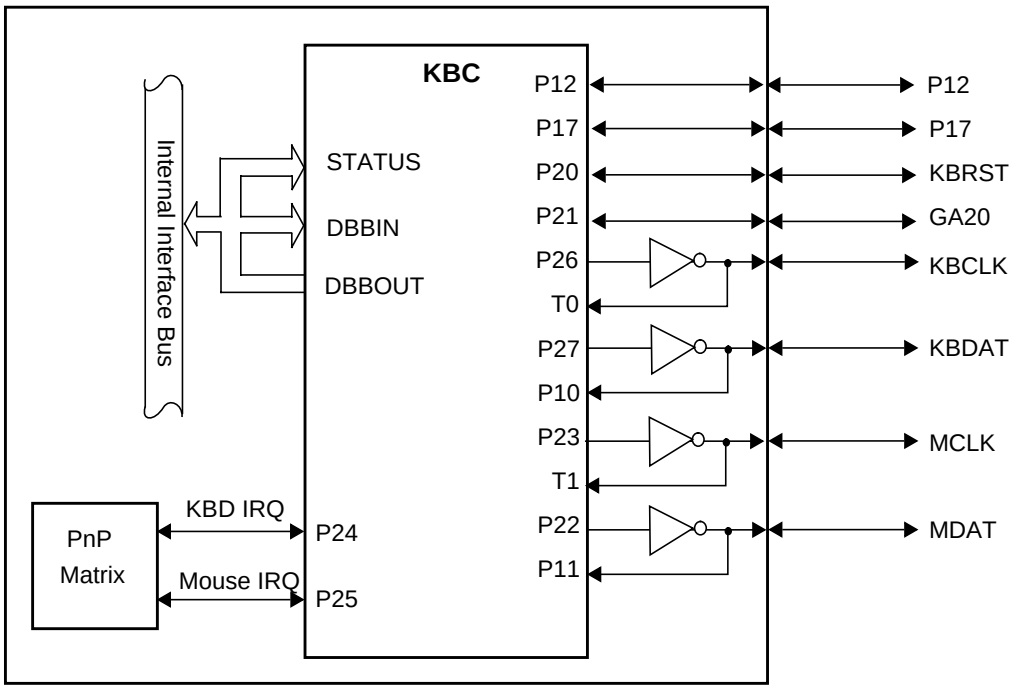


Figure 2-5. Keyboard and Mouse Interfaces

2.0 Device Architecture and Configuration (Continued)

2.11.2 Configuration

Index	Mouse Configuration Register or Action	Type	Reset
30h	Activate. See also bit 0 of the SIOCF1. When the Mouse of the KBC is inactive, the IRQ selected by the Mouse Interrupt Number Register (index 70h) is not asserted. This register has no effect on host KBC commands handling the PS/2 Mouse.	R/W	00h
70h	Mouse Interrupt Number	R/W	0Ch
71h	Mouse Interrupt Type. Bits 1,0 are read/write; other bits are read only.	R/W	02h
74h	Report no DMA assignment	RO	04h
75h	Report no DMA assignment	RO	04h

Index	Keyboard Configuration Register or Action	Type	Reset
30h	Activate. See also bit 0 of the SIOCF1.	R/W	01h
60h	Base Address MSB Register. Bits 7-3 (for A15-11) are read only, 00000b.	R/W	00h
61h	Base Address LSB Register. Bits 2-0 are read only 000b.	R/W	60h
62h	Command Base Address MSB Register. Bits 7-3 (for A15-11) are read only, 00000b.	R/W	00h
63h	Command Base Address LSB. Bits 2-0 are read only 100b.	R/W	64h
70h	KBC Interrupt Number	R/W	01h
71h	KBC Interrupt Type. Bits 1,0 are read/write; others are read only.	R/W	02h
74h	Report no DMA assignment	RO	04h
75h	Report no DMA assignment	RO	04h
F0h	KBC Configuration Register	R/W	40h

2.11.3 KBC Configuration Register

This register is reset by hardware to 40h.

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**KBC Clock Source**		**Reserved**					**TRI-STATE Control**
Reset	0	1	0	0	0	0	0	0
Required						0		

Bit	Description
7-6	**KBC Clock Source.** The clock source can be changed only when the KBC is inactive (disabled). **Bits 7 6 — Function** 0 0 — 8 MHz 0 1 — 12 MHz (default) 1 0 — 16 MHz 1 1 — Reserved
5-1	**Reserved**. Use read-modify-write to change the value of the register. Do not change the value of these bits. Bit 2 must be 0.
0	**TRI-STATE Control**. If KBC is inactive (disabled) when this bit is set, the KBC pins (KBCLK and KBDAT) are in TRI-STATE. If Mouse is inactive (disabled) when this bit is set, the Mouse pins (MCLK and MDAT) are in TRI-STATE. 0: Disabled (default) 1: Enabled when device inactive

Usage Hints: When required to change the clock frequency of the KBC, perform the following:

1. Disable the KBC logical device.
2. Change the frequency setting.
3. Enable the KBC logical device.

2.0 Device Architecture and Configuration (Continued)

2.12 GENERAL-PURPOSE INPUT/OUTPUT (GPIO) PORTS - LOGICAL DEVICE 7

2.12.1 General Description

The GPIO functional block includes 11 pins, arranged in one 8-bit port and one 3-bit port. Both of these ports are standard. The eight runtime registers of these ports are arranged in the GPIO address space shown in Table 2-12. The GPIO base address is 8-byte aligned. Address bits 2-0 are used to indicate the register offset.

Table 2-12. Runtime Registers in GPIO Address Space

Offset	Mnemonic	Name	Reset	Port	Type
00h	GPDO1	GPIO Data Out 1 Register	FFh	1	R/W
01h	GPDI1	GPIO Data In 1 Register	XXh		RO
02h	GPIEN1	GPIO Interrupt Enable 1 Register	00h		R/W
03h	GPST1	GPIO Status 1 Register	00h		R/W1C
04h	GPDO2	GPIO Data Out 2 Register	07h	2	R/W
05h	GPDI2	GPIO Data In 2 Register	0Xh		RO
06h	GPIEN2	GPIO Interrupt Enable 2 Register	00h		R/W
07h	GPST2	GPIO Status 2 Register	00h		R/W1C

2.12.2 Implementation

The standard GPIO port has four runtime registers. Each pin is associated with a configuration register that includes seven configuration bits.

2.12.3 Configuration

Index	Configuration Register or Action	Type	Reset
30h	Activate. See also bit 0 of the SIOCF1 Register.	R/W	00h
60h	Base Address MSB Register	R/W	00h
61h	Base Address LSB Register. Bits 2-0 (for A2-0) are read only, 000b.	R/W	00h
70h	Interrupt Number (For routing the IRQ from the GPIO).	R/W	00h
71h	Interrupt Type. Bit 1 is read/write. Other bits are read only.	R/W	03h
74h	Report no DMA assignment	R	04h
75h	Report no DMA assignment	R	04h
F0h	GPIO Pin Configuration Select Register	R/W	00h
F1h	GPIO Pin Configuration Access Register	R/W	00h

Figure 2-6 describes the organization of these registers.

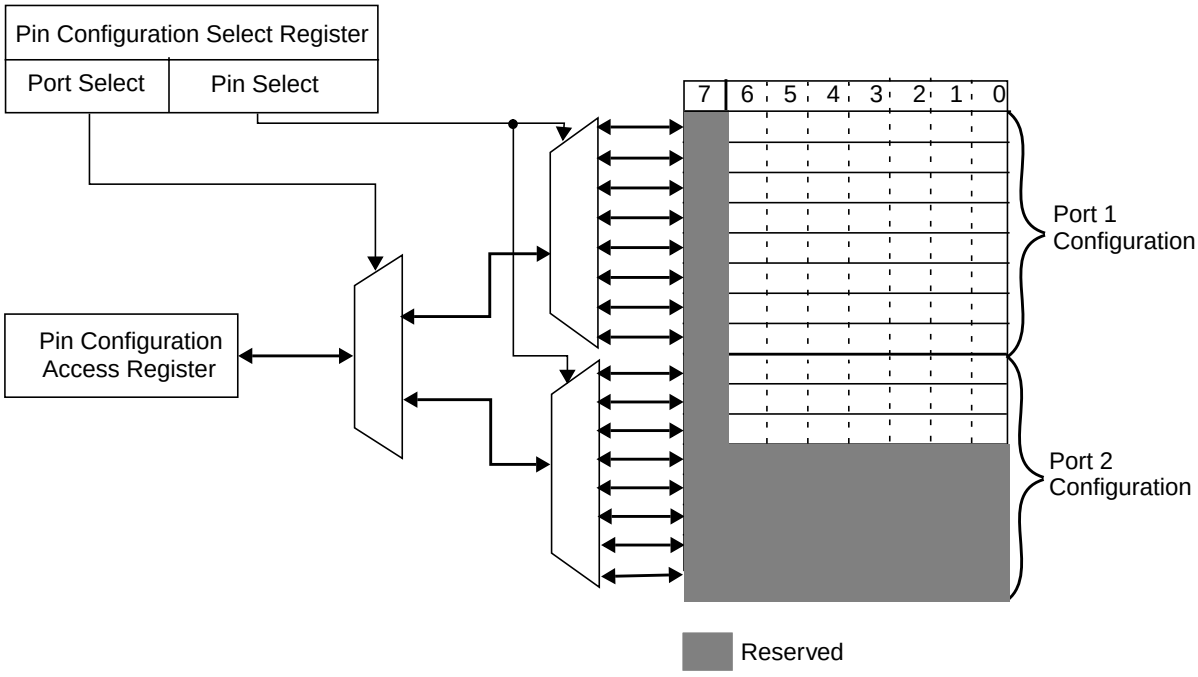


Figure 2-6. GPIO Configuration Registers' Access

2.12.4 GPIO Pin Configuration Select Register

This register selects the GPIO pin (port number and bit number) to be configured (i.e., which register is accessed via the GPIO Pin Configuration Access Register). It is reset by hardware to 00h.

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**		**Port Select**		**Reserved**	**Pin Select**		
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-6	**Reserved**
5-4	**Port Select.** These bits select the GPIO port to be configured: 00: Reserved (default) 01, 10: Binary value of the port number, 1-2 respectively 11: Reserved
3	**Reserved**
2-0	**Pin Select.** These bits select the GPIO pin to be configured in the selected port: 0-7: Binary value of the pin number, 0-7 respectively (default=0)

2.0 Device Architecture and Configuration (Continued)

2.12.5 GPIO Pin Configuration Access Register

This register reflects, for both read and write, the register currently selected by the GPIO Pin Configuration Select Register. All the configuration registers that are accessed via this register have a common bit structure, as shown below. This register is reset by hardware to 44h.

Location: Index F1h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**IRQ Debounce Enable**	**IRQ Polarity**	**IRQ Type**	**Lock**	**Pull-Up Control**	**Output Type**	**Output Enable**
Reset	0	1	0	0	0	1	0	0

Bit	Description
7	**Reserved**
6	**IRQ Debounce Enable** 0: Disabled 1: Enabled (default)
5	**IRQ Polarity.** This bit defines the polarity of the signal that issues an interrupt from the corresponding GPIO pin (falling/low or rising/high). 0: Falling edge or low level input (default) 1: Rising edge or high level input
4	**IRQ Type.** This bit defines the signal type that issues an interrupt from the corresponding GPIO pin. 0: Edge input (default) 1: Level input
3	**Lock**. This bit locks the corresponding GPIO pin. Once this bit is set to 1 by software, it can only be cleared to 0 by system reset or power-off. Pin multiplexing is functional until the Multiplexing Lock bit is 1 (bit 7 of SuperI/O Configuration 3 Register, SIOCF3). 0: No effect (default) 1: Direction, output type, pull-up and output value locked
2	**Pull-Up Control**. This bit is used to enable/disable the internal pull-up capability of the corresponding GPIO pin. It supports open-drain output signals with internal pull-ups and TTL input signals 0: Disabled 1: Enabled (default)
1	**Output Type.** This bit controls the output buffer type (open-drain or push-pull) of the corresponding GPIO pin. 0: Open-drain (default) 1: Push-pull
0	**Output Enable.** This bit indicates the GPIO pin output state. It has no effect on input. 0: TRI-STATE (default) 1: Output enabled

2.0 Device Architecture and Configuration (Continued)

2.13 FAN SPEED CONTROL - LOGICAL DEVICE 8

2.13.1 General Description

This module includes two Fan Speed Controls. The four runtime registers of the two functional blocks are arranged in the address space shown in Table 2-13. The base address is 8-byte aligned. Address bits 2-0 are used to indicate the register offset.

Table 2-13. Runtime Registers in Fan Speed Control Address Space

Offset	Mnemonic	Name	Reset	Function	Type
00h	FCPSR0	Fan Control 0 Pre-Scale Register	00h	Fan Speed Control 0	R/W
01h	FCDCR0	Fan Control 0 Duty Cycle Register	FFh		R/W
02h	FCPSR1	Fan Control 1 Pre-Scale Register	00h	Fan Speed Control 1	R/W
03h	FCDCR1	Fan Control 1 Duty Cycle Register	FFh		R/W
04h-07h	Reserved				

Table 2-14. Fan Speed Control Runtime Register Bitmap

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
00h	FCPSR0	Clock Select	Pre-Scale Value						
01h	FCDCR0	Duty Cycle Value							
02h	FCPSR1	Clock Select	Pre-Scale Value						
03h	FCDCR1	Duty Cycle Value							
04h-07h	Reserved								

2.13.2 Configuration

Index	Configuration Register or Action	Type	Reset
30h	Activate. See also bit 0 of the SIOCF1 Register.	R/W	00h
60h	Base Address MSB Register	R/W	00h
61h	Base Address LSB Register. Bits 2-0 (for A2-0) are read only, 000b.	R/W	00h
70h	Interrupt Number	RO	00h
71h	Interrupt Type	RO	00h
74h	Report no DMA assignment	RO	04h
75h	Report no DMA assignment	RO	04h
F0h	Fan Speed Control Configuration Register	R/W	00h

2.0 Device Architecture and Configuration (Continued)

2.13.3 Fan Speed Control Configuration Register

This register is reset by hardware to 00h.

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Inverse FANOUT1**	**Inverse FANOUT0**	**Fan Speed Control 1 Enable**	**Fan Speed Control 0 Enable**	**Reserved**			**TRI-STATE Control**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**Inverse FANOUT1** 0: The number in FCDCR1 indicates for how many clocks (of 256) FANOUT1 signal is high (default). 1: The number in FCDCR1 indicates for how many clocks (of 256) FANOUT1 signal is low.
6	**Inverse FANOUT0** 0: The number in FCDCR0 indicates for how many clocks (of 256) FANOUT0 signal is high (default). 1: The number in FCDCR0 indicates for how many clocks (of 256) FANOUT0 signal is low.
5	**Fan Speed Control 1 Enable.** When the Fan Speed Interface logical device is active: 0: Clock disabled (stopped). The FSC1 registers are accessible and maintained. FANOUT1 signal is 0 when Inverse FANOUT1 bit is 0. FANOUT1 signal is 1 when Inverse FANOUT1 is 1 (default). 1: Clock enabled and registers accessible
4	**Fan Speed Control 0 Enable.** When the Fan Speed Interface logical device is active: 0: Clock disabled (stopped). The FSC0 registers are accessible and maintained. FANOUT0 signal is 0 when Inverse FANOUT0 bit is 0. FANOUT0 signal is 1 when Inverse FANOUT0 is 1 (default). 1: Clock enabled and registers accessible
3-1	**Reserved**
0	**TRI-STATE Control.** This bit controls the TRI-STATE status of the logical device output pins when it is inactive (disabled). 0: Disabled (default) 1: Enabled when device inactive

3.0 System Wake-Up Control (SWC)

3.1 OVERVIEW

The SWC wakes up the system by asserting the Power-Up Request ($\overline{\text{PWUREQ}}$) output pin, in response to the following maskable system events:

- Modem ring ($\overline{\text{RI1}}$ and $\overline{\text{RI2}}$ pins)
- Telephone ring ($\overline{\text{RING}}$ input pin)
- Any keyboard activity or specific programmable key sequence
- Any mouse activity or specific programmable click/s
- Two general-purpose events (PME1 and PME2 input pins).

This chapter describes the general SWC functional block. A device may include a different implementation. For the device specific implementation, see the *Device Architecture* chapter.

3.2 FUNCTIONAL DESCRIPTION

The SWC monitors seven system events or activities. Each one of them is fed into a dedicated detector that decides when this event is active, according to predetermined (either fixed or programmable) criteria. A set of dedicated registers is used to determine the wake-up criteria, including the Keyboard sequence.

A Wake-Up Events Status Register (WKSR) and a Wake-Up Events Control Register (WKCR) hold a Status bit and Enable bit respectively, for each one of the events.

Upon detection of any active event, the corresponding Status bit is set to 1. If the event is enabled (the corresponding Enable bit is set to 1), the $\overline{\text{PWUREQ}}$ output is asserted. In addition, detection of an active wake-up event may be also routed to any arbitrary IRQ (or SMI over IRQ2 if Serial IRQ is used).

Disabling an event prevents it from issuing $\overline{\text{PWUREQ}}$, but does not affect the Status bits. The $\overline{\text{PWUREQ}}$ signal is active when both the Status and Enable bits equal 1 for at least one event.

The SWC logic is powered by V_{SB}.

The SWC configuration registers are battery backed, powered by V_{PP}. The setup of the wake-up events, including programmable sequences, is retained throughout power failures (no V_{SB}) as long as the battery is connected. V_{PP} is taken from V_{SB} when power is present; otherwise (power-fail), V_{BAT} is used as the V_{PP} source.

System reset does not affect these registers. They are reset only by software reset or power-up of V_{PP}.

3.3 EVENT DETECTION

3.3.1 Modem Ring

High to low transitions on $\overline{\text{RI1}}$ or $\overline{\text{RI2}}$ indicate the detection of ring in external modem connected to Serial Port 1 or 2 respectively and can be used as a wake-up event.

3.3.2 Telephone Ring

A telephone ring can be detected by the SWC by processing the raw signal coming directly from the telephone line into the $\overline{\text{RING}}$ input pin. Detection of a pulse-train with a frequency higher than 16 Hz that lasts at least 0.3 sec is used as a wake-up event.

The $\overline{\text{RING}}$ pulse-train detection is achieved by monitoring the falling edges on $\overline{\text{RING}}$ in time slots of 62.5 msec (a 16 Hz cycle). A positive detection occurs if falling edges of $\overline{\text{RING}}$ are detected in three consecutive time slots, following a time slot in which no $\overline{\text{RING}}$ falling edge is detected. This detection method guarantees the detection of a $\overline{\text{RING}}$ pulse-train with frequencies higher than 16 Hz. It filters out (does not detect) pulses of less than 10 Hz, and may detect pulses between 10 Hz to 16 Hz.

3.3.3 Keyboard and Mouse Activity

The detection of either any activity or a specific predetermined Keyboard or Mouse activity can be used as a wake-up event.

The Keyboard wake-up detection can be programmed to detect:

- Any keystroke
- A specific programmable sequence of up to eight alphanumeric keystrokes
- Any programmable sequence of up to 8 bytes of data received from the keyboard.

The Mouse wake-up detection can be programmed to detect either any Mouse click or movement, or a specific programmable click (left or right) or double-clicks.

3.3.4 General-Purpose Events

A general-purpose event is defined as the detection of falling edge, rising edge, low level, or high level on a specific signal. Each signal's event is configurable via software. PME1 and PME2 may wake up the system from power-off state, or generate an interrupt if the system is in power-on state.

A debouncer of 16 ms is enabled (default) on each event. It may be disabled by software.

3.0 System Wake-Up Control (SWC) (Continued)

3.4 SWC REGISTERS

SWC register offsets are related to a base address determined by the SWC Base Address Register in the device configuration.

The register maps in this chapter use the following abbreviations for Type:

- R/W = Read/Write
- R = Read from a specific address returns the value of a specific register. Write to the same address is to a different register.
- W = Write
- RO = Read Only
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.

3.4.1 SWC Register Map

Offset	Mnemonic	Name	Type	Section
00h	WKCR	Wake-Up Events Control Register	R/W	3.4.2
01h	WKSR	Wake-Up Events Status Register	R/W1C	3.4.3
02h	WKCFG	Wake-Up Configuration Register	R/W	3.4.4
03h	PS2CTL	PS/2 Protocol Control Register	R/W	3.4.5
06h	KDSR	Keyboard Data Shift Register	RO	3.4.6
07h	MDSR	Mouse Data Shift Register	RO	3.4.7
08h-0Fh	PS2KEY0-PS2KEY7	PS/2 Keyboard Key Data Registers	R/W	3.4.8

3.4.2 Wake-Up Events Control Register (WKCR)

This register is set to 07h on power-up of V_{PP} or software reset. Detected wake-up events that are enabled activate the $\overline{\text{PWUREQ}}$ signal.

Location: Offset 00h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**PME2 Event Enable**	**PME1 Event Enable**	**Reserved**	**Mouse Event Enable**	**KBD Event Enable**	**RING Event Enable**	**RI2 Event Enable**	**RI1 Event Enable**
Reset	0	0	0	0	0	1	1	1

Bit	Description
7	**PME2 Event Enable** 0: Disabled (default) 1: Enabled
6	**PME1 Event Enable** 0: Disabled (default) 1: Enabled
5	**Reserved**
4	**Mouse Event Enable** 0: Disabled (default) 1: Enabled
3	**KBD Event Enable** 0: Disabled (default) 1: Enabled

3.0 System Wake-Up Control (SWC) (Continued)

Bit	Description
2	**RING Event Enable** 0: Disabled 1: Enabled (default)
1	**RI2 Event Enable** 0: Disabled 1: Enabled (default)
0	**RI1 Event Enable** 0: Disabled 1: Enabled (default)

3.4.3 Wake-Up Events Status Register (WKSR)

This register is set to 00h on power-up of V_{PP} or software reset. It indicates which wake-up events occurred.

Location: Offset 01h

Type: R/W1C

Bit	7	6	5	4	3	2	1	0
Name	**PME2 Event Status**	**PME1 Event Status**	**Reserved**	**Mouse Event Status**	**KBD Event Status**	**RING Event Status**	**RI2 Event Status**	**RI1 Event Status**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**PME2 Event Status** 0: Event not detected (default) 1: Event detected
6	**PME1 Event Status** 0: Event not detected (default) 1: Event detected
5	**Reserved**
4	**Mouse Event Status** 0: Event not detected (default) 1: Event detected
3	**KBD Event Status** 0: Event not detected (default) 1: Event detected
2	**RING Event Status** 0: Event not detected (default) 1: Event detected
1	**RI2 Event Status** 0: Event not detected (default) 1: Event detected
0	**RI1 Event Status** 0: Event not detected (default) 1: Event detected

3.0 System Wake-Up Control (SWC) (Continued)

3.4.4 Wake-Up Configuration Register (WKCFG)

This register is set to 00h on power-up of V_{PP} or software reset.

Location: Offset 02h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**PME2 Type**	**PME2 Polarity**	**PME1 Type**	**PME1 Polarity**	**Swap KBC Inputs**	**Reserved**	
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**Reserved**
6	**PME2 Type** 0: Edge 1: Level
5	**PME2 Polarity** 0: Falling edge, low level 1: Rising edge, high level
4	**PME1 Type** 0: Edge 1: Level
3	**PME1 Polarity** 0: Falling edge, low level 1: Rising edge, high level
2	**Swap KBC Inputs** 0: No swapping (default) 1: KBD (KBCLK, KBDAT) and Mouse (MCLK, MDAT) inputs swapped
1-0	**Reserved**

3.4.5 PS/2 Protocol Control Register (PS2CTL)

This register is set to 00h on power-up of V_{PP} or software reset. It configures the PS/2 Keyboard and Mouse wake-up features.

Location: Offset 03h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Disable Parity Check**	**Mouse Wake-Up Configuration**			**Keyboard Wake-Up Configuration**			
Reset	0	0	0	0	0	0	0	0

3.0 System Wake-Up Control (SWC) (Continued)

Bit	Description
7	**Disable Parity Check**
6-4	Mouse Wake-Up Configuration **Bits 6 5 4 — Configuration** 0 0 0 — Disable Mouse wake-up detection 0 0 1 — Wake-up on any Mouse movement or button click 0 1 0 — Wake-up on left button click 0 1 1 — Wake-up on left button double-click 1 0 0 — Wake-up on right button click 1 0 1 — Wake-up on right button double-click 1 1 0 — Wake-up on any button single-click (left, right or middle) 1 1 1 — Wake-up on any button double-click (left, right or middle)
3-0	Keyboard Wake-Up Configuration **Bits 3 2 1 0 — Configuration** 0 0 0 0 — Disable Keyboard wake-up detection 0 0 0 1 to 0 1 1 1 — Special key sequence 2-8 PS/2 scan codes (including scan codes for Shift and Alt keys) 1 0 0 0 to 1 1 1 1 — Password enabled with 1-8 keys (excluding scan codes for Shift and Alt keys)

3.4.6 Keyboard Data Shift Register (KDSR)

This register is set to 00h on power-up of V_{PP} or software reset. It stores the Keyboard data shifted in from the Keyboard during transmission, only when Keyboard wake-up detection is enabled.

Location: Offset 06h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**Keyboard Data**							
Reset	0	0	0	0	0	0	0	0

3.4.7 Mouse Data Shift Register (MDSR)

This register is set to 00h on power-up of V_{PP} or software reset. It stores the Mouse data shifted in from the Mouse during transmission, only when Mouse wake-up detection is enabled.

Location: Offset 07h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**					**Mouse Data**		
Reset	0	0	0	0	0	0	0	0

3.0 System Wake-Up Control (SWC) (Continued)

3.4.8 PS/2 Keyboard Key Data Registers (PS2KEY0 - PS2KEY7)

The following eight registers (PS2KEY0-PS2KEY7) store the scan codes for the password or key sequence of the Keyboard wake-up feature.

The first register (PS2KEY0) stores the scan code for the first key in the password/key sequence.

The second register (PS2KEY1) stores the scan code for the second key in the password/key sequence.

The third to eighth registers (PS2KEY2 - PS2KEY7) store the scan code for the third to eighth keys in the password/key sequence.

These registers are set to 00h on power-up of V_{PP} or software reset.

Location: Offset 08h-0Fh

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Scan Code of Keys 0-7**							
Reset	0	0	0	0	0	0	0	0

3.5 SWC REGISTER BITMAP

Register		**Bits**							
Offset	Mnemonic	7	6	5	4	3	2	1	0
00h	WKCR	PME2 Event Enable	PME1 Event Enable	Reserved	Mouse Event Enable	KBD Event Enable	RING Event Enable	RI2 Event Enable	RI1 Event Enable
01h	WKSR	PME2 Event Status	PME1 Evemt Status	Reserved	Mouse Event Status	KBD Event Status	RING Event Status	RI2 Event Status	RI1 Event Status
02h	WKCFG	Reserved	PME2 Type	PME2 Polarity	PME1 Type	PME1 Polarity	Swap KBC Inputs	Reserved	
03h	PS2CTL	Disable Parity Check	Mouse Wake-Up Configuration			Keyboard Wake-Up Configuration			
06h	KDSR	Keyboard Data							
07h	MDSR	Reserved					Mouse Data		
08-0F	PS2KEY0-PS2KEY7	Scan Code of Keys 0-7							

4.0 General-Purpose Input/Output (GPIO) Port

This chapter describes one 8-bit port. A device may include a combination of several ports with different implementations. For the device specific implementation, see the *Device Architecture and Configuration* chapter. If there are fewer than 8 bits per port in a configuration, only the corresponding lower bits are implemented and the remaining bits are reserved. For instance, if there are 3 bits per port, only bits 0-2 are implemented, and the remaining 5 bits are reserved.

4.1 OVERVIEW

The GPIO port is an 8-bit port which is based on eight pins. It features:

- Software capability to manipulate and read pin levels
- Controllable interrupt assertion based on the pin level or level transition
- Ability to capture and manipulate interrupts and their associated status
- Back-drive protected pins.

GPIO port operation is associated with two sets of registers:

- Configuration registers, mapped in the Device Configuration space. These registers are used to statically set up the logical behavior of each pin. There is one 8-bit register for each GPIO pin.
- Four 8-bit runtime registers: GPIO Data Out (GPDO), GPIO Data In (GPDI), GPIO Interrupt Enable (GPIEN) and GPIO Status (GPST). These registers are mapped in the GPIO device IO space (which is determined by the base address registers in the GPIO Device Configuration). They are used to manipulate and/or read the pin values, and to control and handle interrupt generation. Each runtime register corresponds to the 8-pin port, such that bit n in each one of the four registers is associated with GPIOXn pin, where X is the port number.

Each GPIO pin is associated with eight configuration bits and the corresponding bit slice of the four runtime registers, as shown in Figure 4-1.

The functionality of the GPIO port is divided into basic functionality that includes the manipulation and reading of the GPIO pins. This functionality is described in Section 4.2. The enhanced functionality which includes the interrupt assertion and handling is described in Section 4.3.

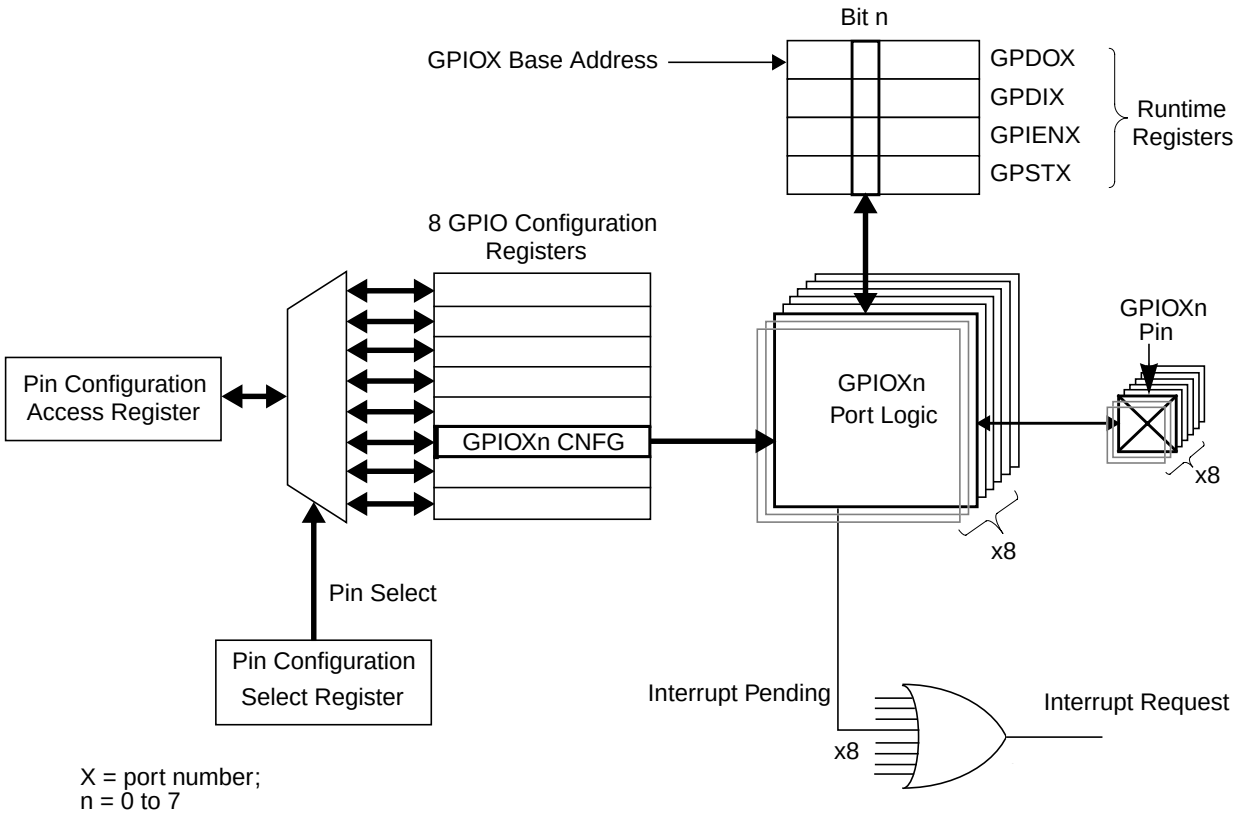


Figure 4-1. GPIO Port Architecture

4.0 General-Purpose Input/Output (GPIO) Port (Continued)

4.2 BASIC FUNCTIONALITY

The basic functionality of each GPIO pin is based on four configuration bits and a bit slice of runtime registers GPDO and GPDI. The configuration and operation of a single pin GPIOXn (pin n in port X) is shown in Figure 4-2.

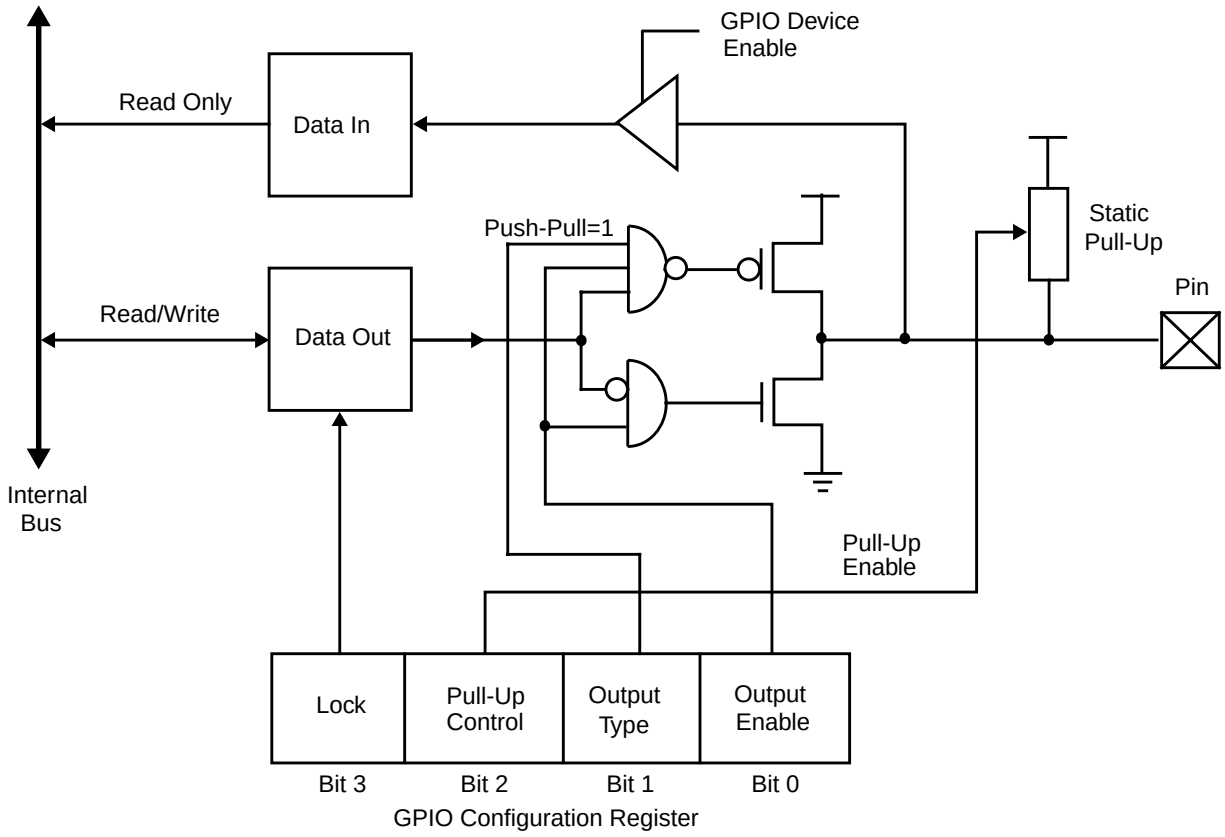


Figure 4-2. GPIO Basic Functionality

4.2.1 Configuration Options

The GPIO Configuration Register controls the following basic configuration options:

- Port Direction - Controlled by the Output Enable bit (bit 0)
- Output Type - Totem pole vs. open-drain. It is controlled by Output Buffer Type (bit 1) by enabling/disabling the pull-up portion of the output buffer.
- Weak Static Pull-up - May be added to any type of port (input, open-drain or totem pole). It is controlled by Pull-Up Control (bit 2).
- Pin Lock - GPIO pin may be locked to prevent any changes in the output value and/or the output characteristics. The lock is controlled by Lock (bit 3). It disables writes to the GPDO Register bits, and to bits 0-3 of the GPIO Configuration Register (Including the Lock bit itself). Once locked, it can be released by hardware reset only.

4.2.2 Operation

The value that is written to the GPDO Register is driven to the pin, if the output is enabled. Reading from the GPDO Register returns its contents, regardless of the pin value or the port configuration. The GPDI Register is a read-only register. Reading from the GPDI Register returns the pin value, regardless of what is driving it (the port itself, configured as an output port, or the external device when the port is configured as an input port). Writing to this register is ignored.

Activation of the GPIO port is controlled by external device specific configuration bit (or a combination of bits). When the port is inactive, access to GPDI and GPDO Registers is disabled, and the inputs are blocked. However, there is no change in the port configuration and in the GPDO value, and hence there is no effect on the outputs of the pins.

4.0 General-Purpose Input/Output (GPIO) Port (Continued)

4.3 INTERRUPT ASSERTION AND HANDLING

The enhanced GPIO port supports interrupt assertion and handling. This functionality is based on three configuration bits and a bit slice of runtime registers GPIEN and GPST. The configuration and operation of the interrupt capability is shown in Figure 4-3.

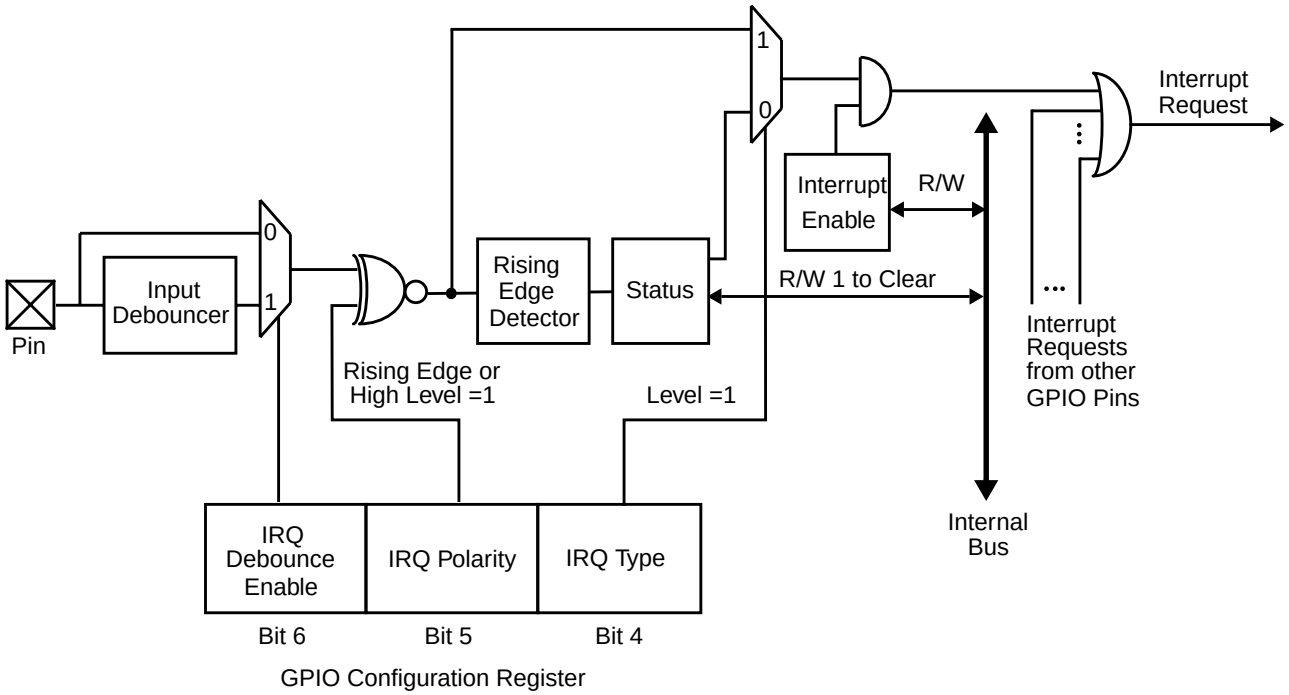


Figure 4-3. Interrupt Assertion

4.3.1 Interrupt Configuration

Each pin in the GPIO port is a potential interrupt source. The interrupt generator can trigger an interrupt upon predetermined behavior of the source pin. The GPIO Configuration Register determines the interrupt generation trigger type for the interrupt assertion.

IRQ Polarity

Two trigger types of interrupt assertion are supported: edge and level. An edge interrupt may be asserted upon a source pin transition either from high to low or low to high. A level interrupt may be asserted when the source pin is in active level. The trigger type is determined by IRQ Type (bit 4 of the GPIO Configuration Register). The direction of the transition (for edge) or the polarity of the active level (for level) is determined by IRQ Polarity (bit 5 of the GPIO Configuration Register).

IRQ Debounce Enable

The input signal for the interrupt can be debounced for about 15 msec. The signal state should be transferred only after a debouncing period during which the signal has no transitions, to ensure that the signal is stable. The debouncer adds 15 msec delay to both assertion and de-assertion level interrupts, and to the assertion of edge interrupts. When working with a level interrupt, it is recommended to disable the debounce if the delay in the interrupt de-assertion is not acceptable.

The debounce is controlled by IRQ Debounce Enable (bit 6 of the GPIO Configuration Register).

4.3.2 Interrupt Assertion

The interrupt assertion for each GPIO pin is controlled by the corresponding bit in the GPIEN Register. Interrupt assertion by a GPIO pin is enabled if the corresponding bit of this register is set to 1.

The GPST Register is a general-purpose edge detector which may be used to reflect the interrupt source pending status for edge-triggered interrupts.

The term *active edge* refers to a change in a GPIO pin level that matches the IRQ Polarity bit (1 for rising edge and 0 for falling edge). *Active level* refers to the GPIO pin level that matches the IRQ Polarity bit (1 for high level and 0 for low level). The corresponding bit of the GPST Register is set by hardware whenever an active edge is detected, regardless of any other bit settings. Writing 1 to the Status bit clears it to 0. Writing 0 is ignored.

4.0 General-Purpose Input/Output (GPIO) Port (Continued)

A GPIO pin is in interrupt pending state if the corresponding bit of the GPIEN Register is set and either:

- The IRQ Type is level and the pin is in active level, or
- The IRQ Type is edge and the corresponding bit of the GPST Register is set.

The target IRQ line is asserted if at least one GPIO pin is in interrupt pending state. The selection of the target IRQ line is determined by the IRQ selection procedure of the device configuration. The assertion of the IRQ line is blocked when the GPIO functional block is deactivated.

If the output is enabled, the IRQ may be initiated by the software when writing to the GPDO Register.

An edge interrupt may be de-asserted by clearing the corresponding GPST bit. However, a level Interrupt source may not be released by software (except for disabling the source), as long as the pin is in active level. When level interrupt is used, it is recommended to disable the input debouncer.

Upon de-activation of the GPIO port, the GPST Register is cleared and access to both the GPST and GPIEN Registers is disabled. The target IRQ line is detached from the GPIO and de-asserted.

Before enabling the interrupts, it is recommended to set the desired interrupt configuration, and then verify that the status registers are cleared.

4.4 GPIO PORT REGISTERS

The register maps in this chapter use the following abbreviations for Type:

- R/W = Read/Write
- R = Read from a specific address returns the value of a specific register. Write to the same address is to a different register.
- W = Write
- RO = Read Only
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.

4.4.1 GPIO Pin Configuration Access Register

This is a group of eight identical configuration registers, each of which is associated with one GPIO pin. The entire set is mapped to the PnP configuration space. The mapping scheme is based on the GPIO Pin Configuration Select Register that functions as an index register, and the specific GPIO Pin Configuration Access Register that reflects the configuration of the currently selected pin. For details on the GPIO Pin Configuration Select Register, refer to the *Device Architecture and Configuration* chapter.

Bits 4-6 are applicable only for the enhanced GPIO port with interrupt support. In the basic port. these bits are reserved, return 0 on read and have no effect on port functionality.

Location: Device specific

Type: R/W (bit 3 is set only)

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**IRQ Debounce Enable**	**IRQ Polarity**	**IRQ Type**	**Lock**	**Pull-Up Control**	**Output Type**	**Output Enable**
Reset	0	1	0	0	0	1	0	0

Bit	Description
7	**Reserved**
6	**IRQ Debounce Enable** 0: Disabled 1: Enabled (default)
5	**IRQ Polarity.** This bit defines the polarity of the signal that issues an interrupt from the corresponding GPIO pin (falling/low or rising/high). 0: Falling edge or low level input (default) 1: Rising edge or high level input

4.0 General-Purpose Input/Output (GPIO) Port (Continued)

Bit	Description
4	**IRQ Type.** This bit defines the signal type that issues an interrupt from the corresponding GPIO pin. 0: Edge input (default) 1: Level input
3	**Lock**. This bit locks the corresponding GPIO pin. Once this bit is set to 1 by software, it can only be cleared to 0 by system reset or power-off. Pin multiplexing is functional until the Multiplexing Lock bit is 1 (bit 7 of SuperI/O Configuration 3 Register (SIOCF3). 0: No effect (default) 1: Direction, output type, pull-up and output value locked
2	**Pull-Up Control**. This bit is used to enable/disable the internal pull-up capability of the corresponding GPIO pin. It supports open-drain output signals with internal pull-ups and TTL input signals 0: Disabled 1: Enabled (default)
1	**Output Type.** This bit controls the output buffer type (open-drain or push-pull) of the corresponding GPIO pin. 0: Open-drain (default) 1: Push-pull
0	**Output Enable.** This bit indicates the GPIO pin output state. It has no effect on input. 0: TRI-STATE (default) 1: Output enabled

4.4.2 GPIO Port Runtime Register Map

Offset	Mnemonic	Name	Type	Section
Device specific[1]	GPDO	GPIO Data Out Register	R/W	4.4.3
Device specific[1]	GPDI	GPIO Data In Register	RO	4.4.4
Device specific[1]	GPIEN	GPIO Interrupt Enable Register	R/W	4.4.5
Device specific[1]	GPST	GPIO Status Register	R/W1C	4.4.6

1. The location of this register is defined in the *Device Architecture and Configuration* chapter in Section 2.12.1.

4.0 General-Purpose Input/Output (GPIO) Port (Continued)

4.4.3 GPIO Data Out Register (GPDO)

Location: Device specific

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Data Out**							
Reset	1	1	1	1	1	1	1	1

Bit	Description
7	**Data Out.** Bits 7-0 correspond to pins 7-0 respectively. The value of each bit determines the value driven on the corresponding GPIO pin when its output buffer is enabled. Writing to the bit latches the written data unless the bit is locked by the GPIO Configuration Register Lock bit. Reading the bit returns its value, regardless of the pin value and configuration. 0: Corresponding pin driven to low when output enabled 1: Corresponding pin driven or released to high (according to buffer type and static pull-up selection) when output enabled
6	
5	
4	
3	
2	
1	
0	

4.4.4 GPIO Data In Register (GPDI)

Location: Device specific

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**Data In**							
Reset	X	X	X	X	X	X	X	X

Bit	Description
7	**Data In.** Bits 7-0 correspond to pins 7-0 respectively. Reading each bit returns the value of the corresponding GPIO pin, regardless of the pin configuration and the GPDO Register value. Write is ignored. 0: Corresponding pin level low 1: Corresponding pin level high
6	
5	
4	
3	
2	
1	
0	

4.0 General-Purpose Input/Output (GPIO) Port (Continued)

4.4.5 GPIO Interrupt Enable Register (GPIEN)

Location: Device specific

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Interrupt Enable**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**Interrupt Enable.** Bits 7-0 correspond to pins 7-0 respectively. Each bit enables Interrupt generation by the corresponding GPIO pin. The bit has no effect on the corresponding Status bit in the GPST Register. 0: IRQ generation by corresponding GPIO pin masked 1: IRQ generation by corresponding GPIO pin enabled
6	
5	
4	
3	
2	
1	
0	

4.4.6 GPIO Status Register (GPST)

Location: Device specific

Type: R/W1C

Bit	7	6	5	4	3	2	1	0
Name	**Status**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**Status.** Bits 7-0 correspond to pins 7-0 respectively. Each bit is an edge detector that is set to 1 by the hardware upon detection of an active edge (i.e. edge that matches the IRQ Polarity bit) on the corresponding GPIO pin. This edge detection is independent of the IRQ Type or the Interrupt Enable bit in the GPIEN Register. However, the bit may reflect the IRQ status for enabled, edge-trigger IRQ sources. Writing 1 to the Status bit clears it to 0. 0: No active edge detected since last cleared 1: Active edge detected
6	
5	
4	
3	
2	
1	
0	

5.0 Fan Speed Control

5.1 OVERVIEW

This chapter describes one Fan Speed Control module. A device may include some modules with different implementations. For the device specific implementation, see the *Device Architecture and Configuration* chapter.

The Fan Speed Control is a programmable Pulse Width Modulation (PWM) generator. The PWM output is used to control the fan's power voltage, which is correlated to the fan's speed. Converting a 0 to 100% duty cycle PWM signal to an analog voltage range is achieved by an external circuit, as shown in Figure 5-1. Some new types of fans accept direct PWM input without any external circuitry.

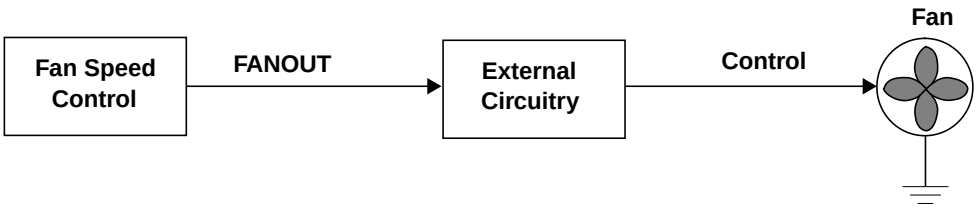


Figure 5-1. Fan Speed Control - System Configuration

5.2 FUNCTIONAL DESCRIPTION

The PWM generator operation is based on a PWM counter and two registers: the Fan Speed Control Pre-Scale Register (FCPSR), used to determine the overall cycle time (or the frequency) of the FANOUT output, and the Fan Speed Control Duty Cycle Register (FCDCR), used to determine the duty cycle of the FANOUT between 0 to 100%.

The PWM counter is an 8-bit, free-running counter that runs continuously in a cyclic manner, i.e its cycle equals 256 clock periods. The PWM output is high as long as the count is lower than the FCDCR value, and flips to low as the counter exceeds that value. The duty cycle (expressed as a percentage) is therefore (FCDCR/256)*100. In particular, the PWM output is continuously low when FCDCR=0 and continuously high when FCDCR=FFh. The FANOUT output may be inverted by an external configuration bit, in which case the FANOUT duty cycle is ([256-FCDCR]/256)*100.

The PWM counter clock is generated by dividing the input clock, either 24 MHz or 200 KHz (according to Clock Select, bit 7 of the FCPSR Register) using a clock divider. The division factor, which must be between 1 and 124, is defined as Pre-Scale Value+1, where Pre-Scale is the binary value stored in bits 6 to 0 of the FCPSR Register. The resulting PWM output frequency is therefore (24 MHz or 200 kHz/([Pre-Scale Value+1]*256). The default selection of 24 MHz input clock allows a programmable FANOUT frequency in the range of 756 Hz to 93.75 KHz. For lower frequencies, selecting the 200 KHz input clock allows a frequency range of 6 Hz to 781 Hz. See Figure 5-2.

The FANOUT frequency must be pre-selected according to the fan type specific requirements prior to enabling the Fan Speed Control. The only run-time change that is required to dynamically control the fan speed is the value of the FCDCR Register. The contents of the FCPSR Register must not be changed when the Fan Speed Control is enabled.

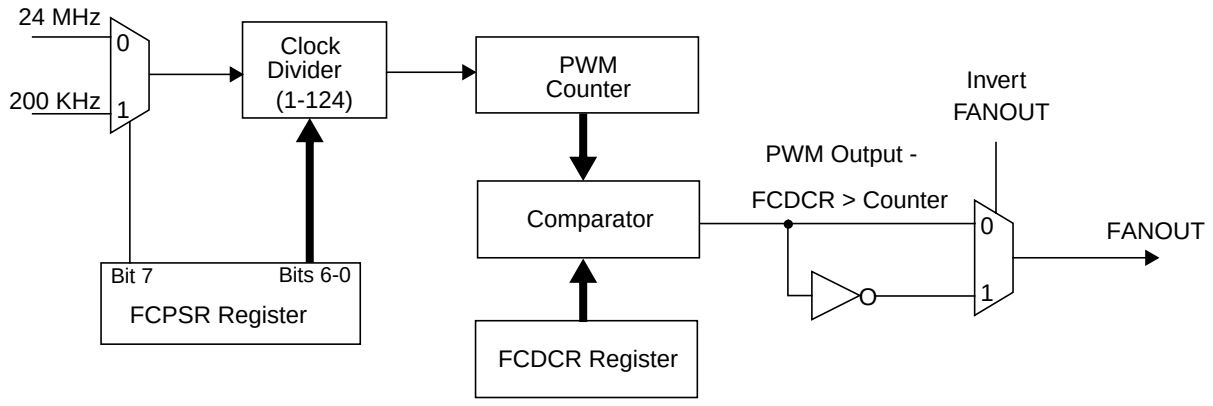


Figure 5-2. PWM Generator (FANOUT)

5.0 Fan Speed Control (Continued)

5.3 FAN SPEED CONTROL REGISTERS

The register maps in this chapter use the following abbreviations for Type:

- R/W = Read/Write
- R = Read from a specific address returns the value of a specific register. Write to the same address is to a different register.
- W = Write
- RO = Read Only
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.

5.3.1 Fan Speed Control Register Map

Offset	Mnemonic	Name	Type	Section
Device specific[1]	FCPSR	Fan Speed Control Pre-Scale Register	R/W	5.3.2
Device specific[1]	FCDCR	Fan Speed Control Duty Cycle Register	R/W	5.3.3

1. The location of this register is defined in the *Device Architecture and Configuration* chapter in Section 2.13.1.

5.3.2 Fan Control Pre-Scale Register (FCPSR)

Location: Device specific

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Clock Select**	**Pre-Scale Value**						
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**Clock Select.** This bit selects the input clock for the clock divider. 0: 24 MHz 1: 200 KHz
6-0	**Pre-Scale Value.** The clock divider for the input clock (24 MHz or 200 KHz) is Pre-Scale Value + 1. Writing 0 transfers the input clock directly to the counter. The maximum clock divider is 124 (7Bh +1). These bits must not be programmed with the values 7Ch, 7Dh, 7Eh and 7Fh as this may produce unpredictable results. The contents of this register should not be changed when the corresponding Fan Speed Control Enable bit of the Fan Speed Control Configuration Register is 1 (See *Device Architecture and Configuration* chapter). Otherwise, there may be unpredictable results.

5.3.3 Fan Control Duty Cycle Register (FCDCR)

Location: Device specific

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Duty Cycle Value**							
Reset	1	1	1	1	1	1	1	1

5.0 Fan Speed Control (Continued)

Bit	Description
7-0	**Duty Cycle.** The binary value of this 8-bit field determines the number of clock cycles, out of a 256-cycle period, during which the PWM output is high (while FANOUT is either equal to or the inverse of the PWM output, depending on the Inverse FANOUT configuration bit). 00h: PWM output is continuously low 01h - FEh: PWM output is high for [Duty Cycle Value] clock cycles and low for [256-Duty Cycle Value] clock cycles FFh: PWM output is continuously high

5.4 FAN SPEED CONTROL BITMAP

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
Device specific[1]	FCPSR	Clock Select	Pre-Scale Value						
Device specific[1]	FCDCR	Duty Cycle Value							

1. The location of this register is defined in the *Device Architecture and Configuration* chapter.

6.0 Floppy Disk Controller (FDC)

Refer to PC87307, PC87309 or PC87317 datasheet.

7.0 Parallel Port

Refer to PC87307, PC87309 or PC87317 datasheet.

8.0 Serial Port 2 with IR

Refer to PC87307, PC87309 or PC87317 datasheet.

9.0 Serial Port 1

Refer to PC87307, PC87309 or PC87317 datasheet.

10.0 Keyboard and Mouse Controller (KBC)

Refer to PC87307, PC87309 or PC87317 datasheet.

11.0 Device Characteristics

11.1 DC ELECTRICAL CHARACTERISTICS

Sections 11.1.6 to 11.1.10 summarize the DC characteristics of all device pins described in the *Signal/Pin Connection and Description* chapter. The characteristics describe the general I/O buffer type. For the exception, refer to the notes at the end of this section.

11.1.1 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{SB}	Standby Supply Voltage	4.5	5.0	5.5	V
V_{BAT}	Battery Supply Voltage	2.4	3.0	3.6	V
T_A	Operating Temperature	0		+70	°C

11.1.2 Absolute Maximum Ratings

Absolute maximum ratings are values beyond which damage to the device may occur. Unless otherwise specified, all voltages are relative to ground.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Supply Voltage		–0.5	TBD	V
V_I	Input Voltage		–0.5	V_{DD} + 0.5	V
V_O	Output Voltage		–0.5	V_{DD} + 0.5	V
T_{STG}	Storage Temperature		–65	+165	°C
P_D	Power Dissipation			1	W
T_L	Lead Temperature Soldering (10 sec)			+260	°C
	ESD Tolerance	C_{ZAP} = 100 pF R_{ZAP} = 1.5 KΩ[1]	2000		V

1. Value based on test complying with RAI-5-048-RA human body model ESD testing.

11.1.3 Capacitance

Symbol	Parameter	Min	Typ	Max	Unit
C_{IN}	Input Pin Capacitance		5	7	pF
C_{IN1}	Clock Input Capacitance	5	8	12	pF
C_{IO}	I/O Pin Capacitance		10	12	pF
C_O	Output Pin Capacitance		6	8	pF

T_A = 25°C, f = 1 MHz

11.0 Device Characteristics (Continued)

11.1.4 Power Consumption under Recommended Operating Conditions

Symbol	Parameter	Conditions	Typ	Max	Unit
I_{CC}	V_{DD} Average Main Supply Current	V_{IL} = 0.5 V, V_{IH} = 2.4 V No Load	32	50	mA
I_{CCLP}	V_{DD} Quiescent Main Supply Current in Low Power Mode	V_{IL} = V_{SS}, V_{IH} = V_{DD} No Load	1.3	1.7	mA
I_{SB}	V_{SB} Average Main Supply Current	V_{IL} = 0.5 V, V_{IH} = 2.4 V No Load		15	mA
I_{SBLP}	V_{SB} Quiescent Main Supply Current in Low Power Mode	V_{IL} = V_{SS}, V_{IH} = V_{SB} V No Load		3	mA
I_{BAT}	V_{BAT} Battery Supply Current	V_{DD}, V_{SB} = 0 V, V_{BAT} = 3 V		250	nA

11.1.5 Input, PCI 5V

Symbol: IN_{PCI}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		2.0	V_{DD} + 0.5	V
V_{IL}	Input Low Voltage		-0.5	0.8	V
I_{IL}[1]	Input Leakage Current	0 < V_{in} < V_{DD}		-/+10	µA

1. Input leakage currents include hi-Z output leakage for all bidirectional buffers with TRI-STATE outputs.

11.1.6 Strap Pin

Symbol: IN_{STRP}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		$0.6V_{DD}$ [1]	V_{DD} [1]	V
I_{IL}	Input Leakage Current	During Reset: V_{IN} = V_{DD}		250	µA
		V_{IN} = V_{SS}		–10	µA

1. Not tested. Guaranteed by design.

11.1.7 Input, TTL Compatible

Symbol: IN_{T}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		2.0	V_{DD}[1]	V
V_{IL}	Input Low Voltage		–0.5[1]	0.8	V
I_{IL}	Input Leakage Current	V_{IN} = V_{DD}		10	µA
		V_{IN} = V_{SS}		–10	µA

1. Not tested. Guaranteed by design.

11.0 Device Characteristics (Continued)

11.1.8 Input with TTL Schmitt Trigger

Symbol: IN_{TS}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		2.0	V_{DD} [1]	V
V_{IL}	Input Low Voltage		–0.5 [1]	0.8	V
I_{IL}	Input Leakage Current	$V_{IN} = V_{DD}$		10	µA
		$V_{IN} = V_{SS}$		–10	µA
V_H	Input Hysteresis		250		mV

1. Not tested. Guaranteed by design.

11.1.9 Output, Totem-Pole Buffer

Symbol: $O_{p/n}$

Output, Totem-Pole buffer that is capable of sourcing *p* mA and sinking *n* mA

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output High Voltage	$I_{OH} = -p$ mA	2.4		V
V_{OL}	Output Low Voltage	$I_{OL} = n$ mA		0.4	V

11.1.10 Output, Open-Drain Buffer

Symbol: OD_n

Output, Open-Drain output buffer that is capable of sinking *n* mA. Output from these signals is open-drain and cannot be forced high.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output Low Voltage	$I_{OL} = n$ mA		0.4	V

Notes:

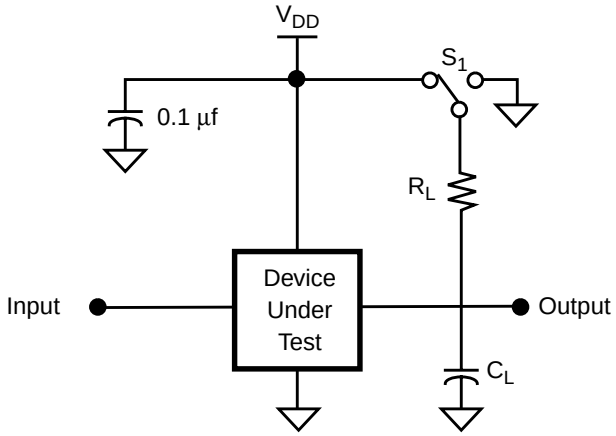
1. All pins are back-drive protected.
2. The following pins have a static pull-up resistor and therefore may have input leakage current (when $V_{IN} = V_{SS}$) of about -250µA: TBD
3. The following pins have a static pull-down resistor and therefore may have input leakage current (when $V_{IN} = V_{DD}$) of about 200µA: TBD
4. Output from SLCT, BUSY/$\overline{WAIT}$ (and PE if bit 2 of PP Confg0 Register is “0”) is open-drain in all SPP modes, except in SPP Compatible mode when the setup mode is ECP-based FIFO and bit 4 of the Control2 parallel port register is 1. Otherwise, output from these signals is level 2. External 4.7 KW pull-up resistors should be used.
5. Output from $\overline{ACK}$, $\overline{ERR}$ (and PE if bit 2 of PP Confg0 Register is “1”) is open-drain in all SPP modes, except in SPP Compatible mode when the setup mode is ECP-based FIFO and bit 4 of the Control2 parallel port register is 1. Otherwise, output from these signals is level 2. External 4.7 KW pull-up resistors should be used.
6. I_{OH} on pins P12 and P17 are driven for 10 nsec after the low-to-high transition.
7. Output from $\overline{STB}$, $\overline{AFD}$, $\overline{INIT}$, $\overline{SLIN}$ is open-drain in all SPP modes, except in SPP Compatible mode when the setup mode is ECP-based (FIFO). Otherwise, output from these signals is Level 2. External 4.7 KΩ pull-up resistors should be used.
8. Output from PD7-0 is open-drain in all SPP modes, except in SPP Compatible mode when the setup mode is ECP-based (FIFO) and bit 4 of the Control2 parallel port register is 1. Otherwise, output from these signals is Level 2. External 4.7 KΩ pull-up resistors should be used.
9. I_{OH} is valid for a GPIO signals only when it is not configured as open-drain.

11.0 Device Characteristics (Continued)

11.2 AC ELECTRICAL CHARACTERISTICS

11.2.1 AC Test Conditions

Load Circuit (Notes 1, 2, 3)



AC Testing Input, Output Waveform

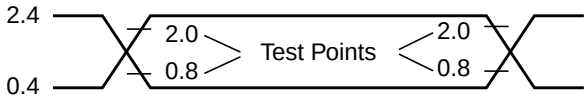


Figure 11-1. AC Test Conditions, T_A = 0 °C to 70 °C, V_{DD} = 5.0 V ±10%

Notes:

1. C_L = 100 pF, includes jig and scope capacitance.
2. S_1 = Open for push-pull output pins.
   S_1 = V_{DD} for high impedance to active low and active low to high impedance measurements.
   S_1 = GND for high impedance to active high and active high to high impedance measurements.
   R_L = 1.0KΩ for µP interface pins.

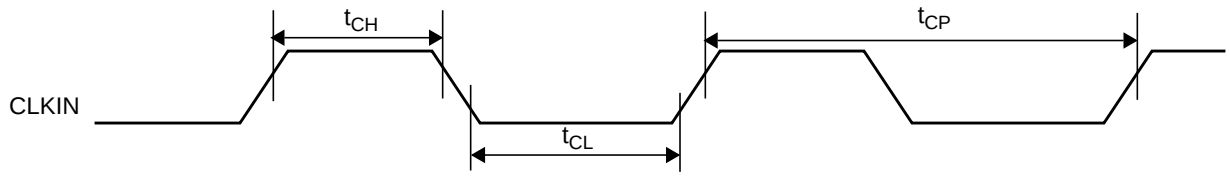
For the FDC open-drive interface pins, S_1 = V_{DD} and R_L = 150Ω

11.2.2 Clock Timing

Symbol	Parameter	48MHz		
		Min	Max	Unit
t_{CH}	Clock High Pulse Width[1]	8.4		nsec
t_{CL}	Clock Low Pulse Width[1]	8.4		nsec
t_{CP}	Clock Period [1]	20	21.5	nsec

1. Not tested. Guaranteed by design.

.



11.0 Device Characteristics (Continued)

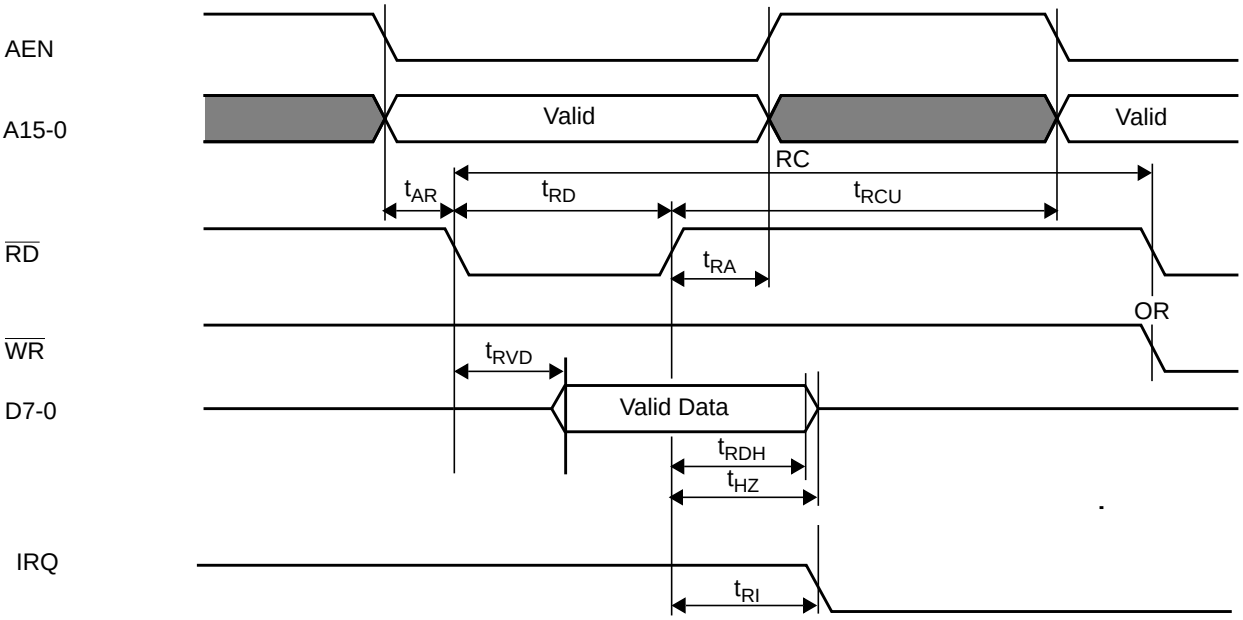
11.2.3 Host Interface I/O Cycle Timing

Symbol	Parameter	Min	Max	Unit
t_{AR}	Valid Address to Read Active	18		nsec
t_{AW}	Valid Address to Write Active	18		nsec
t_{DH}	Data Hold	0		nsec
t_{DS}	Data Setup	18		nsec
t_{HZ}	Read to Floating Data Bus[1]	13	25	nsec
t_{RA}	Address Hold from Inactive Read	0		nsec
t_{RCU}	Read Cycle Update[1]	45		nsec
t_{RD}	Read Strobe Width	60		nsec
t_{RDH}	Read Data Hold	10		nsec
t_{RI}	Read Strobe to Clear IRQ		55	nsec
t_{RVD}	Active Read to Valid Data		55	nsec
t_{WA}	Address Hold from Inactive Write	0		nsec
t_{WCU}	Write Cycle Update[1]	45		nsec
t_{WI}	Write Strobe to Clear IRQ		55	nsec
t_{WR}	Write Strobe Width	60		nsec
RC	Read Cycle = $t_{AR} + t_{RD} + t_{RCU}$[1]	123		nsec
WC	Write Cycle = $t_{AW} + t_{WR} + t_{WC}$[1]	123		nsec
t_{WRR}	$\overline{RD}$ low after $\overline{WR}$ high[1]	80		nsec
t_{RDYA}	$\overline{RD}/\overline{WR}$ active to IOCHRDY active[2]	0	24	nsec
t_{RDYI}	$\overline{WAIT}$ inactive to IOCHRDY inactive[2]		40	nsec
t_{RWI}	IOCHRDY inactive to $\overline{RD}/\overline{WR}$ inactive[2]	10		nsec

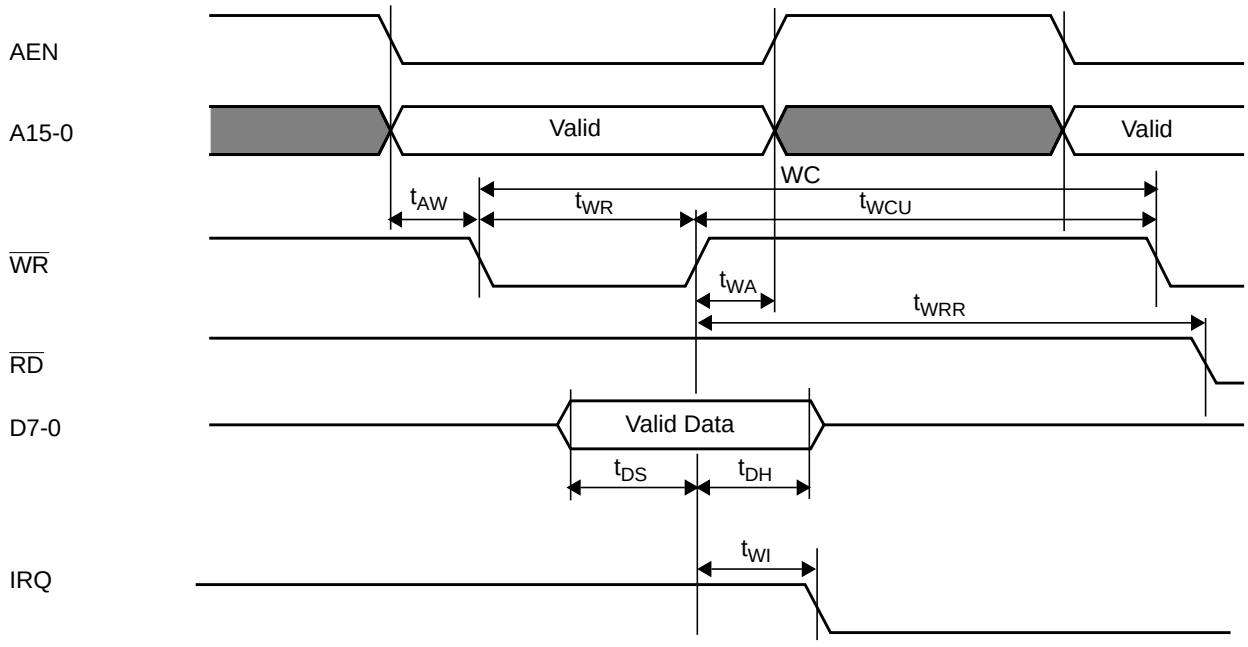
1. Not tested. Guaranteed by design.
2. Applicable for EPP mode only.

11.0 Device Characteristics (Continued)

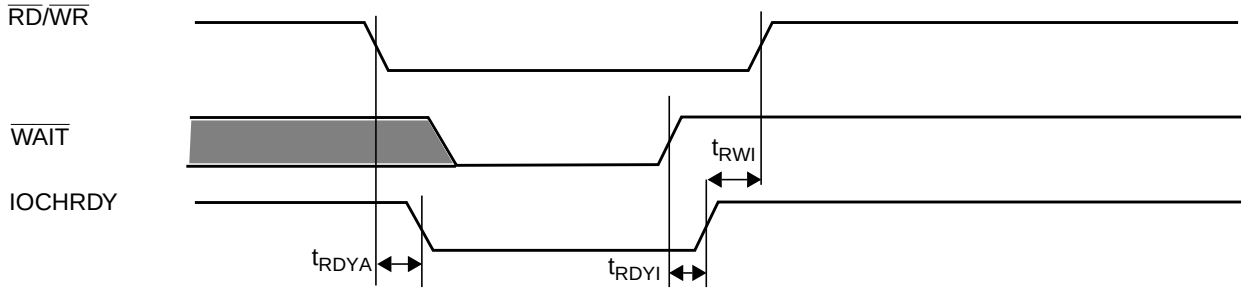
Read



Write



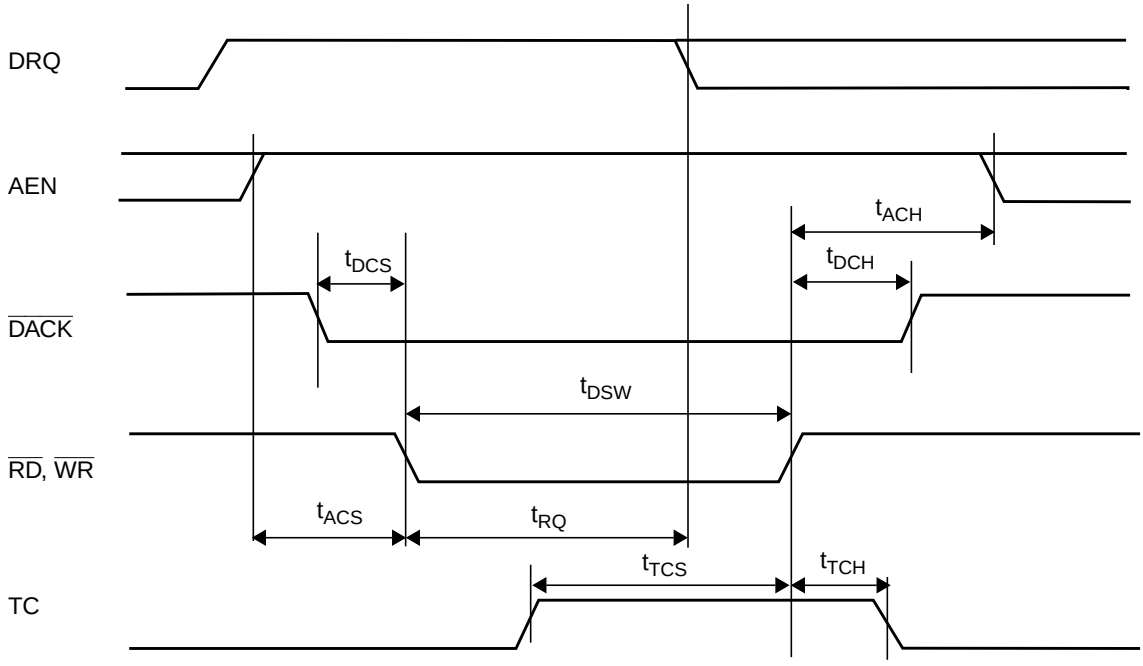
IOCHRDY



11.0 Device Characteristics (Continued)

11.2.4 Host Interface DMA Cycle Timing

Symbol	Parameter	Min	Max	Unit
t_{ACH}	AEN Hold from RD, WR Inactive	0		nsec
t_{ACS}	AEN Signal Setup	15		nsec
t_{DCH}	$\overline{DACK}$ Hold from RD, WR Inactive	0		nsec
t_{DCS}	$\overline{DACK}$ Signal Setup	15		nsec
tDSW	$\overline{RD}$, $\overline{WR}$ Pulse Width	60		nsec
t_{RQS}	DRQ Inactive from $\overline{RD}$, $\overline{WR}$ Active		60	nsec
t_{TCH}	TC Hold from $\overline{RD}$, $\overline{WR}$ Inactive	0		nsec
t_{TCS}	TC Signal Setup	40		nsec

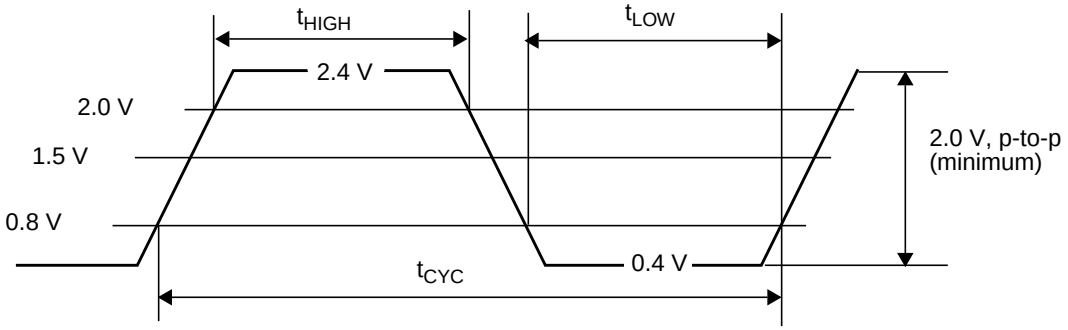


11.0 Device Characteristics (Continued)

11.2.5 PCICLK Timing Specifications

Symbol	Parameter	Min	Max	Units
t_{CYC}[1]	PCICLK Cycle Time	30	∞	ns
t_{HIGH}	PCICLK High Time	11		ns
t_{LOW}	PCCLK Low Time	11		ns
-	PCICLK Slew Rate[2]	1	4	V/ns

1. The PCI may have any clock frequency between nominal DC and 33 MHz. Device operational parameters at frequencies under 16 MHz may be guaranteed by design rather than by testing. The clock frequency may be changed at any time during the operation of the system as long as the clock edges remain “clean” (monotonic) and the minimum cycle and high and low times are not violated. The clock may only be stopped in a low state.
2. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock wavering as shown below.

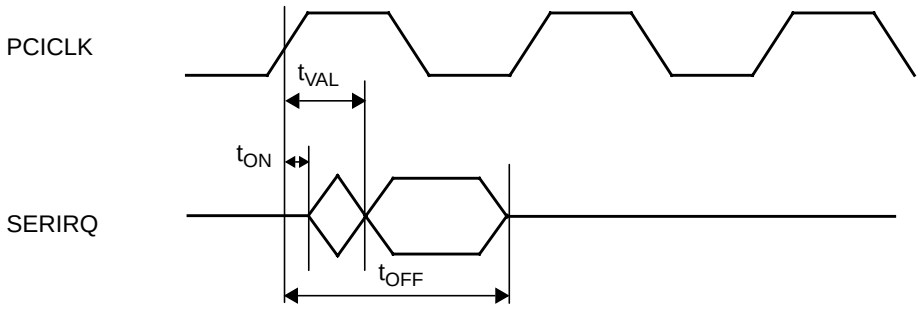


11.0 Device Characteristics (Continued)

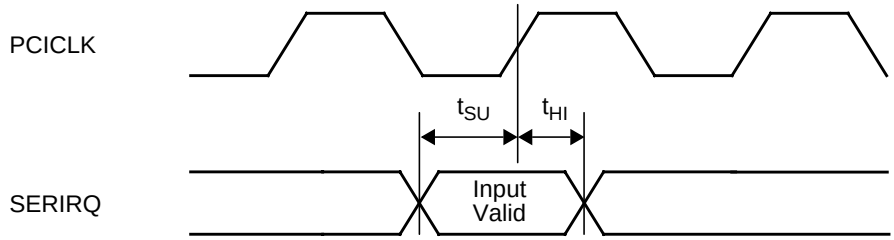
11.2.6 Serial IRQ Timing

Symbol	Description	Reference Conditions	Min (ns)	Max (ns)
t_{VAL}	Output Valid Delay	After RE PCICLK		11
t_{ON}	Float to Active Delay	After RE PCICLK	2	
t_{OFF}	Active to Float Delay	After RE PCICLK		28
t_{SU}	Input Setup Time	Before RE PCICLK	7	
t_{HI}	Input Hold Time	After RE PCICLK	0	

Output



Input

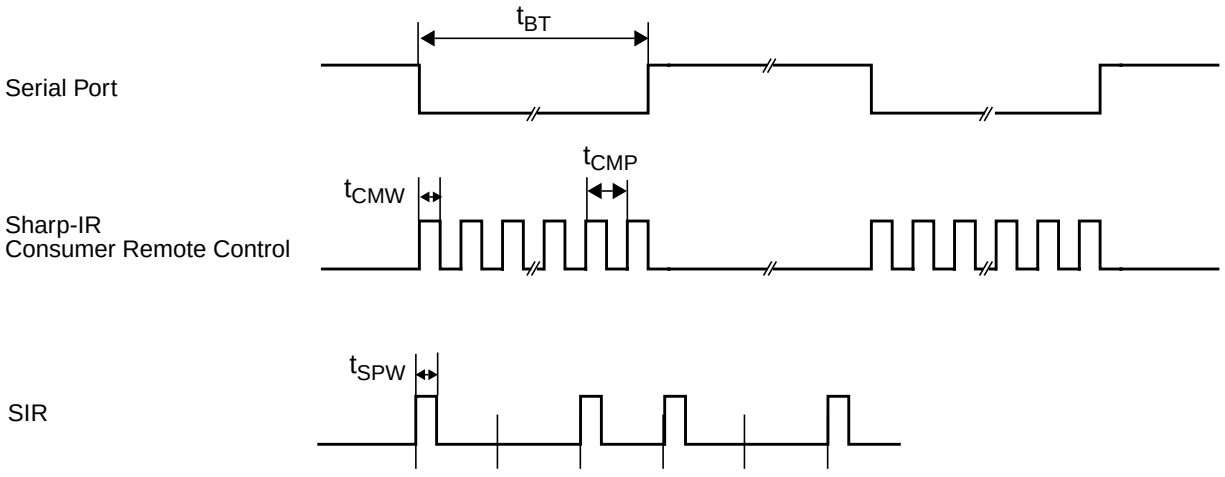


11.0 Device Characteristics (Continued)

11.2.7 Serial Port, Sharp-IR, SIR and Consumer Remote Control Timing

Symbol	Parameter	Conditions	Min	Max	Unit
t_{BT}	Single Bit Time in Serial Port and Sharp-IR	Transmitter	$t_{BTN} - 25$[1]	$t_{BTN} + 25$	nsec
		Receiver	$t_{BTN} - 2\%$	$t_{BTN} + 2\%$	nsec
t_{CMW}	Modulation Signal Pulse Width in Sharp-IR and Consumer Remote Control	Transmitter	$t_{CWN} - 25$[2]	$t_{CWN} + 25$	nsec
		Receiver	500		nsec
t_{CMP}	Modulation Signal Period in Sharp-IR and Consumer Remote Control	Transmitter	$t_{CPN} - 25$[3]	$t_{CPN} + 25$	nsec
		Receiver	t_{MMIN}[4]	t_{MMAX}[4]	nsec
t_{SPW}	SIR Signal Pulse Width	Transmitter, Variable	$(3/16) \times t_{BTN} - 15$[1]	$(3/16) \times t_{BTN} + 15$[1]	nsec
		Transmitter, Fixed	1.48	1.78	µsec
		Receiver	1.00		µsec
S_{DRT}	SIR Data Rate Tolerance. % of Nominal Data Rate.	Transmitter		± 0.87%	
		Receiver		± 2.0%	
t_{SJT}	SIR Leading Edge Jitter % of Nominal Bit Duration.	Transmitter		± 2.5%	
		Receiver		± 6.5%	

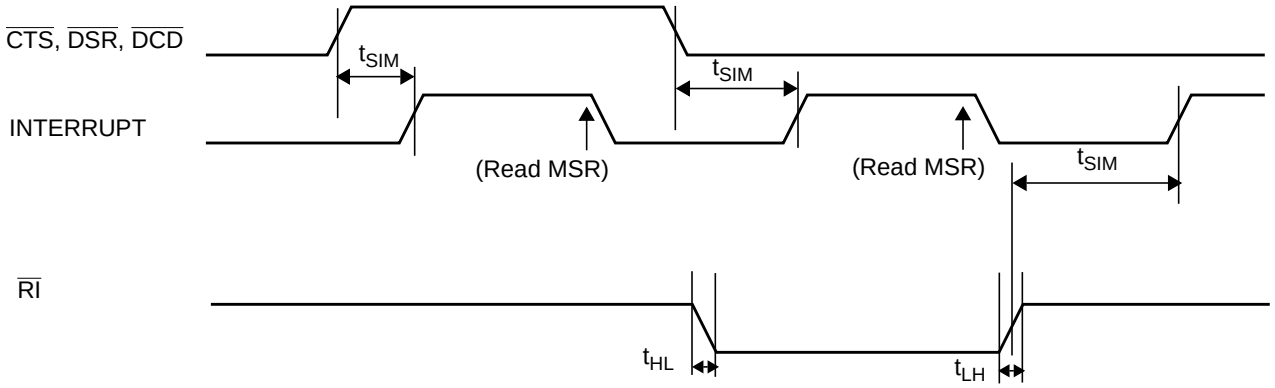
1. t_{BTN} is the nominal bit time in Serial Port, Sharp-IR, SIR and Consumer Remote Control modes. It is determined by the setting of the Baud Generator Divisor registers
2. t_{CWN} is the nominal pulse width of the modulation signal for Sharp-IR and Consumer Remote Control modes. It is determined by the MCPW field (bits 7-5) of the IRTXMC register and the TXHSC bit (bit 2) of the RCCFG register.
3. t_{CPN} is the nominal period of the modulation signal for Sharp-IR and Consumer Remote Control modes. It is determined by the MCFR field (bits 4-0) of the IRTXMC register and the TXHSC bit (bit 2) of the RCCFG register.
4. t_{MMIN} and t_{MMAX} define the time range within which the period of the incoming subcarrier signal has to fall in order for the signal to be accepted by the receiver. These time values are determined by the contents of register IRRXDC and the setting of the RXHSC bit (bit 5) of the RCCFG register



11.0 Device Characteristics (Continued)

11.2.8 Modem Control Timing

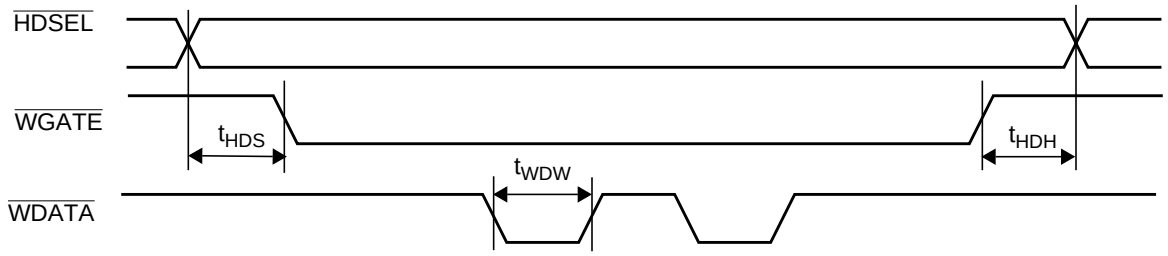
Symbol	Parameter	Min	Max	Unit
t_{HL}	$\overline{RI2,1}$ High to Low Transition	10		nsec
t_{LH}	$\overline{RI2,1}$ Low to High Transition	10		nsec
t_{SIM}	Delay to Set IRQ from Modem Input		40	nsec



11.2.9 FDC Write Data Timing

Symbol	Parameter	Min	Max	Unit
t_{HDH}	$\overline{HDSEL}$ Hold from $\overline{WGATE}$ Inactive[1]	750		µsec
t_{HDS}	$\overline{HDSEL}$ Setup to $\overline{WGATE}$ Active[1]	100		µsec
t_{WDW}	Write Data Pulse Width	See t_{DRP}, t_{ICP} and t_{WDW} values in table below		

1. Not tested. Guaranteed by design.



t_{DRP} t_{ICP} t_{WDW} Values

Data Rate	t_{DRP}	t_{ICP}	t_{ICP} Nominal	t_{WDW}	t_{WDW} Minimum	Unit
1 Mbps	1000	6 x t_{CP}[1]	125	2 x t_{ICP}	250	nsec
500 Kbps	2000	6 x t_{CP}[1]	125	2 x t_{ICP}	250	nsec
300 Kbps	3333	10 x t_{CP}[1]	208	2 x t_{ICP}	375	nsec
250 Kbps	4000	12 x t_{CP}[1]	250	2 x t_{ICP}	500	nsec

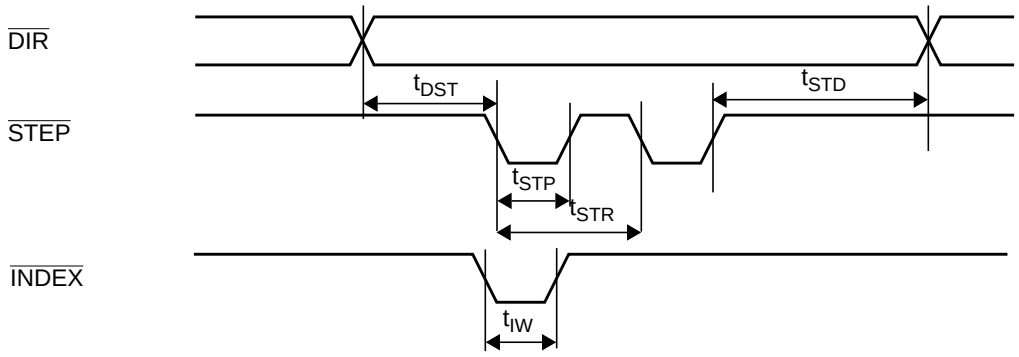
1. t_{CP} is the clock period defined in Section 11.2.2.

11.0 Device Characteristics (Continued)

11.2.10 FDC Drive Control Timing

Symbol	Parameter	Min	Max	Unit
t_{DST}	$\overline{DIR}$ Setup to $\overline{STEP}$ Active[1]	6		µsec
t_{IW}	Index Pulse Width	100		nsec
t_{STD}	$\overline{DIR}$ Hold from $\overline{STEP}$ Inactive	t_{STR}		msec
t_{STP}	$\overline{STEP}$ Active High Pulse Width[1]	8		µsec
t_{STR}	$\overline{STEP}$ Rate Time[1]	1		msec

1. Not tested. Guaranteed by design.



11.2.11 FDC - Read Data Timing

Symbol	Parameter	Min	Max	Unit
t_{RDW}	Read Data Pulse Width	50		nsec

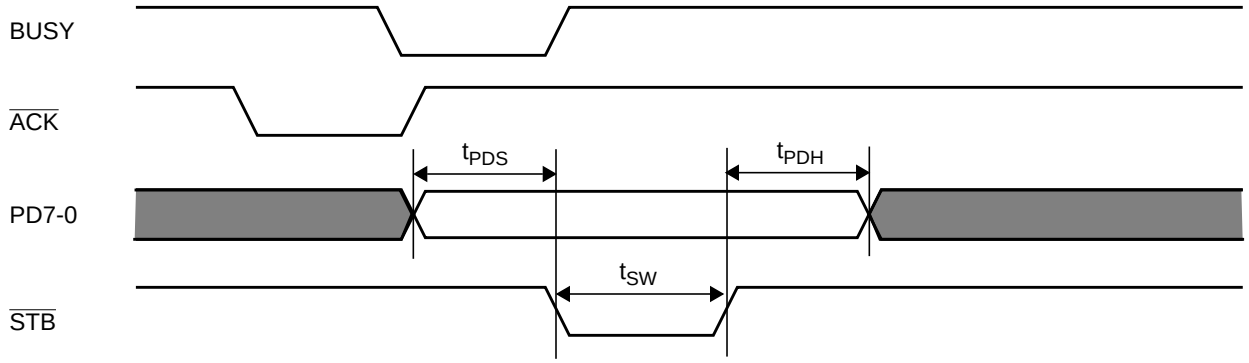


11.0 Device Characteristics (Continued)

11.2.12 Standard Parallel Port Timing

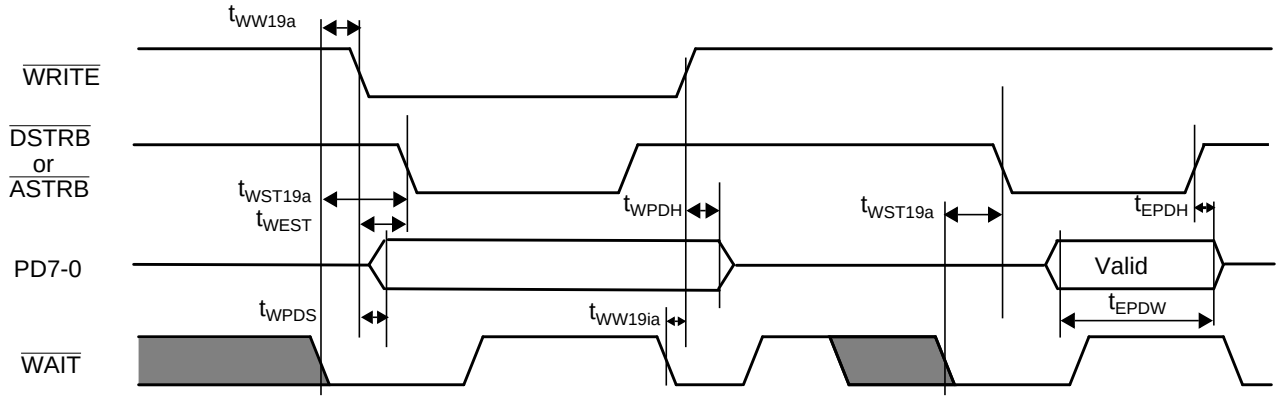
Symbol	Parameter	Conditions	Typ	Max	Unit
t_{PDH}	Port Data Hold	These times are system dependent and are therefore not tested.	500		nsec
t_{PDS}	Port Data Setup	These times are system dependent and are therefore not tested.	500		nsec
t_{SW}	Strobe Width	These times are system dependent and are therefore not tested.	500		nsec

Typical Data Exchange



11.2.13 Enhanced Parallel Port Timing

Symbol	Parameter	Min	Max	EPP 1.7	EPP 1.9	Unit
t_{WW19a}	WRITE Active from WAIT Low		45		✔	nsec
t_{WW19ia}	WRITE Inactive from WAIT Low		45		✔	nsec
t_{WST19a}	DSTRB or ASTRB Active from WAIT Low		65		✔	nsec
t_{WEST}	DSTRB or ASTRB Active after WRITE Active	10		✔	✔	nsec
t_{WPDH}	PD7-0 Hold after WRITE Inactive	0		✔	✔	nsec
t_{WPDS}	PD7-0 Valid after WRITE Active		15	✔	✔	nsec
t_{EPDW}	PD7-0 Valid Width	80		✔	✔	nsec
t_{EPDH}	PD7-0 Hold after DSTRB or ASTRB Inactive	0		✔	✔	nsec

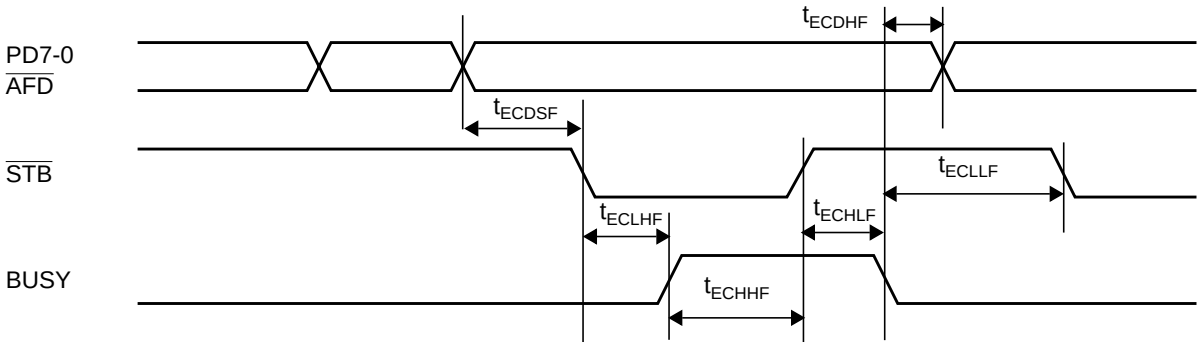


11.0 Device Characteristics (Continued)

11.2.14 Extended Capabilities Port (ECP) Timing

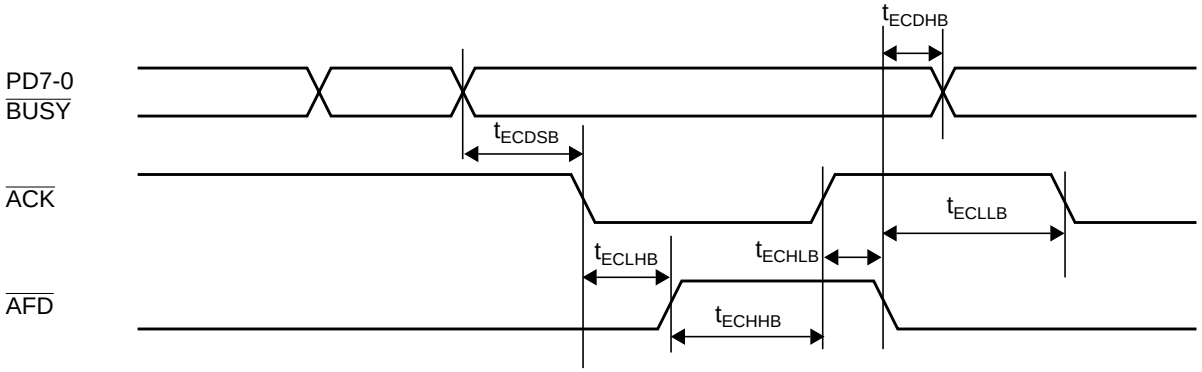
Forward Mode

Symbol	Parameter	Min	Max	Unit
t_{ECDSF}	Data Setup before $\overline{STB}$ Active	0		nsec
t_{ECDHF}	Data Hold after BUSY Inactive	0		nsec
t_{ECLHF}	BUSY Active after $\overline{STB}$ Active	75		nsec
t_{ECHHF}	$\overline{STB}$ Inactive after BUSY Active	0	1	sec
t_{ECHLF}	BUSY Inactive after $\overline{STB}$ Active	0	35	msec
t_{ECLLF}	$\overline{STB}$ Active after BUSY Inactive	0		nsec



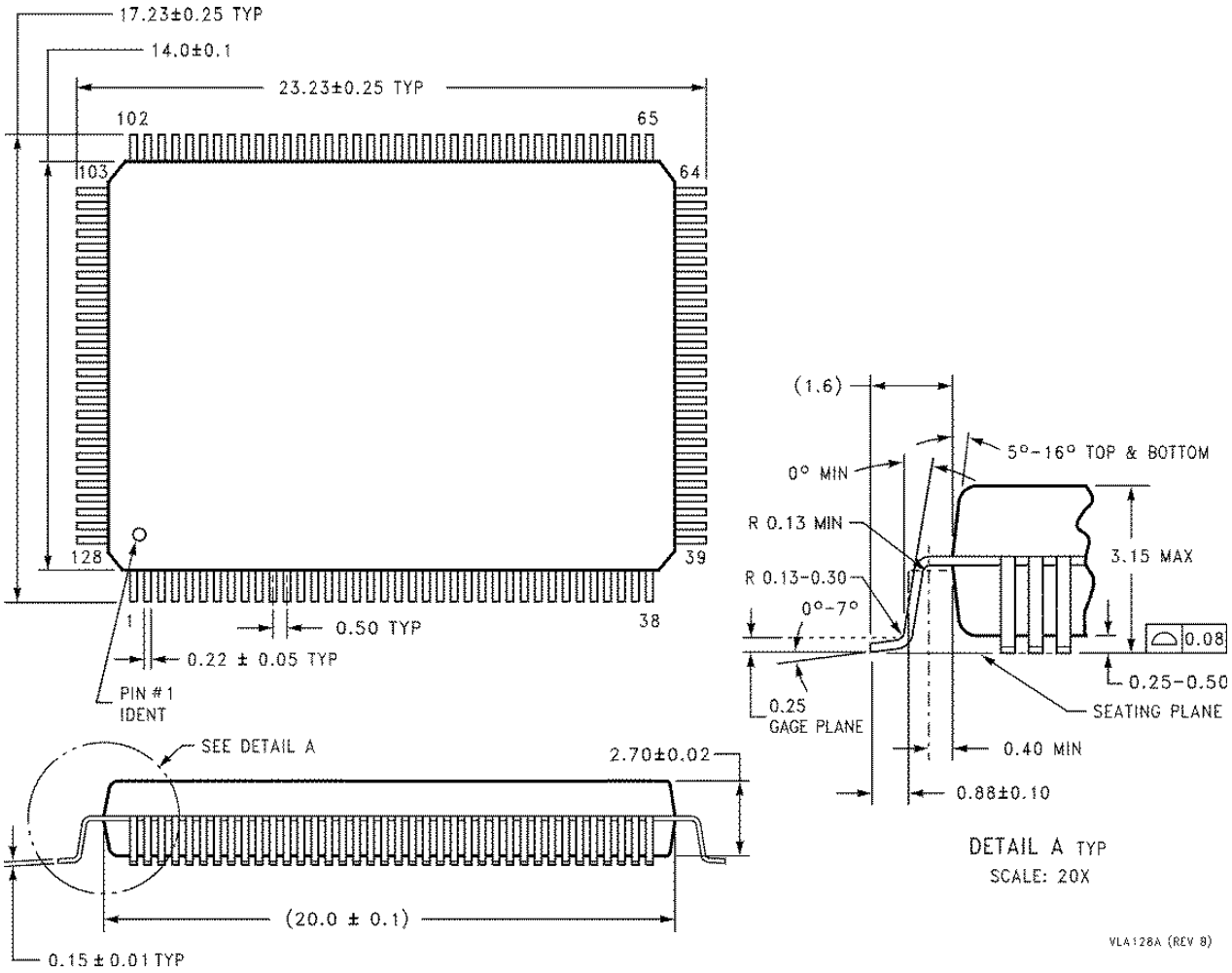
Reverse Mode

Symbol	Parameter	Min	Max	Unit
t_{ECDSR}	Data Setup before $\overline{ACK}$ Active	0		nsec
t_{ECDHR}	Data Hold after $\overline{AFD}$ Active	0		nsec
t_{ECLHR}	$\overline{AFD}$ Inactive after $\overline{ACK}$ Active	75		nsec
t_{ECHHR}	$\overline{ACK}$ Inactive after $\overline{AFD}$ Inactive	0	35	msec
t_{ECHLR}	$\overline{AFD}$ Active after $\overline{ACK}$ Inactive	0	1	sec
t_{ECLLR}	$\overline{ACK}$ Active after $\overline{AFD}$ Active	0		nsec



Physical Dimensions

All dimensions are in millimeters



Plastic Quad Flatpack (PQFP), JEDEC
Order Number PC87351-xxx/VLA
NS Package Number VLA128A

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