Freescale Semiconductor
User Guide

PBMCUSLKUG
Rev. 1, 7/2007

MCU PROJECT BOARD STUDENT LEARNING KIT (PBMCUSLK)

Prototyping Board with Microcontroller Interface

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REVISION

Date	Rev	Comments
December 5, 2006 July 17, 2007	0 1	Initial Release. Added LCD information (part no., and more info. URLs)

CAUTIONARY NOTES

Electrostatic Discharge (ESD) prevention measures should be used when handling this product. ESD damage is not a warranty repair item.

Axiom Manufacturing does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under patent rights or the rights of others.

3) EMC Information on the PBMCUSLK:

1. This product as shipped from the factory with associated power supplies and cables, has been verified to meet with requirements of CE and the FCC as a CLASS A product.

2. This product is designed and intended for use as a development platform for hardware or software in an educational setting or a professional laboratory.

3. In a domestic environment, this product may cause radio interference. In this case, the user is required to take adequate prevention measures.

4. Attaching additional wiring to this product or modifying the products operation from the factory default as shipped may effect its performance and cause interference with nearby electronic equipment. If such interference is detected, suitable mitigating measures should be taken.

TERMINOLOGY

This prototyping module uses option selection jumpers to setup configuration. Terminology for use of the option jumpers is as follows:

Jumper – a plastic shunt that connects 2 terminals electrically

Jumper on, in, or installed - jumper is installed such that 2 pins are connected together

Jumper off, out, or idle - jumper is installed on 1 pin only. It is recommended that jumpers be idled by installing on 1 pin so it will not be lost.

FEATURES

The PBMCUSLK is a full-featured prototyping platform intended for interfacing and programming Freescale MCU development modules in an educational environment. A line of HC(S)12(X), HC(S)08, DSP, and ColdFire modules plug directly into the project board. Other MCU boards can be interfaced directly to the project board by ribbon cable. The PBMCUSLK may also be used as an electronic circuit prototyping environment without MCU support. The project board has been specifically designed for compatibility with the National Instruments Educational Laboratory Virtual Instrumentation Suite (NI-ELVIS). An integrated USB BDM POD has been provided to allow the user to program, erase, and debug supported Freescale MCU modules. Features include:

- Large, Replaceable, Solderless Breadboard Area
- Integrated HC(S)12(X)/HCS08 Multilink BDM
  - Allows debugging target processor via background debug mode
  - Provides all necessary signals to target processor
  - USB port connection
- 60-pin MCU Interface Connector, break-out on both ends of prototype area
- PCI Style Card-Edge connector designed for use with National Instrument's NI-ELVIS platform
- Signal Breakout arranged logically around Breadboard Area
- Power Input from included wall-plug transformer, integrated USB-BDM, or from NI-ELVIS workstation
- On-board voltage regulators provide 4 different voltage levels
  - 5VDC @ 500mA
  - 3.3VDC @ 500mA
  - +15VDC @ 50mA
  - –15VDC @ 50mA
  - NOTE: ± 15V is not available when powered from USB-BDM
  - LED indicators for each voltage level
- User selectable voltage to on-board logic devices
  - Option jumper to enable voltage output to MCU Port Connector
- 2 Banana Connectors
- 1 BNC Connector
- 8-pin Keypad connector
- 1 Single-turn User Potentiometer
  - Connected to MCU_PORT connector w/ separate enable
- 8-character x 2-line LCD panel
  - Fixed and Variable Contrast
  - Selectable Chip Select
  - Option header to disconnect signal lines
- COM Port
  - 9-pin DSUB connector
  - RS-232 Interface with option to isolate transceiver
  - COM_SEL jumper selects configuration between:
    - RS-232 signals to transceiver
    - MON08 Interface Port
  - Access to COM signals at Signal Breakout Connector
- Socket for Optional Crystal Oscillator
  - User selectable output amplitude - 5V or 3.3V
- 8 Active-High Green LED's, Buffered, with enable
  - 4 LED's connected to MCU_PORT connector w/ separate enable
- 8 Active-Low Push Button Switches
  - 4 Push Button Switches connected to MCU_PORT connector w/ separate enable
- 8 Active-High DIP Switches,
- 1 External-drive Buzzer
  - Connected to MCU_PORT connector w/ separate enable
  - Mounting hole placement allows the student to carry the Project Board in a standard 3-Ring binder.

Specifications:

Module Size: 8.5" x 11"

Power Input: +9V @ 1.2A typical

REFERENCES

Reference documents are provided on the support CD in Acrobat Reader format. More information can be found in the Application Notes section of the Freescale Web site.

PBMCUSCHEMSLKREVB.pdf	PBMCUSLK Schematic, Rev B
PBMCUSLKUG.pdf	PBMCUSLK User Guide (this document)
LCD Commands.pdf	Commands for use with Project Board LCD display

Refer to http://www.femacorp.com for the following

LCD Data Sheet (P/N CM0826)	Datasheet for use with the Project Board LCD display

NOTE
Quick Start Guides for using the project board in conjunction with Freescale Student Learning Kit microcontrollers can be found at the following URL www.freescale.com\universityprogram or on the included support CD.

Visit www.freescale.com\universityprogram for current product information, reference materials and updates.

GETTING STARTED

To get started quickly, please refer to the Quick Start Guide of your microcontroller prefixed with PB included on the Support CD. The quick start will show the user how to configure the board for use with the MCU application module. The quick start will also show the user how to install the latest version of Freescale CodeWarrior software tools and how to create, build, and debug a simple application.

NOTE
Install the CodeWarrior Development Studio tools and all applicable patches before attempting to connect the PBMCUSLK to a host PC.

OPERATION

The PBMCUSLK allows quick and easy prototype of electronic circuits with, or without MCU support. A variety of commonly used circuits are pre-installed, configurable and ready for use. Dual-row header sockets placed around the prototyping area provide convenient access to all

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on-board features. Connections between these signals and the breadboard are made using solid, 22ga, jumper wire connected to the proper socket header location. A package of jumper wires is included with the project board. The sections below describe, in detail, the functionality of the PBMCUSLK.

POWER

The PBMCUSLK may be used as a stand-alone prototyping platform or in conjunction with the NI-ELVIS platform. The project board will accept power input from the included wall-plug transformer or from the NI-ELVIS workstation. The project board may also be powered from the integrated USB BDM.

CAUTION
Exercise care when configuring power input and output selections to prevent damage to the project board or connected circuitry.

Input Sources

The PBMCUSLK provides the user 4 discrete working voltage levels: 5V, 3.3V, +15V, and -15V. The 5V and the ±15V rails have multiple input sources while the 3.3V rail is derived from the 5V rail in all configurations. Option headers JP1 (P_SELA), JP2 (PSEL_B), and JP3 (VDD_SEL) configure power routing on the project board. See the Input Selection section below for details on setting up power configuration for the project board.

The 5V rail is driven from one of three input sources, the barrel connector (VIN), the integrated USB BDM, or the NI-ELVIS workstation (J1). The barrel connector input at VIN accepts a 2.1mm, center-positive, barrel plug, allowing power to be supplied by a transformer or desktop power supply. Input voltage on VIN must be kept between +8V and +12V for proper operation. Typical input is +9V. Although VR1 will accept inputs to 20V, increasing the input voltage will increase the voltage drop across the part. This may lead to excessive temperatures causing the part to shut down.

The 5V rail is derived from the on-board voltage regulator at VR1. VR1 supplies a maximum of 1A of current to the project board. The regulator features over-current and over-temperature protection. The regulator will automatically shut down if current or temperature exceeds rated specifications.

The integrated USB BDM drives the 5V rail directly from the USB bus. Note that when powering the project board from the integrated USB BDM, **total** current drain must not exceed **500mA**. Total current drain includes the BDM circuit, all enabled project board circuitry, any attached MCU module, and any additional prototype circuitry connected to the project board. Excessive current drain will violate the USB specification and will cause the USB bus to shutdown.

When attached to the NI-ELVIS workstation, the 5V rail is driven through connector J1 from the workstation. Refer to the NI-ELVIS workstation user manual for further details.

The 3.3V rail is supplied from an on-board regulator located at VR2. The VR2 input is connected to the 5V input through selection header PSEL_B. VR2 supplies a maximum of 500mA of current to the project board. The 3.3V regulator also features over-current and over-temperature protection.

The ±15V rails are supplied from either an on-board boost regulator at PS1 or the NI-ELVIS workstation through connector J1. The PS1 input is derived from VIN connector through the regulator at VR1. If powered from VIN and an external power supply, current on the ±15V rails is limited to 50 mA. In this configuration, PS1 will consume 500mA of current output from VR1. If powered from the NI-ELVIS workstation, the ± 15V rails are provided directly from the workstation. The workstation will provide a maximum current on the ±15V rails of 500 mA. The PS1 voltages and the J1 voltages are diode OR'ed to prevent component damage.

Total current available is dependent on the configuration chosen and the load placed on each voltage rail. For instance, consider the following setup. The project board is powered from a transformer connected to VIN. A 50mA load is placed on the +15V and the –15V rails for the analog portion of the circuit. Additionally, a 500mA load is placed on the 3.3V rail. In this configuration, any load placed on the 5V rail will cause an over-current condition in regulator VR1.

Table 1 below lists current limits for each voltage rail in different input configurations. Each current limit shows the maximum provided except in the case of the USB input. The USB input assumes the USB circuitry consumes 200mA of peak current. It is the users responsibility to ensure current limits are not exceeded in any configuration.

Table 1: Current Limits

POWER LIMITS	USB	5V, 300mA
		3.3V, 200mA
		N/A
	VIN	5V, 500mA
		3.3V, 500mA
		±15V, 50mA
	J1	5V, 500mA
		3.3V, 500mA
		±15V, 500mA
		±12V, 500mA

Total current drain from USB bus **must not** exceed 500 mA. Excessive current drain will violate the USB specification.

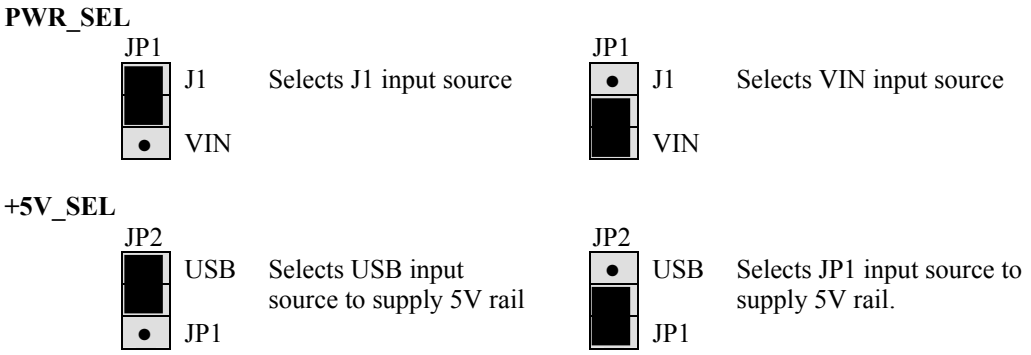
NOTE: 3.3V rail is derived from 5V rail for all inputs. Total current available on 3.3V rail is limited by total current available on 5V rail.

Input Selection

The PBMCUSLK sources power from the VIN barrel connector, the USB BDM, or connector J1. The barrel connector is situated on the project board to prevent connection of an external power supply while connected to the NI-ELVIS workstation. Two selection headers determine the source of input power to the project board. These selection headers are situated to prevent selecting 2 input power sources at the same time.

Selection headers PWR_SEL(JP1) and +5V_SEL (JP2)* illustrated in figure 1 select which input source to supply power to the project board. PWR_SEL selects either connector VIN or connector J1 as an input source. +5V_SEL selects either the output of PWR_SEL(JP1) or the USB BDM as an input source. The output of PWR_SEL connects directly to pin 3 of +5V_SEL. The output of +5V_SEL drives the 5V rail and the input of the 3.3V regulator, VR2.

Figure 1: Input Power Select



Power input on the barrel connector is supplied by the included wall-plug transformer or a desktop power supply. Input voltage on this connector should be between +8V and +12V. Higher input voltages may cause excessive heating and force VR1 into thermal shutdown.

Power input from the USB connector is drawn from the USB bus. Care must be exercised not to draw too much power when connected to the USB bus. USB2.0 specifications limit the total current drain from the bus to less than 500mA. Exceeding this limit will cause the USB device to disconnect and may damage the project board or host PC.

VDD Selection

The operating voltage level VDD supplies all on-board logic devices on the PBMCUSLK. An option header allows the user to set VDD at either 5V or 3.3V.

When the project board is connected to a wall-plug transformer, voltage regulator VR1 provides the 5V rail and regulator VR2 provides the 3.3V rail. Regulator VR1 is rated for a

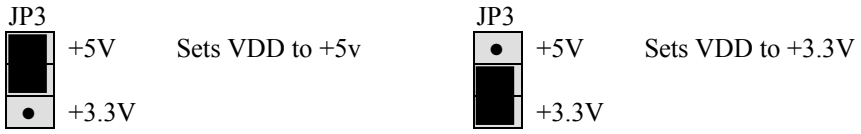
* For project boards labeled MCU Project Board -2 AXM-0368 Rev C these jumpers are labeled PSEL_A and PSEL_B respectively.

maximum current output of 1A while regulator VR2 is rated for a maximum current output of 500mA. In this configuration, ±15V is provided by the regulator at PS1. Both PS1 and VR2 derive their input from VR1. This setup may limit available current in mixed voltage applications. Each regulator is internally current limited to prevent damage from inadvertent, short circuits of **short duration**. The regulator at PS1 is not protected from continuous short-circuits on its output.

When connected to NI-ELVIS, the 5V rail is provided by the workstation. This input also drives the 3.3V regulator at VR2. ±15V is available from the workstation and PS1 is not connected.

A 3-pin option header, VDD_SEL(JP3) shown in figure 2 allows the user to select the operating voltage routed to VDD. The 5V selection routes 5VDC to on-board logic while the 3.3V selection routes 3.3VDC to on-board logic. All voltage levels are conveniently arranged around the prototype area to allowing easy access. ±15V voltage inputs are diode OR'ed and available at connector J4.

Figure 2: VDD _SEL Option Header



CAUTION: **Exercise care to select the correct operating voltage when interfacing to on-board logic to prevent damaging circuit elements.**

±15V Power

The PBMCUSLK includes a DC-DC converter at PS1 to supply ±15V for use in analog circuit construction and analysis. PS1 provides a maximum of 50mA on each output. PS1 draws its input from the +5V rail. The option header 15V_EN* (JP11) shown in table 2 disables the output if not needed. Disabling PS1 when not used conserves power and will prolong the life of the +5V LDO at VR1.

Table 2: 15V_EN Option Header

Shunt	Effect
ON	Enables PS1 output to the project board
OFF	Disables PS1 output to the project board

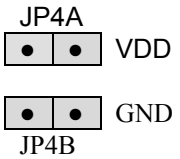
* For project boards labeled MCU Project Board -2 AXM-0368 Rev C this jumper is labeled PS1_EN.

MCU Module Power

The PBMCUSLK may optionally power modules attached to the MCU_PORT connectors. Two, 2-pin jumpers MODULE_POWER VDD(JP4A) and GND(JP4B) enable or disable power and ground to the MCU_PORT pins as illustrated in figure 3. Installing shunts at positions labeled VDD and GND connects MCU_PORT, pin 1 to VDD and MCU_PORT, pin 3 to GND.

NOTE
To complete the circuit, both shunts must be installed. If not used, both shunts should be removed.

Figure 3: MOD_PWR Option Header



Placing a shunt on JP4A routes VDD to MCU_PORT-1.

Placing a shunt on JP4B routes GDN to MCU_PORT-3

CAUTION
When using this option selection make sure the module connected to the MCU_PORT is not configured to source voltage to the project board. Damage to both the project board and attached module may result.

Integrated USB BDM

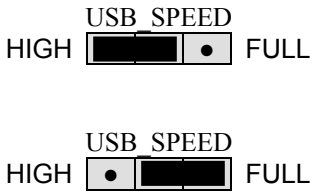
The PBMCUSLK board features an integrated USB Background Debug Mode (BDM) from P&E Microcomputer Systems. The integrated BDM possesses all the necessary signals to support application development and debugging. A USB type B connector provides connection from the target board to the host PC. Communication and control signals (BGND, RESET*) are connected directly to the MCU_PORT connections. This arrangement allows the user to program and debug Freescale HCS08 and HCS12 Application Modules Student Learning kits without the need for external wiring.

The integrated USB BDM provides 5V power and ground to the target board eliminating the need to power the board through VIN or J1. Power provided by the integrated BDM is derived from the USB bus. Total current consumption for the project board, and connected circuitry, must not exceed **500mA**. This is the current supplied by the USB cable to the BDM, target board, and any connected circuitry. Excessive current drain will violate the USB specification causing the USB bus to shutdown.

USB Speed

The communications speed over the USB bus is controlled by the J301 (USB_SPEED) header illustrated in figure 4. When shipped from the factory, the board is configured for high-speed operation. If the user encounters a communication failure, or erratic behavior, USB communication speed may be reduced by setting this option jumper to Full. Slowing the communications rate often resolves any problem encountered.

Figure 4: USB_SPEED Option Header



Configuration:
Selects USB High-speed communications

Selects USB Full-speed communications

CAUTION: Do not allow total current drain to exceed 500mA when powered from the USB BDM.

BDM Voltage

The integrated BDM is designed to interface with either 5V or 3.3V circuits. The VDD level selected on the PBMCUSLK is fed back to the BDM to set output drive levels. The VDD level is selected by VDD_SEL(JP3) option header. Further details on operating voltage selection may be found in the POWER section above.

As noted above, **total** current drain from the integrated BDM must not exceed **500mA.** Excessive current drain will violate the USB 2.0 specification causing the USB bus to shutdown.

User I/O

The PBMCUSLK provides an array of User I/O to allow connection of auxiliary components such as signal input, test equipment, Keypads, or LCD displays. Many of these user features are by default enabled, but can be disconnected through jumper settings. This section describes each of the features in detail, for more information on configuring these features please view the Connected Features section.

LCD Display

The PBMCUSLK includes* an 8-char x 2-line LCD module to support application development requiring character display output. The LCD display is manufactured by FEMA Electronics Corporation, part number CM0826.

LCD PORT

The display is connected by default to the MCU PORT pins through jumpers allowing direct interface to Freescale line of plug-in application modules designed by Axiom Manufacturing. The PBMCUSLK also provide 2 additional LCD connectors to support larger displays. To utilize an alternate display, the installed display must be removed and the correct header installed. The PBMCULSK supports STN, Reflective displays up to 20-char x 4-lines.

The contrast is selectable by the user between either a Fixed Mode or Adjustable Mode. The fixed mode is pre-set to a contrast easily viewable in ambient, indoor lighting. The adjustable mode allows the user to lighten or darken the contrast using the project board potentiometer.

The LCD setup does not support current cursor position read-back.

LCD Port Connectors

The LCD control and data signals can be directly connected to the MCU_PORT I/O headers. The signal arrangement is designed to coincide with the SPI port of Freescale line of plug-in application modules designed by Axiom Manufacturing. To provide maximum flexibility, the select signal SS* has been connected to both a dedicated SS* output and to a GPIO signal on the MCU application module. An option header at SS*, selects the select signal source. An option header at LCD_EN allows the user to isolate the LCD module from the MCU_PORT signal lines. To prevent signal corruption when using the SPI signals as general purpose I/O, the user should remove the shunts on LCD_EN and SS* option headers.

* LCD is not included with older MCUSLK project boards which can be identified with the labeling “MCU Project Board” on the board. The connections are available on this series of boards. However, to use one must separately purchase and LCD and connect it to the project board.

Figure 5, depicts the pin out and signals for the LCD_PORT connector.

Figure 5: LCD_PORT – J13

GND	1	2	VDD
CONTRAST	3	4	RS
R/W*	5	6	EN
DB0	7	8	DB1
DB2	9	10	DB3
LCD_D4	11	12	LCD_D5
LCD_D6	13	14	LCD_D7

SPI data bit definitions to LCD Port:
LCD_D[7..4] – LCD data bits D[3..0]
DB[3..0] – Unused, 10K ohm pull-downs installed
R/W – Read/Write pin, set to 0 volts, Read only
EN – LCD enable input, 1 = LCD enable
CONTRAST – LCD contrast input
RS – Register Select, 0 = LCD Command, 1 = LCD Data

Connector J8 illustrated in figure 6 allows the use of alternate displays up to 20-char x 4-lines. This header is not installed in default configurations. Connector J8 is a mirror image of the LCD_PORT connector.

Figure 6: J8 – Aux. LCD Connector

5V	2	1	GND
RS	4	3	CONSTRAST
EN	6	5	R/W*
DB1	8	7	DB0
DB3	10	9	DB2
LCD_D5	12	11	LCD_D4
LCD_D7	14	13	LCD_D6

SPI data bit definitions to LCD Port:
LCD_D[7..4] – LCD data bits D[3..0]
DB[3..0] – Unused, 10K ohm pull-downs installed
R/W – Read/Write pin, set to 0 volts, Read only
EN – LCD enable input, 1 = LCD enable
CONTRAST – LCD contrast input
RS – Register Select, 0 = LCD Command, 1 = LCD Data

Connector J8 illustrated in figure 7 allows the use of alternate displays up to 20-char x 4-lines. This header is not installed in default configurations.

Figure 7: J9 – Aux. LCD Connector

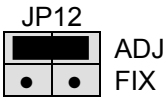
GND	1
5V	2
CONTRAST	3
RS	4
R/W*	5
EN	6
DB0	7
DB1	8
DB2	9
DB3	10
LCD_D4	11
LCD_D5	12
LCD_D6	13
LCD_D7	14

SPI data bit definitions to LCD Port:
LCD_D[7..4] – LCD data bits D[3..0]
DB[3..0] – Unused, 10K ohm pull-downs installed
R/W – Read/Write pin, set to 0 volts, Read only
EN – LCD enable input, 1 = LCD enable
CONTRAST – LCD contrast input
RS – Register Select, 0 = LCD Command, 1 = LCD Data

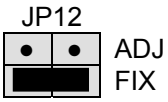
LCD Contrast

The PBMCUSLK offers two methods for controlling the LCD panel contrast, fixed or adjustable, controlled through jumper CONTRAST(JP12) as illustrated in figure 8. The fixed option provides near maximum contrast and supports all STN, Reflective, type LCD panels. The fixed mode is pre-set to a contrast easily viewable in ambient, indoor lighting. The adjustable option allows the use on the project board potentiometer to vary the contrast voltage applied to the LCD panel. This allows the user to apply temperature or lighting compensation if needed.

Figure 8: Contrast Select – JP12



Selects on-board POT to allow adjustment of LCD contrast voltage.

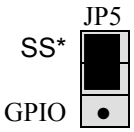


Selects fixed LCD contrast voltage.

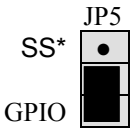
LCD Select

To allow maximum flexibility, the control signal used to transfer data to the LCD panel is selectable. Option header SS_SEL*, described in figure 9, selects between the SPI port SS* signal or the GPIO signal connected to MCU_PORT-25.

Figure 9: SS_SEL Option Header



Selects dedicated SS input source



Selects GPIO signal on MCU_25

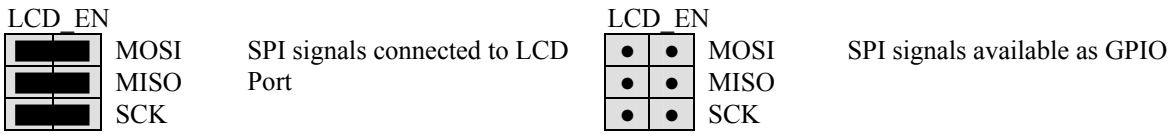
NOTE
To prevent signal corruption when using the SPI signals as GPIO, the user should idle the SPI circuitry by removing the SS* jumper.

* For project boards labeled "MCU Project Board -2 AXM-0368 Rev C" this jumper is labeled SS*.

LCD Enable

The LCD_EN* option header illustrated in figure 10 allows module SPI signals to be used as general purpose I/O if needed. To use the SPI signals as general purpose I/O, simply remove the shunts at this option header.

Figure 10: LCD_EN Option Header



Oscillator Socket

The PBMCUSLK provides a socket for an optional clock oscillator. The socket is configured to accept either 8-pin or 14-pin canned clock oscillators. An AMPL† option jumper described in table 3 allows the use of 5V oscillators to drive 3.3V circuits. Removing the option jumper routes the clock output through a simple voltage divider thereby reducing the output amplitude. Installing the option jumper allows a 5V, peak, clock output. This output is routed to the signal breakout header located adjacent to the breadboard.

Table 3: AMPL Option Header

Shunt	Effect
ON	Oscillator Output at Full Amplitude – $5V_{PP}$
OFF	Oscillator Output at Reduced Amplitude – $3.3V_{PP}$

Switches

The PBMCUSLK provides two types of switches for use as input devices. Eight normally open push button switches

voltage level while in the inactive state.

PUSHBUTTON SWITCHES

Each push button switch is configured for active-low operation. When pressed (closed) the associated signal line is pulled to GND through a 1 kΩ, current-limit resistor. A 10k ohm resistor pulls each signal line to VDD when the switch is released (open). Each push-button switch output is routed to the signal breakout header labeled "USER I/O PB[1..7]" located adjacent to the breadboard. Four push-button switches are connected directly to the MCU_PORT connector, see "Connected Features" section below for details.

* Not applicable for project boards labeled "MCU Project Board"
† For project boards labeled "MCU Project Board -2 AXM-0368 Rev C" this jumper is labeled OSC_OPT.

DIP SWITCHES

Each DIP switch is configured for active-high operation. When ON (closed), each switch leg is individually pulled to VDD through a 100 Ω series, current limit resistor. A 10k ohm resistor pulls each signal line to GND when the switch is OFF (open). Each DIP switch output is routed to the signal breakout header labeled "USER I/O SW[1..7] located adjacent to the breadboard.

LED's

The PBMCUSLK provides 8, green LED's, for use as output indicators. Each LED is configured for active-high operation. Each LED is individually driven by an ACT buffer allowing either 5V or 3.3V input levels. The input level is determined by VDD selection. A 10K ohm resistor holds each buffer input low to prevent inadvertent LED activation. The LED buffer driver may be disabled by removing the shunt at LED_EN as illustrated in table 4. LED inputs are routed to the signal breakout header located adjacent to the breadboard. Four LED's are connected directly to the MCU_PORT connector. See the "Connected Features" section below for details.

Table 4: LED_EN Option Header

Shunt	Effect
ON	Enable LED Output
OFF	Disable LED Output

Keypad

The KEYPAD connector shown in figure 11 supports connection of a passive 12-key or 16-key keypad. The KEYPAD connector is routed directly to the signal breakout header labeled KEYPAD located adjacent to the breadboard. No current-limit is provided on this connection and should be provided by the user if required.

Figure 11: Keypad Connector

KEYPAD 8	8
KEYPAD 7	7
KEYPAD 6	6
KEYPAD 5	5
KEYPAD 4	4
KEYPAD 3	3
KEYPAD 2	2
KEYPAD 1	1

These signal connect directly to the User I/O signal breakout connector located below the breadboard.

Potentiometer

The PBMCUSLK provides a single-turn, 5K ohm trim potentiometer for use in circuit prototyping. Most commonly, the POT may be used to provide analog input signals to the microcontroller. This signal is routed to the signal breakout header labeled “USER I/O POT” located adjacent to the breadboard. A bypass capacitor on the output provides minimal smoothing on the POT signal.

The POT is configured as a Connected Feature. See Connected Features section below for details.

Banana Jack

The PBMCUSLK provides two 4.0mm banana jacks for use as auxiliary I/O. These connectors may be used for auxiliary signal input or for signal output to test equipment. The banana jacks are color-coded, red, and black. The center conductor of each jack is routed to the User I/O Signal Breakout connector labeled USER I/O BANANA [A..B] located adjacent to the breadboard area.

BNC Jack

The PBMCUSLK provides one BNC jack for use as auxiliary I/O. This connector may be used for auxiliary signal input or for signal output to test equipment. The center conductor (BNC+) and shield (BNC-) are routed separately to the User I/O Signal Breakout connector labeled USER I/O BNC[+/-] located adjacent to the breadboard area. For proper operation, both signals must be connected. For most circuit configurations, BNC- should be connected to GND.

Connected Features

To simplify circuit construction and emphasize software development, several user features have been connected to the MCU_PORT through FET switches and jumpers. The FET switches are controlled by enable signals that are also routed to the MCU_PORT header. This setup allows the user to electronically connect and disconnect each connected feature group. A 6-position jumper (UFEA or JP10) allows the user to disconnect the enable signal if applying the associated port to other uses. Connected Features include a POT, 4 push-button switches, and 4 LED’s. Each feature group function is more fully described elsewhere in this User Guide.

POT

The POT signal is routed to MCU_PORT-20 through a FET switch. This feature is controlled by a GPIO port signal on MCU_PORT-32 allowing the user to enable or disable this feature under MCU control. An option header at UFEA isolates this enable signal allowing the user to apply the GPIO signal for other uses.

Table 5: POT Connections

FEATURE	CONNECTION
POT VALUE	MCU_PORT – 20
POT ENABLE	MCU_PORT - 32
OPTION JUMPER	UFEA -4 (POT)

PUSH-BUTTON SWITCHES

PB1 – PB4 are connected the MCU_PORT through a FET bus switch. This feature is controlled by a GPIO port signal connected to MCU_PORT-36 allowing the user enable or disable this feature under MCU control. An option header at UFEA isolates this enable signal allowing the user to apply the GPIO signal for other uses.

Table 6: PB Switch Connections

FEATURE	CONNECTION
PB1 VALUE	MCU_PORT – 9
PB2 VALUE	MCU_PORT – 11
PB3 VALUE	MCU_PORT – 29
PB4 VALUE	MCU_PORT – 31
PB ENABLE	MCU_PORT – 36
OPTION JUMPER	UFEA -2 (PB)

LED's

LED1 – LED4 are connected the MCU_PORT through a FET bus switch. This feature is controlled by a GPIO port signal connected to MCU_PORT-34 allowing the user enable or disable this feature under MCU control. An option header at UFEA isolates this enable signal allowing the user to apply the GPIO signal for other uses.

Table 7: LED Connections

FEATURE	CONNECTION
LED1 VALUE	MCU_PORT – 33
LED2 VALUE	MCU_PORT – 35
LED3 VALUE	MCU_PORT – 37
LED4 VALUE	MCU_PORT - 39
LED ENABLE	MCU_PORT - 34
OPTION JUMPER	UFEA -3 (LED)

Buzzer

The PBMCUSLK features an external drive buzzer for audible applications. The buzzer is connected to a TIMER / PWM port on all current MCU modules. The buzzer is connected directly to the MCU _PORT connector at MCU_PORT – 13 and does not require an enable signal similar to the other Connected Features. The buzzer is connected to the MCU_PORT through an option header at UFEA -2 (PB).

Connected Feature Enable

Each Connected Feature is enabled by applying the appropriate signal level to the enable line for that feature set. Each connected feature group may be enabled or disabled independently of the other groups.

NOTE
Enable signal logic levels are not the same for all feature groups.

Each Connected Feature is enabled as a group; i.e. all push-buttons are enabled or disabled, all LED's are enabled or disabled, the POT is enabled or disabled.

Table 8: User Feature Enable

USER FEATURE	ENABLE SIGNAL		SIGNAL LEVEL	
			ENABLE	DISABLE
Push-Buttons	PB_EN	MCU_PORT-36	0	1
LED's	LED_EN	MCU_PORT-34	0	1
POT	POT_EN	MCU_PORT-32	1	0

NOTE: Enable signal levels are not the same for all Feature Groups

To prevent signal corruption, each enable signal may be isolated from the MCU_PORT. An option header at UFEA* illustrated in table 9 allows each enable signal group to be isolated individually. This allows the GPIO port signal applied to the Connected Feature Enable to be used for other purposes.

Table 9: UFEA Option Header

UFEA				SHUNT	
				ON	OFF
BZ	1	2		ENABLE	DISABLE
PB	3	4		ENABLE	DISABLE
LED	5	6		ENABLE	DISABLE
POT	7	8		ENABLE	DISABLE

* For project boards labeled "MCU Project Board -2 AXM-0368 Rev C" this jumper is labeled JP10.

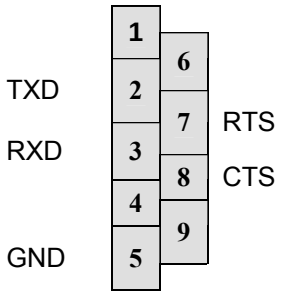
COM Port

The PBMCUSLK is both MONO8 and RS-232 serial communications ready. Many of these user features are by default enabled, but can be disconnected through jumper settings. This section describes each of the features in detail and required jumper configurations.

DB9 Connector

A single DB9 connector shown in figure 12 is provided to support communications applications development on the PBMCUSLK. Signals from the DB9 connector are routed directly to the breakout connector labeled COMM DSUB[1..9] located adjacent to the breadboard. This allows implementation of communication protocols not supported on the PBMCUSLK.

Figure 12: COM Port Connector



Female DB9 connector that interfaces to the DCE serial port via an RS232 transceiver. It provides simple 2-wire asynchronous serial communications without flow control. A straight-through serial cable may be used to a DTE device such a PC

Pins 1, 4, 6, and 9 are routed to the User I/O Signal Breakout connector located adjacent to the breadboard.

RS-232

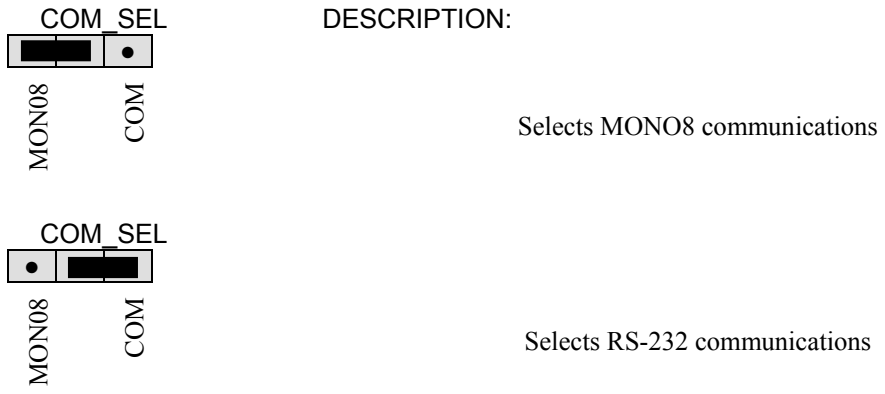
The PBMCUSLK also provides a single RS-232 communications port, configured as a DCE device. An RS-232 transceiver provides RS-232 signal level to TTL/CMOS logic level translation services. The COM_EN option header illustrated in figure 13 allows data and handshake signals to be connected directly to the transceiver. The RS-232 translator operates at either 3.3V or 5V.

Figure 13: COM_EN Option Header

The illustration to the left shows all signals enabled.
Remove shunts to isolate each signal individually

The COM_SEL option header shown in figure 14 configures the transceiver to operate in MONO8 or RS-232 modes.

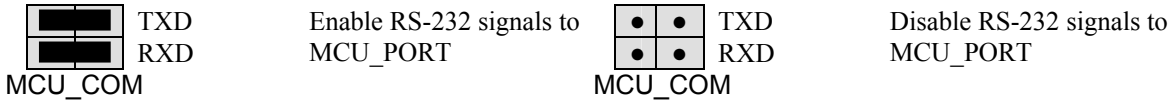
Figure 13: COM_SEL Option Header



Translated RS-232 signals TX and RX are available to the user at the signal breakout header labeled COMM TXD and RXD located adjacent to the breadboard. Translated handshaking signals RTS and CTS are also available. The user will need to configure hand-shaking as required by the communications application used.

To ease application development, communications signals TX and RX are connected the MCU_PORT connect at pins 5 & 7 respectively. This simplifies cable routing when using the PBMCUSLK and an attached module. The MCU_COM option header is used to route these signals from the on-board transceiver to the MCU_PORT headers. To use the signals as general-purpose I/O, simply remove the shunts at the MCU_COM option header as described in figure 15.

Figure 14: MCU_COM Option Header



MON08

MON08 communications are also supported through the COM connector supporting serial monitor operation on HC08 modules. The COM_SEL, shown in figure 14, selects between RS-232 operation and MON08 operation.

A single wire MON08 interface is available to the user at the signal breakout header labeled COMM MONO8 located adjacent to the breadboard. A zener diode and resistor combination provides the high-voltage (VTST) necessary to force MON08 monitor mode. This voltage is fixed at 8.2V and may be excessive for 3.3V HC08 MCU's. It is the users responsibility to reduce the VTST voltage level if necessary. VTST is available when the board is powered either from the VIN connector or from the NI-ELVIS workstation.

Signal Breakout

An important feature of the PBMCUSLK is the large, centrally located, breadboard area. Dual-row socket headers strategically placed around the breadboard provide signal access to the on-board circuits. Signal breakouts may be grouped into 3 broad categories: MCU Access Signals, User I/O Signals, and NI-ELVIS Signals

USER I/O

User I/O signal breakout connectors provide access to all on-board components. Each signal and signal group is labeled to ease signal identification and location. To ease prototyping, each signal is routed to two socket locations. This allows the user to easily route each to signal to multiple locations if desired. The table below details the USER I/O Signal Breakout connectors.

Figure 15: USER I/O Signal Breakout – J10, J11

J10 (USER I/O)

PB 1	1	2
PB 2	3	4
PB 3	5	6
PB 4	7	8
PB 5	9	10
PB 6	11	12
PB 7	13	14
PB 8	15	16
LED 1	17	18
LED 2	19	20
LED 3	21	22
LED 4	23	24
LED 5	25	26
LED 6	27	28
LED 7	29	30
LED 8	31	32
5 V	33	34
GND	35	36
3.3 V	37	38
VTST	39	40
VDD	41	42
POT	43	44
SW1-1	45	46
SW1-2	47	48
SW1-3	49	50
SW1-4	51	52
SW2-1	53	54
SW2-2	55	56
SW2-3	57	58
SW2-4	59	60

J11

	AUX_OSC	1	2
COMMUNICATIONS	MON08	3	4
	TXD	5	6
	RXD	7	8
	RTS	9	10
	CTS	11	12
	DSUB 1	13	14
	DSUB 2	15	16
	DSUB 3	17	18
	DSUB 4	19	20
	DSUB 6	21	22
	DSUB 7	23	24
	DSUB 8	25	26
	DSUB 9	27	28
KEYPAD	KEYPAD 1	29	30
	KEYPAD 2	31	32
	KEYPAD 3	33	34
	KEYPAD 4	35	36
	KEYPAD 5	37	38
	KEYPAD 6	39	40
	KEYPAD 7	41	42
	KEYPAD 8	43	44
USER I/O	VDD	45	46
	5V	47	48
	GND	49	50
	GND	51	52
	BNC+	53	54
	BNC -	55	56
	BANANA B	57	58
	BANANA A	59	60

NOTE: Signal DSUB-9 is connected directly to GND

MCU_PORT

A unique feature of the PBMCUSLK is the ability to interface directly with a line of MCU Development Boards from Axiom Manufacturing. These development boards either plug directly into the MCU_PORT or connect through a ribbon cable. The signals originating at the MCU_PORT connector are routed to two sets of dual-row socket headers located at both ends of the breadboard. All MCU_PORT signals are available at both signal breakout locations. This allows the user to easily prototype circuits at either end of the breadboard. Signal placement at these breakout locations is dependent on signal orientation at the MCU_PORT. See the user manual for the specific MCU module for signal breakout.

Figure 16: MCU_PORT Signal Breakout – J5, J6, J7

J5

M1	1	2	M2
M3	3	4	M4
M5	5	6	M6
M7	7	8	M8
M9	9	10	M10
M11	11	12	M12
M13	13	14	M14
M15	15	16	M16
M17	17	18	M18
M19	19	20	M20
M21	21	22	M22
M23	23	24	M24
M25	25	26	M26
M27	27	28	M28
M29	29	30	M30
M31	31	32	M32
M33	33	34	M34
M35	35	36	M36
M37	37	38	M38
M39	39	40	M40
M41	41	42	M42
M43	43	44	M44
M45	45	46	M46
M47	47	48	M48
M49	49	50	M50
M51	51	52	M52
M53	53	54	M54
M55	55	56	M56
M57	57	58	M58
M59	59	60	M60

J6

M1	1	2	M2
M3	3	4	M4
M5	5	6	M6
M7	7	8	M8
M9	9	10	M10
M11	11	12	M12
M13	13	14	M14
M15	15	16	M16
M17	17	18	M18
M19	19	20	M20
M21	21	22	M22
M23	23	24	M24
M25	25	26	M26
M27	27	28	M28
M29	29	30	M30
M31	31	32	M32
M33	33	34	M34
M35	35	36	M36
M37	37	38	M38
M39	39	40	M40
M41	41	42	M42
M43	43	44	M44
M45	45	46	M46
M47	47	48	M48
M49	49	50	M50
M51	51	52	M52
M53	53	54	M54
M55	55	56	M56
M57	57	58	M58
M59	59	60	M60

J7

M1	1	2	M2
M3	3	4	M4
M5	5	6	M6
M7	7	8	M8
M9	9	10	M10
M11	11	12	M12
M13	13	14	M14
M15	15	16	M16
M17	17	18	M18
M19	19	20	M20
M21	21	22	M22
M23	23	24	M24
M25	25	26	M26
M27	27	28	M28
M29	29	30	M30
M31	31	32	M32
M33	33	34	M34
M35	35	36	M36
M37	37	38	M38
M39	39	40	M40
M41	41	42	M42
M43	43	44	M44
M45	45	46	M46
M47	47	48	M48
M49	49	50	M50
M51	51	52	M52
M53	53	54	M54
M55	55	56	M56
M57	57	58	M58
M59	59	60	M60

NI-ELVIS Interface

The NI-ELVIS interface consists of a PCI style connector located at J1 and 3 dual-row socket headers. Connector J1 connects the PBMCUSLK directly to the NI-ELVIS workstation. All NI-ELVIS signals are routed to a signal breakout connector conveniently located adjacent to the breadboard. Refer to the NI-ELVIS User Guide for details on the functioning of the NI-ELVIS platform. In the figure below, all 'B' pins are on the top layer of the project board and all 'A' pins are on the bottom layer of the project board.

Figure 17: Edge Connector – J1

+15 V	A1	B1	-15 V
+15 V	A2	B2	-15 V
5V_In	A3	B3	GND
5V_In	A4	B4	GND
5V_In	A5	B5	GND
GND	A6	B6	GND
DO 6	A7	B7	DO 7
DO 4	A8	B8	DO 5
DO 2	A9	B9	DO 3
DO 0	A10	B10	DO 1
GND	A11	B11	GND
PCI KEYWAY	A12	B12	PCI KEYWAY
PCI KEYWAY	A13	B13	PCI KEYWAY
DI 6	A14	B14	DI 7
DI 4	A15	B15	DI 5
DI 2	A16	B16	DI 3
DI 0	A17	B17	DI 1
GND	A18	B18	GND
GND	A19	B19	GND
GND	A20	B20	GND
GND	A21	B21	GND
CONN_5V	A22	B22	GND
GND	A23	B23	GND
N/C	A24	B24	ADDRESS 3
ADDRESS 2	A25	B25	ADDRESS 1
ADDRESS 0	A26	B26	GLB_RESET*
LATCH*	A27	B27	RD_ENABLE*
WR_ENABLE*	A28	B28	CONN_5V
Proto Board Present	A29	B29	PFI 6
PFI 5	A30	B30	PFI 7
PFI 2	A31	B31	RESERVED

SCAN CLK	A32	B32	PFI 1
TRIGGER	A33	B33	CTR1_SOURCE
CTR1_GATE	A34	B34	CTR1_OUT
CTR0_SOURCE	A35	B35	CTR0_GATE
CR0_OUT	A36	B36	FREQ_OUT
GND	A37	B37	GND
VOLTAGE HI	A38	B38	VOLTAGE LO
AIGND	A39	B39	AIGND
ACH7+	A40	B40	ACH7-
ACH6+	A41	B41	ACH6-
ACH5+	A42	B42	ACH5-
ACH4+	A43	B43	ACH4-
AIGND	A44	B44	AIGND
ACH3+	A45	B45	ACH3-
ACH2+	A46	B46	ACH2-
ACH1+	A47	B47	ACH1-
ACH0+	A48	B48	ACH0-
AISENSE	A49	B49	N/C
PCI KEYWAY	A50	B50	PCI KEYWAY
PCI KEYWAY	A51	B51	PCI KEYWAY
N/C	A52	B52	N/C
SYNC OUT	A53	B53	FM IN
FUNC OUT	A54	B54	AM IN
GND	A55	B55	CONN_5V
N/C	A56	B56	GND
CURRENT LO	A57	B57	N/C
3-WIRE	A58	B58	CURRENT HI
N/C	A59	B59	N/C
DAC0_2	A60	B60	DAC 1
GND	A61	B61	GND
SUPPLY-	A62	B62	SUPPLY+

Signal Breakout

The following chart shows the signal breakout for the NI-ELVIS signals. These connectors are arranged from left to right above the breadboard. All signals are grouped by function and arranged to provide convenient access to the breadboard. Each signal group is labeled to ease signal identification and location. To ease prototyping, each signal is routed to two socket locations. This allows the user to easily route each to signal to multiple locations if desired. The table below details the NI-ELVS signal breakout connectors.

Figure 18: NI-ELVIS Signal Breakout – J2, J3, J4

J2

1	2	SUPPLY+	
3	4	GND	
5	6	SUPPLY-	
7	8	DAC0	ANA OUT
9	10	DAC 1	
11	12	3-WIRE	DMM
13	14	CURRENT HI	
15	16	CURRENT LO	
17	18	VOLTAGE HI	
19	20	VOLTAGE LO	
21	22	AM IN	Func Gen
23	24	FM IN	
25	26	FUNC OUT	
27	28	SYNC OUT	
29	30	CH A+	O-Scope
31	32	CH A-	
33	34	CH B+	
35	36	CH B-	
37	38	TRIGGER	
39	40	AISENSE	Analog Input
41	42	AIGND	
43	44	ACH0+	
45	46	ACH0-	
47	48	ACH1+	
49	50	ACH1-	
51	52	ACH2+	
53	54	ACH2-	
55	56	ACH3+	
57	58	ACH3-	
59	60	ACH4+	

J3

1	2	ACH4-	Analog
3	4	ACH5+	
5	6	ACH5-	
7	8	FREQ_OUT	Counters
9	10	CTR0_SOURCE	
11	12	CTR0_GATE	
13	14	CTR0_OUT	
15	16	CTR1_SOURCE	
17	18	CTR1_GATE	
19	20	CTR1_OUT	
21	22	5 V	Programmable Function I/O
23	24	5 V	
25	26	RESERVED	
27	28	SCAN CLK	
29	30	PFI 1	
31	32	PFI 2	
33	34	PFI 5	
35	36	PFI 6	
37	38	PFI 7	
39	40	3.3 V	

J4

1	2	3.3 V	Digital I/O
3	4	WR_ENABLE*	
5	6	RD_ENABLE*	
7	8	LATCH*	
9	10	GLB_RESET*	
11	12	ADDRESS 0	
13	14	ADDRESS 1	
15	16	ADDRESS 2	
17	18	ADDRESS 3	
19	20	VDD	
21	22	VDD	
23	24	DO 0	
25	26	DO 1	
27	28	DO 2	
29	30	DO 3	
31	32	DO 4	
33	34	DO 5	
35	36	DO 6	
37	38	DO 7	
39	40	GND	
41	42	DI 0	
43	44	DI 1	
45	46	DI 2	
47	48	DI 3	
49	50	DI 4	
51	52	DI 5	
53	54	DI 6	
55	56	DI 7	
57	58	+15 V	
59	60	-15 V	

TROUBLESHOOTING TIPS

The following is a list of useful problem resolution tips to try before contacting Technical Support for assistance. If the PBMCUSLK still fails to operate properly, contact Axiom Manufacturing at Support@axman.com.

LED's on the PBMCUSLK don't light

- Ensure LED_EN jumper is installed
- Make sure JP1, PWR_SEL is set to source power from the appropriate source
- Verify input power is available
- If the transformer is connected to a power strip, make sure the power strip is turned on.
- Ensure 5VDC between pins VR1-2 and VR1-3
- Measure 3.3VDC between pins VR2-2 and VR2-3

LED's on the MCU Development Module don't light

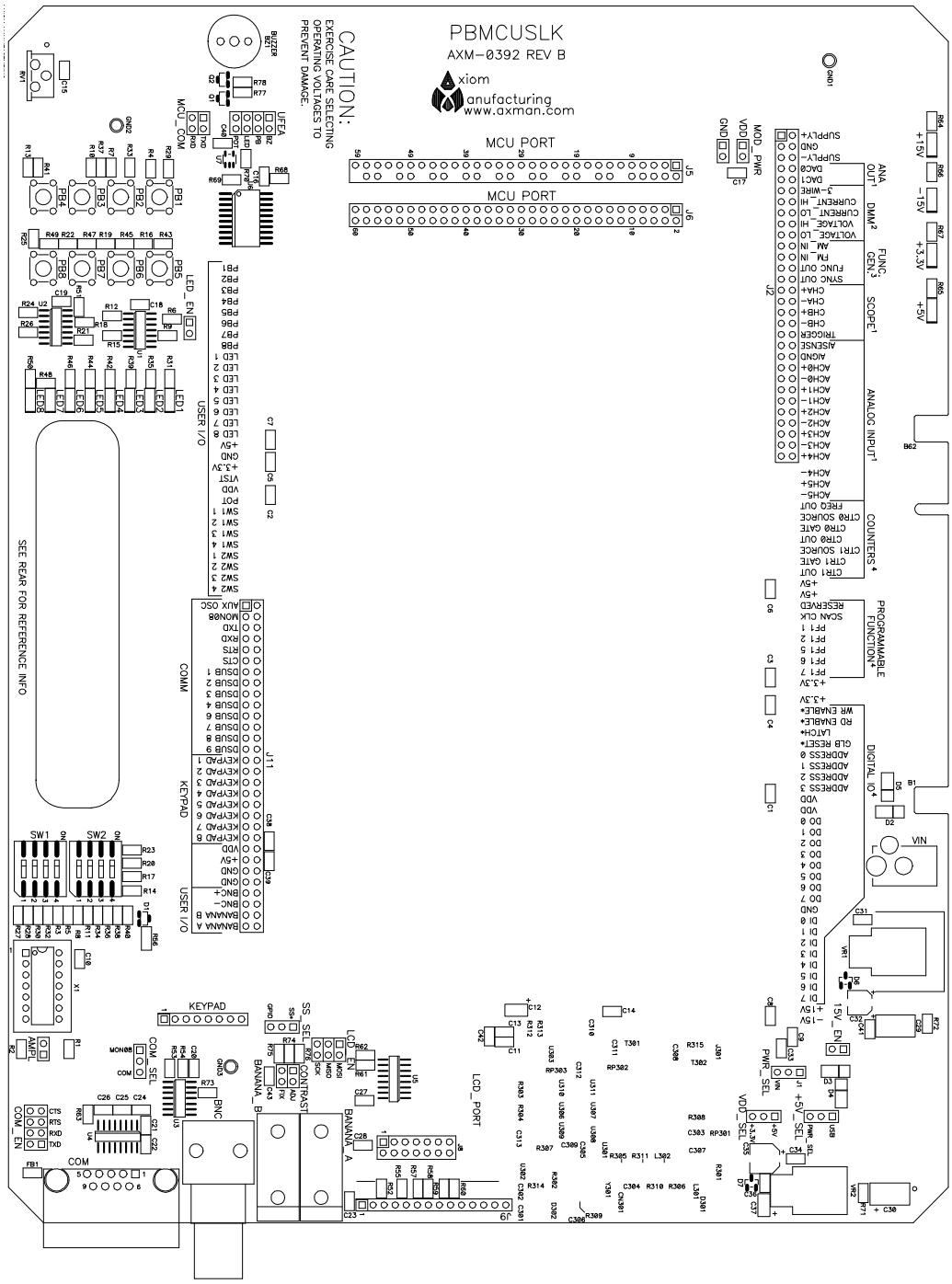
- Make sure the module is properly connected to the PBMCUSLK - 2
- Make sure a power cord is not connected to the module
- Make sure the MODULE POWER option jumpers are installed
- Make sure the PWR_SEL option header on the Development Module is setup properly

No Prompt at the AxIDE Terminal

- Make sure the Serial cable is connected to the HOST PC
- Make sure the correct serial port is selected in the AxIDE program
- Make sure the AxIDE program options setting are configured correctly

APPENDIX A

SILKSCREEN



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