National Semiconductor

PRELIMINARY
March 1991

Programmable Array Logic (PAL®) 24-Pin Medium PAL Series -7, -5, and -4

General Description

The 24-pin medium PAL family contains four of the most popular PAL architectures with speeds as fast as 4.5 ns maximum propagation delay. Series -7, -5 and -4 devices are manufactured using National Semiconductor's proprietary ASPECT™ II TTL process with highly reliable "vertical-fuse" programmable cells. Vertical fuses are implemented using avalanche-induced migration (AIM™) technology offering very high programming yields and is an extension of National's FAST® logic family. The 24-pin medium PAL family provides high-speed user-programmable replacements for conventional SSI/MSI logic with significant chip-count reduction.

Programmable logic devices provide convenient solutions for a wide variety of application-specific functions, including random logic, custom decoders, state machines, etc. By programming the programmable cells to configure AND/OR gate connections, the system designer can implement custom logic as convenient sum-of-products Boolean functions. System prototyping and design iterations can be performed quickly using these off-the-shelf products. A large variety of programming units and software makes design development and functional testing of PAL devices quick and easy.

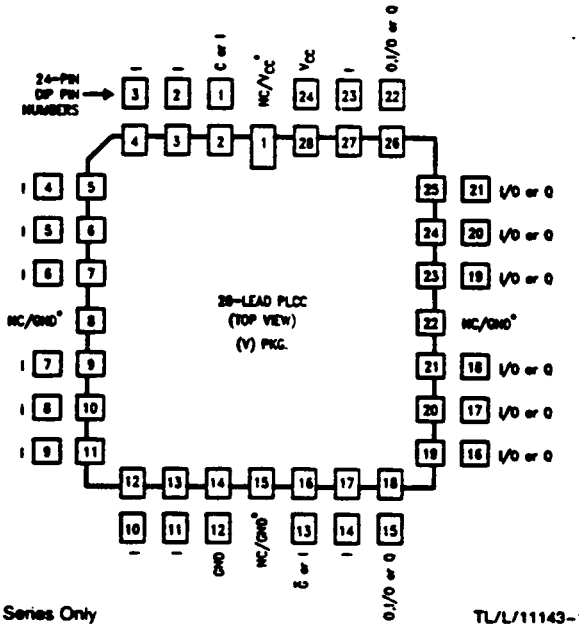
The PAL logic array has a total of 20 complementary input pairs and 8 outputs generated by a single programmable AND gate array with fixed OR-gate connections. Device outputs are either taken directly from the AND-OR functions (combinatorial) or passd through D-type flip-flops (registered). Registers allow the PAL device to implement sequential logic circuits. TRI-STATE® outputs facilitate busing and provide bidirectional I/O capability. The medium PAL family offers a variety of combinatorial and registered output mixtures.

On power-up series -7, -5 and -4 devices reset all registers to simplify sequential circuit design and testing, direct register preload is also provided to facilitate device testing. Security fuses can be programmed to prevent direct copying of proprietary logic patterns.

Features

- 4.5 ns maximum propagation delay (combinatorial outputs)
- Pin compatible with existing PAL families
- High programming yield and reliability of vertical-fuse AIM technology
- Supported by industry standard programming equipment and design development software
- Fully supported by National PLAN™ software
- Power-up reset for registered outputs
- Register preload facilitates device testing
- User programmable replacement for high speed TTL Logic
- Security fuse prevents direct copying of logic patterns
- High noise immunity DIP package

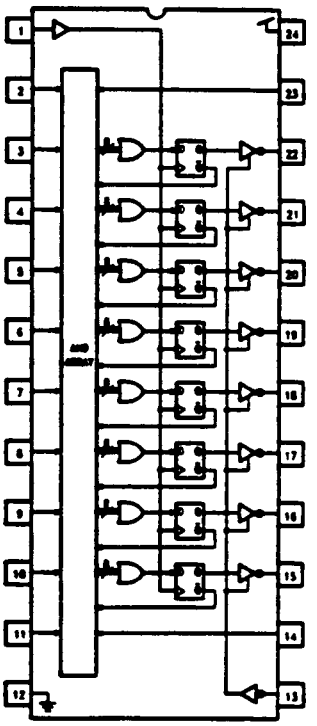
28-Lead PLCC Connection Conversion Diagram



*-4 Series Only

TL/L/11143-1

Block Diagram—PAL20R8



TL/L/11143-2

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.5V to +7.0V
Off-State Output Voltage (Note 2)	−1.5V to +5.5V
Input Current (Note 2)	−30 mA to +5.0 mA
Output Current (I_{OL})	+100 mA
Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−65°C to +125°C
Junction Temperature	−65°C to +150°C
ESD Tolerance (Note 3)	2000V
C_{ZAP} = 100 pF	
R_{ZAP} = 1500Ω	
Test Method: Human Body Model	
Test Specification: NSC SOP-5-028	

Recommended Operating Conditions

Symbol	Parameter		-7 Commercial			-7 Military			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.75	5	5.25	4.5	5	5.5	V
T_A	Operating Free-Air Temperature		0	25	75	−55		125	°C
t_W	Clock Pulse Width	Low	4			5			ns
		High	4			5			ns
t_{SU}	Setup Time from Input or Feedback to Clock		6.5			7			ns
t_H	Hold Time of Input after Clock		0			0			ns
f_{CLK}	Clock Frequency (Note 4)	With Feedback			77			74	MHz
		Without Feedback			125			100	MHz
V_Z	Register Preload Control Voltage		9.5	9.75	10.0	9.5	9.75	10.0	V

Electrical Characteristics Over Recommended Operating Conditions (Note 5)

Symbol	Parameter		Test Conditions	Min	Typ	Max	Units
V_{IL}	Low Level Input Voltage (Note 6)					0.8	V
V_{IH}	High Level Input Voltage (Note 6)			2			V
V_{IC}	Input Clamp Voltage		V_{CC} = Min, I = −18 mA			−1.2	V
I_{IL}	Low Level Input Current (Note 7)		V_{CC} = Max, V_I = 0.4V			−250	μA
I_{IH}	High Level Input Current (Note 7)		V_{CC} = Max, V_I = 2.4V			25	μA
I_I	Maximm Input Current		V_{CC} = Max, V_I = 5.5V			100	μA
V_{OL}	Low Level Output Voltage		V_{CC} = Min, I_{OL} = 24 mA			0.5	V
V_{OH}	High Level Output Voltage		V_{CC} = Min, I_{OH} = −3.2 mA	2.4			V
I_{OZL}	Low Level Off-State Output Current (Note 7)		V_{CC} = Max, V_O = 0.4V			−50	μA
I_{OZH}	High Level Off State Output Current (Note 7)		V_{CC} = Max, V_O = 2.4V			50	μA
I_{OS}	Output Short-Circuit Current (Note 8)	Comm	V_{CC} = 5.0V, V_O = 0.5V	−50		−130	mA
		Mil	V_{CC} = 5.5V, V_O = 0.5V	−50		−200	
I_{CC}	Supply Current		V_{CC} = Max, Outputs Open		125	210	mA
C_I	Input Capacitance		V_{CC} = 5.0V, V_I = 2.0V		5		pF
C_O	Output Capacitance		V_{CC} = 5.0V, V_O = 2.0V		6		pF
$C_{I/O}$	I/O Capacitance		V_{CC} = 5.0V, $V_{I/O}$ = 2.0V		6		pF

Electrical Characteristics Over Recommended Operating Conditions (Continued)

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

Note 2: Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.

Note 3: V_O must not exceed V_{CC} + 1V.

Note 4: f_{CLK} with feedback is derived as $(t_{CLK} + t_{SU}) - 1$. f_{CLK} without feedback is derived as $(2\ t_w) - 1$.

Note 5: All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 6: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

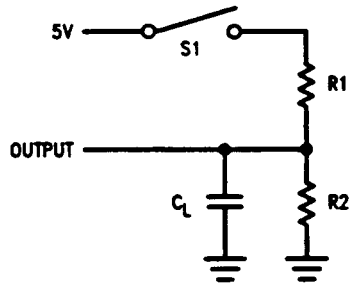
Note 7: Leakage current for bidirectional I/O pins is the worst case between I_{IL} and I_{OZL} or between I_{IH} and I_{OZH}.

Note 8: To avoid invalid readings in other parameter tests it is preferable to conduct the I_{OS} test last. To minimize internal heating, only one output should be shorted at a time with a maximum duration of 1.0 sec. each. Prolonged shorting of a high output may raise the chip temperature above normal and permanent damage may result.

Switching Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions		-7 Commercial			-7 Military			Units
				Min	Typ	Max	Min	Typ	Max	
t_{PD}	Input or Feedback to Combinatorial Output	C_L = 50 pF, S1 Closed	4 Output Switching (DIP)			7				ns
			8 Output Switching (DIP)			7			7.5	ns
			PLCC			7				ns
t_{CLK}	Clock Input to Registered, Output or Feedback	C_L = 50 pF, S1 Closed		3		6.5			6.5	ns
t_{PZXG}	$\overline{G}$ Pin to Registered Output Enabled	C_L = 50 pF, Active High: S1 Open, Active Low: S1 Closed				7			7.5	ns
t_{PXZG}	$\overline{G}$ Pin to Registered Output Disabled	C_L = 5 pF, From V_{OH}: S1 Open, From V_{OL}: S1 Closed				7			7.5	ns
t_{PZXI}	Input to Combinatorial Output Enabled via Product Term	C_L = 50 pF, Active High: S1, Open, Active Low: S1 Closed				7			7.5	ns
t_{PXZI}	Input to Combinatorial Output Disabled via Product Term	C_L = 5 pF, From V_{OH}: S1 Open, From V_{OL}: S1 Closed				7			7.5	ns
t_{RESET}	Power-Up to Registered Output Low					1000			1000	ns

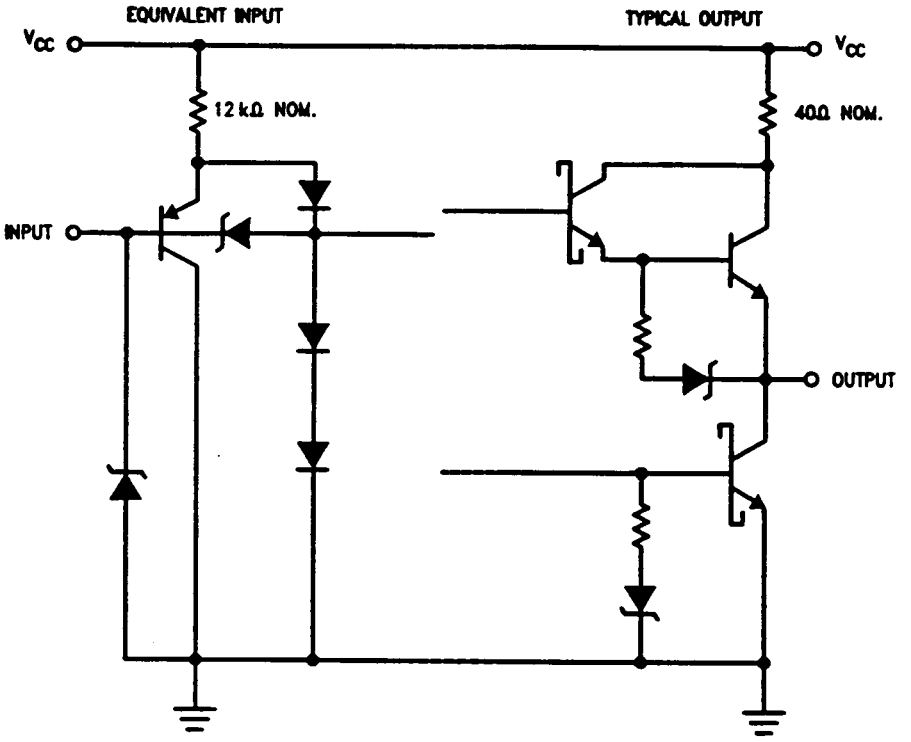
Test Load



TL/L/11143–3

MIL	COMM
R1 = 390Ω	R1 = 200Ω
R2 = 750Ω	R2 = 390Ω

Schematic of Inputs and Outputs



TL/L/11143–4

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.5V to +7.0V
Off-State Output Voltage (Note 2)	−1.5V to +5.5V
Input Current (Note 2)	−30 mA to +5.0 mA
Output Current (I_{OL})	+100 mA
Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−65°C to +125°C
Junction Temperature	−65°C to +150°C

ESD Tolerance (Note 3)
C_{ZAP} = 100 pF
R_{ZAP} = 1500Ω
Test Method: Human Body Model
Test Specification: NSC SOP-5-028

Recommended Operating Conditions

Symbol	Parameter		-5 Commercial			-4 Commercial			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.75	5	5.25	4.75	5	5.25	V
T_A	Operating Free-Air Temperature		0	25	75	0	25	75	°C
t_W	Clock Pulse Width	Low	4			4			ns
		High	4			4			ns
t_{SU}	Setup Time from Input or Feedback to Clock		4			4			ns
t_H	Hold Time of Input after Clock		0			0			ns
f_{CLK}	Clock Frequency (Note 4)	With Feedback			111			118	MHz
		Without Feedback			125			125	MHz
V_Z	Register Preload Control Voltage		9.5	9.75	10.0	9.5	9.75	10.0	V

Electrical Characteristics Over Recommended Operating Conditions (Note 5)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{IL}	Low Level Input Voltage (Note 6)				0.8	V
V_{IH}	High Level Input Voltage (Note 6)		2			V
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I = −18 mA			−1.2	V
I_{IL}	Low Level Input Current (Note 7)	V_{CC} = Max, V_I = 0.4V			−250	μA
I_{IH}	High Level Input Current (Note 7)	V_{CC} = Max, V_I = 2.4V			25	μA
I_I	Maximum Input Current	V_{CC} = Max, V_I = 5.5V			100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 24 mA			0.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = −3.2 mA	2.4			V
I_{OZL}	Low Level Off-State Output Current (Note 7)	V_{CC} = Max, V_O = 0.4V			−50	μA
I_{OZH}	High Level Off State Output Current (Note 7)	V_{CC} = Max, V_O = 2.4V			50	μA
I_{OS}	Output Short-Circuit Current (Note 8)	V_{CC} = 5.0V, V_O = 0.5V	−50		−130	mA
I_{CC}	Supply Current	V_{CC} = Max, Outputs Open		125	210	mA
C_I	Input Capacitance	V_{CC} = 5.0V, V_I = 2.0V		5		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V		6		pF
$C_{I/O}$	I/O Capacitance	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V		6		pF

Electrical Characteristics Over Recommended Operating Conditions (Continued)

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

Note 2: Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.

Note 3: V_O must not exceed V_{CC} + 1V.

Note 4: f_{CLK} with feedback is derived as $(t_{CLK} + t_{SU})^{-1}$. f_{CLK} without feedback is derived as $(2\ t_W)^{-1}$.

Note 5: All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 6: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

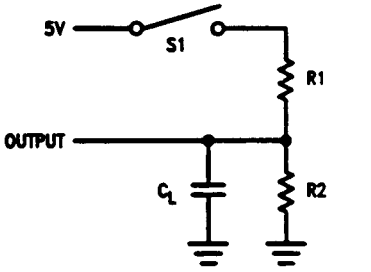
Note 7: Leakage current for bidirectional I/O pins is the worst case between I_{IL} and I_{OZL} or between I_{IH} and I_{OZH}.

Note 8: To avoid invalid readings in other parameter tests it is preferable to conduct the I_{OS} test last. To minimize internal heating, only one output should be shorted at a time with a maximum duration of 1.0 sec. each. Prolonged shorting of a high output may raise the chip temperature above normal and permanent damage may result.

Switching Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions		-5 Commercial			-4 Commercial			Units
				Min	Typ	Max	Min	Typ	Max	
t_{PD}	Input or Feedback to Combinatorial Output	C_L = 50 pF, S1 Closed	4 Output Switching (DIP)			5				ns
			8 Output Switching (DIP)			5.5				ns
			PLCC			5			4.5	ns
t_{CLK}	Clock Input to Registered Output or Feedback	C_L = 50 pF, S1 Closed				5			4.5	ns
t_{PZXG}	$\overline{G}$ Pin to Registered Output Enabled	C_L = 50 pF, Active High: S1 Open, Active Low: S1 Closed				5			4.5	ns
t_{PXZG}	$\overline{G}$ Pin to Registered Output Disabled	C_L = 5 pF, From V_{OH}: S1 Open, From V_{OL}: S1 Closed				5			4.5	ns
t_{PZXI}	Input to Combinatorial Output Enabled via Product Term	C_L = 50 pF, Active High: S1, Open, Active Low: S1 Closed				5			4.5	ns
t_{PXZI}	Input to Combinatorial Output Disabled via Product Term	C_L = 5 pF, From V_{OH}: S1 Open, From V_{OL}: S1 Closed				5			4.5	ns
t_{RESET}	Power-Up to Registered Output Low					1000			1000	ns

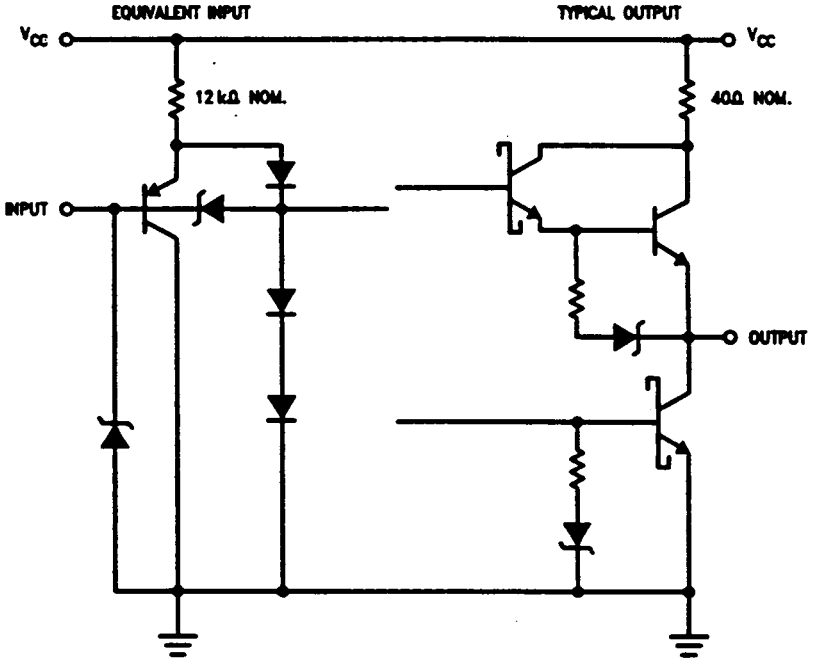
Test Load



TL/L/11143-5

R1 = 200Ω
R2 = 200Ω

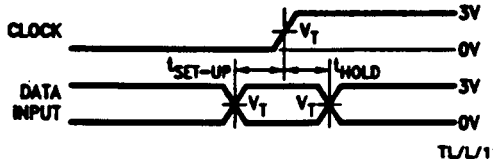
Schematic of Inputs and Outputs



TL/L/11143-6

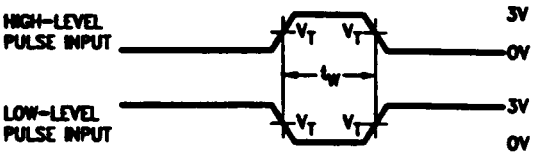
Test Waveforms

Set-Up and Hold



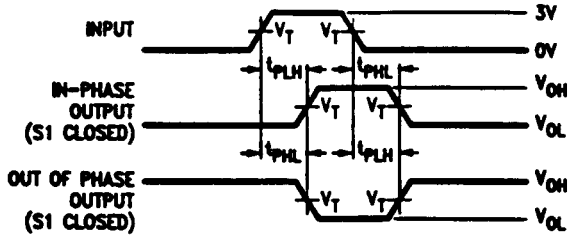
TL/L/11143–7

Pulse Width



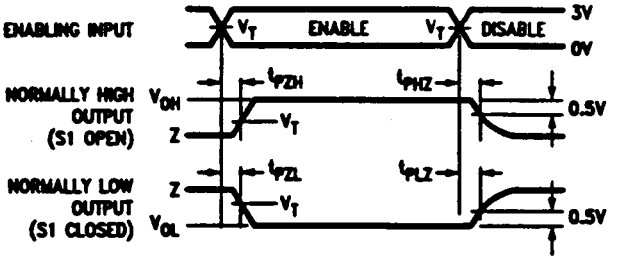
TL/L/11143–9

Propagation Delay



TL/L/11143–8

Enable and Disable



TL/L/11143–10

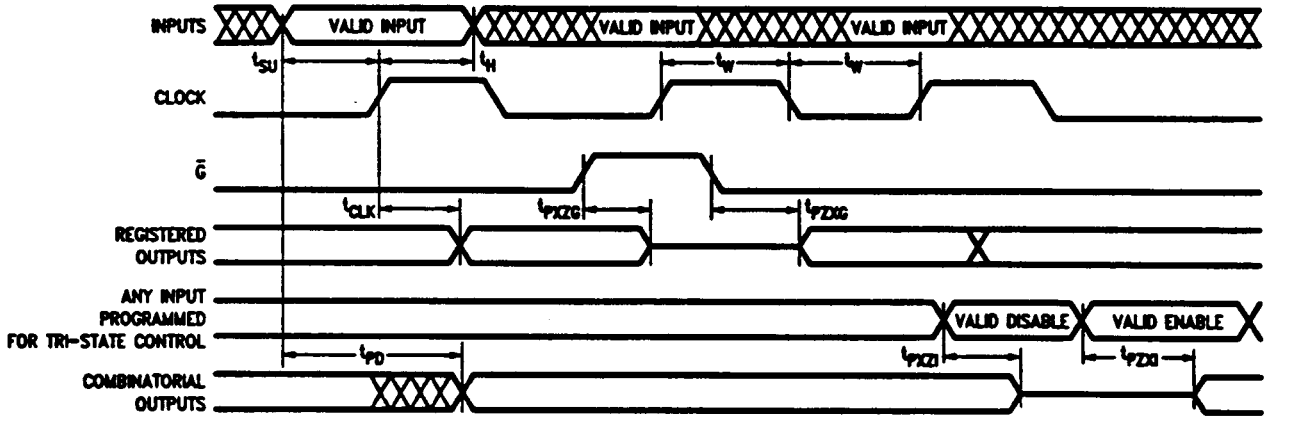
Notes:

V_T = 1.5V

C_L includes probe and jig capacitance.

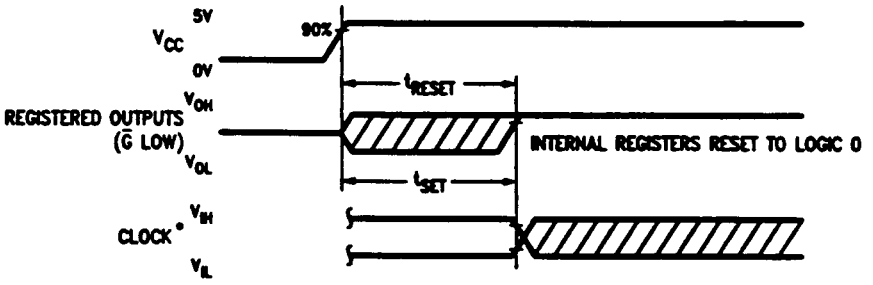
In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

Switching Waveforms



TL/L/11143–11

Power-Up Set/Reset Waveform



TL/L/11143–12

*The clock input should not be switched from low to high until after time t_{RESET} or t_{SET}.

Functional Description

All of the 24-pin medium PAL logic arrays consist of 20 complementary input lines and 64 product-term lines with a programmable cell at each intersection (2560 cells). The product terms are organized into eight groups of eight each. Seven or eight of the product terms in each group connect into an OR-gate to produce the sum-of-products logic function, depending on whether the output is combinatorial or registered.

In the National Series -7, -5 and -4 vertical fuse (AIM) PAL devices, a programmed vertical fuse cell establishes a connection between an input line and a product term. A product term is satisfied (logically true) while all of the input lines connected to it (via unprogrammed fuses for the fuse-link devices, or by programming the corresponding cells for the vertical fuse devices) are in the high logic state. Therefore, if both the true and complement of at least one array input is connected to a product line, that product term is always held in the low logic state (which is the state of all product terms in an unprogrammed fuse-link device). Conversely, if all input lines are disconnected from a product line, the product term and the resulting logic function would be held in the high state (which is the state of all product terms in an unprogrammed National -7, -5 and -4 PAL device). For more information on vertical fuse technology, consult our application note #594.

The medium PAL family consists of four device types with differing mixtures of combinatorial and registered outputs. The 20L8, 20R4, 20R6 and 20R8 architectures have 0, 4, 6 and 8 registered outputs respectively, with the balance of the 8 outputs combinatorial. All outputs are active-low and have TRI-STATE capability.

Each combinatorial output have a seven product-term logic function, with the eighth product term being used for TRI-STATE control. A combinatorial output is enabled while the TRI-STATE product term is satisfied (true). Combinatorial outputs also have feedback paths from the device pins into the logic array (except for two outputs on the 20L8). This allows a pin to perform bidirectional I/O or, if the associated TRI-STATE control product term were programmed to remain unsatisfied (always false), the output driver would remain disabled and the pin could be used as an additional dedicated input.

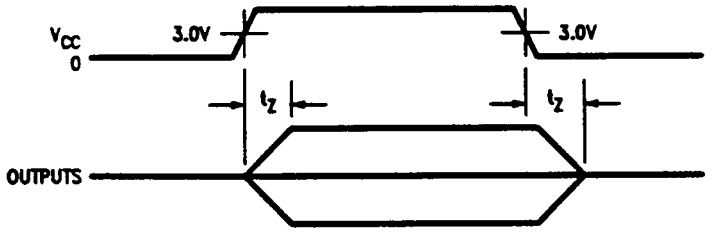
Registered outputs each have an eight product-term logic function feeding into a D-type flip-flop. All registers are triggered by the high-going edge of the clock input pin. All registered outputs are controlled by a common output enable ($\overline{G}$) pin (enabled while low). The output of each register is also fed back into the logic array via an internal path. This provides for sequential logic circuits (state machines, counters, etc.) which can be sequenced even while the outputs are disabled.

Series -7, -5 and -4 medium PAL devices reset all registers to a low state upon power-up (active-low outputs assume high logic levels if enabled). This may simplify sequential circuit design and test. To ensure successful power-up reset, V_{CC} must rise monotonically until the specified operating voltage is attained. During power-up, the clock input should assume a valid, stable logic state as early as possible to avoid interfering with the set or reset operation. The clock input should also remain stable until after the power-up reset operation is completed to allow the registers to capture the proper next state on the first high-going clock transition.

During power-up, all outputs are held in the high-impedance state until DC power supply conditions are met (V_{CC} approximately 3.0V), after which they may be enabled by the TRI-STATE control product terms (combinatorial outputs) or the $\overline{G}$ pin (registered outputs). Whenever V_{CC} goes below 3V (at 25°C), the outputs are disabled as shown in *Figure 1* below.

In an unprogrammed National Series -7, -5 and -4 PAL devices, no array inputs are connected to any product-term lines. Therefore, all combinatorial outputs would be enabled and driving low logic levels (after power-up is completed). All registers would still initialize to the low state, but would become permanently set (low-level outputs, if enabled) following the first clock transition.

As with any TTL logic circuits, unused inputs to a PAL device should be connected to ground, V_{OL}, V_{OH}, or resistively to V_{CC}. However, switching any input not connected to a product term or logic function has no effect on its output logic state.

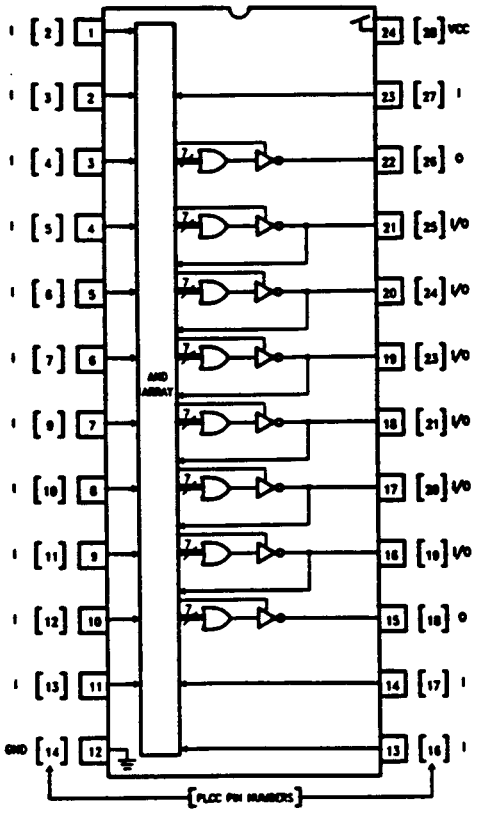


TL/L/11143–13

FIGURE 1. Power-Up TRI-STATE Waveform

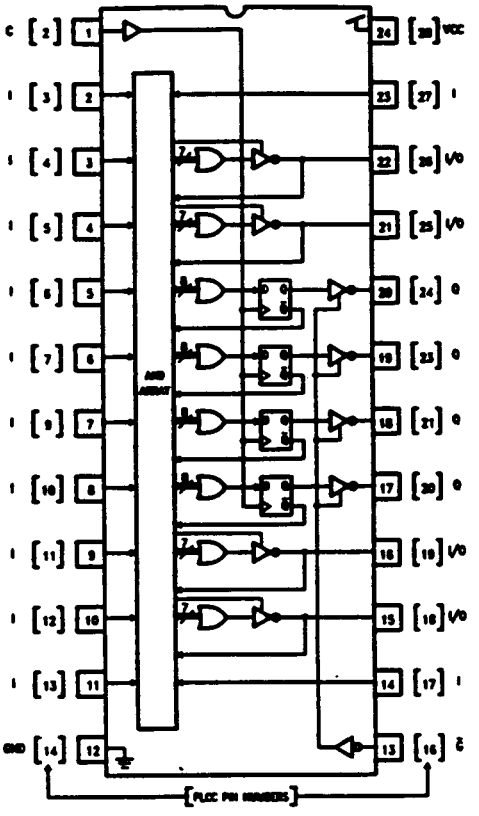
24-Pin Medium PAL Family Block Diagrams—DIP Connections

PAL20L8



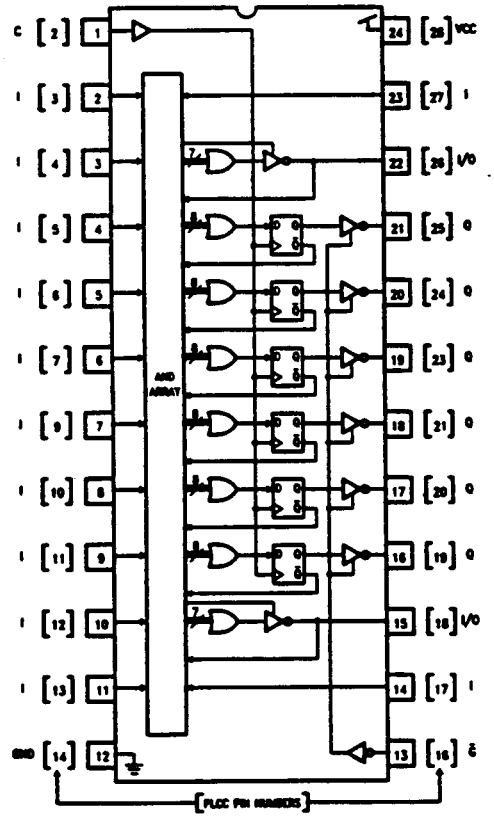
TL/L/11143–14

PAL20R4



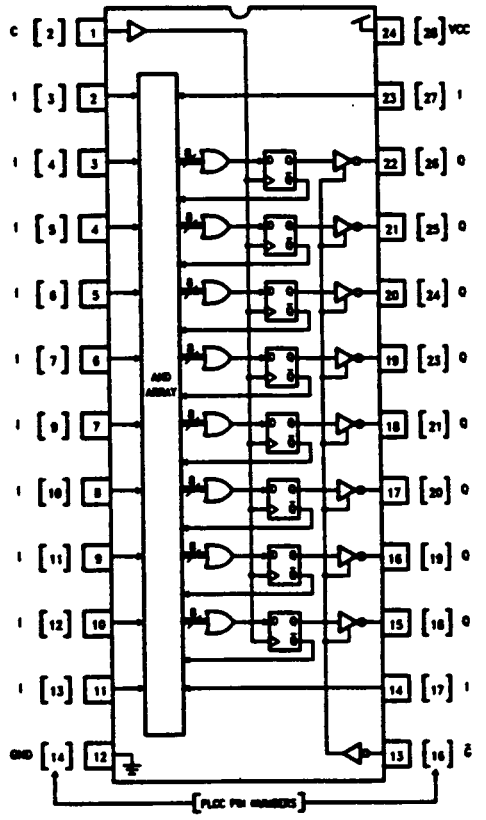
TL/L/11143–15

PAL20R6



TL/L/11143–16

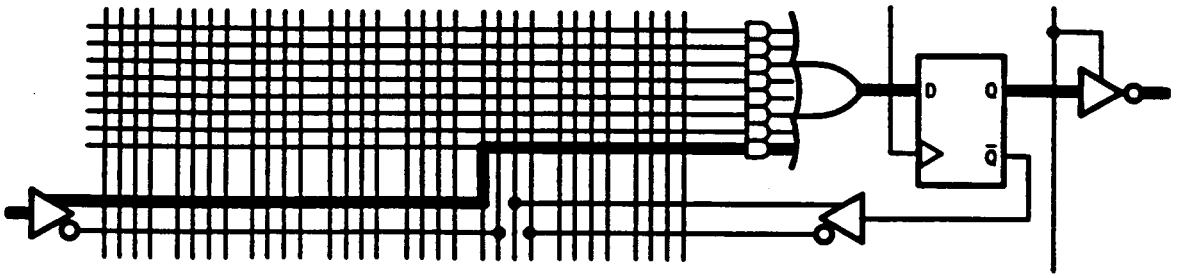
PAL20R8



TL/L/11143–17

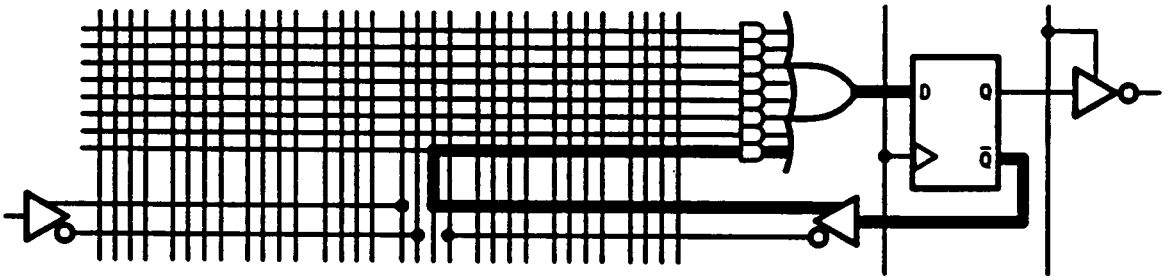
Functional Description (Continued)

Typical Registered Logic Function without Feedback



TL/L/11143–18

Typical Registered Logic Function with Feedback



TL/L/11143–19

Clock Frequency Specification

The clock frequency (f_{CLK}) parameter specifies the maximum speed at which a registered PAL device is guaranteed to operate. Clock frequency is defined differently for the two cases in which register feedback is used versus when it is not. In a data-path type application, where the logic functions fed into the registers are not dependent on register feedback from the previous cycle (i.e., based only on external inputs) the minimum required cycle period (f_{CLK}^{-1} without feedback) is defined as the greater of the minimum clock period (t_w high + t_w low) and minimum "data window" period (t_{SU} + t_H). This assumes optimal alignment between data inputs and the clock input. In sequential logic applications such as state machines, the minimum required cycle period (f_{CLK}^{-1} with feedback) is defined as t_{CLK} + t_{SU}. This provides sufficient time for outputs from the registers to feed back through the logic array and set-up on the inputs to the registers before the end of each cycle.

Output Register Preload

This feature simplifies device testing since any state may be loaded into the registers at any time during the functional test sequence. This allows complete verification of sequential logic circuits, including states that are normally impossible or difficult to reach. Register preload is not an operational mode and is not intended for board level testing because elevated voltage levels are required. The programming system normally provides the preload capability as part of its functional test facility.

The preload function allows the registers to be loaded directly and asynchronously with any desired pattern. These vertical-fuse devices provide two register preload operations:

1. All registers can be reset to the low state (high-level outputs) by applying the elevated control voltage (V_Z) to input pin 2 for time t_D *(Figure 2a)*.
2. Selected registers can be set to the high state (low-level outputs) as follows *(Figure 2b)*.
   a. All registered outputs are disabled by raising $\overline{G}$ input pin 1 to V_{IH}.
   b. After time t_D, the selected registered output pins are raised to the elevated control voltage (V_Z) for time t_D to set the corresponding register.

Security Fuse

Security fuses are provided on all National PAL devices which, when programmed, inhibit any further programming or verifying operations. This feature prevents direct copying of proprietary logic patterns. The security fuses should be programmed only after programming and verifying all other device fuses. Register preload is not affected by the security fuses.

Design Development Support

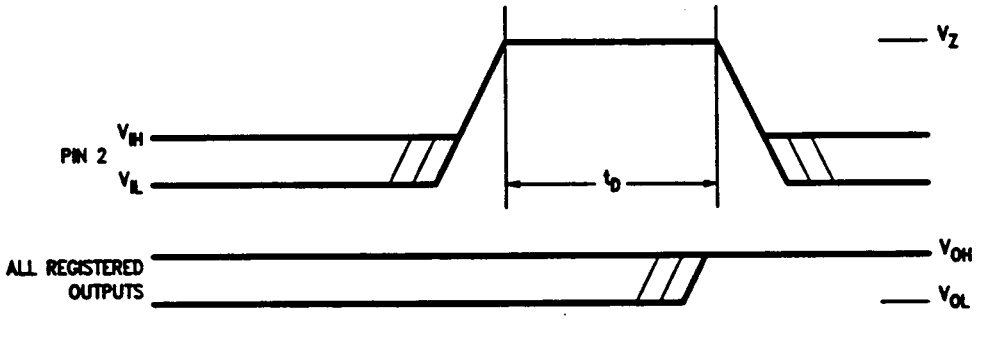
A variety of software tools and industry standard programming hardware is available to support the development of designs using PAL products. Typical software packages accept Boolean logic equations to define desired functions. Most are available to run on personal computers and generate JEDEC-compatible "fuse maps". The industry-standard JEDEC format ensures that the resulting fuse-map files can be down-loaded into a variety of programming equipment. Many software packages and programming units support a multitude of programmable logic products as well. PLAN software package from National Semiconductor supports all of our programmable logic products and is fully JEDEC-compatible.

Design Development Support (Continued)

In National Series -7, -5 and -4 devices, logical and physical connections between array input lines and product-term lines are established when vertical fuse cells are programmed. This is opposite to other PAL products based on fusible links in which connections are established when fuses are left unprogrammed (intact). This difference is compensated by the vertical-fuse PAL programming algorithm so that the *user's design development process looks the same.* (The only functional difference due to vertical-fuse technology is the behavior of "unprogrammed" devices.) The JEDEC programming maps produced by PAL development software for all Medium PAL devices denote a "connection" with a "0", and a "non-connection" with a "1". The programming algorithms for most fuse-link PLDs program fuses where ones are located in the map to remove corresponding connections, whereas the algorithm for National Series PAL -7, -5 and -4 products automatically compensates by programming vertical-fuse cells where zeroes are located in the map to establish connections. Therefore, the *same JEDEC map* representing the user's desired logic equations produces the *same functional results* when using either PAL technology. The user need only provide the appropriate device code and/or adapter for the programming equipment to invoke the proper programming algorithm. Only programmers with the certified National vertical-fuse PAL programming algorithm should be used to program these vertical-fuse devices.

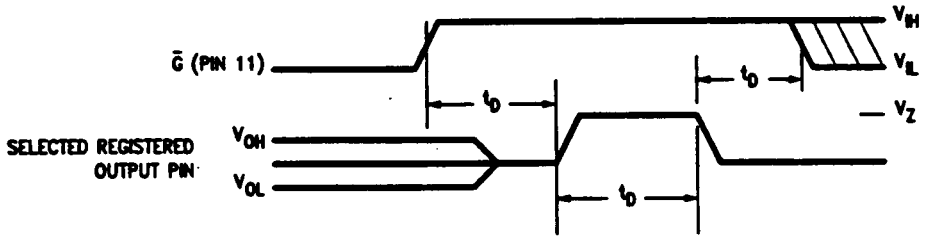
Detailed logic diagrams showing all JEDEC fuse-map addresses for the 24-pin medium PAL family are provided for direct map editing and diagnostic purposes. The DIP and PLCC package for -7, -5 and -4 series are pin for pin replacements for all slower 24-pin medium PAL devices (A, B and D Series). The non-connected (NC) pins on the PLCC package are utilized in the -4 series as extra power and ground pins (V_{CC} and GND) to provide better noise immunity at high switching speeds. For a list of current software and programming support tools available for theses devices, please contact your local National Semiconductor sales representative or distributor. If detailed specifications of the PAL programming algorithm are needed, please contact the National Semiconductor Programmable Device Support Department.

Functional Description (Continued)



TL/L/11143–20

a) To Reset All Registers



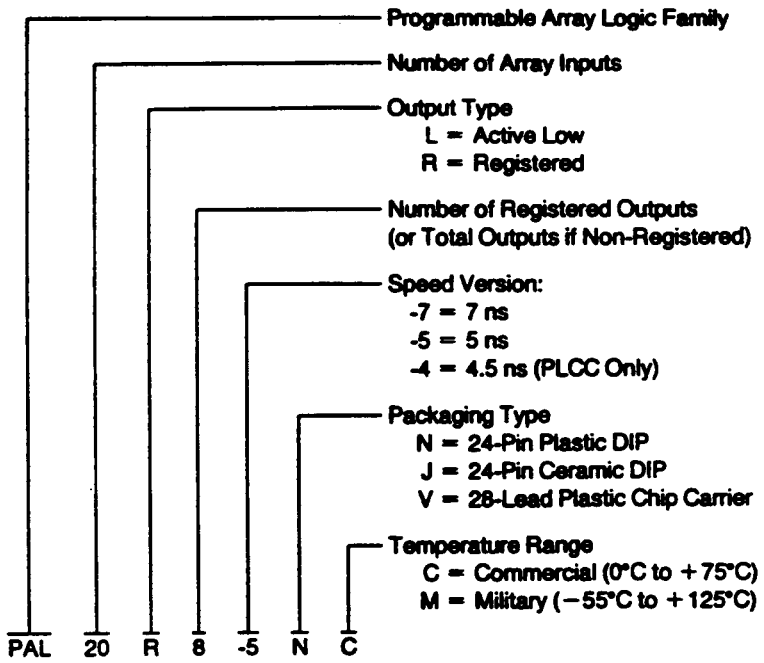
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b) To Set Selected Registers

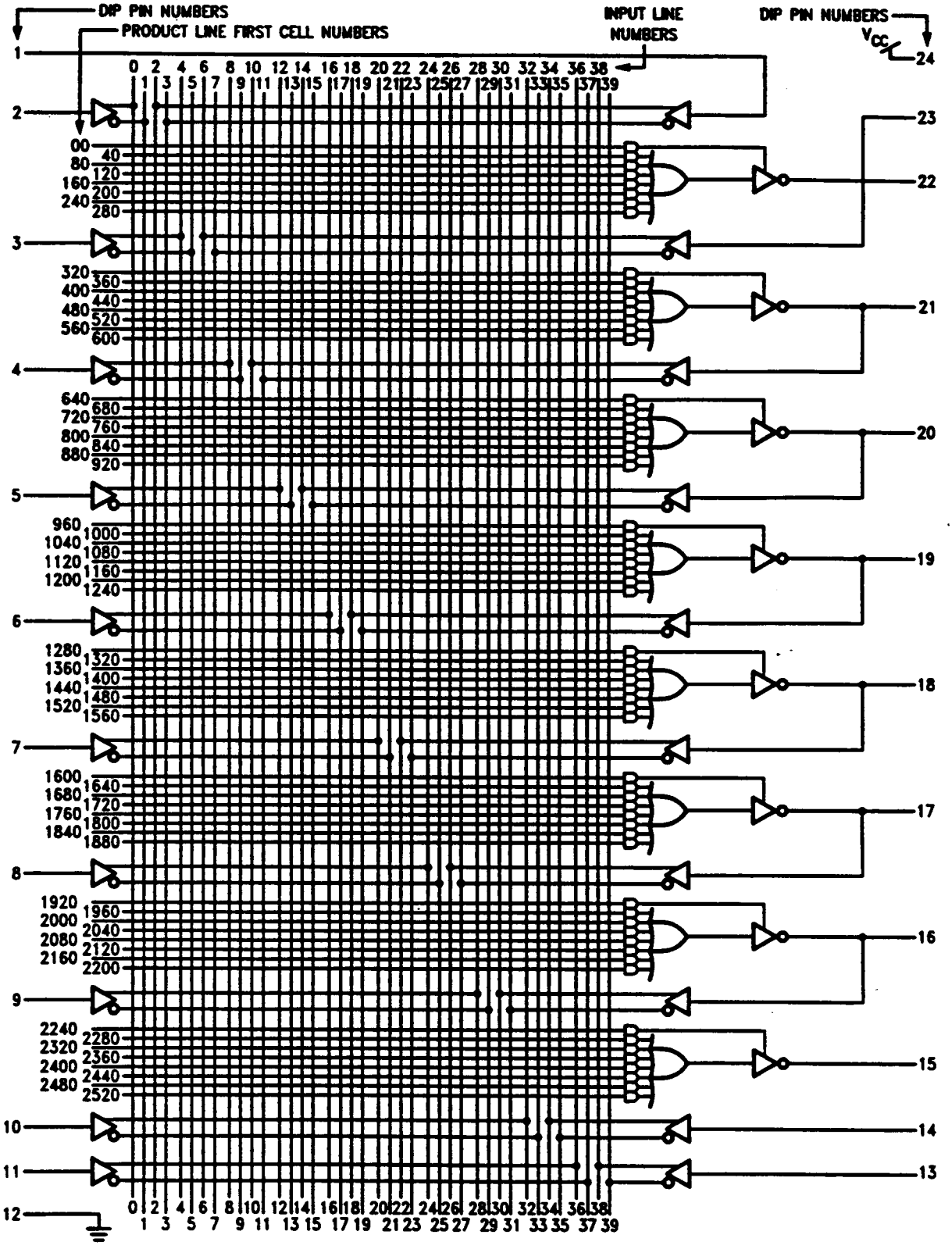
Note: V_Z = 9.5V to 10.0V, t_D min. = 500 ns

FIGURE 2. Register Preload Waveforms

Ordering Information



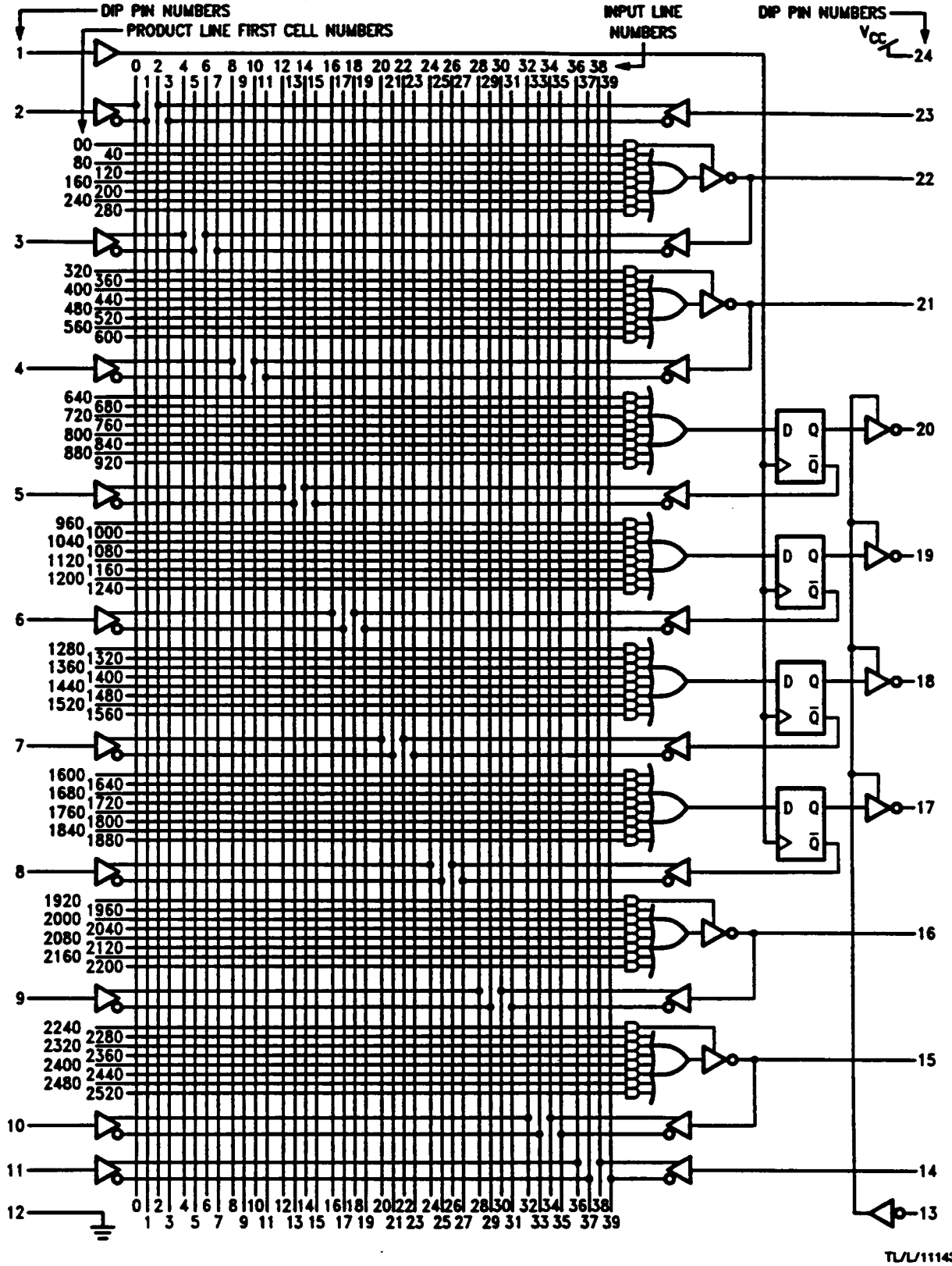
Logic Diagram—PAL20L8



TL/L/11143-22

JEDEC Logic Array Cell Number = Product Line First Cell Number + Input Line Number

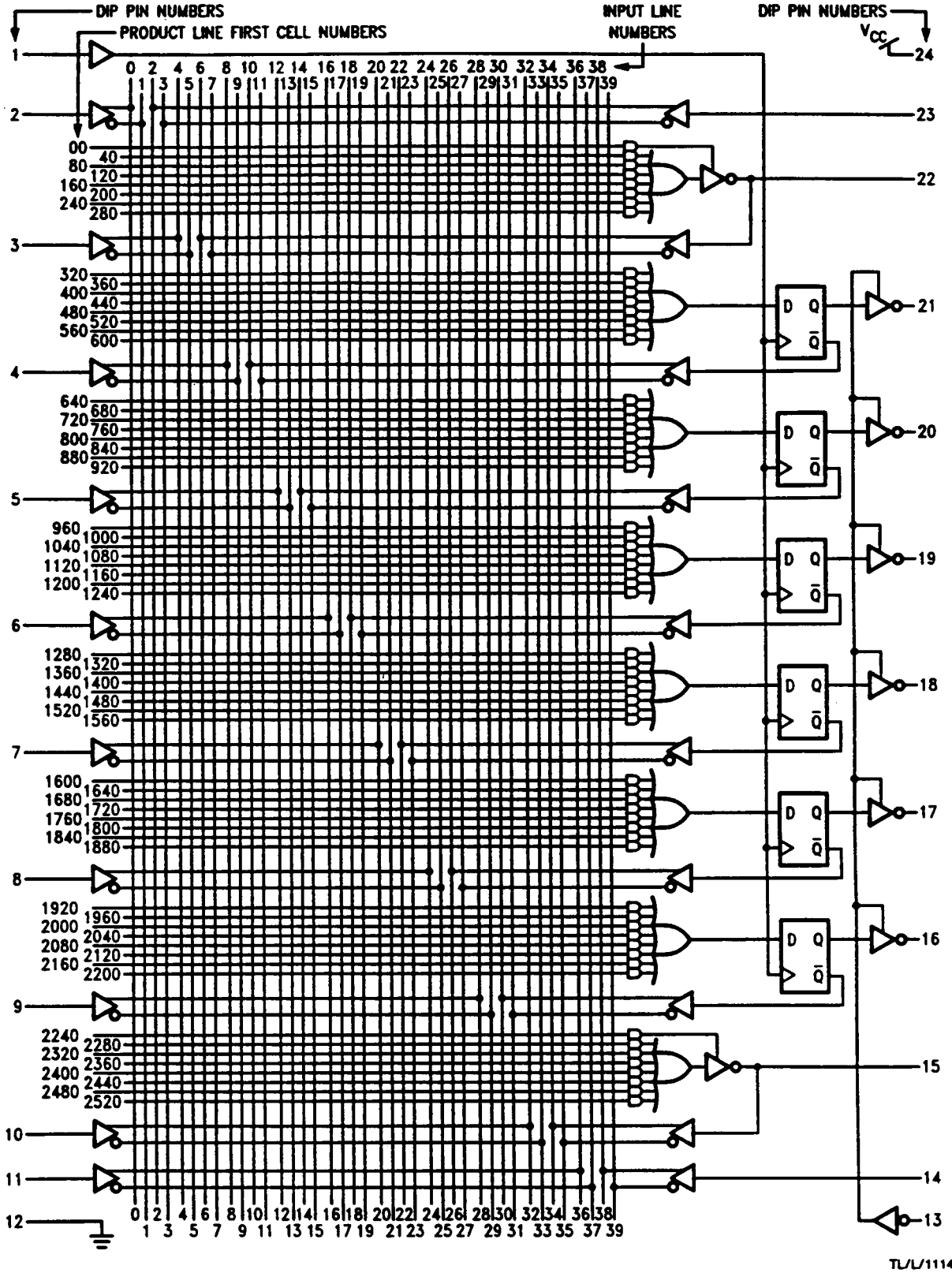
Logic Diagram—PAL20R4



TL/L/11143–23

JEDEC Logic Array Cell Number = Product Line First Cell Number + Input Line Number

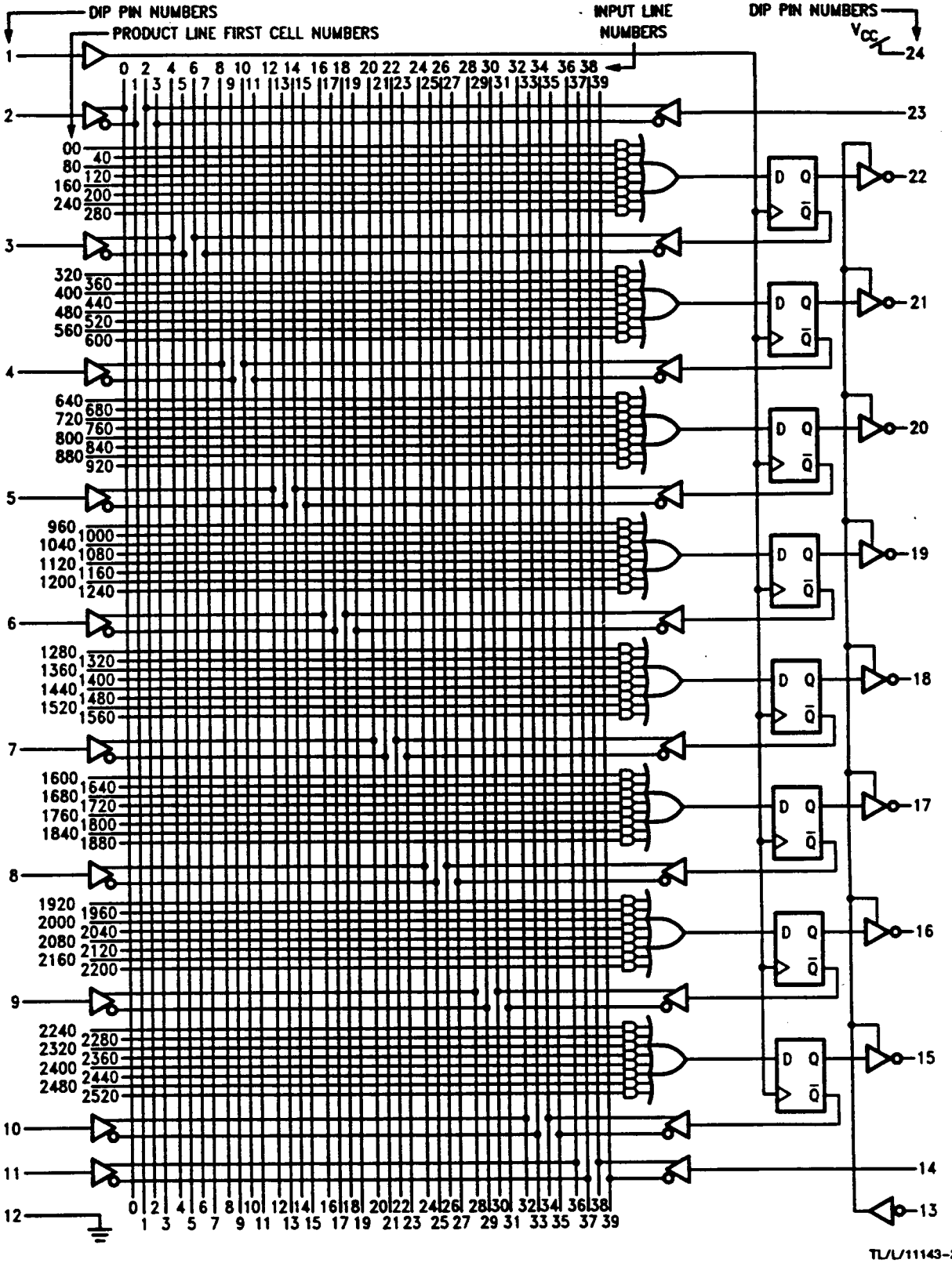
Logic Diagram—PAL20R6



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JEDEC Logic Array Cell Number = Product Line First Cell Number + Input Line Number

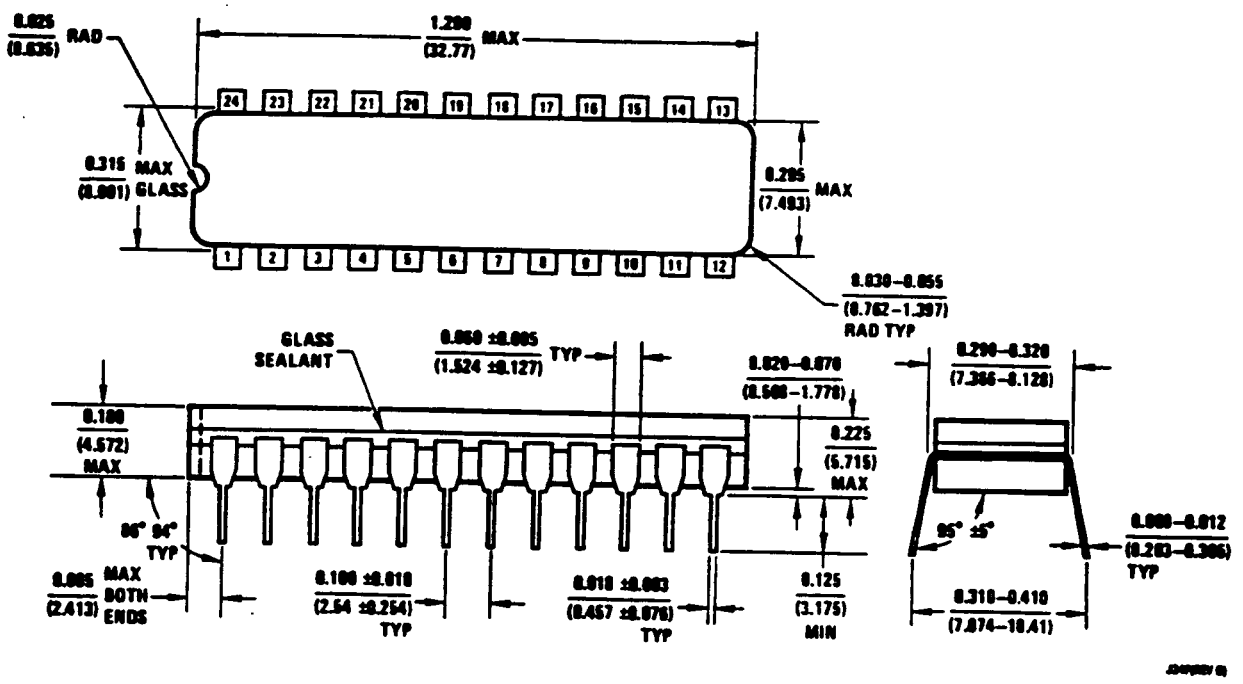
Logic Diagram—PAL20R8



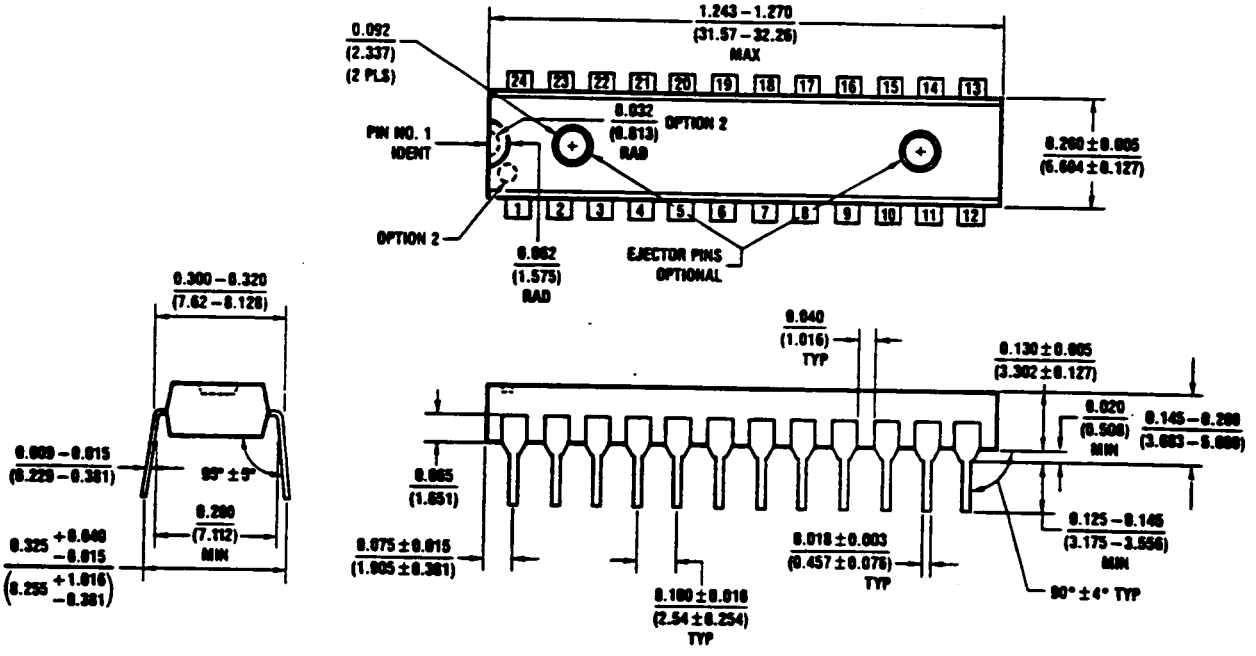
TL/L/11143-25

JEDEC Logic Array Cell Number = Product Line First Cell Number + Input Line Number

Physical Dimensions inches (millimeters)

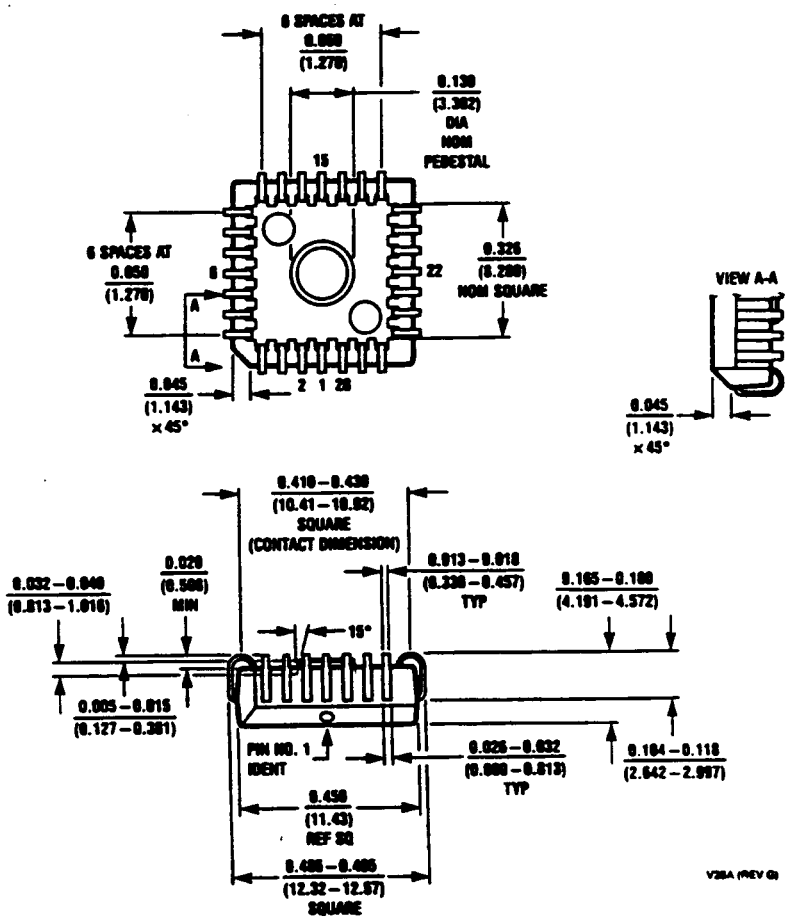


24-Pin Narrow Ceramic Dual-In-Line Package (J)
NS Package Number J24F



24-Pin Narrow Plastic Dual-In-Line Package (N)
NS Package Number N24C

Physical Dimensions inches (millimeters) (Continued)



28-Lead Plastic Chip Carrier Package (V)
NS Package Number V28A

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National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: 1(800) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Industriestrasse 10
D-8080 Furstenfeldbruck
West Germany
Tel: (0-81-41) 103-0
Telex: 527-649
Fax: (08141) 103554

National Semiconductor Japan Ltd.
Sanseido Bldg. 5F
4-15 Nishi Shinjuku
Shinjuku-Ku,
Tokyo 160, Japan
Tel: 3-299-7001
FAX: 3-299-7000

National Semiconductor Hong Kong Ltd.
Suite 513, 5th Floor
Chinachem Golden Plaza,
77 Mody Road, Tsimshatsui East,
Kowloon, Hong Kong
Tel: 3-7231290
Telex: 52996 NSSEA HX
Fax: 3-3112536

National Semiconductores Do Brasil Ltda.
Av. Brig. Faria Lima, 1383
6.0 Andor-Conj. 62
01451 Sao Paulo, SP, Brasil
Tel: (55/11) 212-5066
Fax: (55/11) 211-1181 NSBR BR

National Semiconductor (Australia) PTY, Ltd.
1st Floor, 441 St. Kilda Rd.
Melbourne, 3004
Victory, Australia
Tel: (03) 267-5000
Fax: 61-3-2677458

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