PAC7312 VGA PC Camera Single-Chip with Audio

General Description

The PAC7312 is a single chip with an embedded VGA CMOS image sensor and USB 1.1 interface. It has JPEG image compression and image processing. The generic application is a PC camera. JPEG decoder and auto exposure are performed by software in PC side. And the optical size is 1/4" which can easily be embedded in LCD monitors, notebooks or PDA. It also provides high quality audio sampling function for sound recording. The audio function complies with USB audio device class 1.0.

There are 4 IO-trapping pins with internal pull-low resistors. It is flexible for customers to set PID. It supports the interface to a serial-EEPROM. When the EEPROM function is enabled, the internal control registers can be power-up loaded from external EEPROM. This allows customization of VID, PID, product string.

Features

- VGA resolution, ~1/4"Lens
- Frame rate up to 30fps at following resolution format
  - VGA format (640x480) with JPEG compression
  - CIF format (352x288) with JPEG compression
  - QVGA format (320x240) with JPEG compression
  - QCIF format (176x144) without compression
  - QQVGA format (160x120) without compression
- RGB Bayer's pattern raw data
  - Up to 3fps @VGA format (640x480)
  - Up to 12fps @CIF format (352x288)
  - Up to 12fps @QVGA format (320x240)
  - Up to 30fps @QCIF format (176x144)
  - Up to 30fps @QQVGA format (160x120)
- Standard JPEG compression engine comply to ISO/IEC 10918-1(JPEG)
- AEC/AGC/AWB automatic
- 4 IO-trapping pins to set USB PID
- Support USB suspend mode
- Support video data transfer through USB isochronous transfer
- Snapshot control through USB interrupt pipe
- USB Vendor ID, Product ID, device release number and the string descriptor index via a serial EEPROM (93C46) or by metal mask
- Complete Universal Serial Bus® spec V1.1 compatibility
- Built in 8bits mono audio ADC for audio recording through microphone, 16KHZ sampling rate, 8/16bits PCM format
- USB audio device class 1.0 compatibility

Key Specification

Supply Voltage	5.0V ± 10%
Resolution	640 (H) x 480 (V)
Array Diagonal	4.48mm
Optical format	1/4"
Pixel Size	5.6um x 5.6um
Frame Rate	Up to 30fps
System Clock	12MHz
Color Filter	RGB Bayer Pattern
Scan mode	Progressive
Sensitivity	3.06 V/lux*sec
PGA gain	23.52dB (Max.)
S/N ratio	>45dB
Power consumption	65mA
Package	48-pin PLCC / 37-pin CSP

Ordering Information

Order number	Package Type	Package Size(mm)
PAC7312PE	48-pin PLCC	11.43 x 11.43
PAC7312CS	37-pin CSP	5.06 x 5.55

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1. Pin Assignment

1.1 PLCC Package

Pin#	Name	Type	Description
1	NC	-	No Connection
2	MIC	IN	Microphone input
3	NC	-	No Connection
4	VRB	BYPASS	Analog voltage reference
5	VCM	BYPASS	Analog voltage reference
6	NC	-	No Connection
7	NC	-	No Connection
8	VRT	BYPASS	Analog voltage reference
9	VDDA	BYPASS	Analog power for AD/DA/PGA, 2.5V
10	VDDAY	BYPASS	Sensor reset power reference
11	EPR_DO	IN	Data output of EEPROM
12	VSSQ	GND	Ground for I/O and PHY
13	VDDQ	BYPASS	Power for I/O and PHY
14	EPR_CS/TR2	OUT	Chip Select of EEPROM; (IO trap pin for PID2, internal pull-down 100Kohm)
15	EPR_CK/TR3	OUT	Serial clock of EEPROM; (IO trap pin for PID3, internal pull-down 100Kohm)
16	EPR_DI/TR1	OUT	Data input of EEPROM; (IO trap pin for PID1, internal pull-down 100Kohm)
17	VSSAY	GND	Sensor ground
18	NC	-	No Connection
19	NC	-	No Connection
20	GPO/TR0	OUT	General purpose output; (IO trap pin for PID0, internal pull-down 100Kohm)
21	LED	OUT	LED driver
22	NC	-	No Connection
23	TEST2	IN	Test pin, internal pull-up 100Kohm
24	EPR_EN	IN	Enable signal of EEPROM (1: enable, 0: disable), internal pull-down 100Kohm
25	IOTRAP#	IN	I/O trap enable signal (0: enable, 1: disable, internal pull-down 100Kohm)
26	KEY#	IN	Snapshot control signal (Active Low, internal pull-up 100Kohm)
27	NC	-	No Connection
28	VSSQ	GND	Ground for I/O and PHY
29	VDDD	BYPASS	Logic power for mixed-mode circuit, 2.5V
30	PWR_5V	PWR	Main power, USB bus power
31	NC	-	No Connection
32	VDDQ	BYPASS	Power for I/O and PHY, 3.3V
33	GPIO	IO	General purpose input/output, internal pull-down 100Kohm
34	TEST1	IN	Test pin. Connect to GND in normal operation mode
35	NC	-	No Connection
36	RESET#	IN	Chip power up reset
37	VSSQ	GND	Ground for I/O and PHY
38	XOUT	OUT	Crystal output
39	XIN	IN	Crystal input
40	DP	I/O	DP for USB1.1 PHY
41	DN	I/O	DN for USB1.1 PHY
42	NC	-	No Connection
43	VDDQ	BYPASS	Power for I/O and PHY
44	VDDP	BYPASS	Analog power for PLL
45	VDDAD	BYPASS	Analog voltage reference power for core logic, 2.5V
46	VDDAV	BYPASS	Analog voltage reference
47	VSSA	GND	Analog ground
48	PWR_5V	PWR	Main power, USB bus power

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1.2 CSP Package

Pin#	Name	Type	Description
1	MIC	IN	Microphone input
2	VRB	BYPASS	Analog voltage reference
3	VCM	BYPASS	Analog voltage reference
4	VRT	BYPASS	Analog voltage reference
5	VDDA	BYPASS	Analog power for AD/DA/PGA, 2.5V
6	VDDAY	BYPASS	Sensor reset power reference
7	EPR_DO	IN	Data output of EEPROM
8	VSSQ	GND	Ground for I/O and PHY
9	VDDQ	BYPASS	Power for I/O and PHY
10	EPR_CS/TR2	OUT	Chip Select of EEPROM; (IO trap pin for PID2, internal pull-down 100Kohm)
11	EPR_CK/TR3	OUT	Serial clock of EEPROM; (IO trap pin for PID3, internal pull-down 100Kohm)
12	EPR_DI/TR1	OUT	Data input of EEPROM; (IO trap pin for PID1, internal pull-down 100Kohm)
13	VSSAY	GND	Sensor ground
14	GPI/TR0	OUT	General purpose output; (IO trap pin for PID0, internal pull-down 100Kohm)
15	LED	OUT	LED driver
16	EPR_EN	IN	Enable signal of EEPROM (1: enable, 0: disable), internal pull-down 100Kohm
17	IOTRAP#	IN	I/O trap enable signal (0: enable, 1: disable, internal pull-down 100Kohm)
18	KEY#	IN	Snapshot control signal (Active Low, internal pull-up 100Kohm)
19	NC	-	No Connection
20	VSSQ	GND	Ground for I/O and PHY
21	VDDD	BYPASS	Logic power for mixed-mode circuit, 2.5V
22	PWR_5V	PWR	Main power, USB bus power
23	VDDQ	BYPASS	Power for I/O and PHY
24	GPIO	IO	General purpose input/output, internal pull-down 100Kohm
25	TEST1	IN	Test pin. Connect to GND in normal operation mode
26	RESET#	IN	Chip power up reset
27	VSSQ	GND	Ground for I/O and PHY
28	XOUT	OUT	Crystal output
29	XIN	IN	Crystal input
30	DP	I/O	DP for USB1.1 PHY
31	DN	I/O	DN for USB1.1 PHY
32	VDDQ	BYPASS	Power for I/O and PHY, 3.3V
33	VDDP	BYPASS	Analog power for PLL
34	VDDAD	BYPASS	Analog voltage reference power for core logic, 2.5V
35	VDDAV	BYPASS	Analog voltage reference
36	VSSA	GND	Analog ground
37	PWR_5V	PWR	Main power, USB bus power

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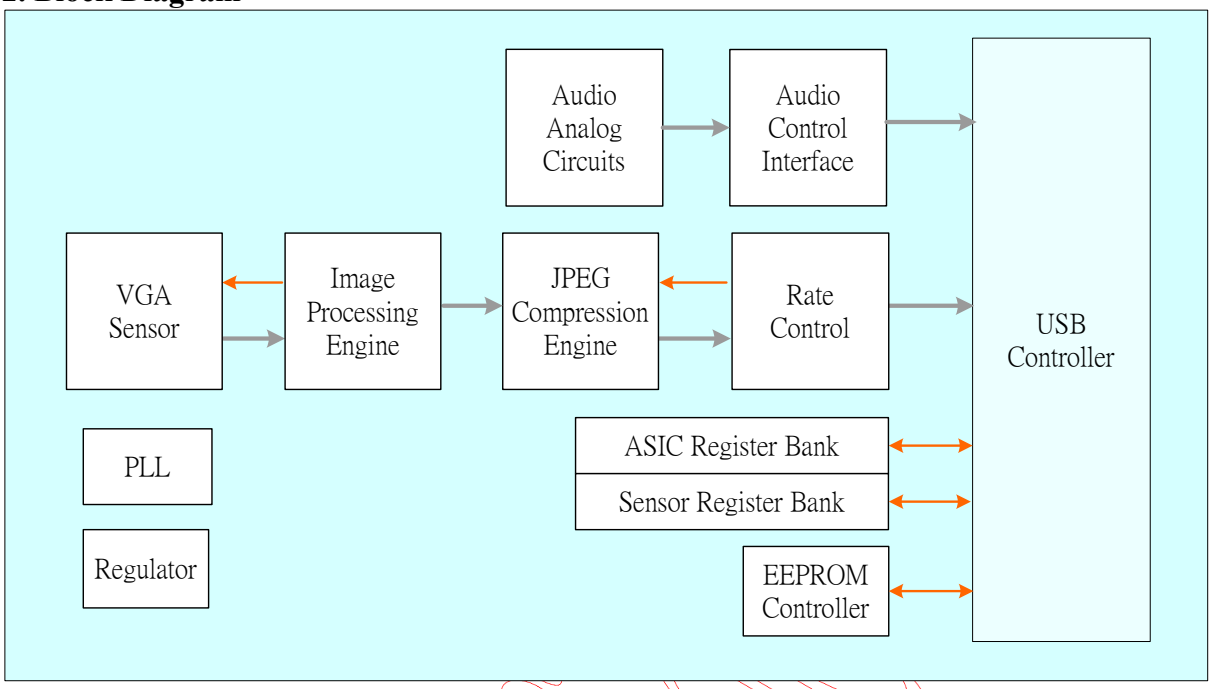
2. Block Diagram



PAC7312 is a single-chip USB camera. It includes a VGA sensor based on PixArt VGA sensor with enhanced image quality and sensitivity, a 48MHz PLL, internal regulators, JPEG image compression, image processing schemed, control registers, on-chip SRAM for image data buffer and USB controller. All register parameters are set by USB interface. And the JPEG compressed image data is transmitted by USB 1.1 isochronous pipe.

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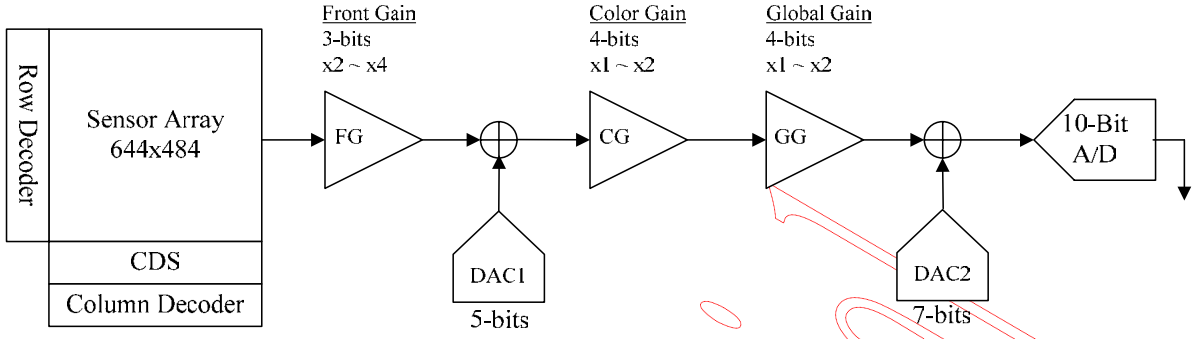
3. Function Description

3.1 Analog Data Path



The PixArt VGA sensor is a 1/4inch CMOS imaging sensor with 644x488 physical pixels. The active region of sensor array is 644x484. The sensor array is cover with Bayer pattern color filters and micro lens.

After a programmable exposure time, the image is sampled first with CDS (Correlated Double Sampling) block to improve S/N ration and reduce fixed pattern noise.

Three analog gain stages are implemented before signal transferred by the 10bit ADC. The front gain stage (FG) can be programmed to fit the saturation level of sensor to the full-range input of ADC. The programmable color gain stage (CG) is used to balance the luminance response difference between B/G/R. The global gain stage (GG) is programmed to adapt the gain to the image luminance.

The fine gained signal will be digitized by the on-chip 10bit ADC. After the image data has been digitized, further alteration to the signal can be applied before the data is output.

The gain stage can be set by digital register, please refer to the following equation to get the mapping gain.

Front Gain =	**2 + (n/4),**	**n = 0, 1, 2, …7**
Color Gain =	**1 + (m/16),**	**m= 0, 1, 2, …15**
Global Gain =	**1 + (q/16),**	**q = 0, 1, 2, …15**

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4. Specifications

Absolute Maximum Ratings

Exposure to absolute maximum rating may affect device reliability.

Symbol	Parameter	Min	Max	Unit	Notes
V_{DD}	DC supply voltage	-0.5	5.5	V	
V_{IN}	DC input voltage	0.5	3.8	V	
V_{OUT}	DC output voltage	-0.5	3.8	V	
T_{STG}	Storage temperature	0	70	℃	

Recommend Operating Condition

Symbol	Parameter	Min	Typ.	Max	Unit	Notes
T_A	Operating Temperature	0	-	40	℃	
V_{DD}	Power supply voltage	4.25	5.0	5.5	V	
F_{CLK}	System clock frequency	-	12	-	MHz	

DC Electrical Characteristics (Typical values at 25°C, V_{DD} =5.0 V)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Type: PWR						
I_{DD}	Operating Current		65		mA	@30 frame/sec
Type: IN & I/O, Reset						
V_{IH}	Input voltage HIGH	2.0		V_{DDQ}	V	
V_{IL}	Input voltage LOW	0		0.8	V	
C_{IN}	Input capacitor			10	pF	
I_{LKG}	Input leakage current			1.0	uA	
Type: OUT & I/O						
V_{OH}	Output voltage HIGH	V_{DDQ}-0.2			V	C_L= 10pf, R_L=1.2kΩ
V_{OL}	Output voltage LOW			0.2	V	C_L= 10pf, R_L=1.2kΩ

Sensor Characteristics (Light source: 3200K halogen lamp; 8bit resolutions)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
PRNU	Photo response non-uniformity	-	1.3	-	%	
VSAT	Saturation output voltage	-	0.832	-	V	
VDARK	Dark output voltage	-	0.055	-	V/sec	
DSNU	Dark signal non-uniformity	-	0.001	-	V	
R	Sensitivity (Red channel)	-	4.590	-	V/Lux*sec	
G	Sensitivity (Green channel)	-	3.060	-	V/Lux*sec	
B	Sensitivity (Blue channel)	-	2.448	-	V/Lux*sec	

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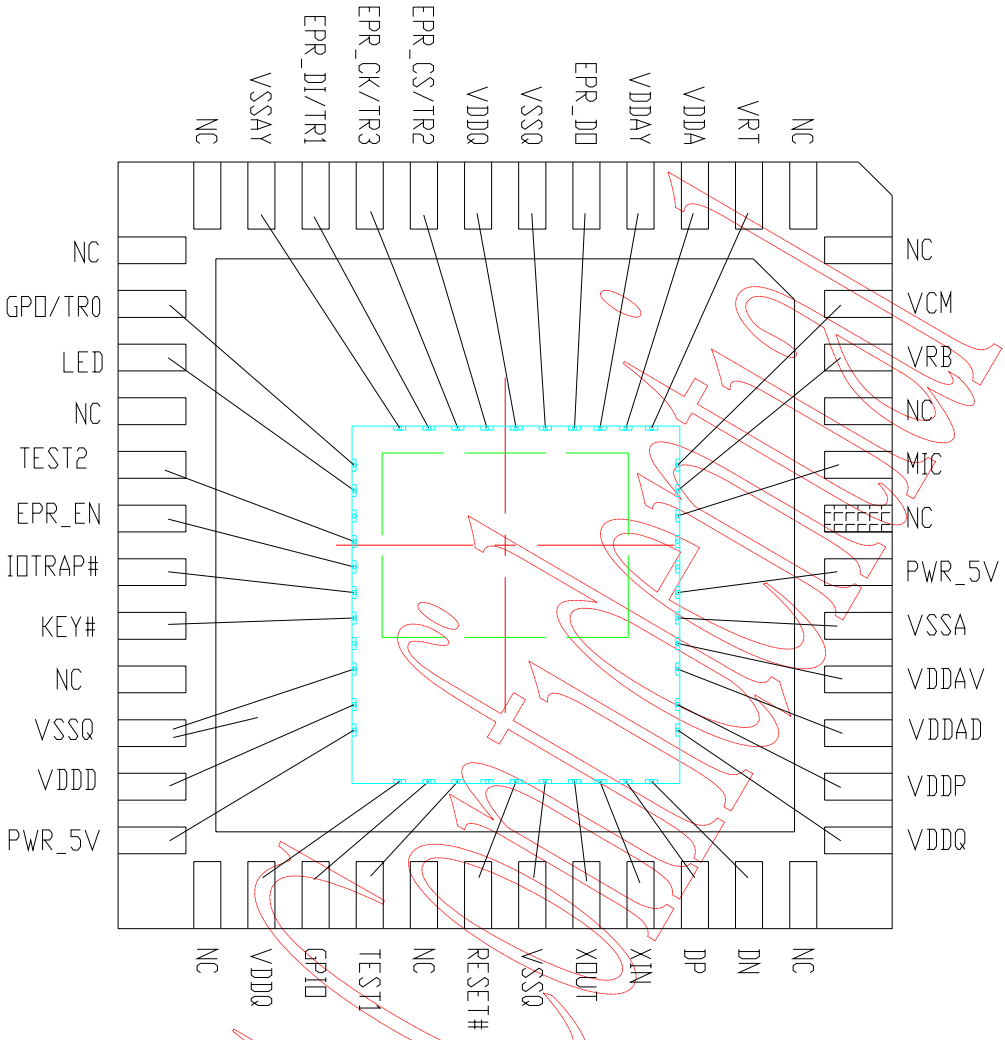
5. Package Information

5.1 PLCC Pin Assignment and Optical Center Information



Note: Sensor Array Center = Package Center

--TOP VIEW—

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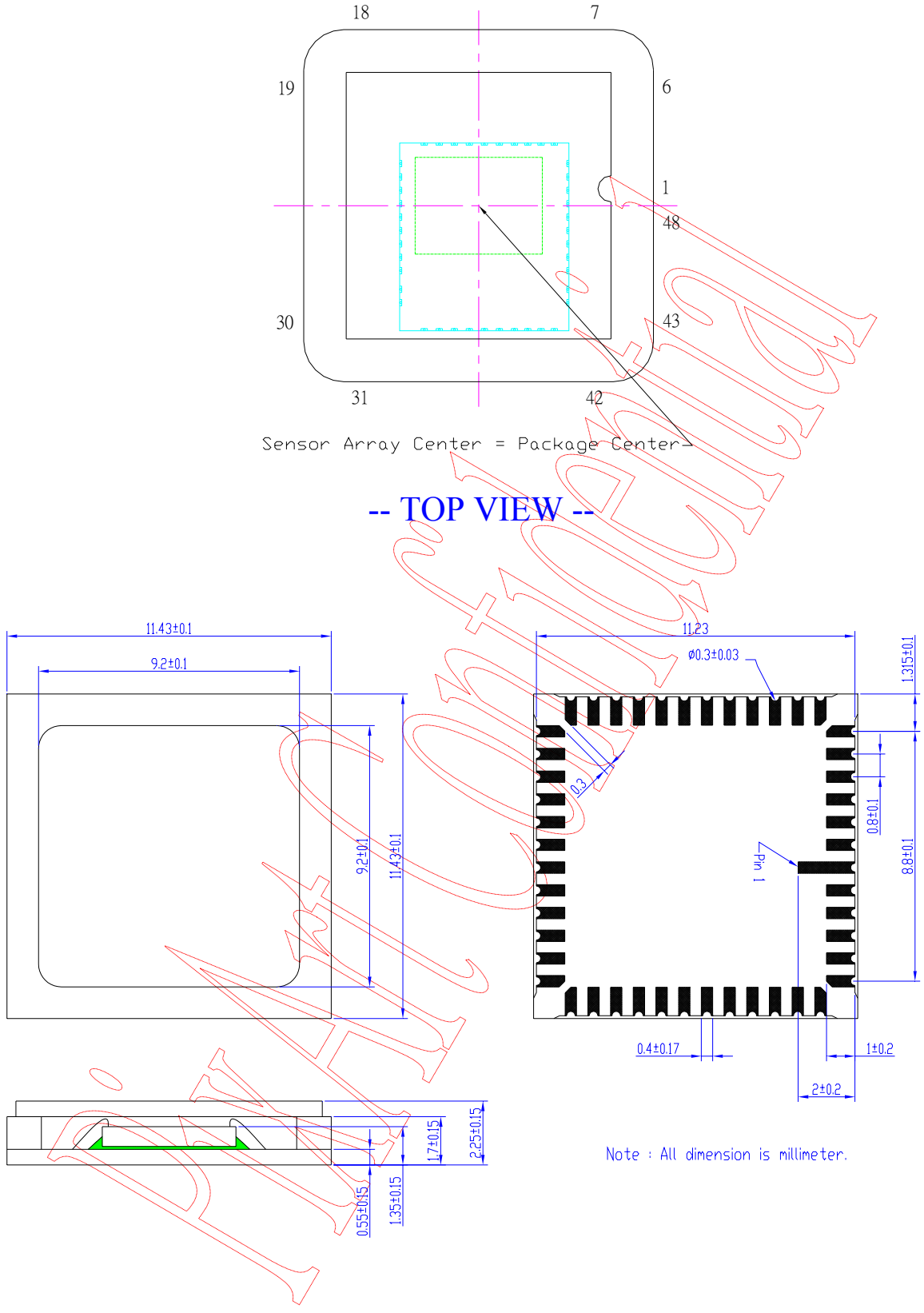
5.2 PLCC Package Outline Dimension



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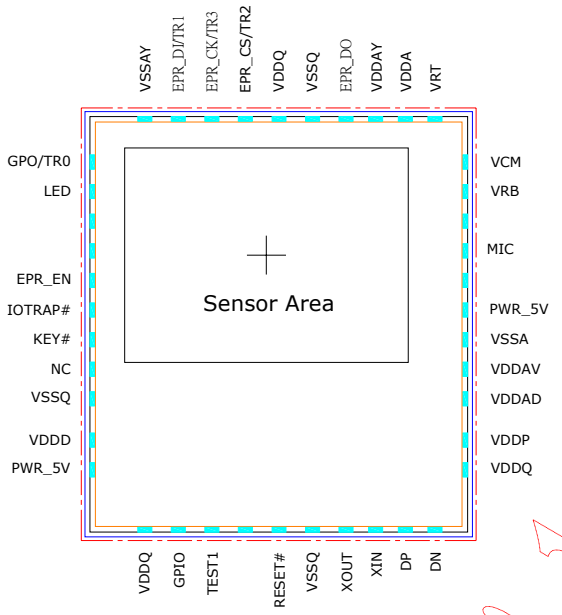
5.3 CSP Pin Assignment

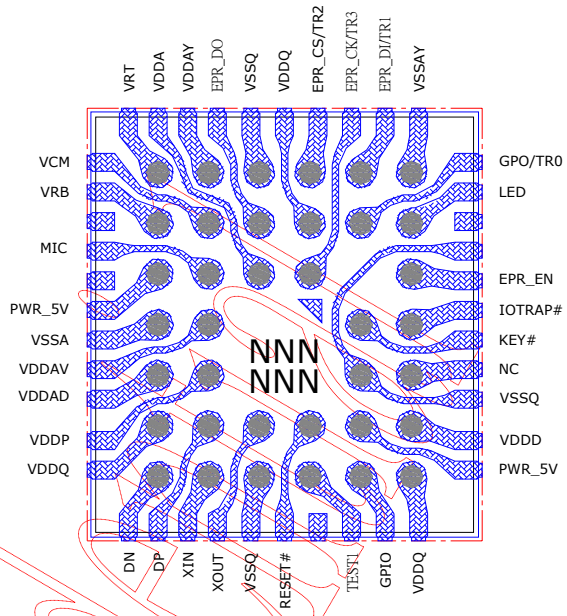
Pad Extension Formation



Top view (Bumps down)

Step Size : 5061 x 5551 um
Die Size : 4841 x 5331 um
Ball Pitch : 650 um
Ball Diameter : 300 um
Scribe Line : 360 um

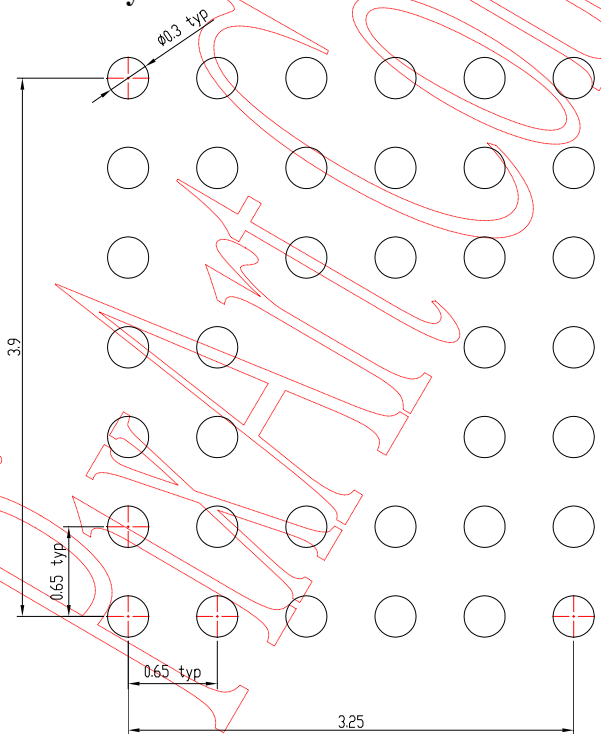
Leads & BGA Formation



Buttom view (Bumps up)

Package Size : 4966 x 5456 um
Marking Code : NNNNNN - Datecode

5.4 Recommend PCB Layout



Note:

1. All diemnsion is millimeter.
2. Top View

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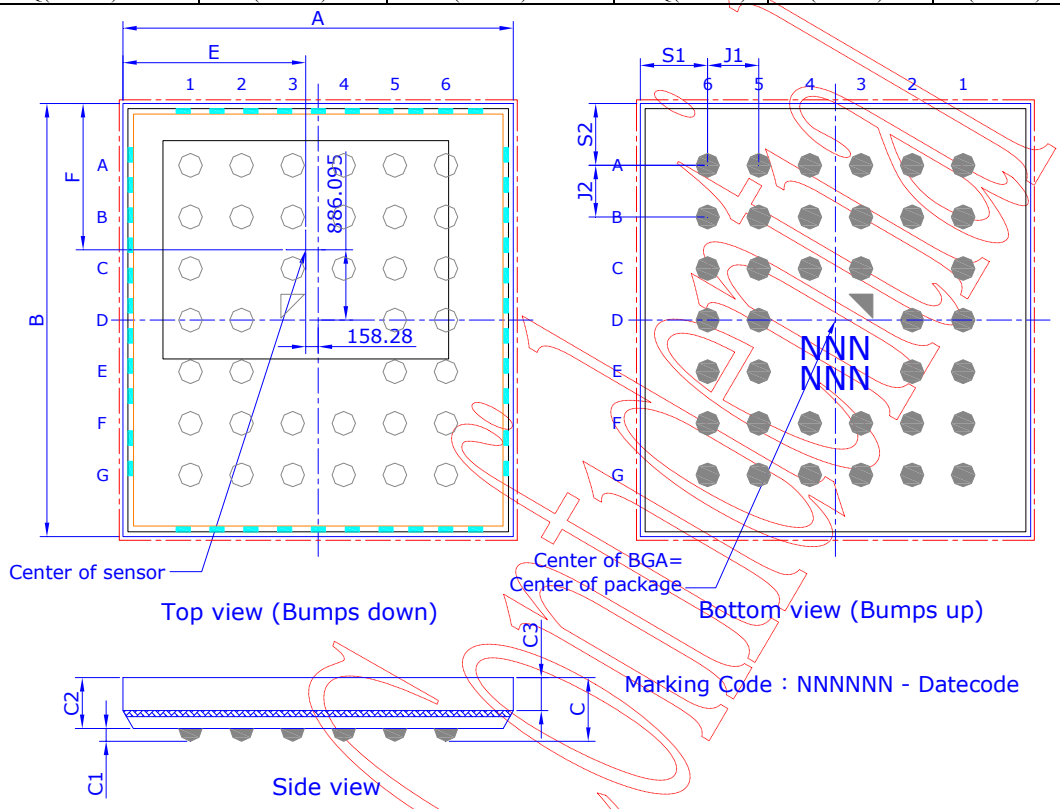
5.5 CSP Package Dimensions and Ball Matrix Table

	1	2	3	4	5	6
A	VSSAY(PIN 13)	EPR_DI/TR(PIN 12)	EPR _CS/TR2(PIN 10)	VSSQ(PIN 8)	VDDAY(PIN 6)	VRT(PIN 4)
B	LED(PIN 15)	GPO/TR0(PIN 14)	VDDQ(PIN 9)	EPR _D0(PIN 7)	VCM(PIN 3)	VRB(PIN 2)
C	VSSQ/EPR_EN(PIN 16)		EPR _CK/TR3(PIN 11)	VDDA(PIN 5)	MIC(PIN 1)	PWR_5V(PIN 37)
D	IOTRAP# (PIN 17)	KEY# (PIN 18)			VDDAV(PIN 35)	VSSA(PIN 36)
E	NC(PIN 19)	VSSQ(PIN 20)			VDDP(PIN 33)	VDDAD(PIN 34)
F	VDDD(PIN 21)	PWR_5V(PIN 22)	RESET# (PIN 26)	XOUT(PIN 28)	DP(PIN 30)	VDDQ(PIN 32)
G	VDDQ(PIN 23)	GPIO(PIN 24)	TEST1(PIN 25)	VSSQ(PIN 27)	XIN(PIN 29)	DN(PIN 31)



	Symbol	Nominal	Min.	Max.
			μm	
Package Body Dimension X	**A**	4966	4941	4991
Package Body Dimension Y	**B**	5456	5431	5481
Package Height	**C**	800	740	860
Ball Height	**C1**	160	130	190
Package Body Thickness	**C2**	640	605	675
Thickness of Glass surface to wafer	**C3**	415	395	435
Ball Diameter	**D**	300	270	330
Total Pin Count	**N**	37		
Pin Count X axis	**N1**	6		
Pin Count Y axis	**N2**	7		
Pins Pitch X axis	**J1**	650		
Pins Pitch Y axis	**J2**	650		
Edge to Pin Center Distance analog X	**S1**	858	828	888
Edge to Pin Center Distance analog Y	**S2**	778	748	808
Edge to Optical Center Distance analog X	**E**	2325	2300	2350
Edge to Optical Center Distance analog Y	**F**	1842	1817	1867

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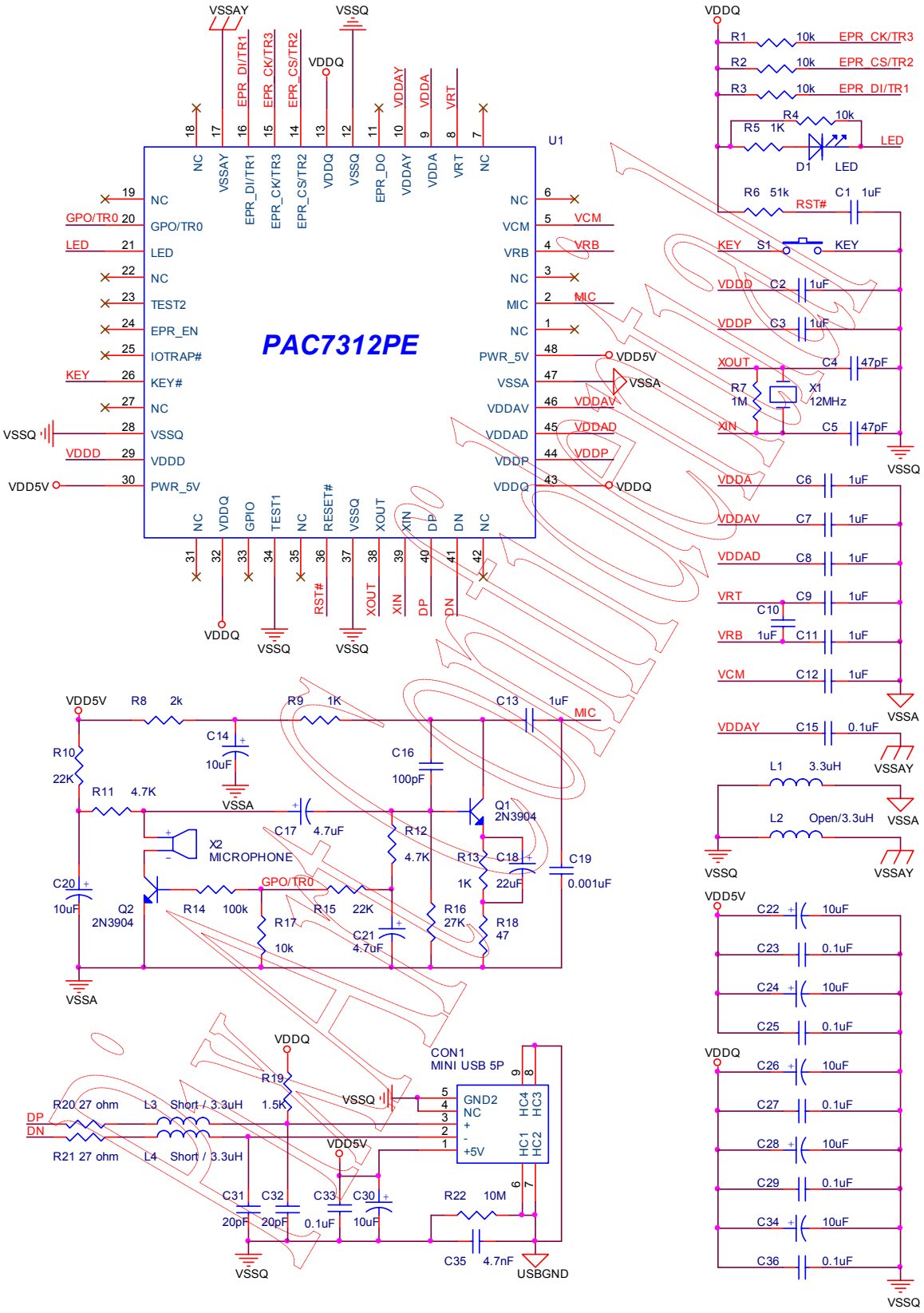
6. Reference Application Circuit

6.1 PLCC Package (PAC7312PE)



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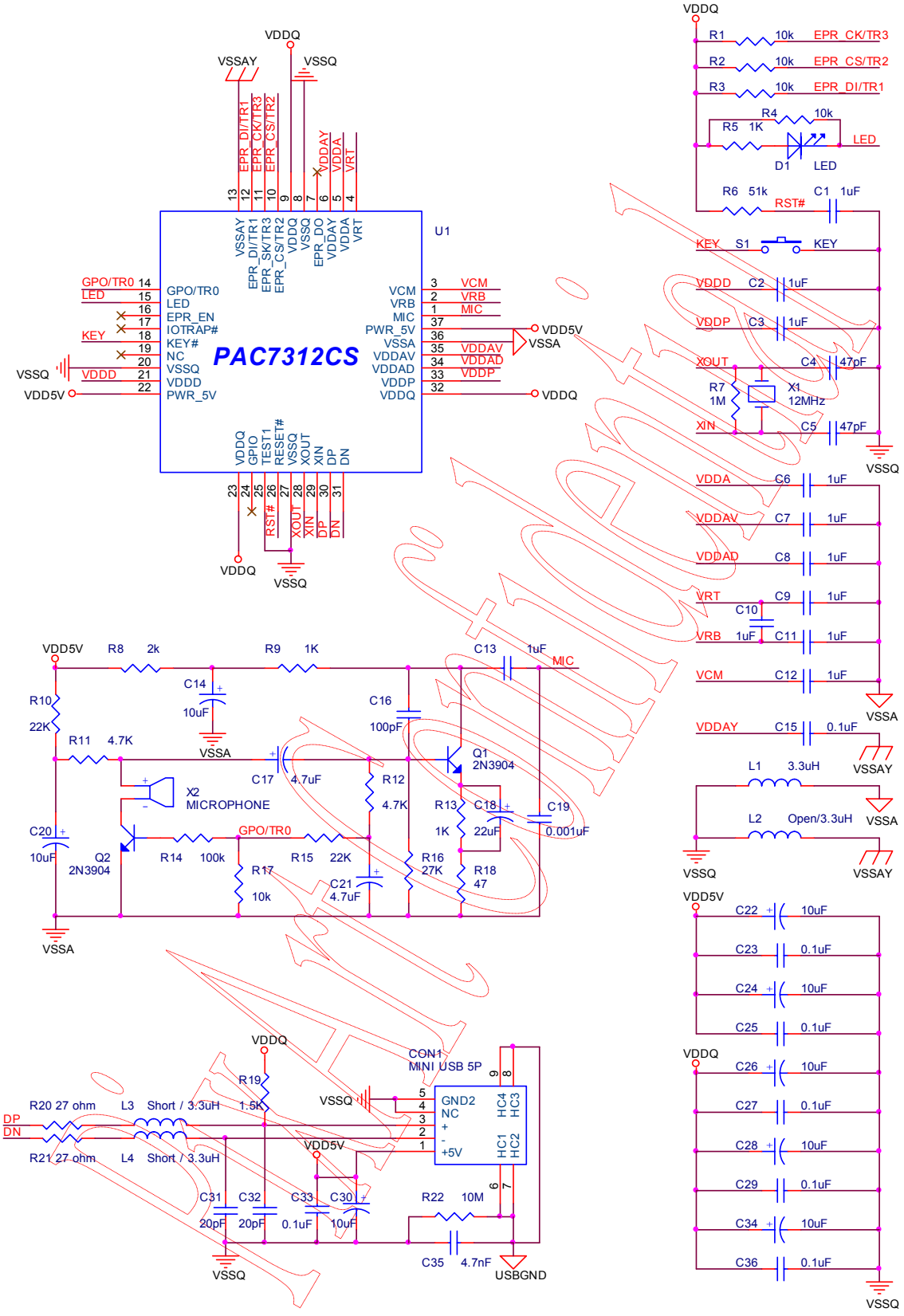
6.2 CSP Package (PAC7312CS)



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7. Update History

Version	Update	Date
V1.0	Creation, Preliminary 1st version	10/27/2004
V1.1	4. Specifications 5. Package information	10/29/2004
V1.2	4. Specifications 5. Package information	11/04/2004
V1.3	4. Specifications 5. Package information 6. Reference Application Circuit	06/28/2005
V1.4	5. Package information 6. Reference Application Circuit	07/01/2005
V1.5	General Description 5. Package information 6. Reference Application Circuit (Change list: C4, C5, C13, C14, C17, C19, C20, C21, R8, R9, R10, R11, R12, R15, R18, L2)	10/07/2005

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