PAC7302 VGA Output PC Camera SOC with Audio

PAC7301 VGA Output PC Camera SOC without Audio

General Description

The PAC7301/PAC7302 is a VGA output PC Camera SOC with embedded CMOS image sensor and USB 1.1 interface. It embedded a JPEG image compression engine and an image signal processor (ISP). The JPEG decoder and auto exposure control are performed by software in PC side. The PAC7301/PAC7302 can achieve a compact module size by using it's 1/6" optical size which can easily be embedded in LCD monitors and notebooks. The chip provides IO-trapping pins with internal pull-up resistors. Hence it is flexible for customers to set PID on module PCB. It supports an interface connect to a serial-EEPROM. When the EEPROM function is enabled, the internal control register setting will be auto loaded to the external EEPROM. This allows customization of VID, PID, product string…etc. PAC7301/PAC7302 also provide a high quality audio ADC function for sound recording. The audio-in function complies with USB audio device class 1.0. The PAC7301/PAC7302 is powered by 5V and in PLCC/CSP/LGA package

1. Feature

- Embedded CMOS image sensor with VGA output
- Frame rate up to 30fps@VGA for PC mode video
- Embedded PixArt 3rd generation ISP and JPEG compression engine
- AEC/AGC/AWB automatic
- On chip 10bit ADC for image date converter
- External 12MHz crystal input
- 5 IO-trapping pins to set USB PID
- Support video data transfer through USB isochronous transfer
- Snapshot and LED control function
- Built-in EEPROM controller for customized VID, PID etc
- USB1.1 compliance and support USB suspend mode
- Embedded audio function (PAC7301/PAC7302)
  - -- 10bits ADC for audio recording through microphone,
  - -- sampling rate @ 16K/48KHz, 16bits PCM format
  - -- USB audio device class 1.0 compatible
- On chip regulator(LDO) for internal use
- 5V single power supply

Frame rate up to 30fps at following resolution format
.. VGA format (640x480) with JPEG compression
.. CIF format (352x288) with JPEG compression
.. QVGA format (320x240) with JPEG compression
.. QCIF format (176x144) without compression
.. QQVGA format (160x120) without compression

2. Ordering Information

Order number	Package Type	Package Size(mm)
PAC7302PE	48-pin PLCC	11.43 x 11.43
PAC7302PM	40-pin PLCC	9.0x9.0
PAC7301/PAC7302LT	35-pin CSP	3.95x3.95
PAC7302LG	30-pin LGA	3.95x3.95

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PixArt Imaging Inc.
E-mail: fae_service@PixArt.com.tw

3. Pin Assignment

3.1 PLCC Package(11.43X11.43)

Pin#	Name	Type	Description
1	MIC_N	IN	Microphone negative input
2	VSSA_AUDIO	GND	Audio analog circuit GND
3	VDDADC33	BYPASS	Audio ADC power ,3.3V
4	GPI3	IN	General purpose input pin
5	GPO1	OUT	General purpose output pin
6	NC	-	No Connection
7	NC	-	No Connection
8	TEST2	IN	Test pin. Connect to GND in normal operation mode, internal pull-down 100Kohm
9	RESET#	IN	Chip power up reset
10	GPI1	IN	General purpose input pin
11	VSSQ	GND	Digital Ground for I/O and PHY, digital core.
12	EPR_DO/TR3	IN	Data out of EEPROM (IO trap pin for PID3, internal pull-up 100Kohm)
13	EPR_DI/TR0	OUT	Data input of EEPROM (IO trap pin for PID0, internal pull-up 100Kohm)
14	EPR_SK/TR2	OUT	Serial clock of EEPROM (IO trap pin for PID2, internal pull-up 100Kohm)
15	EPR_CS/TR1	OUT	Chip select of EEPROM (IO trap pin for PID1, internal pull-up 100Kohm)
16	LED	OUT	LED driver
17	GPI2	IN	General purpose input pin
18	NC	-	No Connection
19	NC	-	No Connection
20	EPR_EN	IN	EEPROM enable pin active high
21	AUD_EnH	IN	Audio enable pin, High active, internal pull-up 100Kohm
22	VSSQ	GND	Digital Ground for I/O and PHY, digital core.
23	VDDD	BYPASS	Logic power for digital circuit, 1.8V
24	VDDMD5	PWR	5V power for digital circuit
25	VDDQ	BYPASS	Power for I/O and PHY, 3.3V
26	OSC_OUT	OUT	Crystal output
27	OSC_IN	IN	Crystal input
28	DN	I/O	DN for USB1.1 PHY
29	DP	I/O	DP for USB1.1 PHY
30	NC	-	No Connection
31	NC	-	No Connection
32	GPO2	OUT	General purpose output pin, internal pull-up 100Kohm, reserve VID
33	KEY#	IN	Snapshot control signal (Active Low, internal pull-up 100Kohm)
34	VSSA	GND	Analog ground
35	VSSAY	GND	Sensor ground
36	VDDA	BYPASS	Analog power for Video PGA/ADC 2.5V
37	VDDAYM	BYPASS	Analog power for sensor CDS 2.5V
38	VDDAY	BYPASS	Analog power for sensor array 2.5V
39	VDDA33	BYPASS	Analog power output 3.3V(for 2.5 regulator use)
40	VDDMA5	PWR	5V power for video analog circuit
41	TEST1	IN	Test pin. Connect to GND in normal operation mode, internal pull-down 100Kohm
42	NC	-	No Connection
43	NC	-	No Connection
44	VDDMA5_AUD	PWR	5V power for analog audio circuit
45	VDDPGA33	BYPASS	Analog power output for audio PGA 3.3V
46	VCOM	BYPASS	Microphone common mode voltage reference(audio power)

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47	VDDMIC28	BYPASS	Analog MIC reference audio power 2.8V
48	MIC_P	IN	Microphone positive input

3.2 PLCC Package(9X9)

Pin#	Name	Type	Description
1	MIC_N	IN	Microphone negative input
2	VSSA_AUDIO	GND	Audio analog circuit GND
3	VDDADC33	BYPASS	Audio ADC power ,3.3V
4	GPI3	IN	General purpose input pin
5	GPO1	OUT	General purpose output pin
6	TEST2	IN	Test pin. Connect to GND in normal operation mode, internal pull-down 100Kohm
7	RESET#	IN	Chip power up reset
8	GPI1	IN	General purpose input pin
9	VSSQ	GND	Digital Ground for I/O and PHY, digital core.
10	EPR_DO/TR3	IN	Data out of EEPROM (IO trap pin for PID3, internal pull-up 100Kohm)
11	EPR_DI/TR0	OUT	Data input of EEPROM (IO trap pin for PID0, internal pull-up 100Kohm)
12	EPR_SK/TR2	OUT	Serial clock of EEPROM (IO trap pin for PID2, internal pull-up 100Kohm)
13	EPR_CS/TR1	OUT	Chip select of EEPROM (IO trap pin for PID1, internal pull-up 100Kohm)
14	LED	OUT	LED driver
15	GPI2	IN	General purpose input pin
16	EPR_EN	IN	EEPROM enable pin active high
17	AUD_EnH	IN	Audio enable pin, High active, internal pull-up 100Kohm
18	VSSQ	GND	Digital Ground for I/O and PHY, digital core.
19	VDDD	BYPASS	Logic power for digital circuit, 1.8V
20	VDDMD5	PWR	5V power for digital circuit
21	VDDQ	BYPASS	Power for I/O and PHY, 3.3V
22	OSC_OUT	OUT	Crystal output
23	OSC_IN	IN	Crystal input
24	DN	I/O	DN for USB1.1 PHY
25	DP	I/O	DP for USB1.1 PHY
26	GPO2	OUT	General purpose output pin, internal pull-up 100Kohm, reserve VID
27	KEY#	IN	Snapshot control signal (Active Low, internal pull-up 100Kohm)
28	VSSA	GND	Analog ground
29	VSSAY	GND	Sensor ground
30	VDDA	BYPASS	Analog power for Video PGA/ADC 2.5V
31	VDDAYM	BYPASS	Analog power for sensor CDS 2.5V
32	VDDAY	BYPASS	Analog power for sensor array 2.5V
33	VDDA33	BYPASS	Analog power output 3.3V(for 2.5 regulator use)
34	VDDMA5	PWR	5V power for video analog circuit
35	TEST1	IN	Test pin. Connect to GND in normal operation mode, internal pull-down 100Kohm
36	VDDMA5_AUD	PWR	5V power for analog audio circuit
37	VDDPGA33	BYPASS	Analog power output for audio PGA 3.3V
38	VCOM	BYPASS	Microphone common mode voltage reference(audio power)
39	VDDMIC28	BYPASS	Analog MIC reference audio power 2.8V
40	MIC_P	IN	Microphone positive input

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3.3 CSP Package

Pin#	Name	Type	Description
1	GPO1	OUT	General purpose output pin
2	VDDADC33	BYPASS	Audio ADC power ,3.3V
3	MIC_N	IN	Microphone negative input
4	VDDMIC28	BYPASS	Analog MIC reference audio power 2.8V
5	VDDPGA33	BYPASS	Analog power output for audio PGA 3.3V
6	VDDMA5_AUD	PWR	5V power for analog audio circuit
7	RESET#	IN	Chip power up reset
8	GPI3	IN	General purpose input pin
9	VSSA_AUDIO	GND	Audio analog circuit GND
10	MIC_P	IN	Microphone positive input
11	VDDMA5	PWR	5V power for video analog circuit
12	VDDA33	BYPASS	Analog power output 3.3V(for 2.5 regulator use)
13	VSSQ	GND	Digital Ground for I/O and PHY, digital core.
14	GPI1	IN	General purpose input pin
15	VCOM	BYPASS	Microphone common mode voltage reference(audio power)
16	VDDAY	BYPASS	Analog power for sensor array 2.5V
17	VDDAYM	BYPASS	Analog power for sensor CDS 2.5V
18	EPR_DI/TR0	OUT	Data input of EEPROM (IO trap pin for PID0, internal pull-up 100Kohm)
19	EPR_SK/TR2	OUT	Serial clock of EEPROM (IO trap pin for PID2, internal pull-up 100Kohm)
20	EPR_DO/TR3	IN	Data out of EEPROM (IO trap pin for PID3, internal pull-up 100Kohm)
21	VDDA	BYPASS	Analog power for Video PGA/ADC 2.5V
22	KEY#	IN	Snapshot control signal (Active Low, internal pull-up 100Kohm)
23	VSSAY	GND	Sensor ground
24	EPR_CS/TR1	OUT	Chip select of EEPROM (IO trap pin for PID1, internal pull-up 100Kohm)
25	LED	OUT	LED driver
26	VDDD	BYPASS	Logic power for digital circuit, 1.8V
27	VDDQ	BYPASS	Power for I/O and PHY, 3.3V
28	OSC_IN	IN	Crystal input
29	VSSA	GND	Analog ground
30	EPR_EN	IN	EEPROM enable pin active high
31	VSSQ	GND	Ground for I/O and PHY
32	VDDMD5	PWR	5V power for digital circuit
33	OSC_OUT	OUT	Crystal output
34	DN	I/O	DN for USB1.1 PHY
35	DP	I/O	DP for USB1.1 PHY

3.4 LGA Package

Pin#	Name	Type	Description
1	GPO1	OUT	General purpose output pin
2	VDDADC33	BYPASS	Audio ADC power ,3.3V
3	VSSA_AUDIO	GND	Audio analog circuit GND
4	MIC_N	IN	Microphone negative input
5	MIC_P	IN	Microphone positive input
6	VDDMIC28	BYPASS	Analog MIC reference audio power 2.8V
7	VCOM	BYPASS	Microphone common mode voltage reference(audio power)
8	VDDPGA33	BYPASS	Analog power output for audio PGA 3.3V

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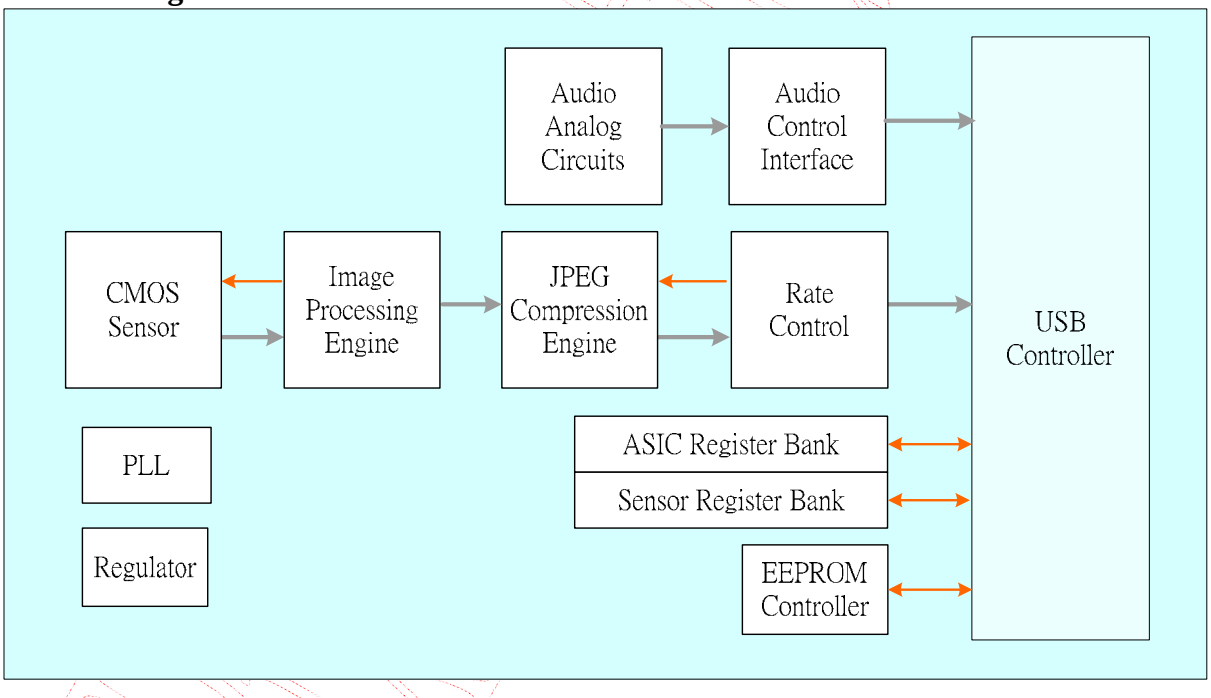
9	VDDMA5	PWR	5V power for video analog circuit
10	VDDA33	BYPASS	Analog power output 3.3V(for 2.5 regulator use)
11	VDDAY	BYPASS	Analog power for sensor array 2.5V
12	VDDAYM	BYPASS	Analog power for sensor CDS 2.5V
13	VDDA	BYPASS	Analog power for Video PGA/ADC 2.5V
14	VSSA	GND	Analog ground
15	KEY#	IN	Snapshot control signal (Active Low, internal pull-up 100Kohm)
16	DP	I/O	DP for USB1.1 PHY
17	DN	I/O	DN for USB1.1 PHY
18	OSC_IN	IN	Crystal input
19	OSC_OUT	OUT	Crystal output
20	VDDQ	BYPASS	Power for I/O and PHY, 3.3V
21	VDDMD5	PWR	5V power for digital circuit
22	VDDD	BYPASS	Logic power for digital circuit, 1.8V
23	VSSQ	GND	Digital Ground for I/O and PHY, digital core.
24	EPR_EN	IN	EEPROM enable pin active high
25	LED	OUT	LED driver
26	NC	-	No Connection
27	NC	-	No Connection
28	VSSQ	GND	Digital Ground for I/O and PHY, digital core.
29	GPI1	IN	General purpose input pin
30	RESET#	IN	Chip power up reset

4. Block Diagram



PAC7301/PAC7302 is a USB PC Camera SOC with enhanced image quality and sensitivity, internal regulators, JPEG image compression, image processing schemed, control registers, on-chip SRAM for image data buffer and USB controller. All register parameters are set by USB interface. And the JPEG compressed image data is transmitted by USB 1.1 isochronous pipe.

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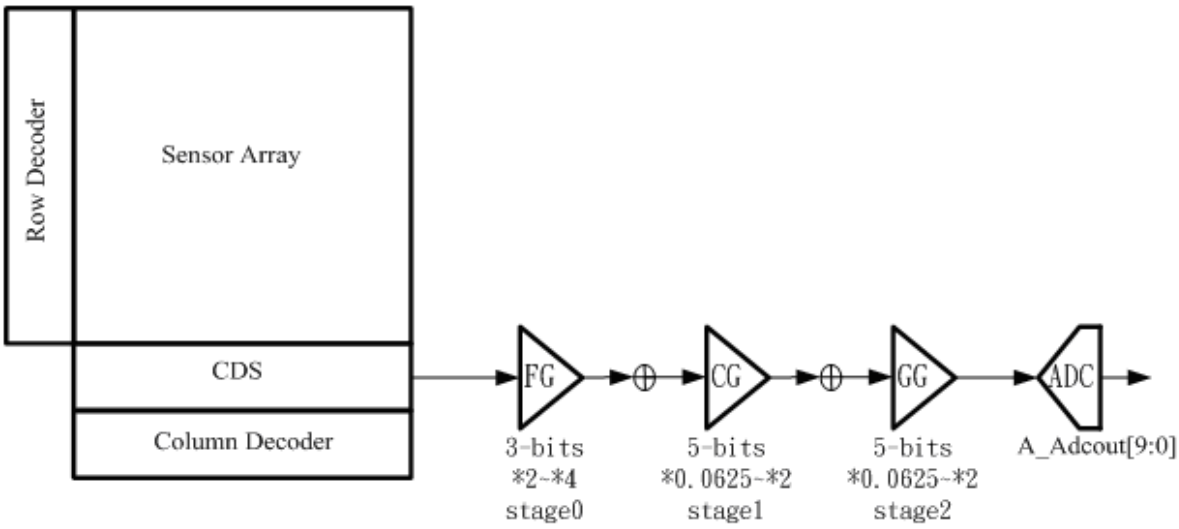
5. Function Description

5.1 Analog Data Path



The sensor array is covered by Bayer pattern color filters and micro lens.

After a programmable exposure time, the image is sampled first with CDS (Correlated Double Sampling) block to improve S/N ration and reduce fixed pattern noise.

Three analog gain stages are implemented before signal transferred by the 10bit ADC. The front gain stage (FG) can be programmed to fit the saturation level of sensor to the full-range input of ADC. The programmable color gain stage (CG) is used to balance the luminance response difference between B/G/R. The global gain stage (GG) is programmed to adapt the gain to the image luminance.

The fine gained signal will be digitized by the on-chip 10bit ADC. After the image data has been digitized, further alteration to the signal can be applied before the data is output.

The gain stage can be set by digital register, please refer to the following equation to get the mapping gain.

Front Gain =	**2 + (n/4),**	**n = 0, 1, 2, …7**
Color Gain =	**(1 +m)/16,**	**m= 0, 1, 2, …31**
Global Gain =	**(1 +q)/16,**	**q = 0, 1, 2, …31**

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6. Specifications

Absolute Maximum Ratings

Exceeding the Absolute Maximum Ratings shown below invalidates all AC and DC electrical specifications and may result in permanent device damage.

Symbol	Parameter	Min	Max	Unit	Notes
T_{STG}	Ambient storage temperature	-25	125	°C	
V_{DD}	DC supply voltage	-0.5	5.5	V	
V_{IN}	DC input voltage	0.5	3.8	V	
V_{OUT}	DC output voltage	-0.5	3.8	V	
ESD	ESD Rating, Human Body model		2	kV	

Recommend Operating Condition

Symbol	Parameter		Min	Typ.	Max	Unit	Notes
T_A	Temperature Range	Operation	-10	-	70	°C	
		Stable Image	0	-	50	°C	
V_{DD}	Power supply voltage		4.5	5.0	5.5	V	
F_{CLK}	System clock frequency		-	12.0	-	MHz	

DC Electrical Characteristics (Typical values at 25°C, V_{DD} =5.0V, F_{CLK}=12.0MHz)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Type: PWR						
I_{DD}	Operating Current	-	35	-	mA	@30 frame/sec
I_{DD}	Suspend Current	-	-	500	uA	
Type: IN & I/O, Reset						
V_{IH}	Input voltage HIGH	2	-	VDDQ	V	
V_{IL}	Input voltage LOW	0	-	0.8	V	
C_{IN}	Input capacitor	-	-	10	pF	
I_{LKG}	Input leakage current	-	-	1.0	uA	
Type: OUT & I/O						
V_{OH}	Output voltage HIGH	Vddq-0.2	-	-	V	C_L= 10pf, R_L=1.2kΩ
V_{OL}	Output voltage LOW	-	-	0.2	V	C_L= 10pf, R_L=1.2kΩ

Sensor Characteristics (Light source: 3200K halogen lamp; 8bit resolutions)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
PRNU	Photo response non-uniformity	-	1.2	-	%	
VSAT	Saturation output voltage	-	1	-	V	
VDARK	Dark output voltage	-	1.08m	-	V/sec	
DSNU	Dark signal non-uniformity	-	0.001	-	V	
R	Sensitivity (Red channel)	-	1.19	-	V/((uw/cm2)*sec)	
G	Sensitivity (Green channel)	-	1.2	-	V/((uw/cm2)*sec)	
B	Sensitivity (Blue channel)	-	0.85	-	V/((uw/cm2)*sec)	

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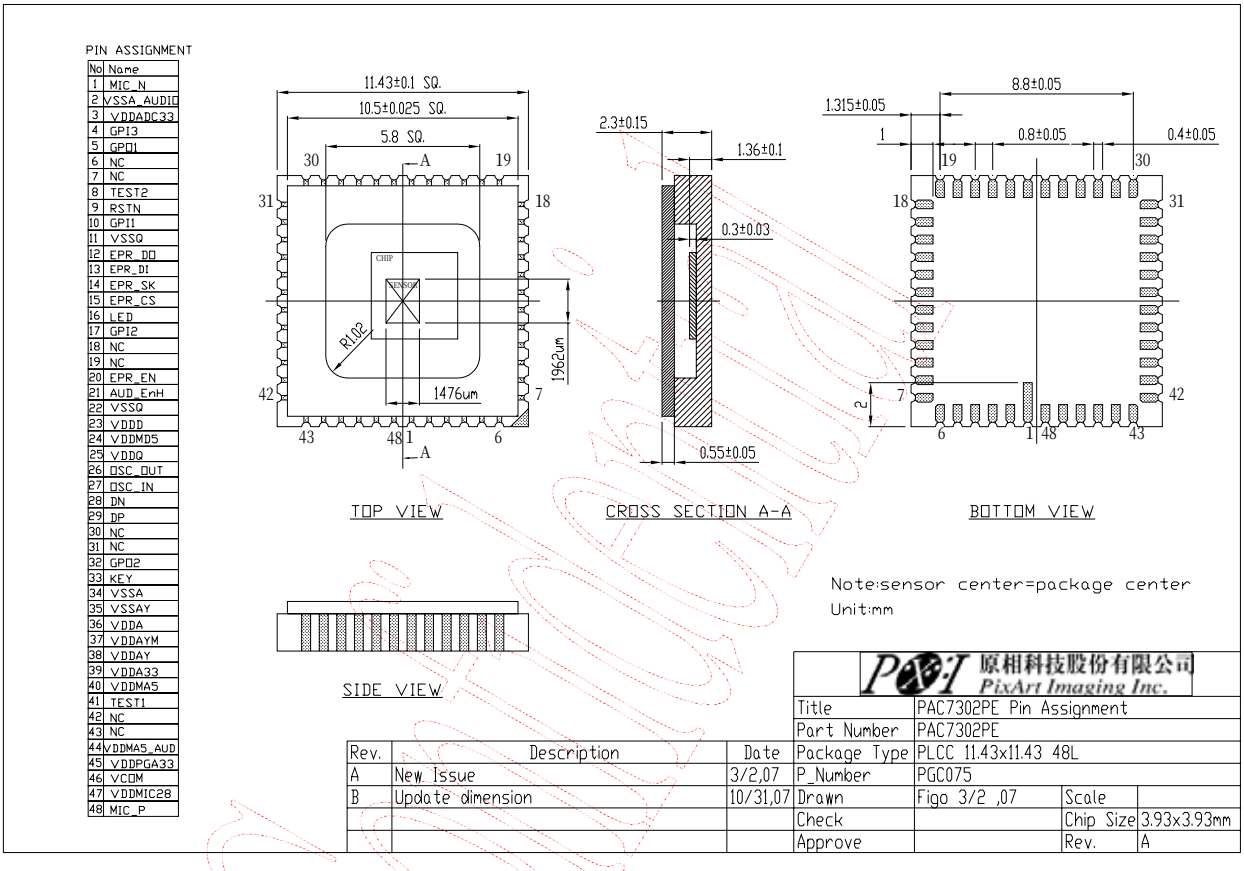
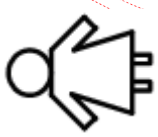
7. Package Information

7.1 .1 PAC7302PE(11.43X11.43) Pin Assignment and Optical Center Information



Note: Sensor Array Center = Package Center



--TOP VIEW—

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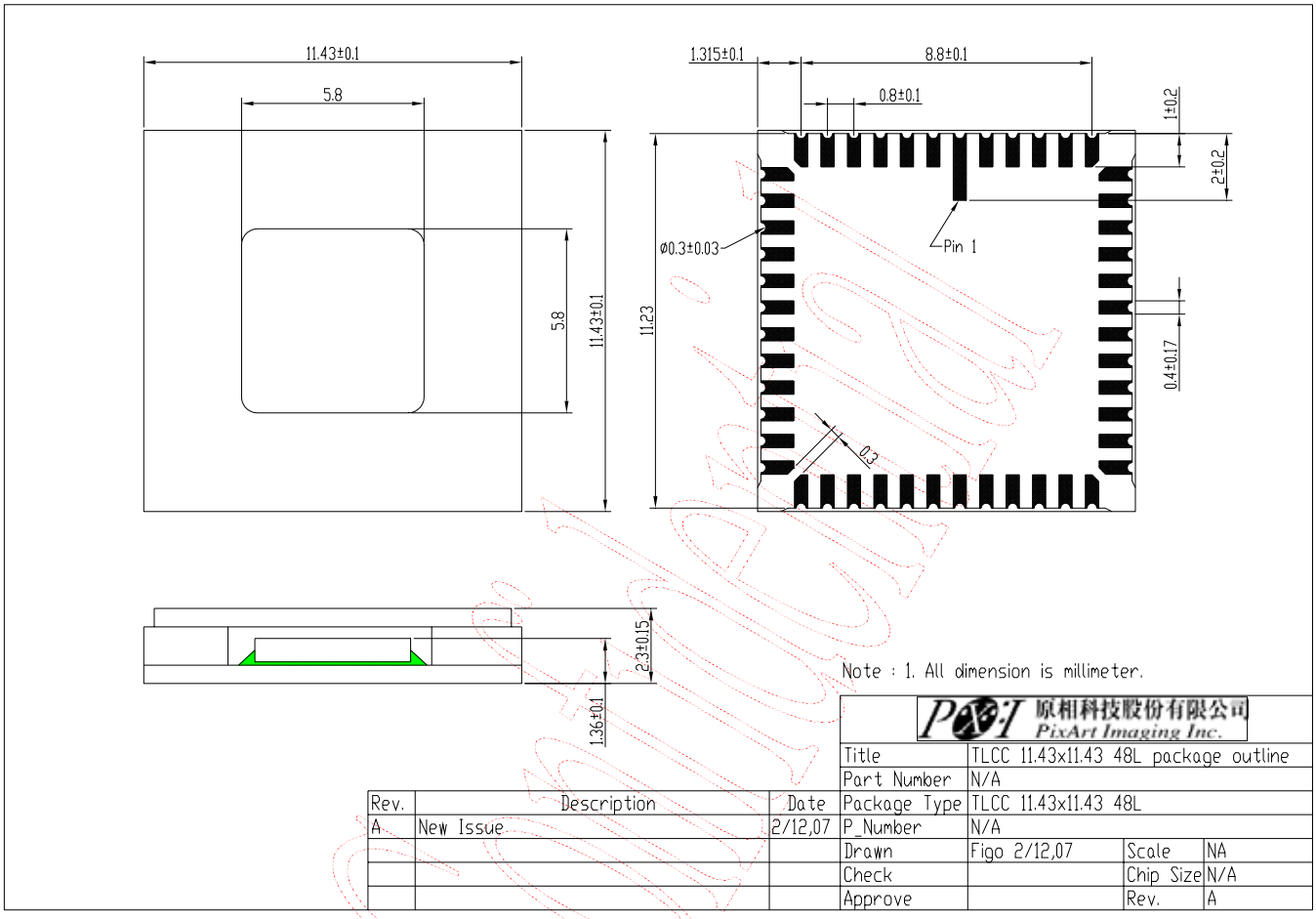
7.1.2 PAC7302PE(11.43X11.43) Package Outline Dimension



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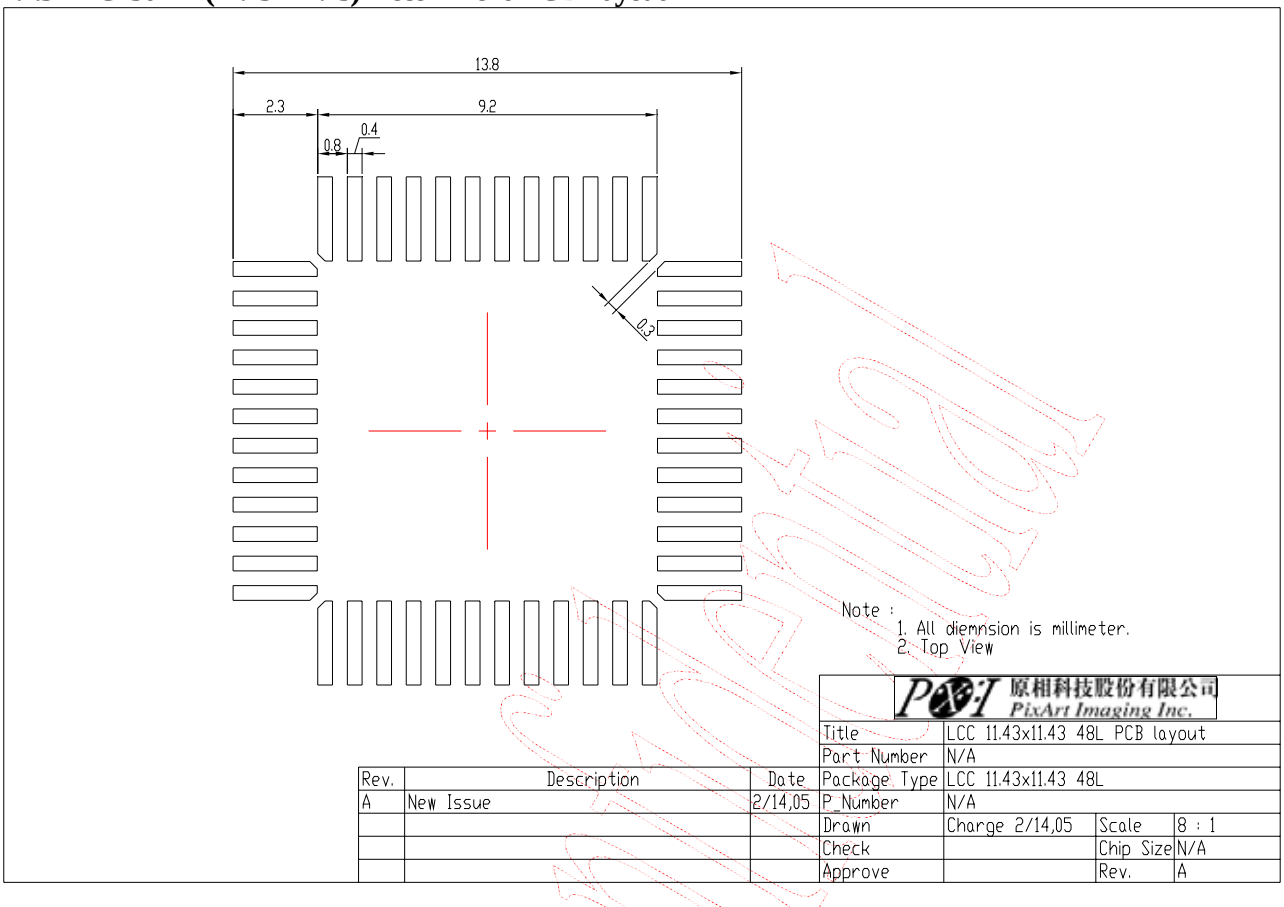
7.1.3 PAC7302PE(11.43X11.43) Recommend PCB Layout



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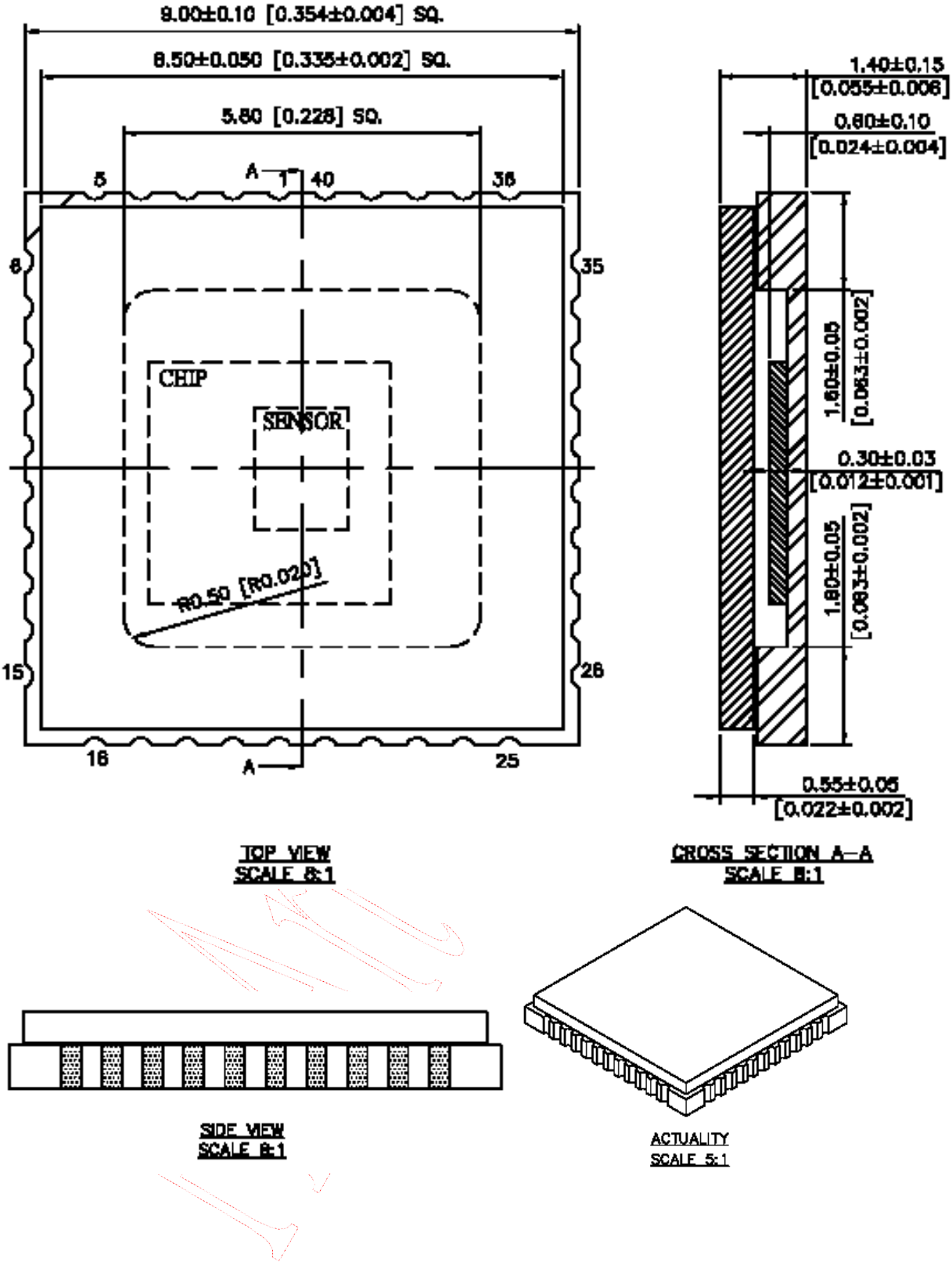
7.2 PAC7302PM(9.0x9.0) Pin Assignment and Optical Center Information



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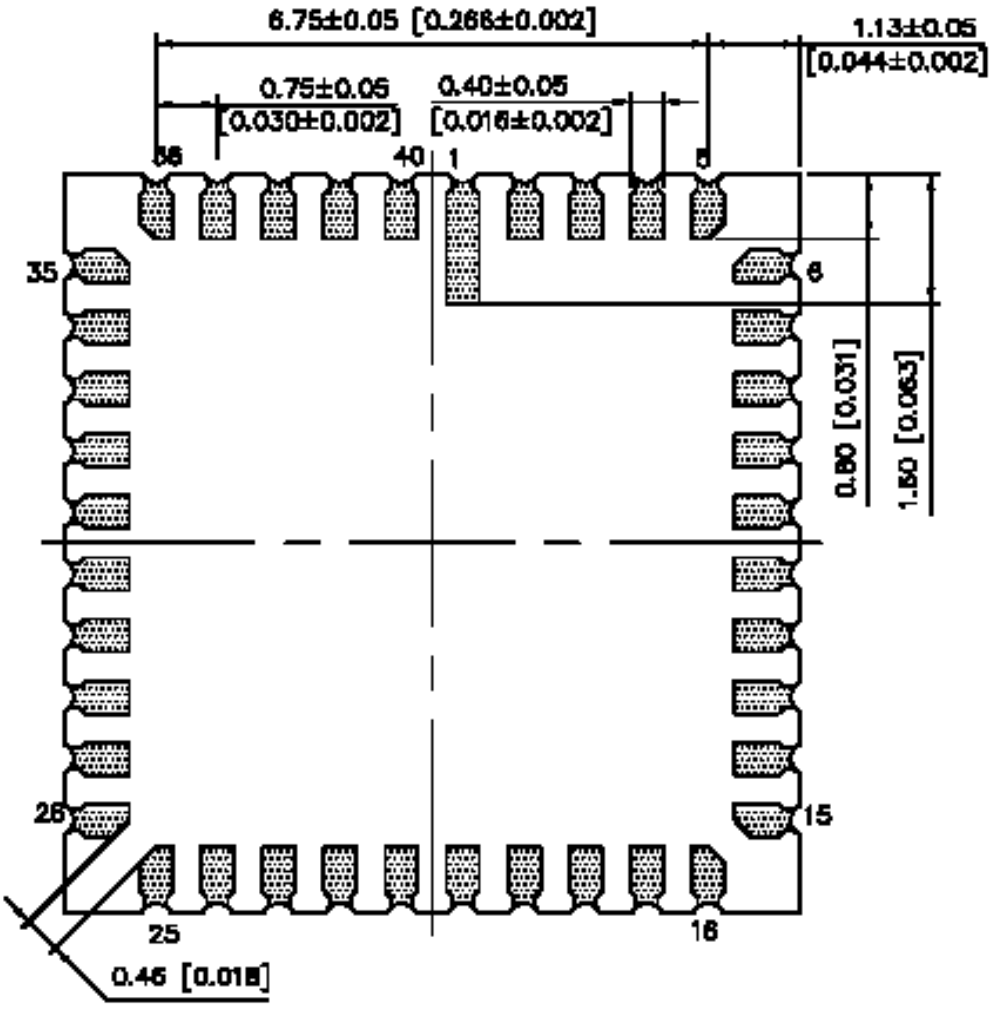

BOTTOM VIEW
SCALE 8:1

PIN ASSIGNMENT

No	Name
1	MIC_N
2	VSSA_AUDIO
3	VDDADC33
4	GPI3
5	GPO1
6	TEST2
7	RSTN
8	GPI1
9	VSSQ
10	EPR_DO
11	EPR_DI
12	EPR_SK
13	EPR_CS
14	LED
15	GPI2
16	EPR_EN
17	AUD_EnH
18	VSSQ
19	VDDD
20	VDDMD5
21	VDDQ
22	OSC_OUT
23	OSC_IN
24	DN
25	DP
26	GPO2
27	KEY
28	VSSA
29	VSSAY
30	VDDA
31	VDDAYM
32	VDDAY
33	VDDA33
34	VDDMA5
35	TEST1
36	VDDMA5_AUD
37	VDDPGA33
38	VCOM
39	VDDMIC28
40	MIC_P

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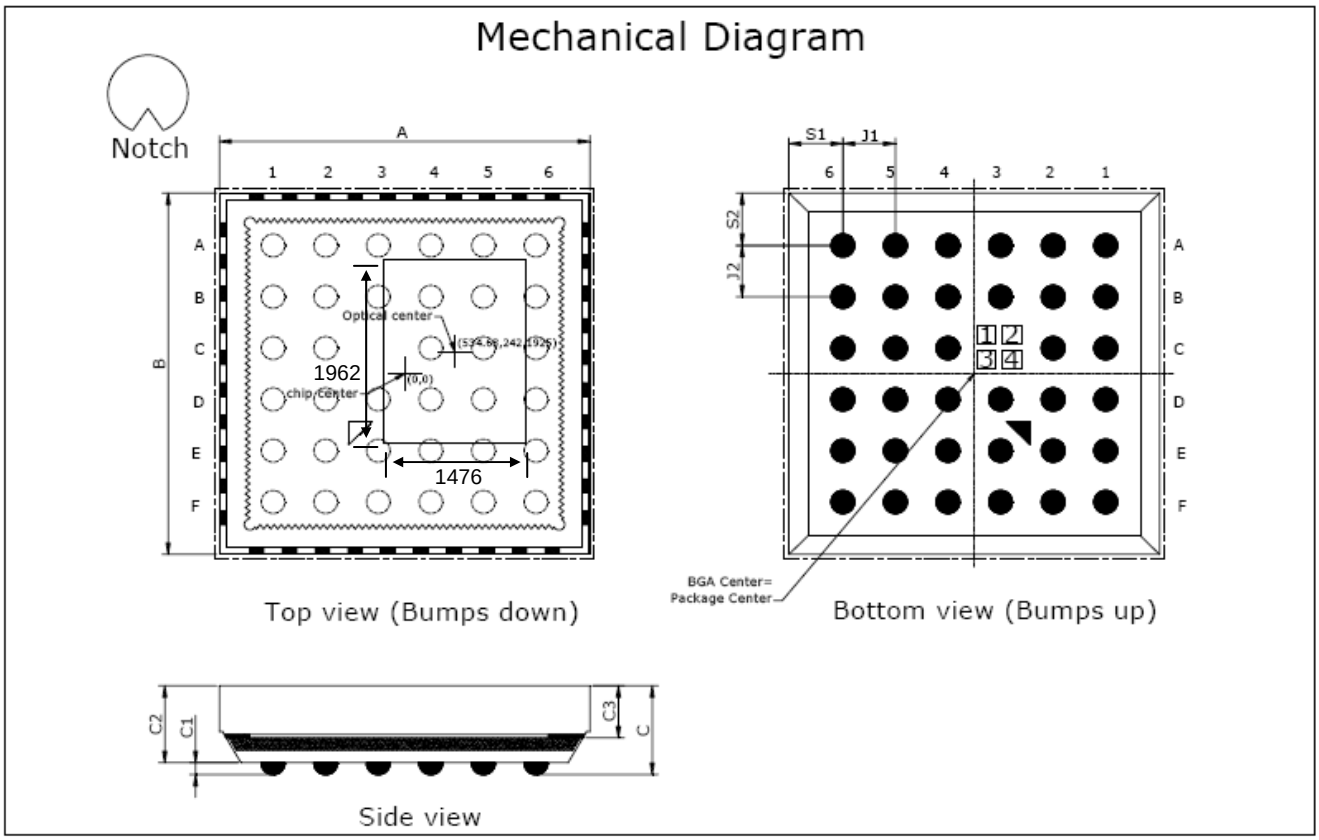
7.3.1 CSP Pin Assignment and Optical Center Information

	Symbol	Nominal	Min.	Max.
			μm	
Package Body Dimension X	A	3947	3922	3972
Package Body Dimension Y	B	3947	3922	3972
Package Height	C	955	895	1015
Ball Height	C1	130	100	160
Package Body Thickness	C2	825	780	870
Thickness of Glass surface to wafer	C3	545	525	565
Ball Diameter	D	250	220	280
Total Pin Count	N	35		
Pin Count X axis	N1	6		
Pin Count Y axis	N2	6		
Pins Pitch X axis	J1	560		
Pins Pitch Y axis	J2	560		
Edge to Pin Center Distance along	S1	574	544	604
Edge to Pin Center Distance along	S2	574	544	604



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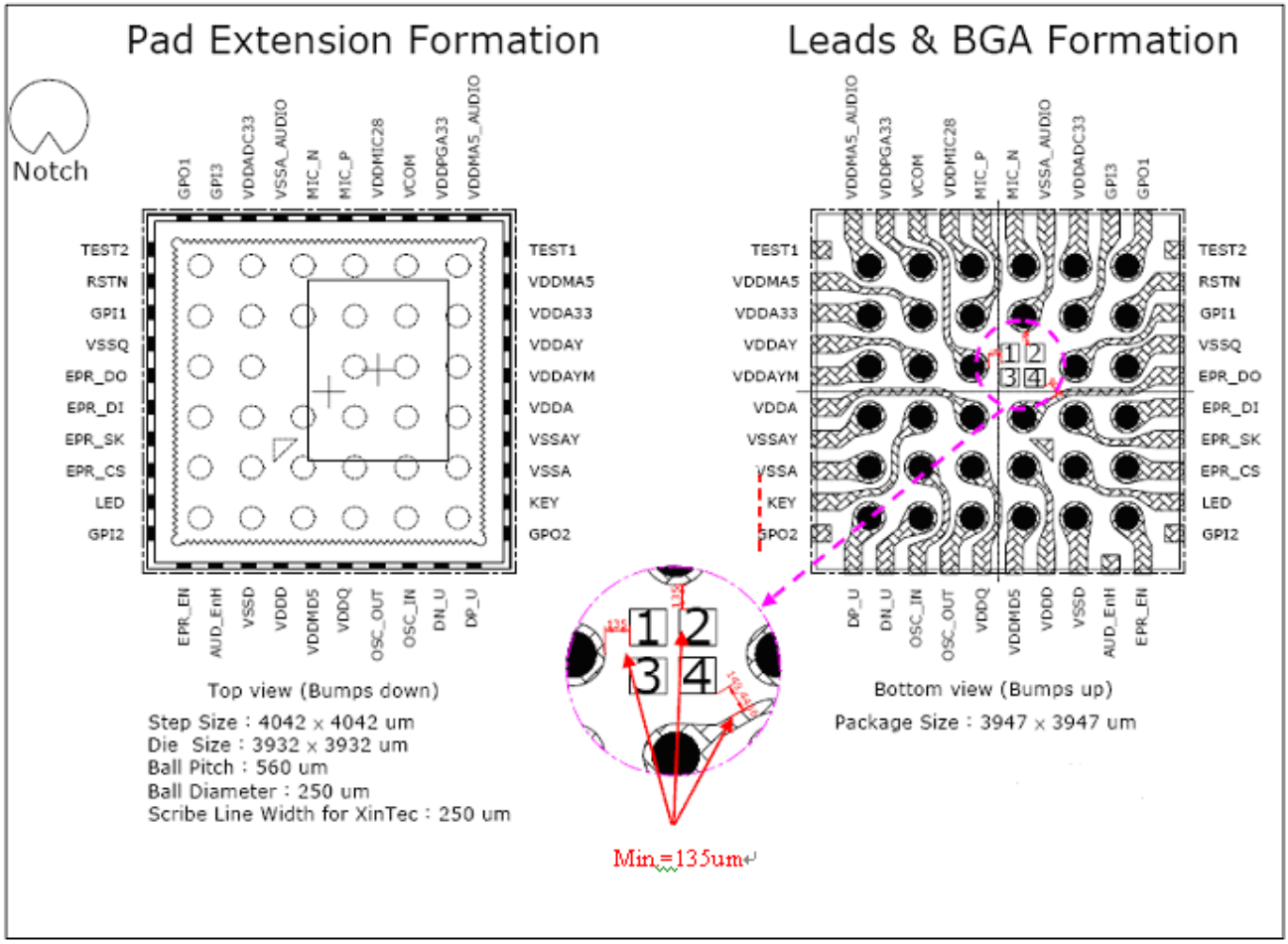
7.3.2.CSP Package Ball Matrix Table

	1	2	3	4	5	6
A	GPO1(PIN 1)	VDDADC33(PIN 2)	MIC_N(PIN 3)	VDDMIC28(PIN 4)	VDDPGA33(PIN 5)	VDDMA5_AUDIO(PIN 6)
B	RSTN(PIN 7)	GPI3(PIN 8)	VSSA_AUDIO(PIN 9)	MIC_P(PIN 10)	VDDMA5(PIN 11)	VDDA33(PIN 12)
C	VSSQ (PIN 13)	GPI1(PIN14)		VCOM(PIN 15)	VDDAY(PIN 16)	VDDAYM(PIN 17)
D	EPR_DI(PIN 18)	EPR_SK (PIN 19)	EPR_DO (PIN 20)	VDDA (PIN 21)	KEY(PIN 22)	VSSAY(PIN 23)
E	EPR_CS(PIN 24)	LED(PIN 25)	VDDD (PIN 26)	VDDQ (PIN 27)	OSC_IN(PIN 28)	VSSA(PIN 29)
F	EPR_EN(PIN 30)	VSSQ(PIN 31)	VDDMD5 (PIN32)	OSC_OUT(PIN 33)	DN(PIN 34)	DP(PIN 35)



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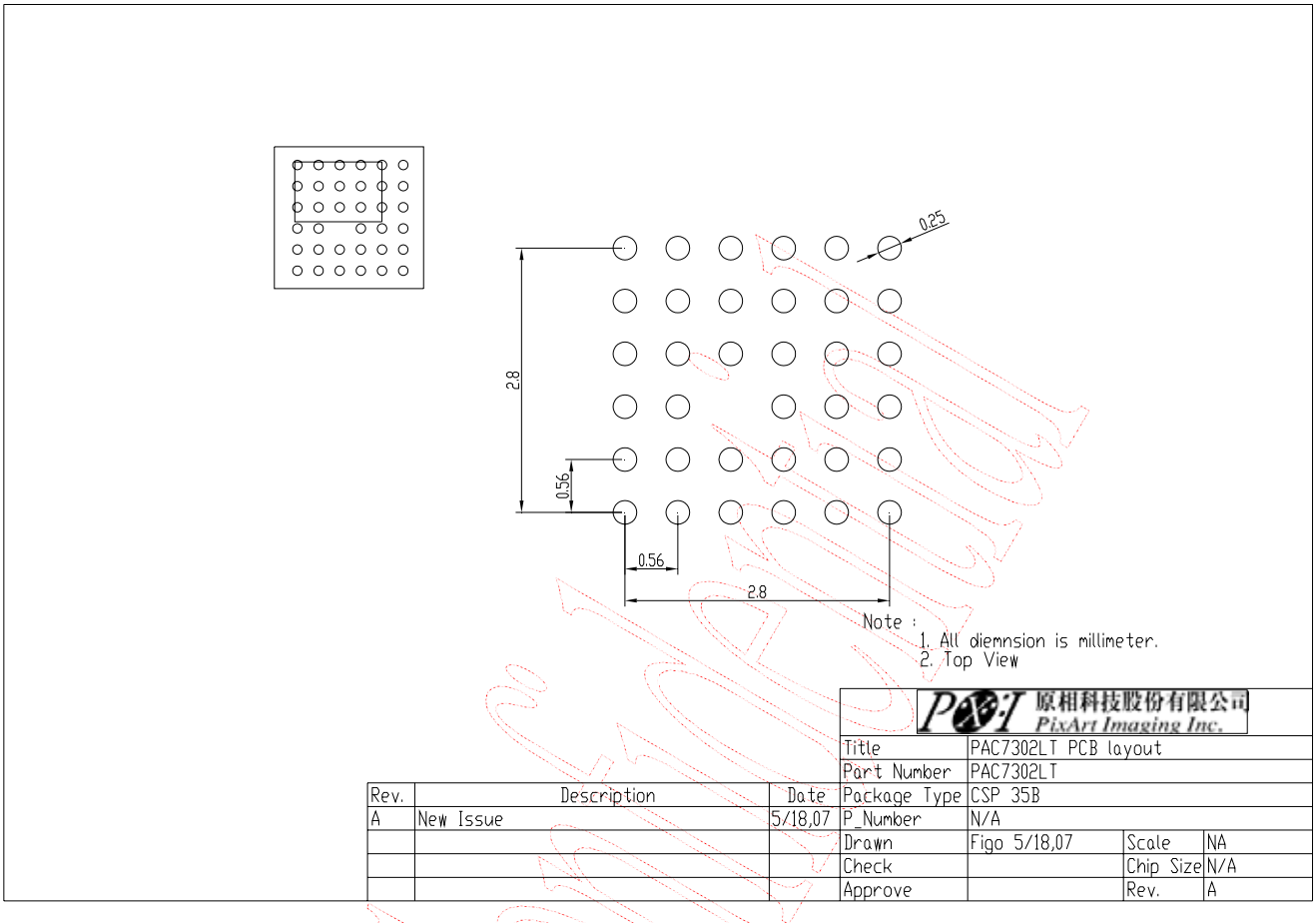
7.3.3 PAC7302LT Recommend PCB Layout



Rev.	Description	Date
A	New Issue	5/18,07

Title	PAC7302LT PCB layout		
Part Number	PAC7302LT		
Package Type	CSP 35B		
P_Number	N/A		
Drawn	Figo 5/18,07	Scale	NA
Check		Chip Size	N/A
Approve		Rev.	A

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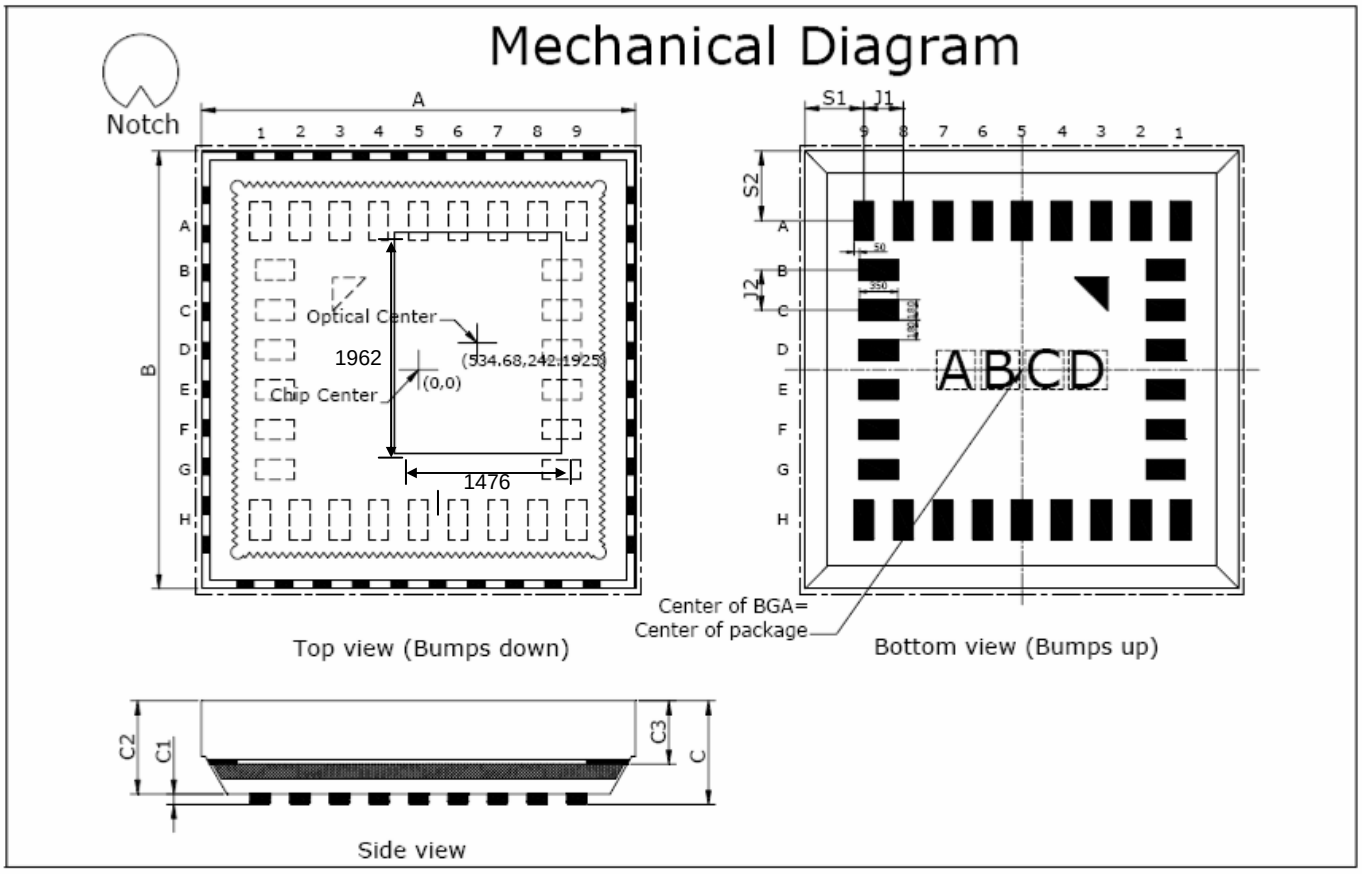
7.4.1 LGA Pin Assignment and Optical Center Information

	Symbol	Nominal	Min.	Max.
		μm		
Package Body Dimension X	A	3947	3922	3972
Package Body Dimension Y	B	3947	3922	3972
Package Height	C	925		
Ball Height	C1	100		
Package Body Thickness	C2	825	790	860
Thickness of Glass surface to wafer	C3	545	525	565
Total Pin Count	N	30		
Pin Count X axis	N1	9		
Pin Count Y axis	N2	6		
Pins Pitch X axis	J1	360		
Pins Pitch Y axis	J2	360		
Edge to Pin Center Distance along X	S1	534	504	564
Edge to Pin Center Distance along Y	S2	629	599	659



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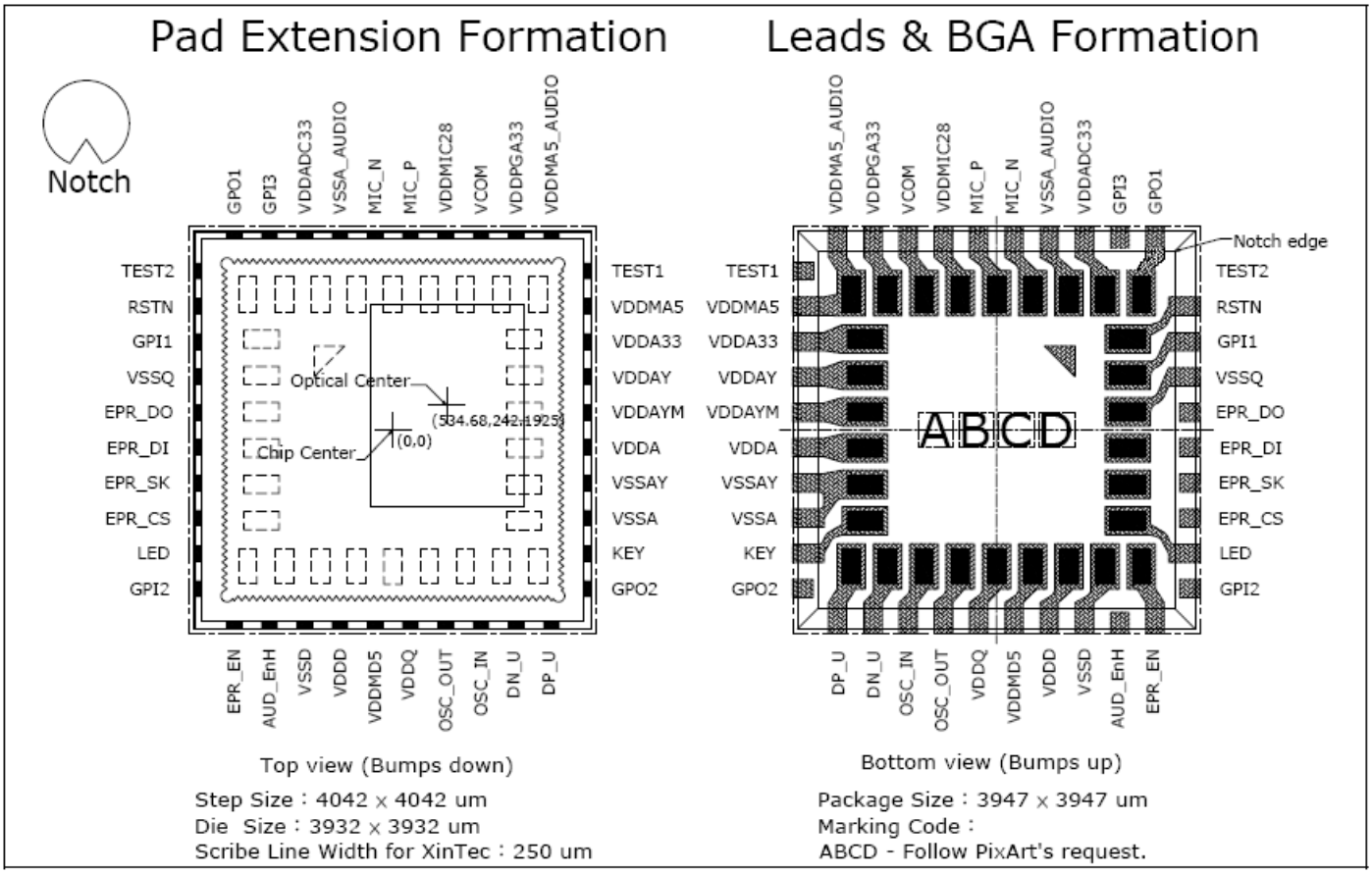
7.4.2.LGA Package Ball Matrix Table

	1	2	3	4	5	6	7	8	9
A	GPO1(P1)	VDDADC33(P2)	VSSA_AUDIO(P3)	MIC_N(P4)	MIC_P(P5)	VDDMIC28(P6)	VCOM(P7)	VDDPGA33(P8)	VDDMA5(P9)
B	RSTN(P30)								VDDA33(P10)
C	GPI1(P29)								VDDAY(P11)
D	VSSQ(P28)								VDDAYM(P12)
E	NC(P27)								VDDA(P13)
F	NC(P26)								VSSAY(P14)
G	LED(P25)								KEY(P15)
H	EPR_EN(P24)	VSSQ(P23)	VDDD(P22)	VDDMD5(P21)	VDDQ(P20)	OSC_OUT(P19)	OSC_IN(P18)	DN(P17)	DP(P16)



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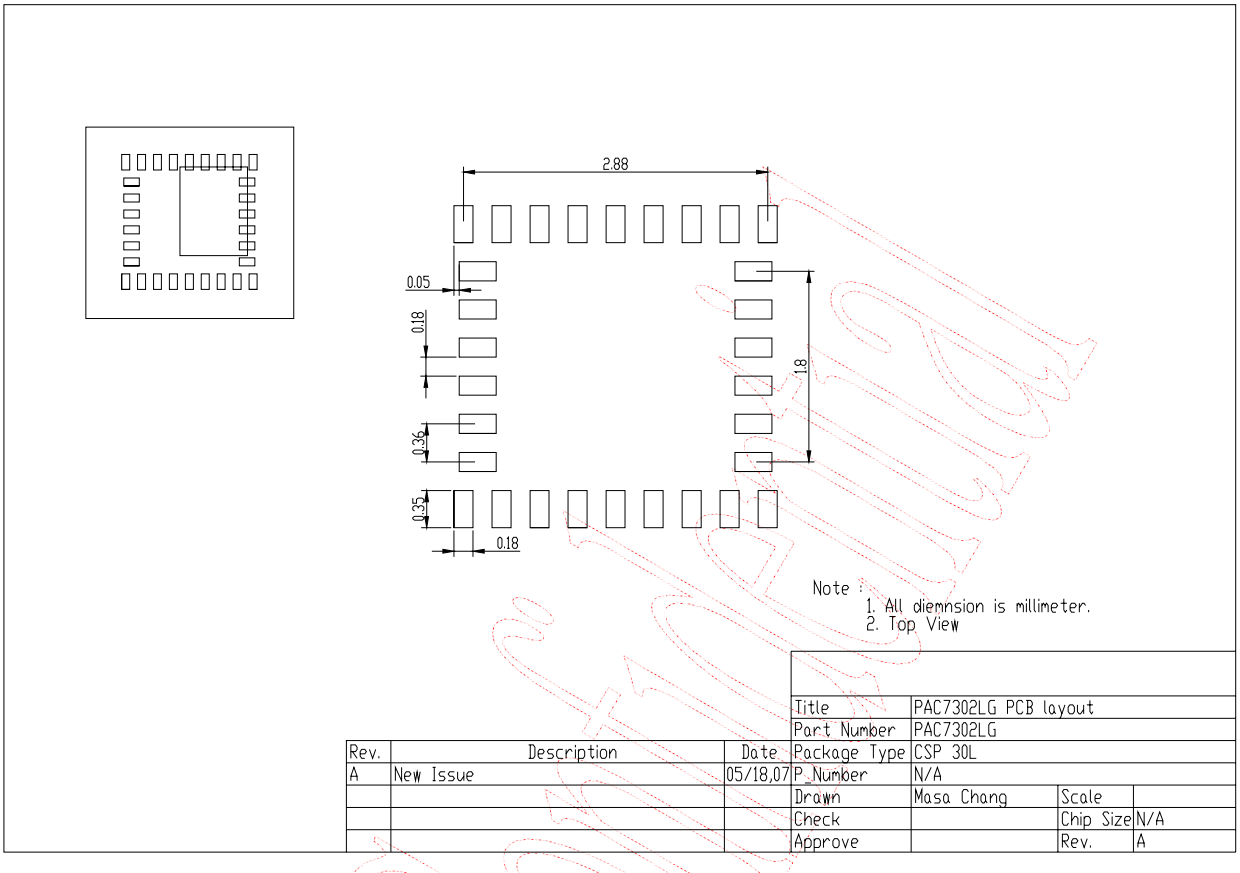
7.4.3 PAC7302LG Recommend PCB Layout



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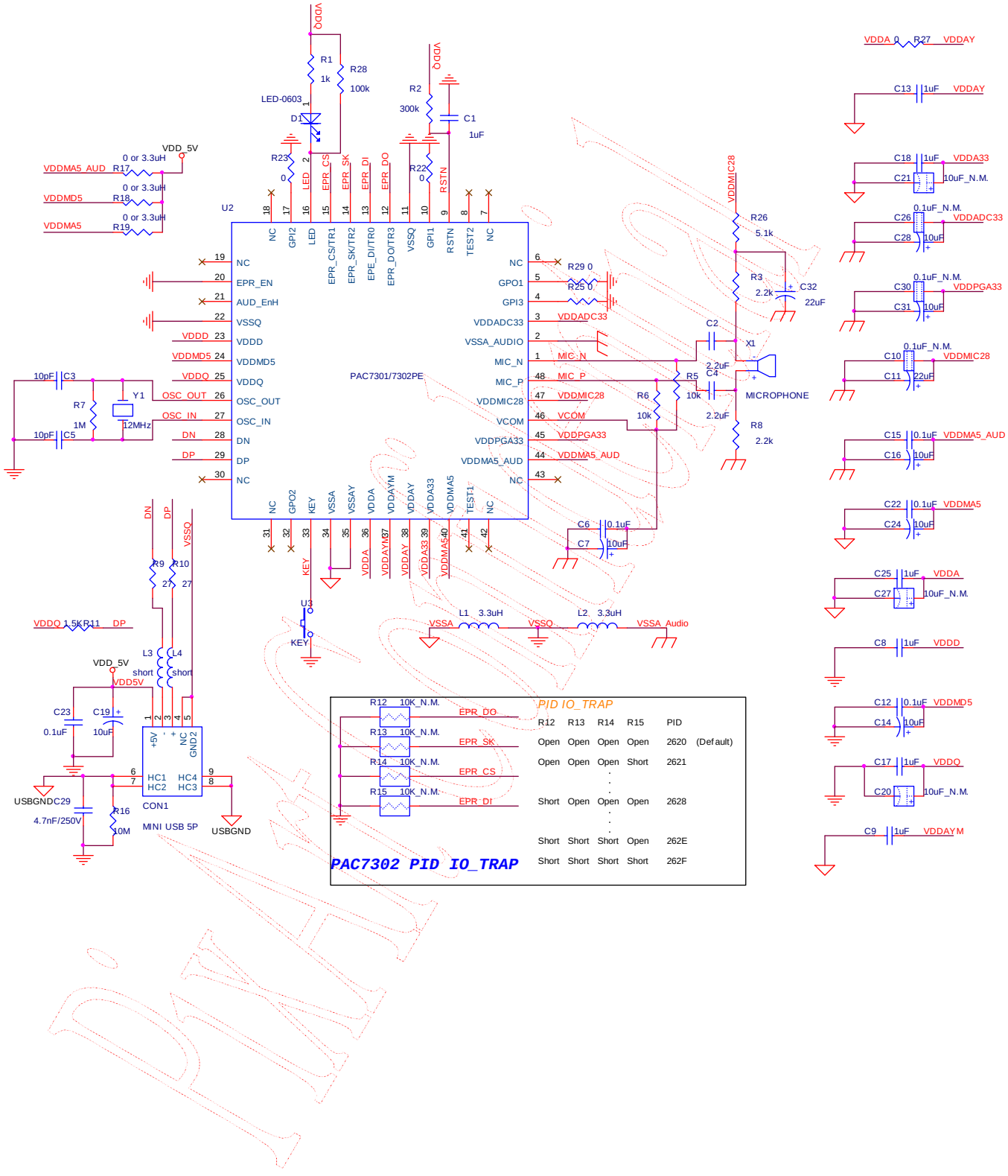
8. Reference Application Circuit

8.1 PLCC(11.43x11.43) Package (PAC7302PE)



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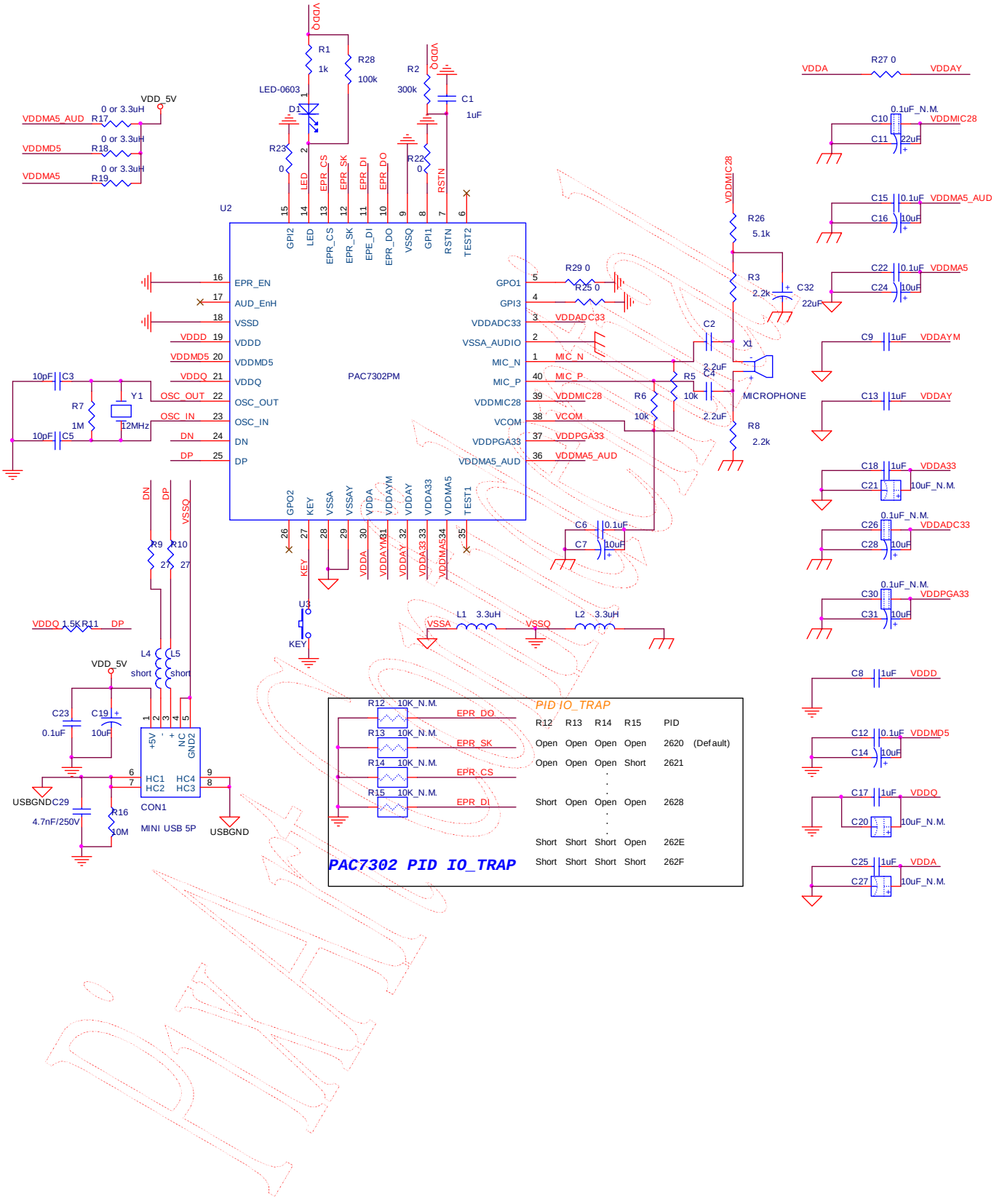
8.2 PLCC (9.0x9.0) Package (PAC7302PM)



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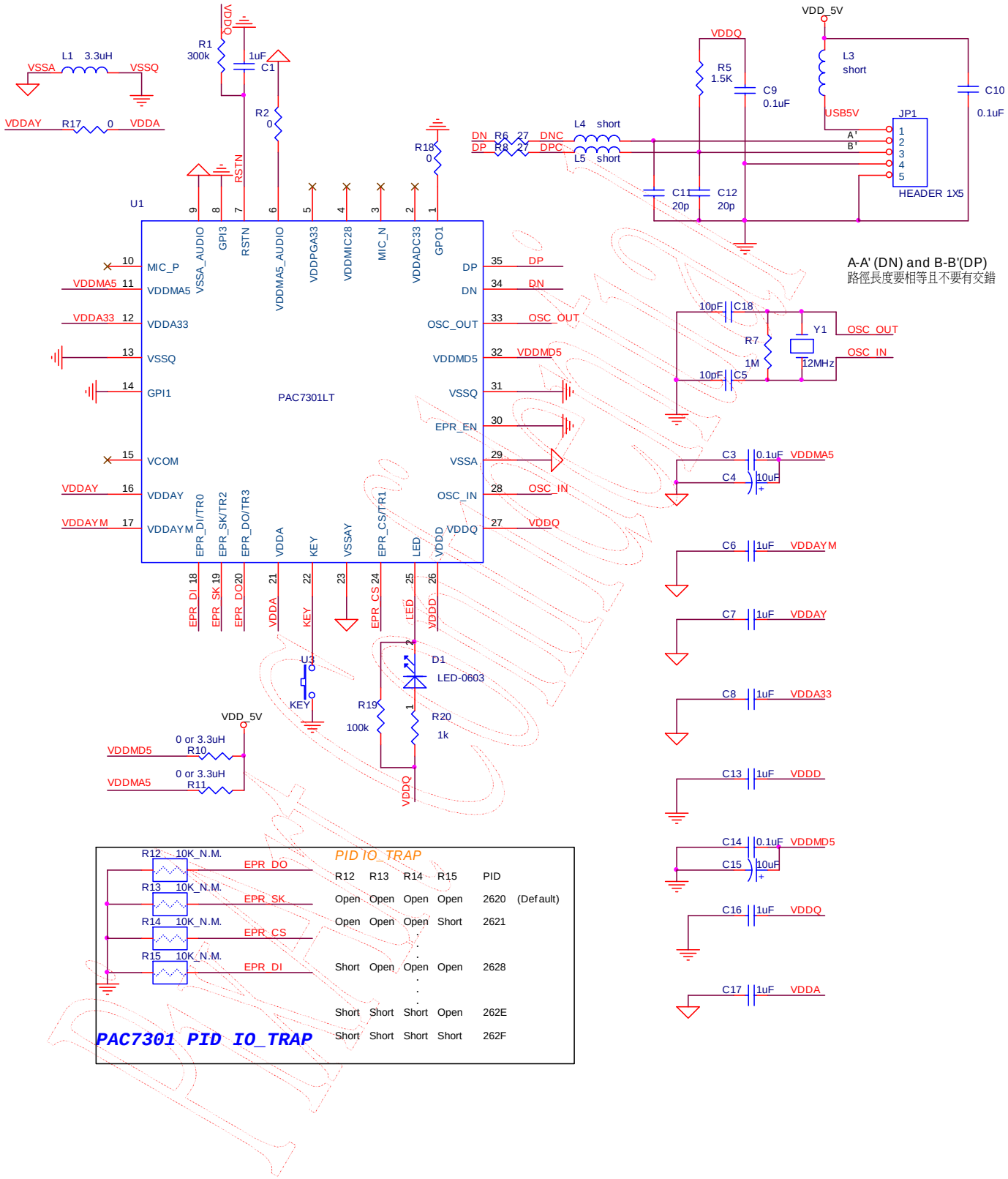
8.3.1 CSP Package (PAC7301LT, no MIC)



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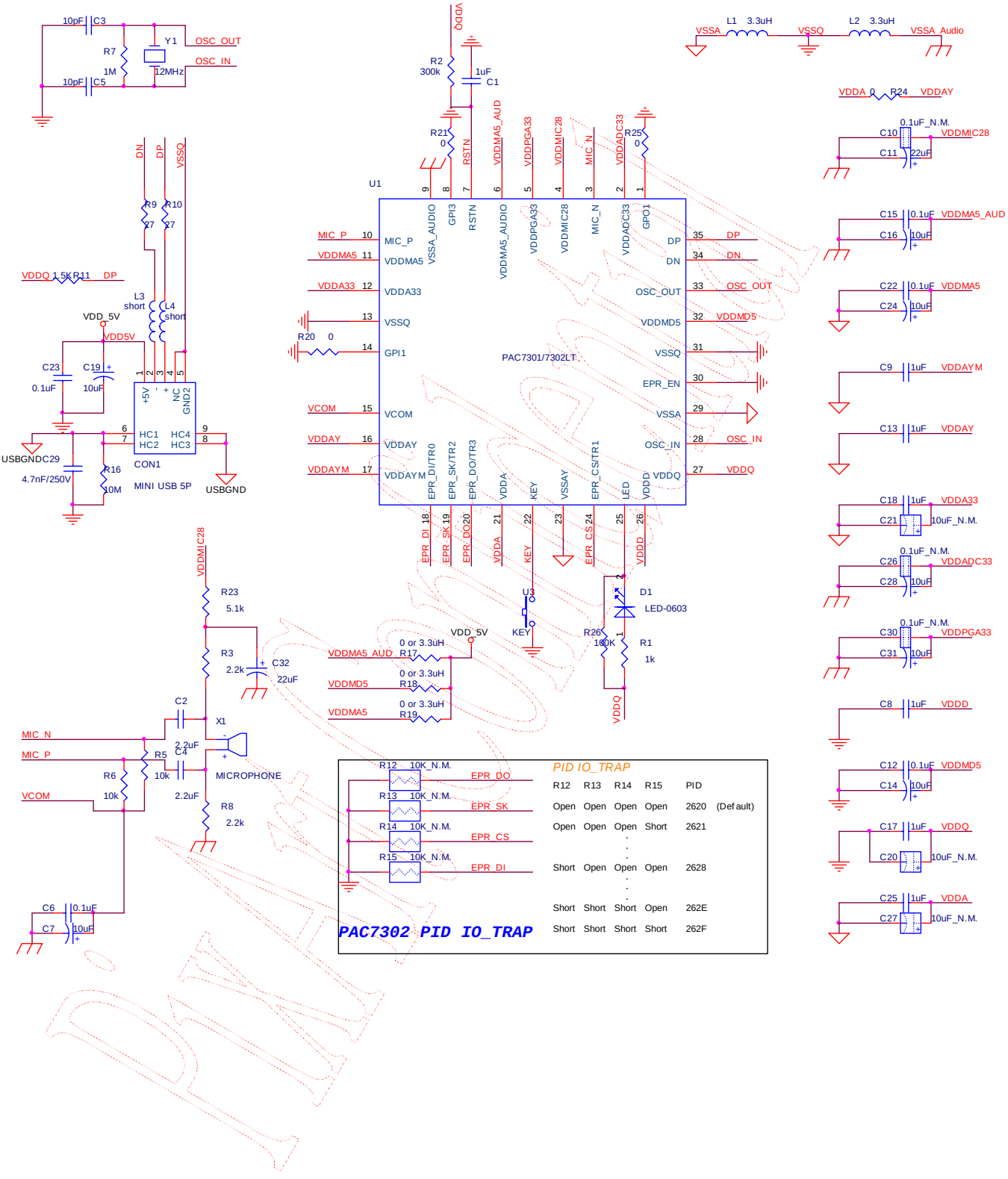
8.3.2 CSP Package (PAC7302LT)



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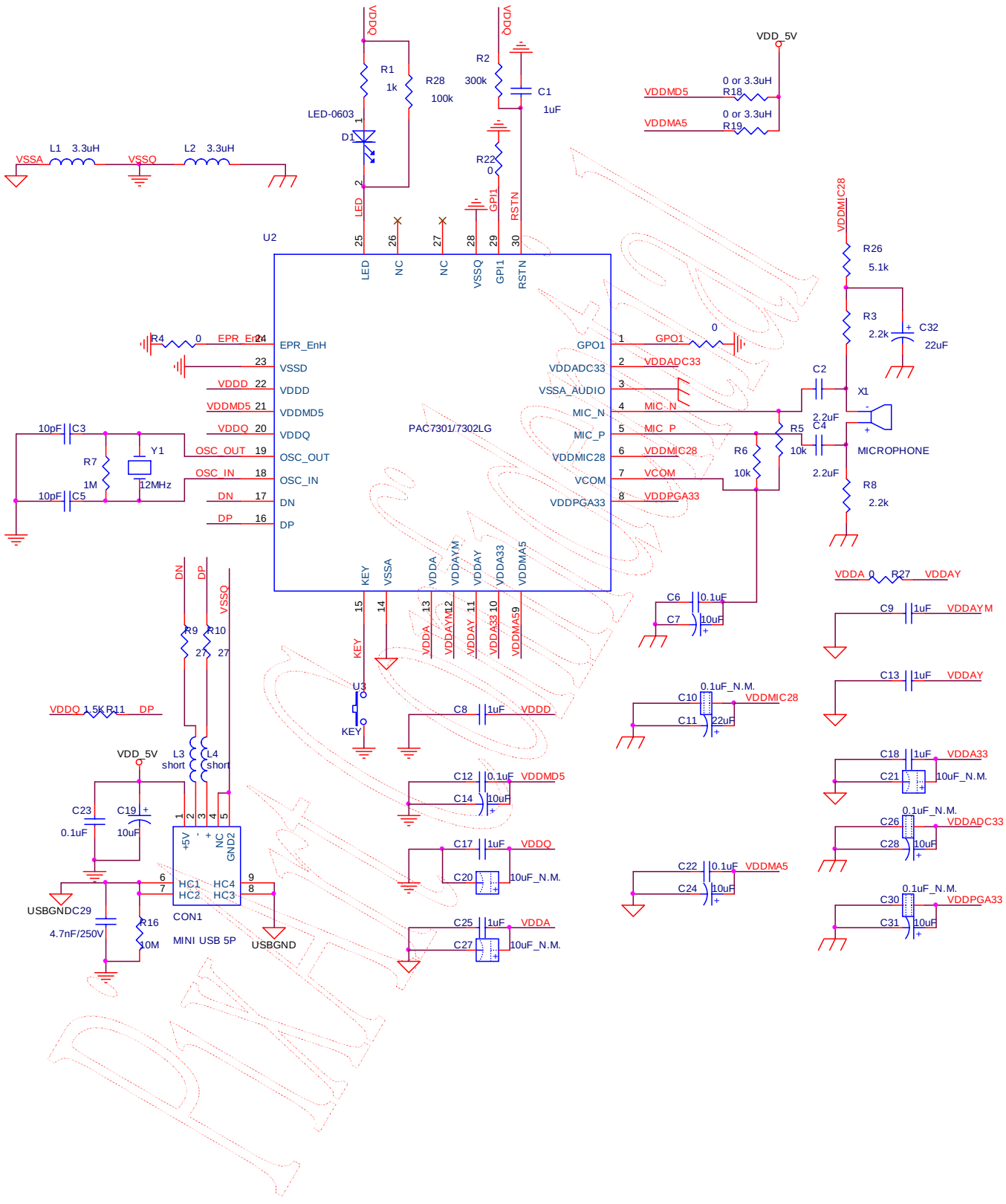
8.4 LGA Package (PAC7302LG)



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9. Update History

Version	Update	Date
V0.1	Creation, Preliminary 1st version	11/24/2006
V0.2	Added circuit/package information for 2nd version	12/07/2006
V0.3	Changed circuit/package information for 3rd version	12/25/2006
V0.4	Modified some string for 4th version	12/26/2006
V0.5	Modified CSP package LC type for 5th version	12/26/2006
V0.6	Modified MIC circuit for 6th version	01/23/2007
V0.7	Modified MIC circuit for 7th version and changed CSP package LT type	01/29/2007
V0.8	Support PAC7302PE/PM/LT/LG package.	04/09/2007
V0.9	Write the Specifications TBD value	05/02/2007
V1.0	LGA GPO1 replace GPI3, update PAC7301CS circuit	05/18/2007
V1.1	GPO1/LED modified circuit for suspend, and update PAC7301/7302 circuit	06/29/2007
V1.2	Update LGA/CSP package for marking code revision	08/22/2007
V1.3	Modified reference circuit symbol.	08/28/2007
V1.4	Added package sensor array dimension and update the newest package information. Only update reference circuit symbol.	11/01/2007

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