

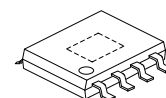
**PA6203**

Preliminary

CMOS IC**1.25-W MONO FULLY
DIFFERENTIAL AUDIO POWER
AMPLIFIER****■ DESCRIPTION**

The UTC **PA6203** is a mono fully-differential audio amplifier, capable of delivering 1.25W of continuous average power to an 8-Ω BTL load with less than 1% distortion from a 5V power supply.

The UTC **PA6203** is ideal for PDA/smart phone applications due to features such as -85-dB supply voltage rejection from 90Hz to 5kHz, improved RF rectification immunity and a fast start-up with minimal pop. The device operates from 2.5V to 5.5V, drawing only 1.7mA of quiescent supply current.



HSOP-8

■ FEATURES

- * 1.25W into 8Ω from a 5-V supply at THD=1% (Typ.)
- * 2.5V-5.5V operation
- * Low supply current: 1.7mA typ at 5V
- * Shutdown Control<10μA
- * Only five external components
 - Improved PSRR (90dB) for direct battery operation
 - Fully differential design reduces RF rectification
 - Improved CMRR eliminates two input coupling capacitors
 - C_(BYPASS) is optional due to fully differential design and high PSRR

■ APPLICATIONS

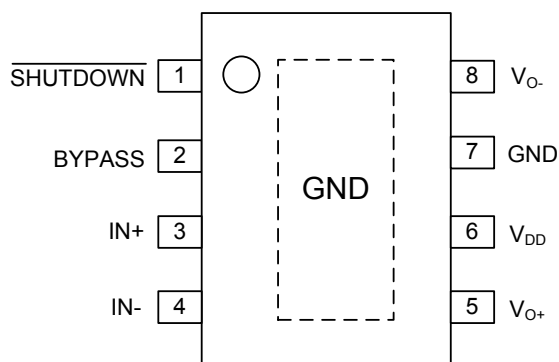
- * Designed for wireless or cellular handsets and PDAs

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
PA6203L-SH2-T	PA6203G-SH2-T	HSOP-8	Tube
PA6203L-SH2-R	PA6203G-SH2-R	HSOP-8	Tape Reel

PA6203L-SH2-T	(1)Packing Type	(1) T: Tube, R: Tape Reel
	(2)Package Type	(2) SH2: HSOP-8
	(3)Halogen Free	(3) L: Lead Free, G: Halogen Free

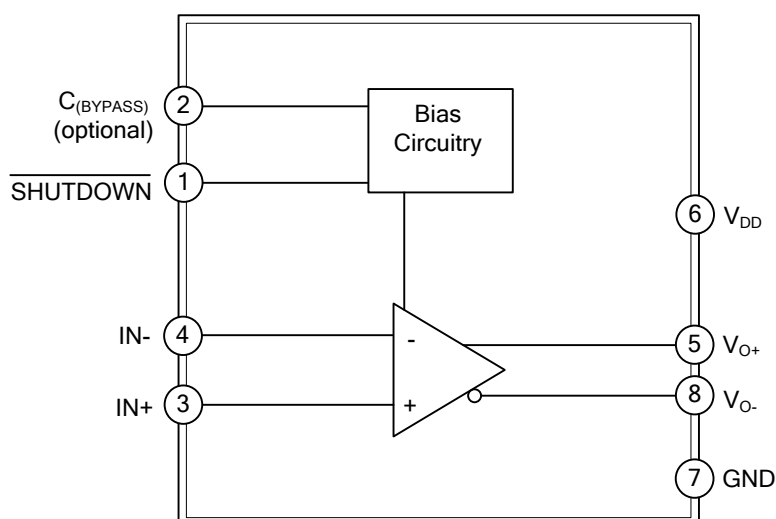
PIN CONFIGURATION



PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	SHUTDOWN	Shutdown terminal (active low logic)
2	BYPASS	Mid-supply voltage, adding a bypass capacitor improves PSRR
3	IN+	Positive differential input
4	IN-	Negative differential input
5	VO+	Positive BTL output
6	VDD	Supply voltage terminal
7	GND	High-current ground
8	VO-	Negative BTL output
	Thermal Pad	Connect to ground. Thermal Pad must be soldered down in all applications to properly secure device on the PCB.

BLOCK DIAGRAM



■ **ABSOLUTE MAXIMUM RATING** (Over operating free-air temperature range, unless otherwise noted)

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage		V_{DD}	-0.3~6	V
Input Voltage	INx and SHUTDOWN Pins	V_I	-0.3~ $V_{DD}+0.3$	V
Continuous Total Power Dissipation		P_D	Internally Limited	
Operating Free-air Temperature		T_A	-40~85	°C
Junction Temperature		T_J	-40~125	°C
Storage Temperature		T_{STG}	-65~150	°C
Lead Temperature From Case For 10 Seconds			260	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ **THERMAL DATA**

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient		θ_{JA}	42.3	°C/W
Junction to Case		θ_{JC}	12	°C/W

■ **RECOMMENDED OPERATING CONDITIONS**

PACKAGE		SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage		V_{DD}	2.5		5.5	V
High-Level Input Voltage	SHUTDOWN	V_{IH}	2			V
Low-Level Input Voltage	SHUTDOWN	V_{IL}			0.8	V
Common-Mode Input Voltage	V=2.5V, 5.5V, CMRR≤-60dB	V_{IC}	0.5		$V_{DD}-0.8$	V
Operating Free-Air Temperature		T_A	-40		85	°C
Load Impedance		Z_L	6.4	8		Ω

■ **ELECTRICAL CHARACTERISTICS** ($T_A=25^{\circ}\text{C}$, Gain=1V/V, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Offset Voltage (Measured Differentially)	$ V_{OO} $	$V_I=0\text{V}$, $V_{DD}=2.5\text{V}\sim 5.5\text{V}$			9	mV
Power Supply Rejection Ratio	PSRR	$V_{DD}=2.5\text{V}\sim 5.5\text{V}$		-90	-70	dB
Common Mode Rejection Ratio	CMRR	$V_{DD}=3.6\text{V}\sim 5.5\text{V}$, $V_{IC}=0.5\text{V}\sim V_{DD}-0.8$		-70	-65	dB
		$V_{DD}=2.5\text{V}$, $V_{IC}=0.5\text{V}\sim 1.7\text{V}$		-62	-55	
Low-Level Output Voltage	V_{OL}	$R_L=8\Omega$, $V_{IN+}=V_{DD}$, $V_{IN-}=0\text{V}$ or $V_{IN+}=0\text{V}$, $V_{IN-}=V_{DD}$	$V_{DD}=5.5\text{V}$	0.30	0.46	V
			$V_{DD}=3.6\text{V}$	0.22		
			$V_{DD}=2.5\text{V}$	0.19	0.26	
High-Level Output Voltage	V_{OH}	$R_L=8\Omega$, $V_{IN+}=V_{DD}$, $V_{IN-}=0\text{V}$ or $V_{IN+}=0\text{V}$, $V_{IN-}=V_{DD}$	$V_{DD}=5.5\text{V}$	4.8	5.12	V
			$V_{DD}=3.6\text{V}$	3.28		
			$V_{DD}=2.5\text{V}$	2.1	2.24	
High-Level Input Current	$ I_{IH} $	$V_{DD}=5.5\text{V}$, $V_I=5.8\text{V}$			1.2	μA
Low-Level Input Current	$ I_{IL} $	$V_{DD}=5.5\text{V}$, $V_I=-0.3\text{V}$			1.2	μA
Supply Current	I_{DD}	SHUTDOWN=2V, $V_{DD}=2.5\text{V}\sim 5.5\text{V}$, No Load		1.7	2	mA
Supply Current in Shutdown Mode	$I_{DD(SD)}$	SHUTDOWN=0.8V, $V_{DD}=2.5\text{V}\sim 5.5\text{V}$, No Load		0.01	0.9	μA

■ OPERATING CHARACTERISTICS (T_A=25°C, Gain=1V/V, R_L=8Ω)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output Power	P _O	THD+N=1%, f=1kHz	V _{DD} =5V		1.25		W
			V _{DD} =3.6V		0.63		W
			V _{DD} =2.5V		0.3		W
Total Harmonic Distortion Plus Noise	THD+N	V _{DD} =5V, P _O =1W, f=1kHz			0.06		%
		V _{DD} =3.6V, P _O =0.5W, f=1kHz			0.07		
		V _{DD} =2.5V, P _O =200mW, f=1kHz			0.08		
Supply Ripple Rejection Ratio	K _{SVR}	C _(BYPASS) =0.47μF, V _{DD} =3.6V~5.5V, Inputs Ac-Grounded with C _I =2μF	f=217Hz~2kHz, V _{RIPPLE} =200mV _{PP}		-87		dB
		C _(BYPASS) =0.47μF, V _{DD} =2.5V~3.6V, Inputs Ac-Grounded with C _I =2μF	f=217Hz~2kHz, V _{RIPPLE} =200mV _{PP}		-82		dB
		C _(BYPASS) =0.47μF, V _{DD} =2.5V~5.5V, Inputs Ac-Grounded with C _I =2μF	f=40Hz~20kHz, V _{RIPPLE} =200mV _{PP}		≤-74		dB
Signal-To-Noise Ratio	SNR	V _{DD} =5V, P _O =1W			104		dB
Output Voltage Noise	V _N	f=20Hz~20kHz	No Weighting		17		μV _{RMS}
			A Weighting		13		
Common Mode Rejection Ratio	CMRR	V _{DD} =2.5V~5.5V, Resistor Tolerance=0.1%, Gain=4V/V, V _{ICM} =200mV _{PP}	f=20Hz~1kHz		≤-85		dB
			f=20Hz~20kHz		≤-74		dB
Input Impedance	Z _I				2		MΩ
Output Impedance	Z _O	Shutdown Mode		>10k			
Shutdown Attenuation		f=20Hz~20kHz, R _F =R _I =20kΩ			-80		dB

■ TYPICAL APPLICATION CIRCUIT

Table 1. Typical Component Values

COMPONENT	VALUE	UNIT
R_I	10	k Ω
R_F	10	k Ω
$C_{(BYPASS)}$ (Note 1)	0.22	μ F
C_S	1	μ F
C_I	0.22	μ F

Note: 1. $C_{(BYPASS)}$ is optional

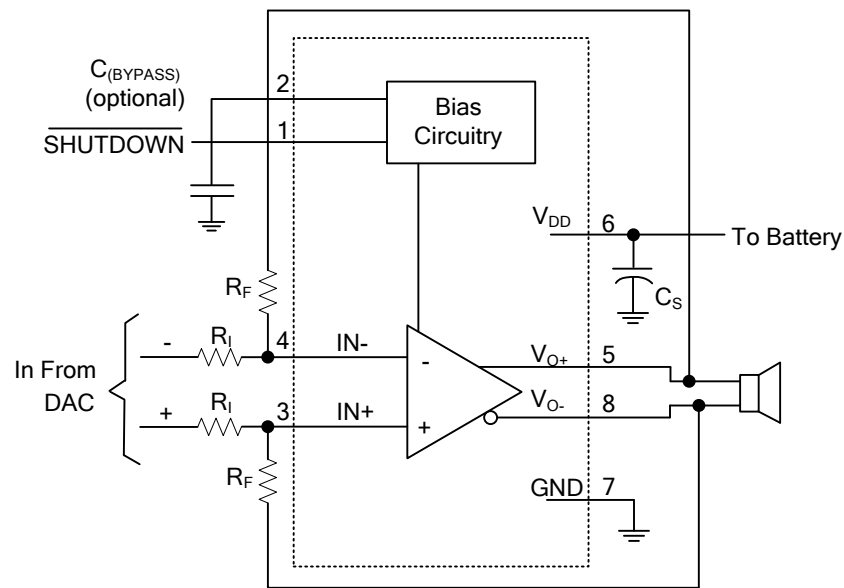


Figure 1. Typical Differential Input Application Schematic

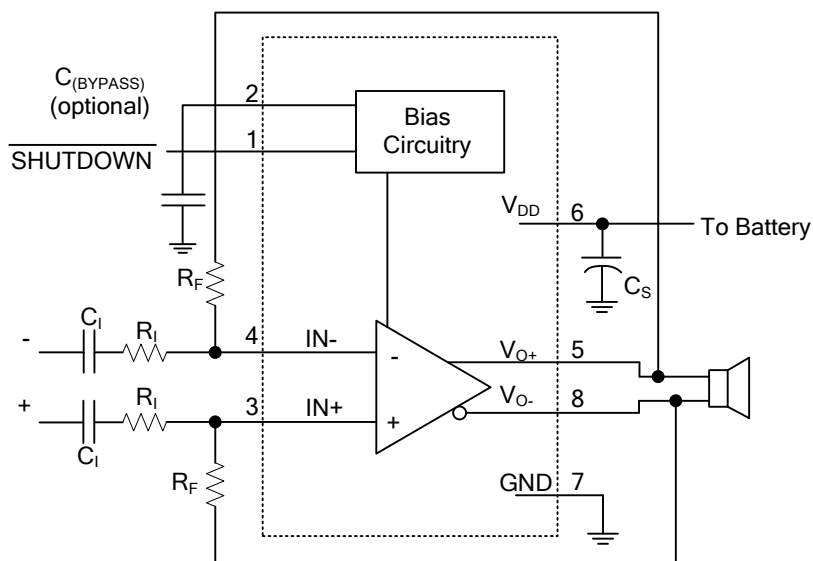


Figure 2. Differential Input Application Schematic Optimized With Input Capacitors

■ TYPICAL APPLICATION CIRCUIT(Cont.)

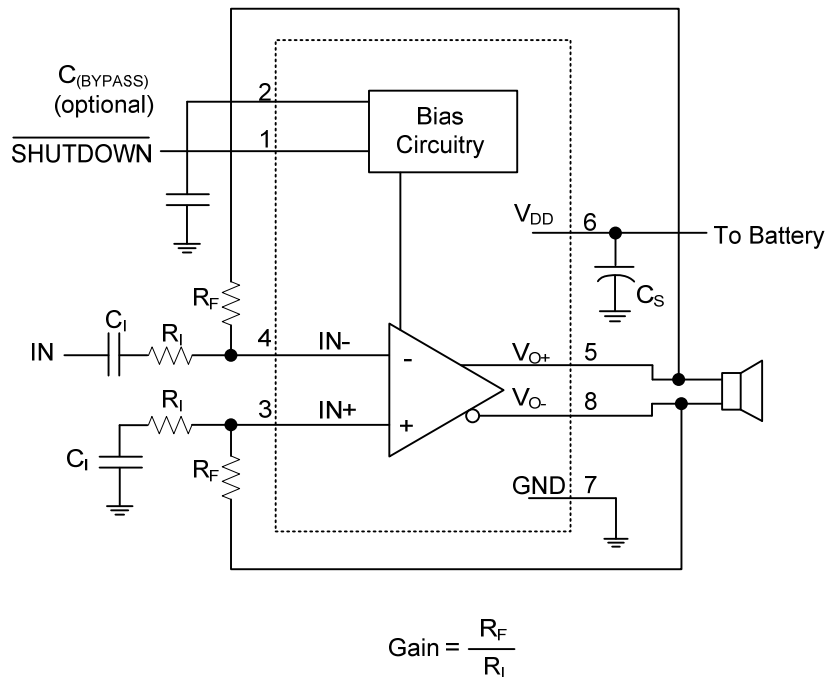


Figure 3. Single-Ended Input Application Schematic

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