PROTEK DEVICES
ANALOG PRODUCTS DIVISION

PA5331
Low Power 24-Bit, Stereo Audio CODEC With Headphone Amplifier

FEATURES

ADC
- 24-bit, 8 kHz to 96 kHz sampling frequency
- 95 dB dynamic range, 95 dB signal to noise ratio, -85 dB THD+N
- Stereo or mono microphone interface with microphone amplifier
- Auto level control and noise gate
- 3-to-1 analog input selection
- Various analog input mixing and gains

DAC
- 24-bit, 8 kHz to 96 kHz sampling frequency
- 96 dB dynamic range, 96 dB signal to noise ratio, -83 dB THD+N
- 40 mW headphone amplifier, pop noise free
- Stereo enhancement
- Bass and Treble
- Various analog output mixing and gains

LOW POWER
- 1.8V to 3.3V operation
- 7 mW playback; 16 mW playback and record

SYSTEM
- I^2C or SPI µC interface
- 256Fs, 384Fs, USB 12 MHz or 24 MHz
- Master or slave serial port
- I^2S, Left Justified, DSP/PCM Mode

APPLICATIONS
- GPS
- Bluetooth
- MP3, MP4, PMP
- Cell phone
- Digital camera, camcorder
- Portable audio devices

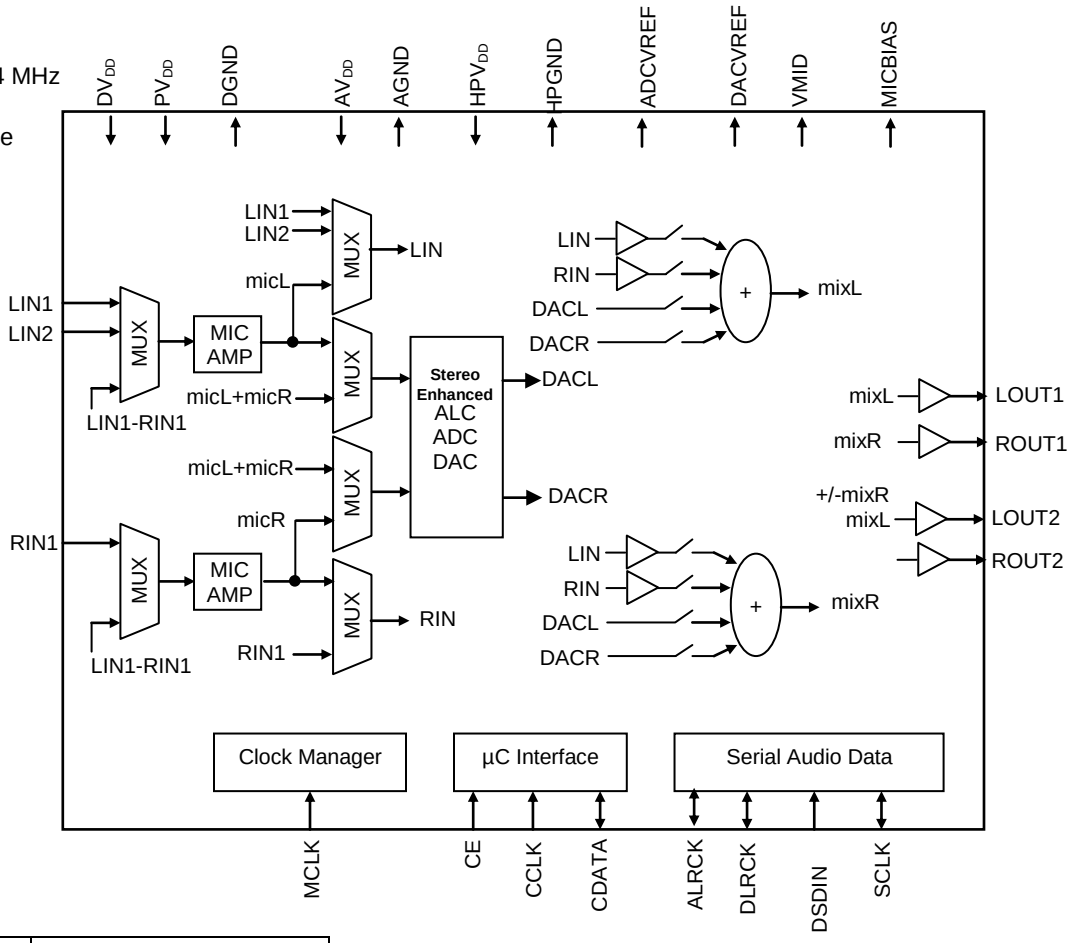
GENERAL DESCRIPTION

The PA5331 is a high performance, low power and low cost audio CODEC. It consists of 2-ch ADC, 2-ch DAC, microphone amplifier, headphone amplifier, digital sound effects, and analog mixing and gain functions.

The PA5331 uses advanced multi-bit delta-sigma modulation technique to convert data between digital and analog.

The multi-bit delta-sigma modulators make the device with low sensitivity to clock jitter and low out of band noise.

BLOCK DIAGRAM



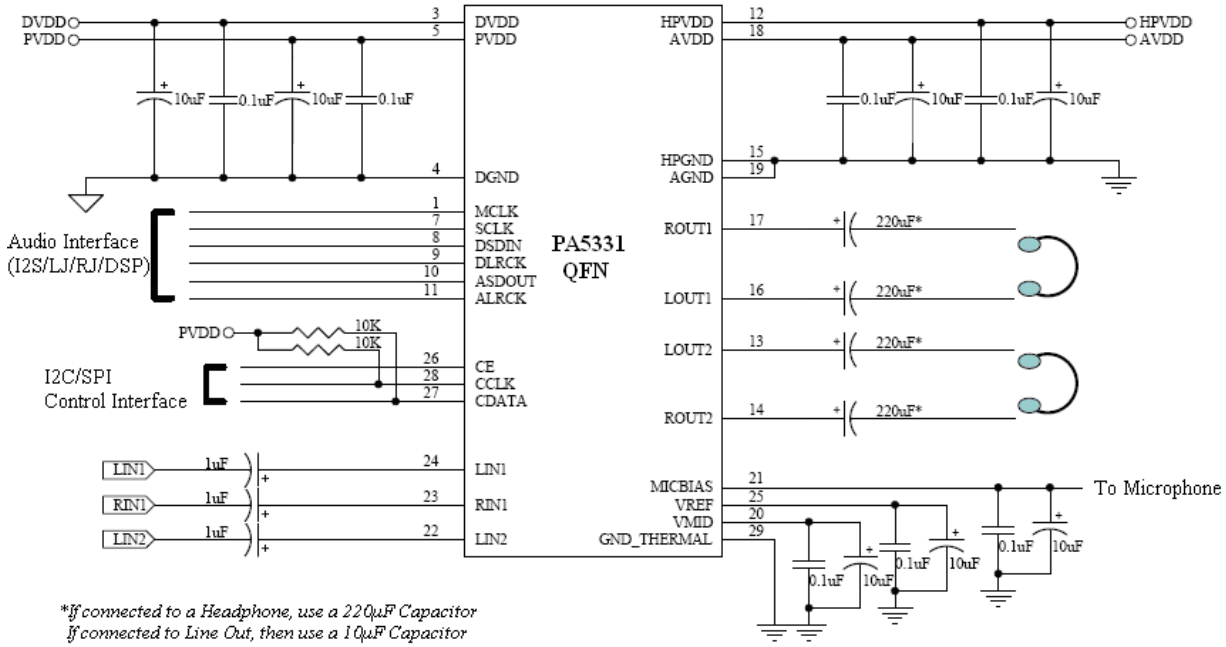
ORDERING INFORMATION

Temperature Range	Package	Part Number
-40 to 85 °C	QFN-28	PA5331-T7

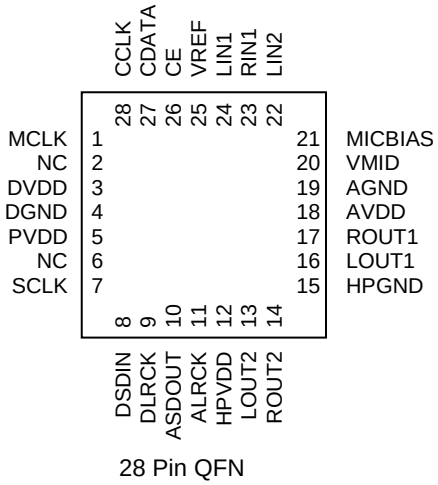
561 E. Elliot Road #175 Chandler, AZ 85225 Tel: (480) 539-2900. Fax: (480) 632-1715
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NOT FOR USE IN LIFE SUPPORT SYSTEMS

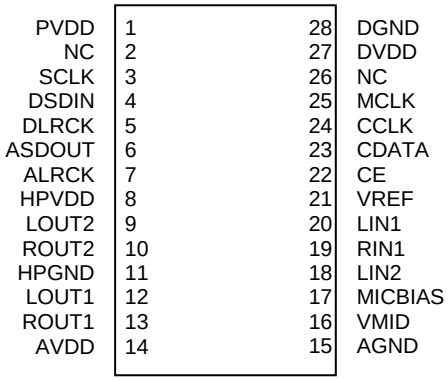
TYPICAL APPLICATION



28-PIN QFN, 28-PIN SSOP LAYOUT



28 Pin QFN



28 Pin SSOP

28-PIN QFN, 28-PIN SSOP PIN DESCRIPTIONS

The PA5331 is pin compatible to WM8731 except the yellow highlighted pins in the following table.

QFN PIN	SSOP PIN	NAME	I/O	DESCRIPTION
1	25	MCLK	I	Master clock
2	26	NC		No connect
3	27	DVDD	Supply	Digital core supply
4	28	DGND	Supply	Digital ground (return path for both DVDD and PVDD)
5	1	PVDD	Supply	Digital IO supply
6	2	NC		No connect
7	3	SCLK	I/O	Audio data bit clock
8	4	DSDIN	I	DAC audio data
9	5	DLRCK	I/O	DAC audio data left and right clock
10	6	ASDOUT	O	ADC audio data
11	7	ALRCK	I/O	ADC audio data left and right clock
12	8	HPVDD	Supply	Supply for analog output drivers (LOUT1/2, ROUT1/2)
13	9	LOUT2	O	Left output 2 (line or headphone)
14	10	ROUT2	O	Right output 2 (line or headphone)
15	11	HPGND	Supply	Ground for analog output drivers (LOUT1/2, ROUT1/2)
16	12	LOUT1	O	Left output 1 (line or headphone)
17	13	ROUT1	O	Right output 1 (line or headphone)
18	14	AVDD	Supply	Analog supply
19	15	AGND	Supply	Analog ground
20	16	VMID	O	Decoupling capacitor
21	17	MICBIAS	O	Microphone bias
22	18	LIN2	I	Left channel input 2
23	19	RIN1	I	Right channel input 1
24	20	LIN1	I	Left channel input 1
25	21	VREF	0	Decoupling capacitor
26	22	CE	I	Control select or device address selection
27	23	CDATA	I/O	Control data input or output
28	24	CCLK	I	Control clock input

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... MIN-0.3V MAX +5.0V
Input Voltage ..... MIN GND-0.3V MAX V_{DD}+0.3V
Operating Temperature.....MIN -40°C MAX +85°C
Storage Temperature.....MIN -65°C MAX +150°C
Note: Continuous operation at or beyond these conditions may permanently damage the device.

RECOMMENDED OPERATING CONDITIONS

Analog Supply Voltage ..... MIN 1.7V MAX 3.6V
Digital Supply Voltage ..... MIN 1.5V MAX 3.6V

ADC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify:
AVDD=+3.3V, DVDD=+1.8V, AGND=0V, DGND=0V, Ambient temperature=+25°C, Fs=48 KHz, 96 KHz or 192 KHz, MCLK/LRCK=256.

PARAMETER	MIN	TYP	MAX	UNIT
ADC Performance				
Dynamic Range (Note 1)	85	95	98	dB
THD+N	-88	-85	-75	dB
Channel Separation (1KHz)	80	85	90	dB
Signal to Noise ratio	85	95	98	dB
Inter-channel Gain Mismatch		0.1		dB
Gain Error			±5	%
Filter Frequency Response – Single Speed				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Pass-band Ripple			±0.05	dB
Stop-band Attenuation	50			dB
Filter Frequency Response – Double Speed				
Pass-band	0		0.4167	Fs
Stop-band	0.5833			Fs
Pass-band Ripple			±0.005	dB
Stop-band Attenuation	50			dB
Analog Input				
Full Scale Input Level		AVDD/3.3		Vrms
Input Impedance		20		KΩ

Note
1. The value is measured used A-weighted filter.

DAC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify:
AVDD=+3.3V, DVDD=+1.8V, AGND=0V, DGND=0V, Ambient temperature=+25°C, Fs=48 KHz, 96 KHz or 192 KHz, MCLK/LRCK=256.

PARAMETER	MIN	TYP	MAX	UNIT
DAC Performance				
Dynamic Range (Note 1)	83	96	98	dB
THD+N	-85	-83	-75	dB
Channel Separation (1KHz)	80	85	90	dB
Signal to Noise ratio	83	96	98	dB
Inter-channel Gain Mismatch		0.05		dB
Filter Frequency Response – Single Speed				

Pass-band	0		0.4535	Fs
Stop-band	0.5465			Fs
Pass-band Ripple			±0.05	dB
Stop-band Attenuation	40			dB
Filter Frequency Response – Double Speed				
Pass-band	0		0.4167	Fs
Stop-band	0.5833			Fs
Pass-band Ripple			±0.005	dB
Stop-band Attenuation	40			dB
De-emphasis Error at 1 KHz (Single Speed Mode Only)				
Fs = 32KHz Fs = 44.1KHz Fs = 48KHz			0.002 0.013 0.0009	dB
Analog Output				
Full Scale Output Level		AVDD/3.3		Vrms

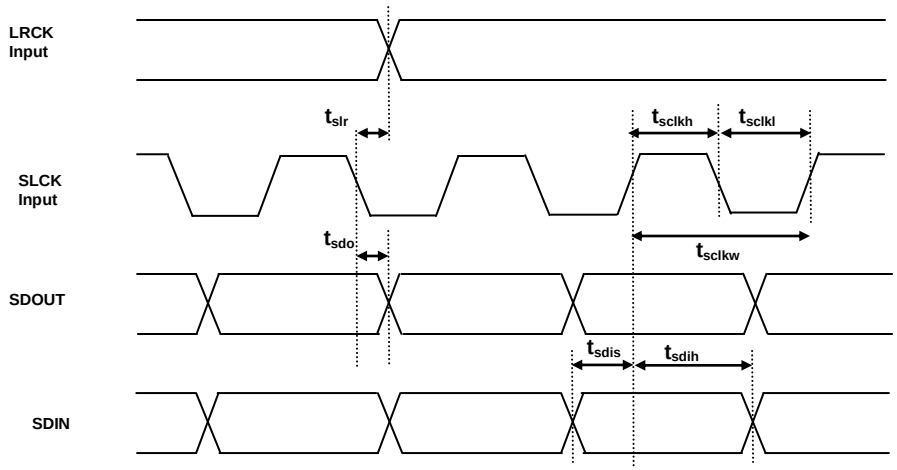
Note
1. The value is measured used A-weighted filter.

POWER CONSUMPTION CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT
Normal Operation Mode				
DVDD=1.8V, AVDD=1.8V: Play back Play back and record DVDD=3.3V, AVDD=3.3V: Play back Play back and record		 7 16 31 59		mW
Power Down Mode				
DVDD=1.8V, AVDD=1.8V DVDD=3.3V, AVDD=3.3V		0.3 1.9		mW

SERIAL AUDIO PORT SWITCHING SPECIFICATIONS

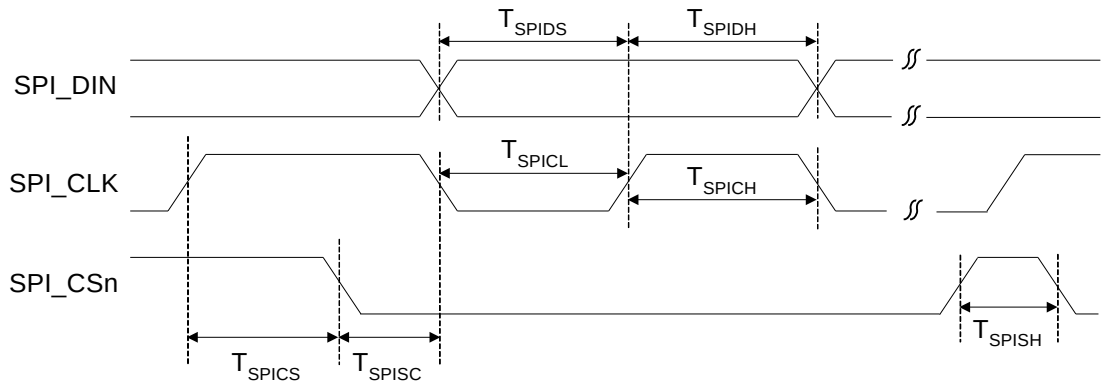
PARAMETER	Symbol	MIN	MAX	UNIT
MCLK frequency			51.2	MHz
MCLK duty cycle		40	60	%
LRCK frequency			200	KHz
LRCK duty cycle		40	60	%
SCLK frequency			26	MHz
SCLK pulse width low	T_{SCLKL}	15		ns
SCLK Pulse width high	T_{SCLKH}	15		ns
SCLK falling to LRCK edge	T_{SLR}	–10	10	ns
SCLK falling to SDOUT valid	T_{SDO}	0		ns
SDIN valid to SCLK rising setup time	T_{SDIS}	10		ns
SCLK rising to SDIN hold time	T_{SDIH}	10		ns



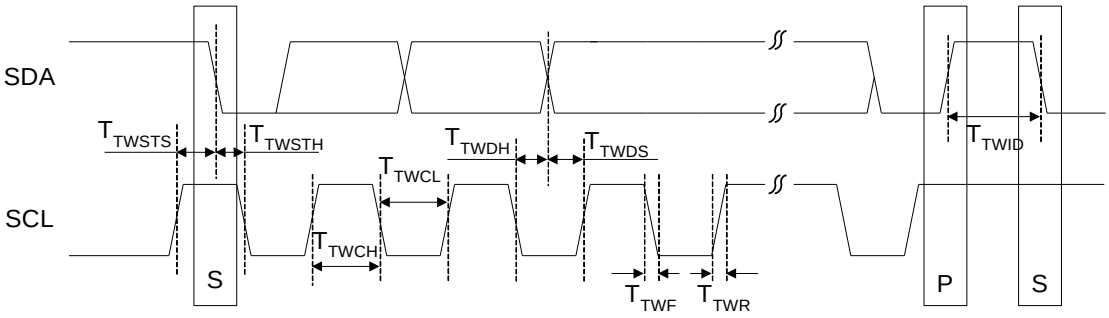
Serial Audio Port Timing

SERIAL CONTROL PORT SWITCHING SPECIFICATIONS

PARAMETER	Symbol	MIN	MAX	UNIT
SPI Mode				
SPI_CLK clock frequency			10	MHz
SPI_CLK edge to SPI_CSn falling	T_{SPICS}	5		ns
SPI_CSn High Time Between transmissions	T_{SPISH}	500		ns
SPI_CSn falling to SPI_CLK edge	T_{SPISC}	10		ns
SPI_CLK low time	T_{SPICL}	45		ns
SPI_CLK high time	T_{SPICH}	45		ns
SPI_DIN to SPI_CLK rising setup time	T_{SPIDS}	10		ns
SPI_CLK rising to DATA hold time	T_{SPIDH}	15		ns
2-wire Mode				
SCL Clock Frequency	F_{SCL}		100	KHz
Bus Free Time Between Transmissions	T_{TWID}	4.7		us
Start Condition Hold Time	T_{TWSTH}	4.0		us
Clock Low time	T_{TWCL}	4.0		us
Clock High Time	T_{TWCH}	4.0		us
Setup Time for Repeated Start Condition	T_{TWSTS}	4.7		us
SDA Hold Time from SCL Falling	T_{TWDH}	0.1		us
SDA Setup time to SCL Rising	T_{TWDS}	100		ns
Rise Time of SCL	T_{TWR}		25	us
Fall Time SCL	T_{TWF}		25	ns



Serial Control Port SPI Timing



Serial Control Port 2-wire Timing

CLOCK MODES AND SAMPLING FREQUENCIES

According to the input serial audio data sampling frequency, the device can work in two speed modes: single speed or double speed. The ranges of the sampling frequency in these two modes are listed in Table 1. The device can work either in master clock mode or slave clock mode.

In slave mode, LRCK and SCLK are supplied externally. LRCK and SCLK must be synchronously derived from the system clock with specific rates. The device can auto detect MCLK/LRCK ratio according to Table 1. The device only supports the MCLK/LRCK ratios listed in Table 1. The LRCK/SCLK ratio is normally 64.

Table 1 Slave Mode Sampling Frequencies and MCLK/LRCK Ratio

Speed Mode	Sampling Frequency	MCLK/LRCK Ratio
Single Speed	8kHz – 50kHz	256, 384, 512, 768, 1024
Double Speed	50kHz – 100kHz	128, 192, 256, 384, 512

In master mode, LRCK and SCLK are derived internally from MCLK. The available MCLK/LRCK ratios and SCLK/LRCK ratios are listed in Table 2Table 2 Master Mode Sampling Frequencies and MCLK/LRCK Ratio

MCLK CLKDIV2=0	MCLK CLKDIV2=1	ADC Sample Rate (ALRCK)	ADCFsRatio [4:0]	DAC Sample Rate (DLRCK)	DACFsRatio [4:0]	SCLK Ratio
Normal Mode						
12.288 MHz	24.576MHz	8 kHz (MCLK/1536)	01010	8 kHz (MCLK/1536)	01010	MCLK/6
		8 kHz (MCLK/1536)	01010	48 kHz (MCLK/256)	00010	MCLK/4
		12 kHz (MCLK/1024)	00111	12 kHz (MCLK/1024)	00111	MCLK/4
		16 kHz (MCLK/768)	00110	16 kHz (MCLK/768)	00110	MCLK/6
		24 kHz (MCLK/512)	00100	24 kHz (MCLK/512)	00100	MCLK/4
		32 kHz (MCLK/384)	00011	32 kHz (MCLK/384)	00011	MCLK/6
		48 kHz (MCLK/256)	00010	8 kHz (MCLK/1536)	01010	MCLK/4
		48 kHz (MCLK/256)	00010	48 kHz (MCLK/256)	00010	MCLK/4
		96 kHz (MCLK/128)	00000	96 kHz (MCLK/128)	00000	MCLK/2
11.2896 MHz	22.5792MHz	8.0182 kHz (MCLK/1408)	01001	8.0182 kHz (MCLK/1408)	01001	MCLK/4
		8.0182 kHz (MCLK/1408)	01001	44.1 kHz (MCLK/256)	00010	MCLK/4
		11.025 kHz (MCLK/1024)	00111	11.025 kHz (MCLK/1024)	00111	MCLK/4
		22.05 kHz (MCLK/512)	00100	22.05 kHz (MCLK/512)	00100	MCLK/4
		44.1 kHz (MCLK/256)	00010	8.0182 kHz (MCLK/1408)	01001	MCLK/4
		44.1 kHz (MCLK/256)	00010	44.1 kHz (MCLK/256)	00010	MCLK/4
		88.2 kHz (MCLK/128)	00000	88.2 kHz (MCLK/128)	00000	MCLK/2
18.432 MHz	36.864MHz	8 kHz (MCLK/2304)	01100	8 kHz (MCLK/2304)	01100	MCLK/6
		8 kHz (MCLK/2304)	01100	48 kHz (MCLK/384)	00011	MCLK/6
		12 kHz (MCLK/1536)	01010	12 kHz (MCLK/1536)	01010	MCLK/6
		16 kHz (MCLK/1152)	01000	16 kHz (MCLK/1152)	01000	MCLK/6
		24 kHz (MCLK/768)	00110	24 kHz (MCLK/768)	00110	MCLK/6
		32 kHz (MCLK/576)	00101	32 kHz (MCLK/576)	00101	MCLK/6
		48 kHz (MCLK/384)	00011	8 kHz (MCLK/2304)	01100	MCLK/6
		48 kHz (MCLK/384)	00011	48 kHz (MCLK/384)	00011	MCLK/6
		96 kHz (MCLK/192)	00001	96 kHz (MCLK/192)	00001	MCLK/3
16.9344 MHz	33.8688MHz	8.0182 kHz (MCLK/2112)	01011	8.0182 kHz (MCLK/2112)	01011	MCLK/6
		8.0182 kHz (MCLK/2112)	01011	44.1 kHz (MCLK/384)	00011	MCLK/6
		11.025 kHz (MCLK/1536)	01010	11.025 kHz (MCLK/1536)	01010	MCLK/6
		22.05 kHz (MCLK/768)	00110	22.05 kHz (MCLK/768)	00110	MCLK/6
		44.1 kHz (MCLK/384)	00011	8.0182 kHz (MCLK/2112)	01011	MCLK/6
		44.1 kHz (MCLK/384)	00011	44.1 kHz (MCLK/384)	00011	MCLK/6
		88.2 kHz (MCLK/192)	00001	88.2 kHz (MCLK/192)	00001	MCLK/3
USB Mode						
12 MHz	24MHz	8 kHz (MCLK/1500)	11011	8 kHz (MCLK/1500)	11011	MCLK
		8 kHz (MCLK/1500)	11011	48 kHz (MCLK/250)	10010	MCLK
		8.0214 kHz (MCLK/1496)	11010	8.0214 kHz (MCLK/1496)	11010	MCLK
		8.0214 kHz (MCLK/1496)	11010	44.118 kHz (MCLK/272)	10011	MCLK
		11.0259 kHz (MCLK/1088)	11001	11.0259 kHz (MCLK/1088)	11001	MCLK
		12 kHz (MCLK/1000)	11000	12 kHz (MCLK/1000)	11000	MCLK
		16 kHz (MCLK/750)	10111	16 kHz (MCLK/750)	10111	MCLK
		22.0588 kHz (MCLK/544)	10110	22.0588 kHz (MCLK/544)	10110	MCLK
		24 kHz (MCLK/500)	10101	24 kHz (MCLK/500)	10101	MCLK
		32 kHz (MCLK/375)	10100*	32 kHz (MCLK/375)	10100*	MCLK
		44.118 kHz (MCLK/272)	10011	8.0214 kHz (MCLK/1496)	11010	MCLK
		44.118 kHz (MCLK/272)	10011	44.118 kHz (MCLK/272)	10011	MCLK
		48 kHz (MCLK/250)	10010	8 kHz (MCLK/1500)	11011	MCLK
		48 kHz (MCLK/250)	10010	48 kHz (MCLK/250)	10010	MCLK
		88.235 kHz (MCLK/136)	10001	88.235 kHz (MCLK/136)	10001	MCLK
		96 kHz (MCLK/125)	10000	96 kHz (MCLK/125)	10000	MCLK

MICRO-CONTROLLER CONFIGURATION INTERFACE

The device supports standard SPI and 2-wire micro-controller configuration interface. External micro-controller can completely configure the device through writing to internal configuration registers. Please see section for the details of configuration register definition.

The identical device pins are used to configure either SPI or 2-wire interface. In SPI mode, pin CE, CCLK and CDATA function as SPI_CSn, SPI_CLK and SPI_DIN. In 2-wire mode, pin CE, CCLK and CDATA function as AD0, SCL and SDA. To select SPI mode, apply high to low transition signal to CE pin. Otherwise the device will operate in 2-wire interface mode.

SPI

PA5331 has a SPI (Serial Peripheral Interface) compliant synchronous serial slave controller inside the chip. It provides the ability to allow the external master SPI controller to access the internal registers, and thus control the operations of chip.

All lines on the SPI bus are unidirectional: The SPI_CLK is generated by the master controller and is primarily used to synchronize data transfer, the SPI_DIN line carries data from the master to the slave; SPI_CSn is generated by the master to select PA5331.

The timing diagram of this interface is given in Figure 1. The high to low transition at SPI_CSn pin indicates the SPI interface selected. Each write procedure contains 3 words, i.e. Chip Address plus R/W bit, internal register address and internal register data. Every word length is fixed at 8 bits. The input SPI_DIN data are sampled at the rising edge of SPI_CLK clock. The MSB bit in each word is transferred firstly. The transfer rate can be up to 10M bps.

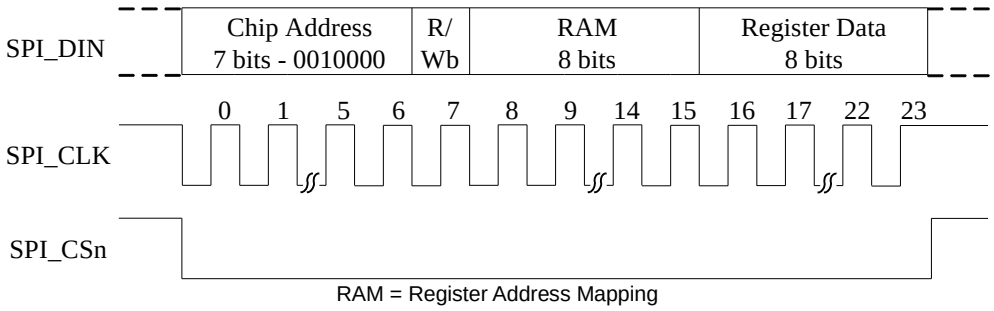


Figure 1 SPI Configuration Interface Timing Diagram

2-wire

2-wire interface is a bi-directional serial bus that uses a serial data line (SDA) and a serial clock line (SCL) for data transfer. The timing diagram for data transfer of this interface is given in Figure 2. Data are transmitted synchronously to SCL clock on the SDA line on a byte-by-byte basis. Each bit in a byte is sampled during SCL high with MSB bit being transmitted firstly. Each transferred byte is followed by an acknowledge bit from receiver to pull the SDA low. The transfer rate of this interface can be up to 100k bps.

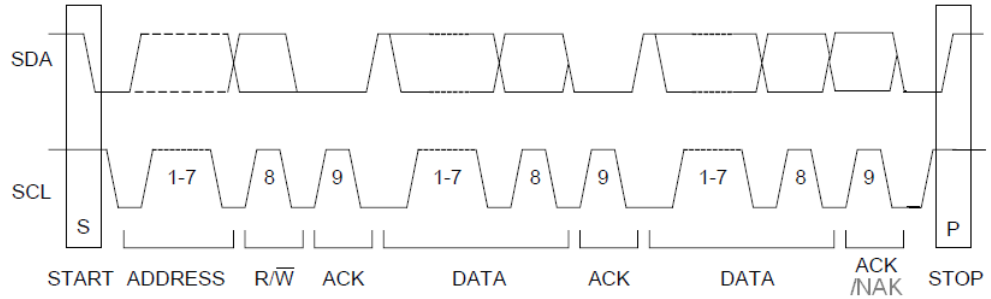


Figure 2 Complete Data Transfer for 2-wire Interface

A master controller initiates the transmission by sending a “start” signal, which is defined as a high-to-low transition at SDA while SCL is high. The first byte transferred is the slave address. It is a seven-bit chip address followed by a RW bit. The chip address must be 001000x, where x equals AD0 (pin CE). The RW bit indicates the slave data transfer direction. Once an acknowledge bit is received, the data transfer starts to proceed on a byte-by-byte basis in the direction specified by the RW bit. The master can terminate the communication by generating a “stop” signal, which is defined as a low-to-high transition at SDA while SCL is high.

In 2-wire interface mode, the registers can be written and read. The formats of "write" and "read" instructions are shown in Table 3 and Table 4. Please note that, to read data from a register, you must set R/W bit to 0 to access the register address and then set R/W to 1 to read data from the register. There are no acknowledge bit after data to be written or read, this is the only difference from the I^2C protocol.

Table 3 Write Data to Register in 2-wire Interface Mode

Chip Address	R/W	Register Address		Data to be written		
001000	AD0	0	ACK	RAM	ACK	DATA

Table 4 Read Data from Register in 2-wire Interface Mode

Chip Address	R/W	Register Address		
001000	AD0	0	ACK	RAM
Chip Address	**R/W**	**Data to be read**		
001000	AD0	1	ACK	DATA

CONFIGURATION REGISTER DEFINITION

SPI and 2-wire configuration interface share the same registers because there is only one interface active at any time. There are total of 53 user programmable 8-bit registers in this device. These registers control the operations of ADC and DAC. External master controller can access these registers by using the slave address specified in RAM (Register Address Map) register as shown in the Table 5.

Table 5 Bit Content of Register Address Map

	B7	B6	B5	B4	B3	B2	B1	B0
Reg. 00	SCPReset	LRCM	DACMCLK	SameFs	SeqEn	EnRef	VMIDSEL	
Reg. 01	TSDEN	PdnOC	LPVcmMod	LPVrefBuf	PdnAna	PdnIbiasgen	VrefrLo	PdnVrefbuf
Reg. 02	adc_DigPDN	dac_DigPDN	adc_stm_rst	dac_stm_rst	ADCDLL_PDN	DACDLL_PDN	adcVref_PDN	dacVref_PDN
Reg. 03	PdnAINL	PdnAINR	PdnADCL	PdnADCR	PdnMICB	PdnADCBiasgen	flashLP	int1LP
Reg. 04	PdnDACL	PdnDACR	LOUT1	ROUT1	LOUT2	ROUT2	MONO	OUT3
Reg. 05	LPDACL	LPDACR	LPLOUT1	OC[2]	LPLOUT2	OC[3]	LPMONO	LPOUT3
Reg. 06	LPPGA	LPLMIX	LPRMIX	LPMMIX	LPMOUTINV	LPOUT2INV	LPADCvrp	LPDACvrp
Reg. 07		VSEL						
Reg. 08	MSC	MCLKDIV2	BCLK_INV	BCLKDIV				
Reg. 09	MicAmpL				MicAmpR			
Reg. 10	LINSEL		RINSEL					
Reg. 11	DS			MONOMIX		TRI	OC[1:0]	
Reg. 12	DATSEL		ADCLRP	ADCWL			ADCFORMAT	
Reg. 13			ADCFsMode	ADCFsRatio				
Reg. 14	ADC_invL	ADC_invR	ADC_HPF_L	ADC_HPF_R				
Reg. 15	ADCRampRate	ADCSoftRamp	ADCZeroCrs	ADCLeR	ADCMute			
Reg. 16	LADCVOL							
Reg. 17	RADCVOL							
Reg. 18	ALCSEL		MAXGAIN			MINGAIN		
Reg. 19	ALCLVL				ALCHLD			
Reg. 20	ALCDCY				ALCATK			
Reg. 21	ALCMODE	ALCZC	TIME_OUT	WIN_SIZE				
Reg. 22	NGTH					NGG		NGAT

Reg. 23	DACLRSWAP	DACLRP	DACWL			DACFORMAT		
Reg. 24			DACFsMode	DACFsRatio				
Reg. 25	DACRampRate		DACSoftRamp	DACZeroCrs	DACLeR	DACMute	AutoMute	
Reg. 26	DACVolumeL (LDACVOL)							
Reg. 27	DACVolumeR (RDACVOL)							
Reg. 28	DeemphasisMode		DAC_invL	DAC_invR	ClickFree			
Reg. 29	ZeroL	ZeroR	Mono	SE			Vpp_scale	
Reg. 30			Shelving_a[29:24]					
Reg. 31	Shelving_a[23:16]							
Reg. 32	Shelving_a[15:8]							
Reg. 33	Shelving_a[7:0]							
Reg. 34			Shelving_b[29:24]					
Reg. 35	Shelving_b[23:16]							
Reg. 36	Shelving_b[15:8]							
Reg. 37	Shelving_b[7:0]							
Reg. 38			LMIXSEL			RMIXSEL		
Reg. 39	LD2LO	LI2LO	LI2LOVOL					
Reg. 40	RD2LO	RI2LO	RI2LOVOL					
Reg. 41	LD2RO	LI2RO	LI2ROVOL					
Reg. 42	RD2RO	RI2RO	RI2ROVOL					
Reg. 43	LD2MO	LI2MO	LI2MOVOL					
Reg. 44	RD2MO	RI2MO	RI2MOVOL					
Reg. 45	ROUT2INV	OUT3SW		VROI	HPSWEN	HPSWPOL	MOUTINV	
Reg. 46		LOUT1VOL						
Reg. 47		ROUT1VOL						
Reg. 48		LOUT2VOL						
Reg. 49		ROUT2VOL						
Reg. 50		MONOOUTVOL						
Reg. 51	hpLout1_ref1	hpLout1_ref2	hpRout1_ref1	hpRout1_ref2	hpOut3_ref1	hpOut3_ref2	hpMono_ref1	hpMono_ref2
Reg. 52	spkLout2_ref1	spkLout2_ref2	spkRout2_ref1	spkRout2_ref2	mixer_ref1	mixer_ref2	MREF1	MREF2

CHIP CONTROL AND POWER MANAGEMENT

Register 0 – Chip Control 1, Default 0000 0110

Bit Name	Bit	Description
SCPReset	7	0 – normal (default) 1 – reset control port register to default
LRCM	6	0 – ALRCK disabled when both ADC disabled; DLRCK disabled when both DAC disabled (default) 1 – ALRCK and DLRCK disabled when all ADC and DAC disabled
DACMCLK	5	0 – when SameFs=1, ADCMCLK is the chip master clock source (default) 1 – when SameFs=1, DACMCLK is the chip master clock source
SameFs	4	0 – ADC Fs differs from DAC Fs (default) 1 – ADC Fs is the same as DAC Fs
SeqEn	3	0 – internal power up/down sequence disable (default) 1 – internal power up/down sequence enable
EnRef	2	0 – disable reference 1 – enable reference (default)
VMIDSEL	1:0	00 – Vmid disabled 01 – 50 kΩ divider enabled 10 – 500 kΩ divider enabled (default) 11 – 5 kΩ divider enabled

Register 1 – Chip Control 2, Default 0001 1100

Bit Name	Bit	Description
TSDEN	7	0 – thermal shutdown disabled (default) 1 – thermal shutdown enabled
PdnOC	6	0 – over current shutdown disabled (default) 1 – over current shutdown enabled
LPVcmMod	5	0 – normal (default) 1 – low power
LPVrefBuf	4	0 – normal 1 – low power (default)
PdnAna	3	0 – normal 1 – entire analog power down (default)
PdnIbiasgen	2	0 – normal 1 – ibiasgen power down (default)
VrefLo	1	0 – normal (default) 1 – low power
PdnVrefbuf	0	0 – normal (default) 1 – power down

Register 2 – Chip Power Management, Default 1100 0011

Bit Name	Bit	Description
adc_DigPDN	7	0 – normal 1 – resets ADC DEM, filter and serial data port (default)
dac_DigPDN	6	0 – normal 1 – resets DAC DSM, DEM, filter and serial data port (default)
adc_stm_rst	5	0 – normal (default) 1 – reset ADC state machine to power down state
dac_stm_rst	4	0 – normal (default) 1 – reset DAC state machine to power down state
ADCDLL_PDN	3	0 – normal (default) 1 – ADC_DLL power down, stop ADC clock
DACDLL_PDN	2	0 – normal (default) 1 – DAC DLL power down, stop DAC clock
adcVref_PDN	1	0 – ADC analog reference power up 1 – ADC analog reference power down (default)
dacVref_PDN	0	0 – DAC analog reference power up 1 – DAC analog reference power down (default)

Register 3 – ADC Power Management, Default 1111 1100

Bit Name	Bit	Description
PdnAINL	7	0 – normal 1 – left analog input power down (default)
PdnAINR	6	0 – normal 1 – right analog input power down (default)
PdnADCL	5	0 – left ADC power up 1 – left ADC power down (default)
PdnADCR	4	0 – right ADC power up 1 – right ADC power down (default)
PdnMICB	3	0 – microphone bias power on 1 – microphone bias power down (high impedance output, default)
PdnADCBiasgen	2	0 – normal 1 – power down (default)
flashLP	1	0 – normal (default) 1 – flash ADC low power
int1LP	0	0 – normal (default) 1 – int1 low power

Register 4 – DAC Power Management, Default 1100 0000

Bit Name	Bit	Description
PdnDACL	7	0 – left DAC power up 1 – left DAC power down (default)
PdnDACR	6	0 – right DAC power up 1 – right DAC power down (default)
LOUT2	5	0 – LOUT2 disabled (default) 1 – LOUT2 enabled
ROUT2	4	0 – ROUT2 disabled (default) 1 – ROUT2 enabled
LOUT1	3	0 – LOUT1 disabled (default) 1 – LOUT1 enabled
ROUT1	2	0 – ROUT1 disabled (default) 1 – ROUT1 enabled
MONO	1	0 – reserved (default) 1 – reserved
OUT3	0	0 – reserved (default) 1 – reserved

Register 5 – Chip Low Power 1, Default 0000 0000

Bit Name	Bit	Description
LPDACL	7	0 – normal (default) 1 – low power
LPDACR	6	0 – normal (default) 1 – low power
LPLOUT1	5	0 – normal (default) 1 – low power
OC[2]	4	0 – over current setting (default) 1 – over current setting
LPLOUT2	3	0 – normal (default) 1 – low power
OC[3]	2	0 – over current setting (default) 1 – over current setting
LPMONO	1	0 – normal (default) 1 – low power
LPOUT3	0	0 – normal (default) 1 – low power

Register 6 – Chip Low Power 2, Default 0000 0000

Bit Name	Bit	Description

LPPGA	7	0 – normal (default) 1 – low power
LPLMIX	6	0 – normal (default) 1 – low power
LPRMIX	5	0 – normal (default) 1 – low power
LPMMIX	4	0 – normal (default) 1 – low power
LPMOUTINV	3	0 – normal (default) 1 – low power
LPOUT2INV	2	0 – normal (default) 1 – low power
LPADCvrp	1	0 – normal (default) 1 – low power
LPDACvrp	0	0 – normal (default) 1 – low power

Register 7 – Analog Voltage Management, Default 0111 1100

Bit Name	Bit	Description
VSEL	6:0	1111100 – normal (default)

Register 8 – Master Mode Control, Default 1000 0000

Bit Name	Bit	Description
MSC	7	0 – slave serial port mode 1 – master serial port mode (default)
MCLKDIV2	6	0 – MCLK not divide (default) 1 – MCLK divide by 2
BCLK_INV	5	0 – normal (default) 1 – BCLK inverted
BCLKDIV	4:0	00000 – master mode BCLK generated automatically based on the clock table (default) Others – MCLK/N, N=1~31

ADC CONTROL

Register 9 – ADC Control 1, Default 0000 0000

Bit Name	Bit	Description
MicAmpL	7:4	Left channel PGA gain 0000 – 0 dB (default) 0001 – +3 dB 0010 – +6 dB 0011 – +9 dB 0100 – +12 dB 0101 – +15 dB 0110 – +18 dB 0111 – +21 dB 1000 – +24 dB
MicAmpR	3:0	Right channel PGA gain 0000 – 0dB (default) 0001 – +3 dB 0010 – +6 dB 0011 – +9 dB 0100 – +12 dB 0101 – +15 dB 0110 – +18 dB 0111 – +21 dB 1000 – +24 dB

Register 10 – ADC Control 2, Default 0000 0000

Bit Name	Bit	Description
LINSEL	7:6	Left channel input select 00 – reserved (default) 01 – LINPUT1 10 – reserved 11 – L-R differential (either LINPUT1-RINPUT1, selected by DS)
RINSEL	5:4	Right channel input select 00 – reserved (default) 01 – RINPUT1 10 – LINPUT2 11 – L-R differential (either LINPUT1-RINPUT1, selected by DS)

Register 11 – ADC Control 3, Default 0000 0110

Bit Name	Bit	Description
DS	7	Differential input select 0 – reserved (default) 1 – LINPUT1-RINPUT1
MONOMIX	4:3	00 – stereo (default) 01 – analog mono mix to left ADC 10 – analog mono mix to right ADC 11 – reserved
TRI	2	0 – ASDOUT is ADC normal output (default) 1 – ASDOUT tri-stated, ALRCK, DLRCK and SCLK are inputs
OC[1:0]	1:0	00 – over current setting (default)

Register 12 – ADC Control 4, Default 0000 0000

Bit Name	Bit	Description
DATSEL	7:6	00 – left data = left ADC, right data = right ADC 01 – left data = left ADC, right data = left ADC 10 – left data = right ADC, right data = right ADC 11 – left data = right ADC, right data = left ADC
ADCLRP	5	I2S, left justified or right justified mode: 0 – left and right normal polarity 1 – left and right inverted polarity DSP/PCM mode: 0 – MSB is available on 2nd BCLK rising edge after ALRCK rising edge 1 – MSB is available on 1st BCLK rising edge after ALRCK rising edge
ADCWL	4:2	000 – 24-bit serial audio data word length 001 – 20-bit serial audio data word length 010 – 18-bit serial audio data word length 011 – 16-bit serial audio data word length 100 – 32-bit serial audio data word length
ADCFORMAT	1:0	00 – I2S serial audio data format 01 – left justify serial audio data format 10 – right justify serial audio data format 11 – DSP/PCM mode serial audio data format

Register 13 – ADC Control 5, Default 0000 0110

Bit Name	Bit	Description
ADCFsMode	5	0 – single speed mode (default) 1 – double speed mode
ADCFsRatio	4:0	Master mode ADC MCLK to sampling frequency ratio

		00000 – 128 00001 – 192 00010 – 256 00011 – 384 00100 – 512 00101 – 576 00110 – 768 (default) 00111 – 1024 01000 – 1152 01001 – 1408 01010 – 1536 01011 – 2112 01100 – 2304 Other – reserved	10000 – 125 10001 – 136 10010 – 250 10011 – 272 10100 – 375 10101 – 500 10110 – 544 10111 – 750 11000 – 1000 11001 – 1088 11010 – 1496 11011 – 1500

Register 14 – ADC Control 6, Default 0011 0000

Bit Name	Bit	Description
ADC_invL	7	0 – normal (default) 1 – left channel polarity inverted
ADC_invR	6	0 – normal (default) 1 – right channel polarity inverted
ADC_HPF_L	5	0 – disable ADC left channel high pass filter 1 – enable ADC left channel high pass filter (default)
ADC_HPF_R	4	0 – disable ADC right channel high pass filter 1 – enable ADC right channel high pass filter (default)

Register 15 – ADC Control 7, Default 0011 0000

Bit Name	Bit	Description
ADCRampRate	7:6	00 – 0.5 dB per 4 LRCK digital volume control ramp rate (default) 01 – 0.5 dB per 8 LRCK digital volume control ramp rate 10 – 0.5 dB per 16 LRCK digital volume control ramp rate 11 – 0.5 dB per 32 LRCK digital volume control ramp rate
ADCSoftRamp	5	0 – disabled digital volume control soft ramp 1 – enabled digital volume control soft ramp (default)
ADCZeroCrs	4	0 – disabled digital volume control change at zero cross 1 – enabled digital volume control change at zero cross (default)
ADCLeR	3	0 – normal (default) 1 – both channel gain control is set by ADC left gain control register
ADCMute	2	0 – normal (default) 1 – mute ADC digital output

Register 16 – ADC Control 8, Default 1100 0000

Bit Name	Bit	Description
LADCVOL	7:0	Digital volume control attenuates the signal in 0.5 dB incremental from 0 to –96 dB. 00000000 – 0 dB 00000001 – -0.5 dB 00000010 – -1 dB … 11000000 – -96 dB (default)

Register 17 – ADC Control 9, Default 1100 0000

Bit Name	Bit	Description
RADCVOL	7:0	Digital volume control attenuates the signal in 0.5 dB incremental from 0 to –96 dB. 00000000 – 0 dB 00000001 – -0.5 dB 00000010 – -1 dB … 11000000 – -96 dB (default)

Register 18 – ADC Control 10, Default 0011 1000

Bit Name	Bit	Description
ALCSEL	7:6	00 – ALC off 01 – ALC right channel only 10 – ALC left channel only 11 – ALC stereo
MAXGAIN	5:3	Set maximum gain of PGA 000 – -6.5 dB 001 – -0.5 dB 010 – 5.5 dB 011 – 11.5 dB 100 – 17.5 dB 101 – 23.5 dB 110 – 29.5 dB 111 – 35.5 dB
MINGAIN	2:0	Set minimum gain of PGA 000 – -12 dB 001 – -6 dB 010 – 0 dB 011 – +6 dB 100 – +12 dB 101 – +18 dB 110 – +24 dB 111 – +30 dB

Register 19 – ADC Control 11, Default 1011 0000

Bit Name	Bit	Description
ALCLVL	7:4	ALC target 0000 – –22.5dBFS 0001 – –21.0dBFS …… 1100 – –4.5dBFS 1101 – –3dBFS 1110 – –1.5dBFS 1111 – –1.5dBFS
ALCHLD	3:0	ALC hold time before gain is increased 0000 – 0ms 0001 – 2.67ms 0010 – 5.33ms …… (time doubles with every step) 1001 – 0.68s 1010 or higher – 1.36s

Register 20 – ADC Control 12, Default 0011 0010

Bit Name	Bit	Description
ALCDCY	7:4	ALC decay (gain ramp up) time, ALC mode/limiter mode: 0000 – 410 us/90.8 us 0001 – 820 us/182us 0010 – 1.64 ms/363us …… (time doubles with every step) 1001 – 210 ms/46.5 ms 1010 or higher – 420 ms/93 ms
ALCATK	3:0	ALC attack (gain ramp down) time, ALC mode/limiter mode: 0000 – 104 us/22.7 us 0001 – 208 us/45.4 us 0010 – 416 us/90.8 us …… (time doubles with very step) 1001 – 53.2 ms/11.6 ms 1010 or higher – 106 ms/23.2 ms

Register 21 – ADC Control 13, Default 0000 0110

Bit Name	Bit	Description
ALCMODE	7	Determines the ALC mode of operation: 0 – ALC mode (Normal Operation) 1 – Limiter mode.
ALCZC	6	ALC uses zero cross detection circuit. 0 – disable (recommended) 1 – enable
TIME_OUT	5	Zero Cross time out 0 – disable (default) 1 – enable
WIN_SIZE	4:0	Windows size for peak detector ,set the window size to N*16 samples 00110 – 96 samples (default) 00111 – 102 samples ….. 11111 – 496 samples

Register 22 – ADC Control 14, Default 0000 0000

Bit Name	Bit	Description
NGTH	7:3	Noise gate threshold 00000 – -76.5 dBFS 00001 – -75 dBFS …… 11110 – -31.5 dBFS 11111 – -30 dBFS
NGG	2:1	Noise gate type x0 – PGA gain held constant 01 – mute ADC output 11 – reserved
NGAT	0	Noise gate function enable 0 – disable 1 – enable

DAC CONTROL

Register 23 – DAC Control 1, Default 0000 0000

Bit Name	Bit	Description
DACLRSWAP	7	0 – normal 1 – left and right channel data swap
DACLRP	6	I2S, left justified or right justified mode: 0 – left and right normal polarity 1 – left and right inverted polarity DSP/PCM mode: 0 – MSB is available on 2nd BCLK rising edge after ALRCK rising edge 1 – MSB is available on 1st BCLK rising edge after ALRCK rising edgeLRCK Polarity
DACWL	5:3	000 – 24-bit serial audio data word length 001 – 20-bit serial audio data word length 010 – 18-bit serial audio data word length 011 – 16-bit serial audio data word length 100 – 32-bit serial audio data word length
DACFORMAT	2:1	00 – I2S serial audio data format 01 – left justify serial audio data format 10 – right justify serial audio data format 11 – DSP/PCM mode serial audio data format
	0	

Register 24 – DAC Control 2, Default 0000 0110

Bit Name	Bit	Description
DACFsMode	5	0 – single speed mode (default)

		1 – double speed mode
DACFsRatio	4:0	Master mode DAC MCLK to sampling frequency ratio 00000 — 128; 00001 — 192; 00010 — 256; 00011 — 384; 00100 — 512; 00101 — 576; 00110 — 768; (default) 00111 — 1024; 01000 — 1152; 01001 — 1408; 01010 — 1536; 01011 — 2112; 01100 — 2304; 10000 — 125; 10001 — 136; 10010 — 250; 10011 — 272; 10100 — 375; 10101 — 500; 10110 — 544; 10111 — 750; 11000 — 1000; 11001 — 1088; 11010 — 1496; 11011 — 1500; Other — Reserved.

Register 25 – DAC Control 3, Default 0011 0010

Bit Name	Bit	Description
DACRampRate	7:6	00 – 0.5 dB per 4 LRCK digital volume control ramp rate (default) 01 – 0.5 dB per 32 LRCK digital volume control ramp rate 10 – 0.5 dB per 64 LRCK digital volume control ramp rate 11 – 0.5 dB per 128 LRCK digital volume control ramp rate
DACSoftRamp	5	0 – disabled digital volume control soft ramp 1 – enabled digital volume control soft ramp (default)
DACZeroCrs	4	0 – disabled digital volume control change at zero cross 1 – enabled digital volume control change at zero cross (default)
DACLeR	3	0 – normal (default) 1 – both channel gain control is set by DAC left gain control register
DACMute	2	0 – normal (default) 1 – mute analog outputs for both channels
AutoMute	1	0 – disable 1 – enable (default)

Register 26 – DAC Control 4, Default 1100 0000

Bit Name	Bit	Description
LDACVOL	7:0	Digital volume control attenuates the signal in 0.5 dB incremental from 0 to –96 dB. 00000000 – 0 dB 00000001 – -0.5 dB 00000010 – -1 dB … 11000000 – -96 dB (default)

Register 27 – DAC Control 5, Default 1100 0000

Bit Name	Bit	Description
RDACVOL	7:0	Digital volume control attenuates the signal in 0.5 dB incremental from 0 to –96 dB. 00000000 – 0 dB 00000001 – -0.5 dB 00000010 – -1 dB … 11000000 – -96 dB (default)

Register 28 – DAC Control 6, Default 0000 1000

Bit Name	Bit	Description
DeemphasisMode (DEEMP)	7:6	00 – de-emphasis frequency disabled (default) 01 – 32 KHz de-emphasis frequency in single speed mode 10 – 44.1 KHz de-emphasis frequency in single speed mode 11 – 48 KHz de-emphasis frequency in single speed mode

DAC_invL	5	0 – normal DAC left channel analog output no phase inversion (default) 1 – normal DAC left channel analog output 180 degree phase inversion
DAC_invR	4	0 – normal DAC right channel analog output no phase inversion (default) 1 – normal DAC right analog output 180 degree phase inversion
ClickFree	3	0 – disable digital click free power up and down 1 – enable digital click free power up and down (default)

Register 29 – DAC Control 7, Default 0000 0110

Bit Name	Bit	Description
ZeroL	7	0 – normal (default) 1 – set Left Channel DAC output all zero
ZeroR	6	0 – normal (default) 1 – set Right Channel DAC output all zero
Mono	5	0 – stereo (default) 1– mono (L+R)/2 into DACL and DACR
SE	4:2	SE strength, total 8 settings, L=L+(L-R)*a, R=R+(R-L)*a, where a is from 0 to 7/8 000 – 0 (default) …… 111 – 7/8
Vpp_scale	1:0	00 – Vpp set at 3.5V (0.7 modulation index) (default) 01 – Vpp set at 4.0V 10 – Vpp set at 3.0V 11 – Vpp set at 2.5V

Register 30 – DAC Control 8, Default 0001 1111

Bit Name	Bit	Description
Shelving_a[29:24]	5:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

Register 31 – DAC Control 9, Default 1111 0111

Bit Name	Bit	Description
Shelving_a[23:16]	7:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

Register 32 – DAC Control 10, Default 1111 1101

Bit Name	Bit	Description
Shelving_a[15:8]	7:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

Register 33 – DAC Control 11, Default 1111 1111

Bit Name	Bit	Description
Shelving_a[7:0]	7:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

Register 34 – DAC Control 12, Default 0001 1111

Bit Name	Bit	Description
Shelving_b[29:24]	5:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

Register 35 – DAC Control 13, Default 1111 0111

Bit Name	Bit	Description
Shelving_b[23:16]	7:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

Register 36 – DAC Control 14, Default 1111 1101

Bit Name	Bit	Description
Shelving_b[15:8]	7:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

Register 37 – DAC Control 15, Default 1111 1111

Bit Name	Bit	Description
Shelving_b[7:0]	7:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

Register 38 – DAC Control 16, Default 0000 0000

Bit Name	Bit	Description
LMIXSEL	5:3	Left input select for output mix 000 – reserved (default) 001 – LIN1 010 – reserved 011 – left ADC input (after mic amplifier)
RMIXSEL	2:0	Right input select for output mix 000 – reserved (default) 001 – RIN1 010 – LIN2 011 – right ADC input (after mic amplifier)

Register 39 – DAC Control 17, Default 0011 1000

Bit Name	Bit	Description
LD2LO	7	0 – left DAC to left mixer disable (default) 1 – left DAC to left mixer enable
LI2LO	6	0 – LIN signal to left mixer disable (default) 1 – LIN signal to left mixer enable
LI2LOVOL	5:3	LIN signal to left mixer gain 000 – 6 dB 001 – 3 dB 010 – 0 dB 011 – -3 dB 100 – -6 dB 101 – -9 dB 110 – -12 dB 111 – -15 dB (default)

Register 40 – DAC Control 18, Default 0011 1000

Bit Name	Bit	Description
RD2LO	7	0 – right DAC to left mixer disable (default) 1 – right DAC to left mixer enable
RI2LO	6	0 – RIN signal to left mixer disable (default) 1 – RIN signal to left mixer enable
RI2LOVOL	5:3	RIN signal to left mixer gain 000 – 6 dB 001 – 3 dB 010 – 0 dB 011 – -3 dB 100 – -6 dB 101 – -9 dB 110 – -12 dB 111 – -15 dB (default)

Register 41 – DAC Control 19, Default 0011 1000

Bit Name	Bit	Description
LD2RO	7	0 – left DAC to right mixer disable (default) 1 – left DAC to right mixer enable

LI2RO	6	0 – LIN signal to right mixer disable (default) 1 – LIN signal to right mixer enable
LI2ROVOL	5:3	LIN signal to right mixer gain 000 – 6 dB 001 – 3 dB 010 – 0 dB 011 – -3 dB 100 – -6 dB 101 – -9 dB 110 – -12 dB 111 – -15 dB (default)

Register 42 – DAC Control 20, Default 0011 1000

Bit Name	Bit	Description
RD2RO	7	0 – right DAC to right mixer disable (default) 1 – right DAC to right mixer enable
RI2RO	6	0 – RIN signal to right mixer disable (default) 1 – RIN signal to right mixer enable
RI2ROVOL	5:3	RIN signal to right mixer gain 000 – 6 dB 001 – 3 dB 010 – 0 dB 011 – -3 dB 100 – -6 dB 101 – -9 dB 110 – -12 dB 111 – -15 dB (default)

Register 43 – DAC Control 21, Default 0011 1000

Bit Name	Bit	Description
LD2MO	7	0 – reserved (default) 1 – reserved
LI2MO	6	0 – reserved (default) 1 – reserved
LI2MOVOL	5:3	reserved

Register 44 – DAC Control 22, Default 0011 1000

Bit Name	Bit	Description
RD2MO	7	0 – reserved (default) 1 – reserved
RI2MO	6	0 – reserved (default) 1 – reserved
RI2MOVOL	5:3	reserved

Register 45 – DAC Control 23, Default 0000 0000

Bit Name	Bit	Description
ROUT1INV	7	0 – ROUT1 no inversion (default) 1 – ROUT1 signal inverted
OUT3SW	6:5	Reserved
VROI	4	0 – 1.5k VREF to analog output resistance (default) 1 – 40k VREF to analog output resistance
HPSWEN	3	0 – headphone switch disabled (default) 1 – headphone switch enabled
HPSWPOL	2	0 – HPDETECT high=headphone (default) 1 – HPDETECT high=speaker
MOUTINV	1	0 – reserved (default) 1 – reserved

Register 46 – DAC Control 24, Default 0000 0000

Bit Name	Bit	Description
LOUT2VOL	5:0	LOUT2 volume 000000 – -30dB (default) 000001 – -29dB 000010 – -28dB … 011110 – 0dB 011111 – 1dB … 100100 – 6dB

Register 47 – DAC Control 25, Default 0000 0000

Bit Name	Bit	Description
ROUT2VOL	5:0	ROUT2 volume 000000 – -30dB (default) 000001 – -29dB 000010 – -28dB … 011110 – 0dB 011111 – 1dB … 100100 – 6dB

Register 48 – DAC Control 26, Default 0000 0000

Bit Name	Bit	Description
LOUT1VOL	5:0	LOUT1 volume 000000 – -30dB (default) 000001 – -29dB 000010 – -28dB … 011110 – 0dB 011111 – 1dB … 100100 – 6dB

Register 49 – DAC Control 27, Default 0000 0000

Bit Name	Bit	Description
ROUT1VOL	5:0	ROUT1 volume 000000 – -30dB (default) 000001 – -29dB 000010 – -28dB … 011110 – 0dB 011111 – 1dB … 100100 – 6dB

Register 50 – DAC Control 28, Default 0000 0000

Bit Name	Bit	Description
MONOOUTVOL	5:0	Reserved

Register 51 – DAC Control 29, Default 0000 0000

Bit Name	Bit	Description
hpLout1_ref1	7	Reserved
hpLout1_ref2	6	Reserved
hpRout1_ref1	5	Reserved
hpRout1_ref2	4	Reserved

hpOut3_ref1	3	Reserved
hpOut3_ref2	2	Reserved
hpMono_ref1	1	Reserved
hpMono_ref2	0	Reserved

Register 52 – DAC Control 30, Default 0000 0000

Bit Name	Bit	Description
spkLout2_ref1	7	Reserved
spkLout2_ref2	6	Reserved
spkRout2_ref1	5	Reserved
spkRout2_ref2	4	Reserved
mixer_ref1	3	Reserved
mixer_ref2	2	Reserved
MREF1	1	Reserved
MREF2	0	Reserved

DIGITAL AUDIO INTERFACE

The PA5331 provides four formats of serial audio data interface to the input of the DAC or output from the ADC through LRCK, SCLK and SDIN/SDOUT pins. The four formats are I^2S, left justified, right justified and DSP/PCM mode. DAC input DSDIN is sampled by PA5331 on the rising edge of DSCLK. ADC data is out on ASDOUT and changes on the falling edge of ASCLK. The relationship of SDATA (SDIN/SDOUT), SCLK and LRCK with the three formats is shown through Figure 3 to Figure 7.

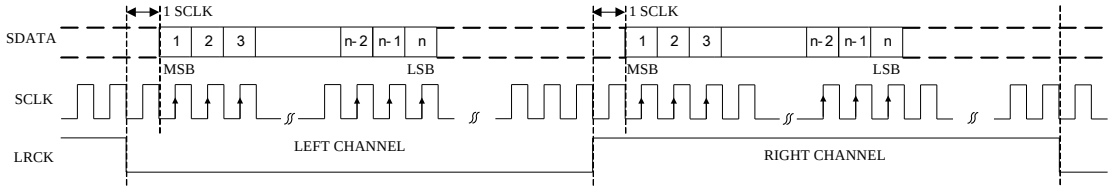


Figure 3 I^2S Serial Audio Data Format Up To 24-bit

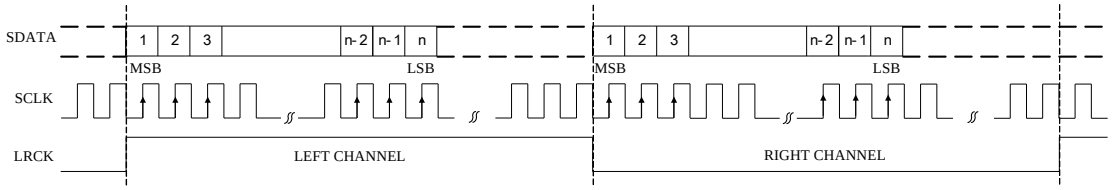


Figure 4 Left Justified Serial Audio Data Format Up To 24-bit

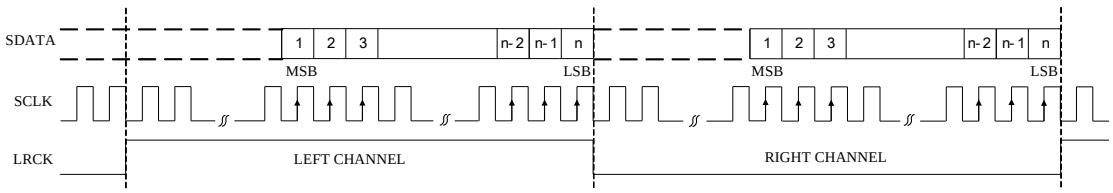


Figure 5 Right Justified Serial Audio Data Format Up To 24-bit

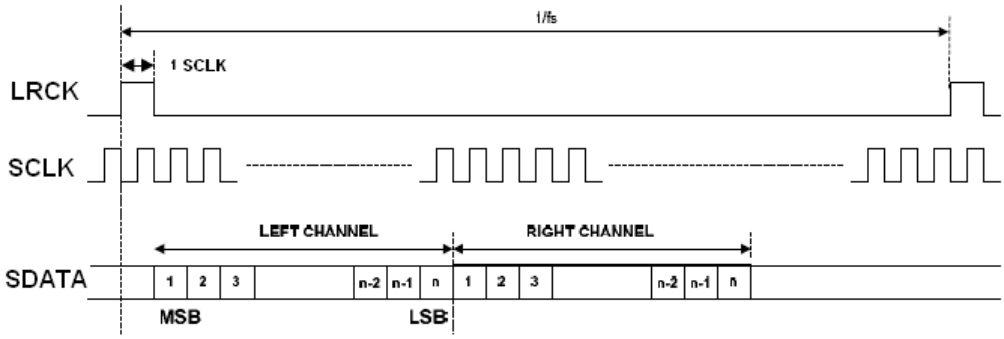


Figure 6 DSP/PCM Mode A

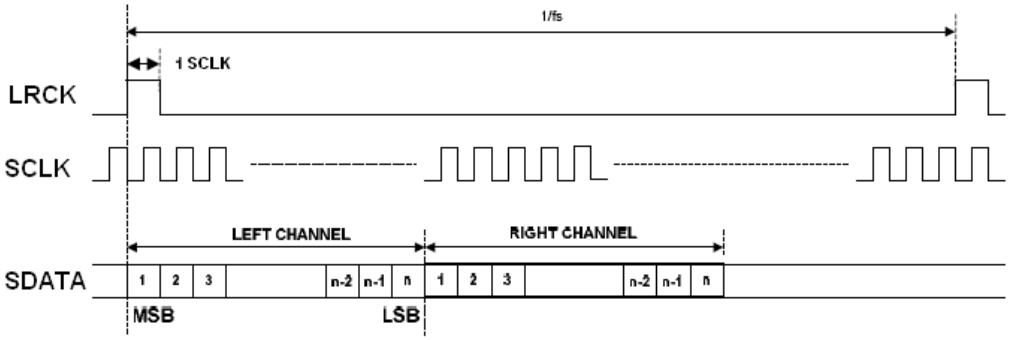
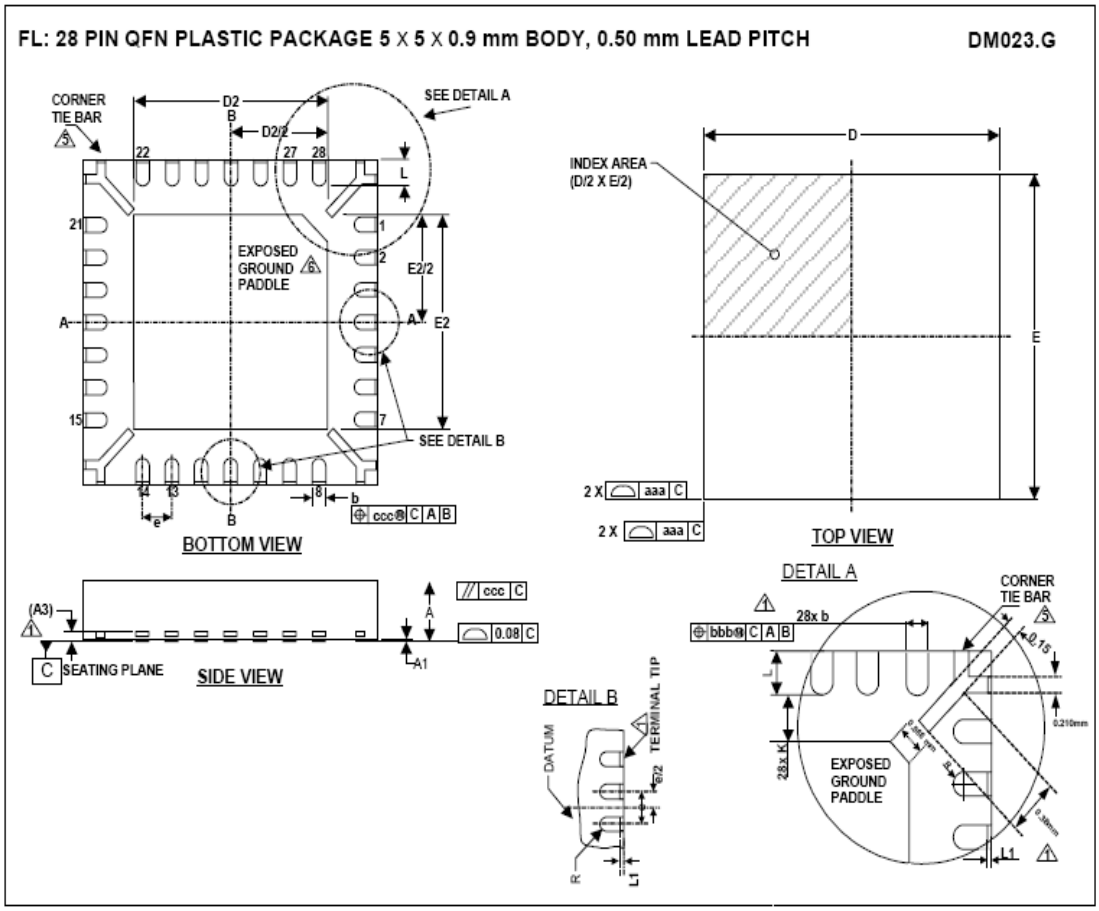


Figure 7 DSP/PCM Mode B

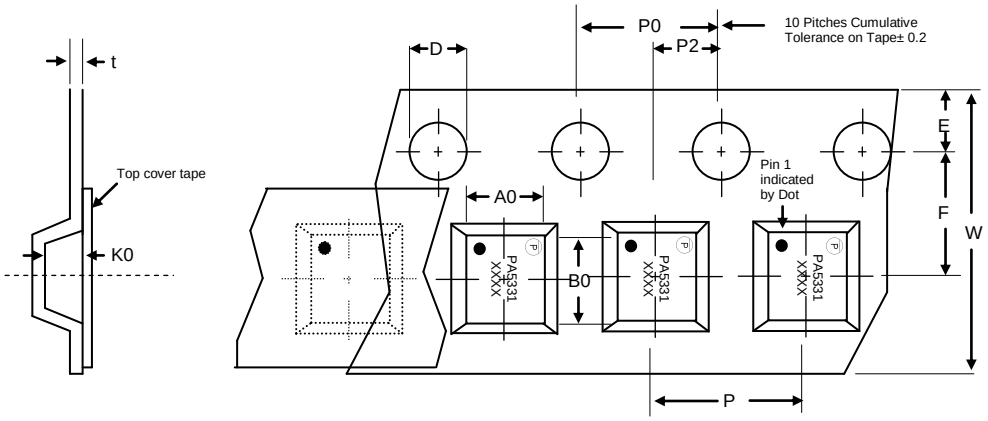
PACKAGE DIMENSIONS AND MEASUREMENTS



Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
A	0.85	0.90	1.00	
A1	0	0.02	0.05	
A3		0.2 REF		
b	0.18	0.23	0.30	1
D		5.00 BSC		
D2	3.2	3.3	3.4	2
E		5.00 BSC		
E2	3.2	3.3	3.4	2
e		0.5 BSC		
L	0.35	0.4	0.45	
L1			0.1	1
R	b(min)/2			
K	0.20			
Tolerances of Form and Position				
aaa	0.15			
bbb	0.10			
ccc	0.10			
REF:	JEDEC, MO-220, VARIATION VHHD-1			

Tape and Reel Specifications

Reel Dia	A0	B0	K0	D	E	F	W	P0	P2	P	t-max
178 (7”)	5.10±0.05	5.10±0.05	1.00±0.05	1.50±0.10	1.75±0.10	5.50±0.05	12.00±0.30	4.00±0.10	2.00±0.05	8.00±0.10	0.30



Life Support Policy

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