P89LPC952/954

8-bit microcontroller with accelerated two-clock 80C51 core 8 kB/16 kB 3 V byte-erasable flash with 10-bit ADC

Rev. 04 — 24 July 2008 Product data sheet

1. General description

The P89LPC952/954 is a single-chip microcontroller, available in low cost packages, based on a high performance processor architecture that executes instructions in two to four clocks, six times the rate of standard 80C51 devices. Many system-level functions have been incorporated into the P89LPC952/954 in order to reduce component count, board space, and system cost.

2. Features

2.1 Principal features

- 8 kB/16 kB byte-erasable flash code memory organized into 1 kB sectors and 64-byte pages. Single-byte erasing allows any byte(s) to be used as non-volatile data storage.
- 256-byte RAM data memory and a 256-byte auxiliary on-chip RAM.
- 8-input multiplexed 10-bit ADC with window comparator that can generate an interrupt for in or out of range results. Two analog comparators with selectable inputs and reference source.
- Two 16-bit counter/timers (each may be configured to toggle a port output upon timer overflow or to become a PWM output) and a 23-bit system timer that can also be used as a RTC.
- Two enhanced UARTs with a fractional baud rate generator, break detect, framing error detection, and automatic address detection; 400 kHz byte-wide I^2C-bus communication port and SPI communication port.
- High-accuracy internal RC oscillator option, with clock doubler option, allows operation without external oscillator components. The RC oscillator option is selectable and fine tunable. Fast switching between the internal RC oscillator and any oscillator source provides optimal support of minimal power active mode with fast switching to maximum performance.
- 2.4 V to 3.6 V V_{DD} operating range. I/O pins are 5 V tolerant (may be pulled up or driven to 5.5 V).
- 44-pin and 48-pin packages with 40 and 42 I/O pins minimum while using on-chip oscillator and reset options.
- Port 5 has high current sourcing/sinking (20 mA) for all Port 5 pins. All other port pins have high sinking capability (20 mA). A maximum limit is specified for the entire chip.
- Watchdog timer with separate on-chip oscillator, requiring no external components. The watchdog prescaler is selectable from eight values.

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2.2 Additional features

- A high performance 80C51 CPU provides instruction cycle times of 111 ns to 222 ns for all instructions except multiply and divide when executing at 18 MHz. This is six times the performance of the standard 80C51 running at the same clock frequency. A lower clock frequency for the same performance results in power savings and reduced EMI.
- Serial flash In-Circuit Programming (ICP) allows simple production coding with commercial EPROM programmers. Flash security bits prevent reading of sensitive application programs.
- Serial flash In-System Programming (ISP) allows coding while the device is mounted in the end application.
- In-Application Programming (IAP) of the flash code memory. This allows changing the code in a running application.
- Low voltage (brownout) detect allows a graceful system shutdown when power fails. May optionally be configured as an interrupt.
- Idle and two different power-down reduced power modes. Improved wake-up from Power-down mode (a LOW interrupt input starts execution). Typical power-down current is 1 μA (total power-down with voltage comparators disabled).
- On-chip power-on reset allows operation without external reset components. A software reset function is also available.
- Programmable external reset pin (P1.5) configuration options: open drain bidirectional reset input/output, reset input with pull-up, push-pull reset output, input-only port. A reset counter and reset glitch suppression circuitry prevent spurious and incomplete resets.
- Only power and ground connections are required to operate the P89LPC952/954 when internal reset option is selected.
- Configurable on-chip oscillator with frequency range options selected by user programmed flash configuration bits. Oscillator options support frequencies from 20 kHz to the maximum operating frequency of 18 MHz.
- Oscillator fail detect. The watchdog timer has a separate fully on-chip oscillator allowing it to perform an oscillator fail detect function.
- Programmable port output configuration options: quasi-bidirectional, open drain, push-pull, input-only.
- Port ‘input pattern match’ detect. Port 0 may generate an interrupt when the value of the pins match or do not match a programmable pattern.
- Controlled slew rate port outputs to reduce EMI. Outputs have approximately 10 ns minimum ramp times.
- Four interrupt priority levels.
- Eight keypad interrupt inputs, plus two additional external interrupt inputs.
- Schmitt trigger port inputs.
- Second data pointer.
- Extended temperature range.
- Emulation support.

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3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
P89LPC952FA	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2
P89LPC952FBD	LQFP44	plastic low profile quad flat package; 44 leads; body 10 × 10 × 1.4 mm	SOT389-1
P89LPC954FA	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2
P89LPC954FBD44	LQFP44	plastic low profile quad flat package; 44 leads; body 10 × 10 × 1.4 mm	SOT389-1
P89LPC954FBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

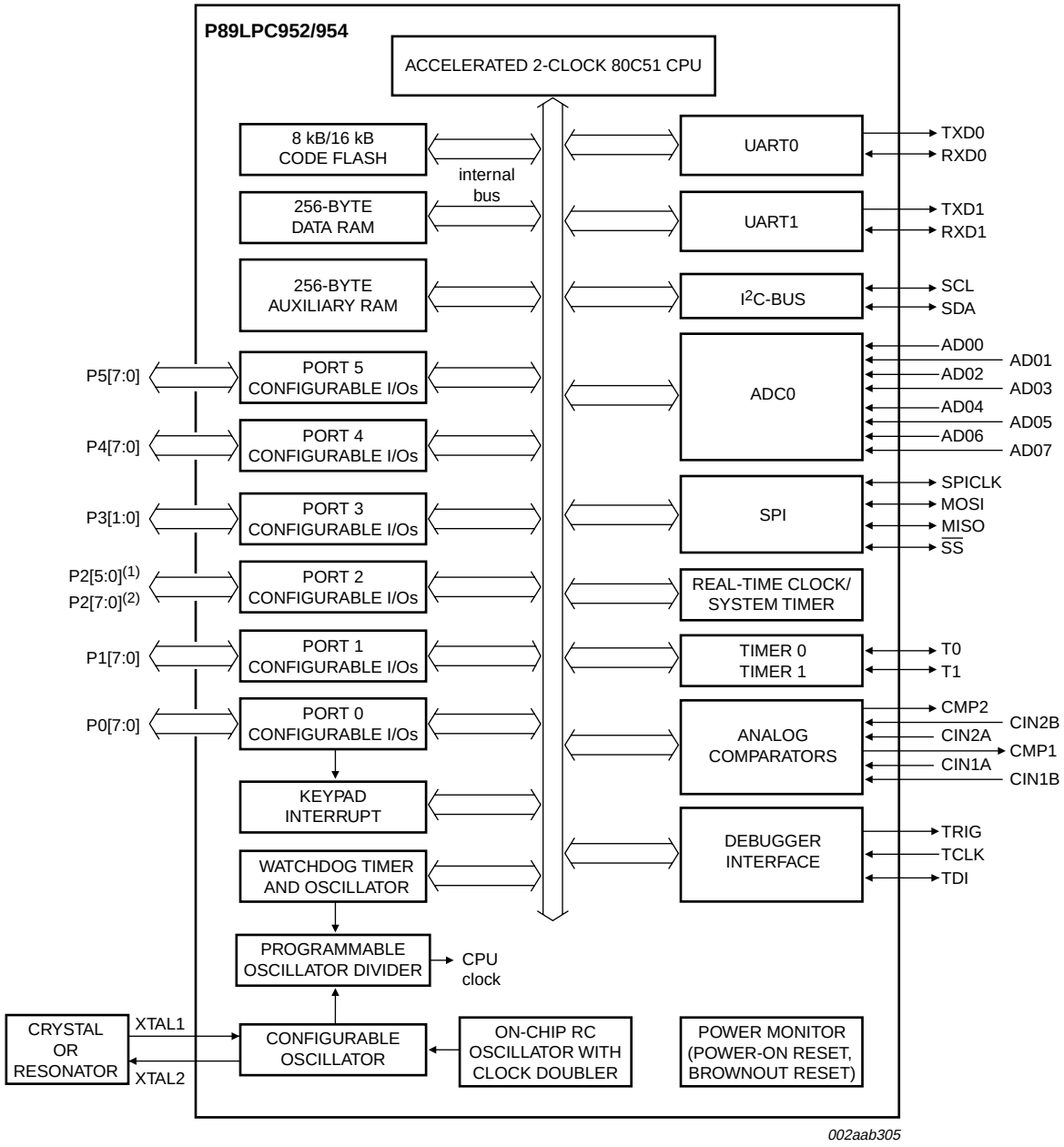
3.1 Ordering options

Table 2. Ordering options

Type number	Flash memory	Temperature range	Frequency
P89LPC952FA	8 kB	–40 °C to +85 °C	0 MHz to 18 MHz
P89LPC952FBD	8 kB	–40 °C to +85 °C	0 MHz to 18 MHz
P89LPC954FA	16 kB	–40 °C to +85 °C	0 MHz to 18 MHz
P89LPC954FBD44	16 kB	–40 °C to +85 °C	0 MHz to 18 MHz
P89LPC954FBD48	16 kB	–40 °C to +85 °C	0 MHz to 18 MHz

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4. Block diagram



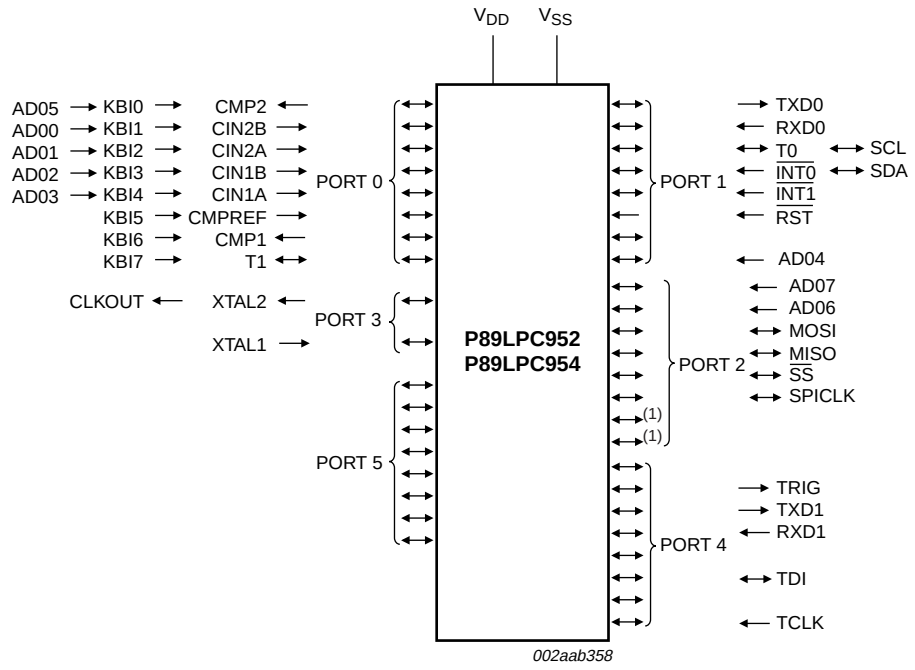
(1) 44-pin package.

(2) 48-pin package.

Fig 1. Block diagram

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5. Functional diagram



(1) 48-pin package.

Fig 2. Functional diagram

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6. Pinning information

6.1 Pinning

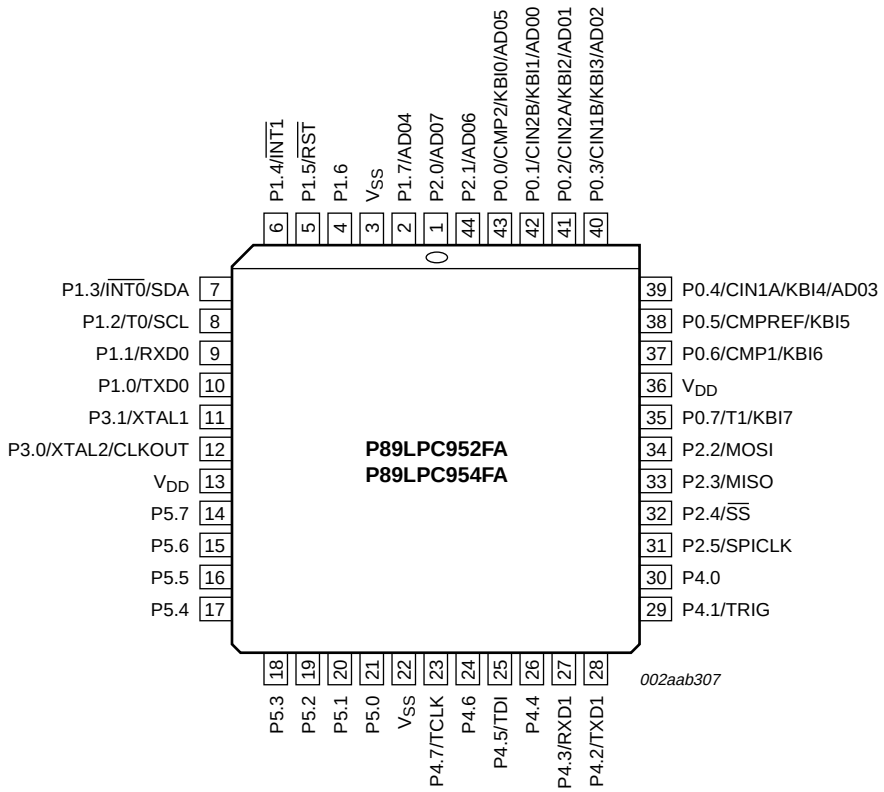


Fig 3. PLCC44 pin configuration

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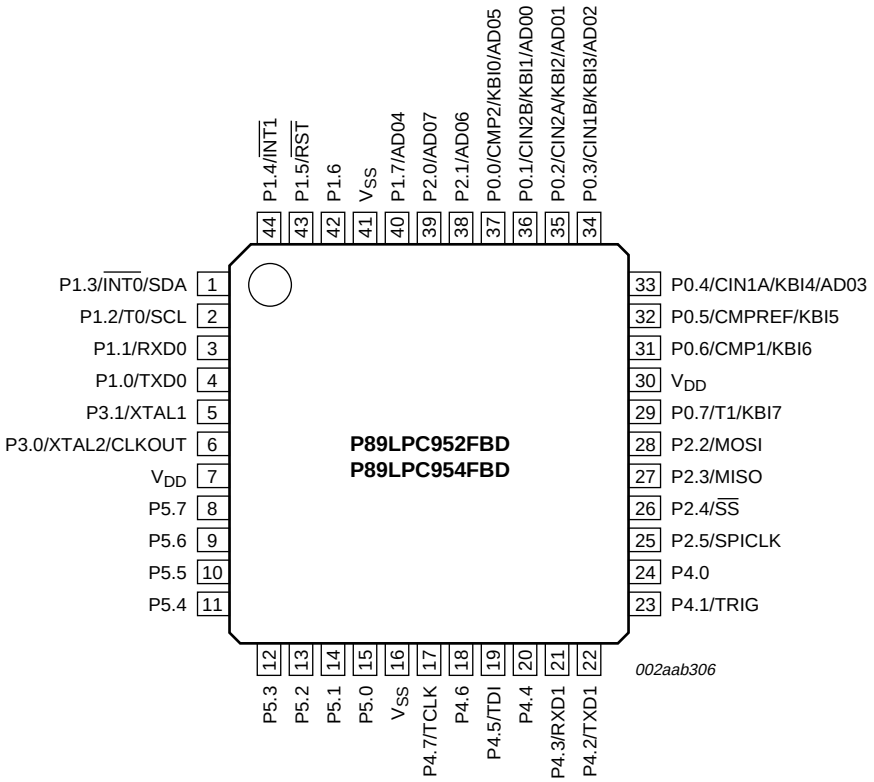


Fig 4. LQFP44 pin configuration

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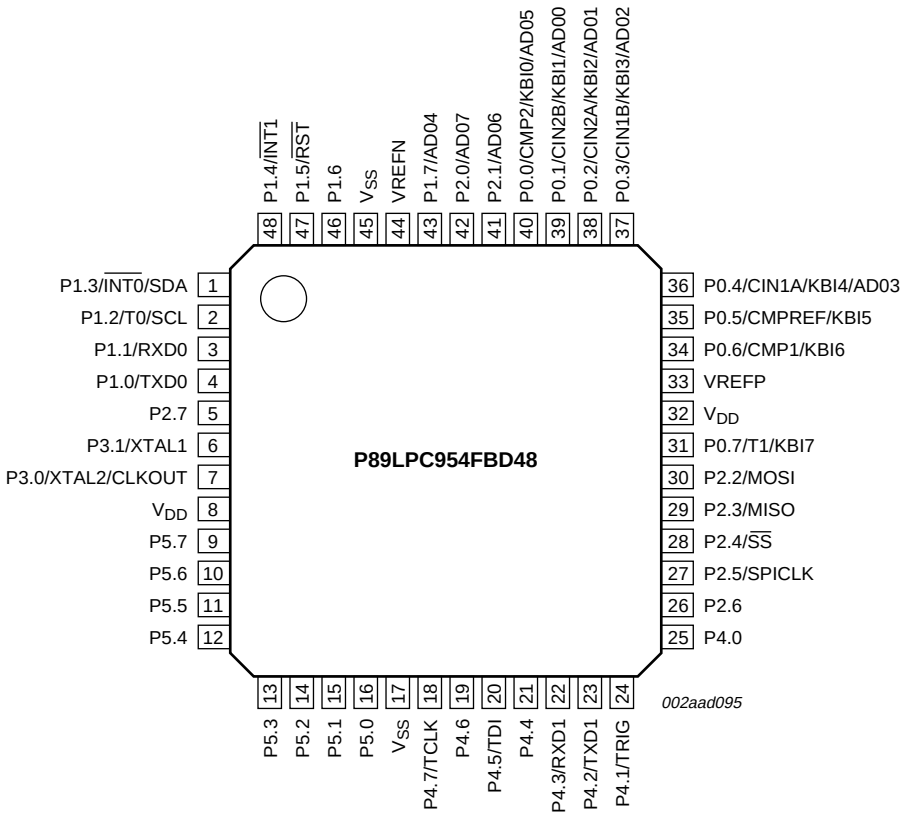


Fig 5. LQFP48 pin configuration

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6.2 Pin description

Table 3. Pin description

Symbol	Pin			Type	Description
	LQFP48	PLCC44	LQFP44		
P0.0 to P0.7				I/O	**Port 0:** Port 0 is an 8-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.13.1 “Port configurations” and Table 11 “Static characteristics” for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt triggered inputs. Port 0 also provides various special functions as described below:
P0.0/CMP2/ KBI0/AD05	40	43	37	I/O	**P0.0 —** Port 0 bit 0.
				O	**CMP2 —** Comparator 2 output.
				I	**KBI0 —** Keyboard input 0.
				I	**AD05 —** ADC0 channel 5 analog input.
P0.1/CIN2B/ KBI1/AD00	39	42	36	I/O	**P0.1 —** Port 0 bit 1.
				I	**CIN2B —** Comparator 2 positive input B.
				I	**KBI1 —** Keyboard input 1.
				I	**AD00 —** ADC0 channel 0 analog input.
P0.2/CIN2A/ KBI2/AD01	38	41	35	I/O	**P0.2 —** Port 0 bit 2.
				I	**CIN2A —** Comparator 2 positive input A.
				I	**KBI2 —** Keyboard input 2.
				I	**AD01 —** ADC0 channel 1 analog input.
P0.3/CIN1B/ KBI3/AD02	37	40	34	I/O	**P0.3 —** Port 0 bit 3.
				I	**CIN1B —** Comparator 1 positive input B.
				I	**KBI3 —** Keyboard input 3.
				I	**AD02 —** ADC0 channel 2 analog input.
P0.4/CIN1A/ KBI4/AD03	36	39	33	I/O	**P0.4 —** Port 0 bit 4.
				I	**CIN1A —** Comparator 1 positive input A.
				I	**KBI4 —** Keyboard input 4.
				I	**AD03 —** ADC0 channel 3 analog input.
P0.5/CMPREF/ KBI5	35	38	32	I/O	**P0.5 —** Port 0 bit 5.
				I	**CMPREF —** Comparator reference (negative) input.
				I	**KBI5 —** Keyboard input 5.

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Table 3. Pin description *...continued*

Symbol	Pin			Type	Description
	LQFP48	PLCC44	LQFP44		
P0.6/CMP1/KBI6	34	37	31	I/O	**P0.6 —** Port 0 bit 6.
				O	**CMP1 —** Comparator 1 output.
				I	**KBI6 —** Keyboard input 6.
P0.7/T1/KBI7	31	35	29	I/O	**P0.7 —** Port 0 bit 7.
				I/O	**T1 —** Timer/counter 1 external count input or overflow output.
				I	**KBI7 —** Keyboard input 7.
P1.0 to P1.7				I/O, I [1]	**Port 1:** Port 1 is an 8-bit I/O port with a user-configurable output type, except for three pins as noted below. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 7.13.1 "Port configurations" and Table 11 "Static characteristics" for details. P1.2 to P1.3 are open drain when used as outputs. P1.5 is input only. All pins have Schmitt triggered inputs. Port 1 also provides various special functions as described below:
P1.0/TXD0	4	10	4	I/O	**P1.0 —** Port 1 bit 0.
				O	**TXD0 —** Transmitter output for serial port 0.
P1.1/RXD0	3	9	3	I/O	**P1.1 —** Port 1 bit 1.
				I	**RXD0 —** Receiver input for serial port 0.
P1.2/T0/SCL	2	8	2	I/O	**P1.2 —** Port 1 bit 2 (open-drain when used as output).
				I/O	**T0 —** Timer/counter 0 external count input or overflow output (open-drain when used as output).
				I/O	**SCL —** I^2C-bus serial clock input/output.
P1.3/$\overline{INT0}$/SDA	1	7	1	I/O	**P1.3 —** Port 1 bit 3 (open-drain when used as output).
				I	**$\overline{INT0}$ —** External interrupt 0 input.
				I/O	**SDA —** I^2C-bus serial data input/output.
P1.4/$\overline{INT1}$	48	6	44	I/O	**P1.4 —** Port 1 bit 4.
				I	**$\overline{INT1}$ —** External interrupt 1 input.

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Table 3. Pin description *...continued*

Symbol	Pin			Type	Description
	LQFP48	PLCC44	LQFP44		
P1.5/$\overline{\text{RST}}$	47	5	43	I	**P1.5 —** Port 1 bit 5 (input only).
				I	**$\overline{\text{RST}}$ —** External Reset input during power-on or maybe a reset input/output if selected via UCFG1 and UCFG2. When functioning as a reset input or input/output, a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. When functioning as a reset output or input/output an internal reset source will drive this pin LOW. Also used during a power-on sequence to force ISP mode. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.**
P1.6	46	4	42	I/O	**P1.6 —** Port 1 bit 6.
P1.7/AD04	43	2	40	I/O	**P1.7 —** Port 1 bit 7.
				I	**AD04 —** ADC0 channel 4 analog input.
P2.0 to P2.5				I/O	**Port 2:** Port 2 is an 8-bit I/O port with a user-configurable output type. During reset Port 2 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 2 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.13.1 “Port configurations” and Table 11 “Static characteristics” for details. All pins have Schmitt triggered inputs. Port 2 also provides various special functions as described below:
P2.0/AD07	42	1	39	I/O	**P2.0 —** Port 2 bit 0.
				I	**AD07 —** ADC0 channel 7 analog input.
P2.1/AD06	41	44	38	I/O	**P2.1 —** Port 2 bit 1.
				I	**AD06 —** ADC0 channel 6 analog input.
P2.2/MOSI	30	34	28	I/O	**P2.2 —** Port 2 bit 2.
				I/O	**MOSI —** SPI master out slave in. When configured as master, this pin is output; when configured as slave, this pin is input.
P2.3/MISO	29	33	27	I/O	**P2.3 —** Port 2 bit 3.
				I/O	**MISO —** When configured as master, this pin is input, when configured as slave, this pin is output.
P2.4/$\overline{\text{SS}}$	28	32	26	I/O	**P2.4 —** Port 2 bit 4.
				I/O	**$\overline{\text{SS}}$ —** SPI Slave select.

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Table 3. Pin description *...continued*

Symbol	Pin			Type	Description
	LQFP48	PLCC44	LQFP44		
P2.5/SPICLK	27	31	25	I/O	**P2.5 —** Port 2 bit 5.
				I/O	**SPICLK —** SPI clock. When configured as master, this pin is output; when configured as slave, this pin is input.
P2.6	26	-	-	I/O	**P2.6 —** Port 2 bit 6.
P2.7	5	-	-	I/O	**P2.7 —** Port 2 bit 7.
P3.0 to P3.1				I/O	**Port 3:** Port 3 is a 2-bit I/O port with a user-configurable output type. During reset Port 3 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 3 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.13.1 “Port configurations” and Table 11 “Static characteristics” for details. All pins have Schmitt triggered inputs. Port 3 also provides various special functions as described below:
P3.0/XTAL2/ CLKOUT	7	12	6	I/O	**P3.0 —** Port 3 bit 0.
				O	**XTAL2 —** Output from the oscillator amplifier (when a crystal oscillator option is selected via the flash configuration.
				O	**CLKOUT —** CPU clock divided by 2 when enabled via SFR bit (ENCLK -TRIM.6). It can be used if the CPU clock is the internal RC oscillator, watchdog oscillator or external clock input, except when XTAL1/XTAL2 are used to generate clock source for the RTC/system timer.
P3.1/XTAL1	6	11	5	I/O	**P3.1 —** Port 3 bit 1.
				I	**XTAL1 —** Input to the oscillator circuit and internal clock generator circuits (when selected via the flash configuration). It can be a port pin if internal RC oscillator or watchdog oscillator is used as the CPU clock source, **and** if XTAL1/XTAL2 are not used to generate the clock for the RTC/system timer.
P4.0 to P4.7				I/O	**Port 4:** Port 4 is an 8-bit I/O port with a user-configurable output type. During reset Port 4 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 4 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.13.1 “Port configurations” and Table 11 “Static characteristics” for details. All pins have Schmitt triggered inputs. Port 4 also provides various special functions as described below:
P4.0	25	30	24	I/O	**P4.0 —** Port 4 bit 0.
P4.1/TRIG	24	29	23	I/O	**P4.1 —** Port 4 bit 1.
				O	**TRIG —** Debugger trigger output.
P4.2/TXD1	23	28	22	I/O	**P4.2 —** Port 4 bit 2.
				O	**TXD1 —** Transmitter output for serial port 1.
P4.3/RXD1	22	27	21	I/O	**P4.3 —** Port 4 bit 3.
				I	**RXD1 —** Receiver input for serial port 1.

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Table 3. Pin description *...continued*

Symbol	Pin			Type	Description
	LQFP48	PLCC44	LQFP44		
P4.4	21	26	20	I/O	**P4.4 —** Port 4 bit 4.
P4.5/TDI	20	25	19	I/O	**P4.5 —** Port 4 bit 5.
				I/O	**TDI —** Serial data input/output for debugger interface.
P4.6	19	24	18	I/O	**P4.6 —** Port 4 bit 6.
P4.7/TCLK	18	23	17	I/O	**P4.7 —** Port 4 bit 7.
				I	**TCLK —** Serial clock input for debugger interface.
P5.0 to P5.7				I/O	**Port 5:** Port 5 is an 8-bit I/O port with a user-configurable output type. During reset Port 5 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 5 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.13.1 “Port configurations” and Table 11 “Static characteristics” for details. All pins have Schmitt triggered inputs. Port 5 also provides various special functions as described below:
P5.0	16	21	15	I/O	**P5.0 —** Port 5 bit 0. High current source.
P5.1	15	20	14	I/O	**P5.1 —** Port 5 bit 1. High current source.
P5.2	14	19	13	I/O	**P5.2 —** Port 5 bit 2. High current source.
P5.3	13	18	12	I/O	**P5.3 —** Port 5 bit 3. High current source.
P5.4	12	17	11	I/O	**P5.4 —** Port 5 bit 4. High current source.
P5.5	11	16	10	I/O	**P5.5 —** Port 5 bit 5. High current source.
P5.6	10	15	9	I/O	**P5.6 —** Port 5 bit 6. High current source.
P5.7	9	14	8	I/O	**P5.7 —** Port 5 bit 7. High current source.
V_{SS}	17, 45	3, 22	16, 41	I	**Ground:** 0 V reference.
VREFN	44	-	-		negative ADC reference voltage
V_{DD}	8, 32	13, 36	7, 30	I	**Power supply:** This is the power supply voltage for normal operation as well as Idle and Power-down modes.
VREFP	33	-	-		positive ADC reference voltage

[1] Input/output for P1.0 to P1.4, P1.6, P1.7. Input for P1.5.

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7. Functional description

Remark: Please refer to the P89LPC952/954 *User's Manual* for a more detailed functional description.

7.1 Special function registers

Remark: SFR accesses are restricted in the following ways:

- User must **not** attempt to access any SFR locations not defined.
- Accesses to any defined SFR locations must be strictly for the functions for the SFRs.
- SFR bits labeled '-', '0' or '1' can **only** be written and read as follows:
  - '-' Unless otherwise specified, **must** be written with '0', but can return any value when read (even if it was written with '0'). It is a reserved bit and may be used in future derivatives.
  - '0' **must** be written with '0', and will return a '0' when read.
  - '1' **must** be written with '1', and will return a '1' when read.

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Table 4. Special function registers

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
	Bit address		E7	E6	E5	E4	E3	E2	E1	E0		
ACC[1]	Accumulator	E0H									00	0000 0000
AD0CON	ADC0 control register	97H	ENBI0	ENADCI0	TMM0	EDGE0	ADCI0	ENADC0	ADCS01	ADCS00	00	0000 0000
AD0INS	ADC0 input select	A3H	ADI07	ADI06	ADI05	ADI04	ADI03	ADI02	ADI01	ADI00	00	0000 0000
AD0MODA	ADC0 mode register A	C0H	BNDI0	BURST0	SCC0	SCAN0	-	-	-	-	00	0000 0000
AD0MODB	ADC0 mode register B	A1H	CLK2	CLK1	CLK0	-	-	-	-	-	00	000x 0000
AUXR1	Auxiliary function register	A2H	CLKLP	EBRR	ENT1	ENT0	SRST	0	-	DPS	00	0000 00x0
	Bit address		F7	F6	F5	F4	F3	F2	F1	F0		
B[1]	B register	F0H									00	0000 0000
BRGR0_0	Baud rate generator 0 rate low	BEH									00	0000 0000
BRGR1_0	Baud rate generator 0 rate high	BFH									00	0000 0000
BRGCON_0	Baud rate generator 0 control	BDH	-	-	-	-	-	-	SBRGS_0	BRGEN_0	00[3]	xxxx xx00
CMP1	Comparator 1 control register	ACH	-	-	CE1	CP1	CN1	OE1	CO1	CMF1	00[2]	xx00 0000
CMP2	Comparator 2 control register	ADH	-	-	CE2	CP2	CN2	OE2	CO2	CMF2	00[2]	xx00 0000
DIVM	CPU clock divide-by-M control	95H									00	0000 0000
DPTR	Data pointer (2 bytes)											

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Table 4. Special function registers *…continued*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
DPH	Data pointer high	83H									00	0000 0000
DPL	Data pointer low	82H									00	0000 0000
FMADRH	Program flash address high	E7H									00	0000 0000
FMADRL	Program flash address low	E6H									00	0000 0000
FMCON	Program flash control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV	OI	70	0111 0000
	Program flash control (Write)	E4H	FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1	FMCMD.0		
FMDATA	Program flash data	E5H									00	0000 0000
I2ADR	I^2C-bus slave address register	DBH	I2ADR.6	I2ADR.5	I2ADR.4	I2ADR.3	I2ADR.2	I2ADR.1	I2ADR.0	GC	00	0000 0000
	Bit address		**DF**	**DE**	**DD**	**DC**	**DB**	**DA**	**D9**	**D8**		
I2CON[1]	I^2C-bus control register	D8H	-	I2EN	STA	STO	SI	AA	-	CRSEL	00	x000 00x0
I2DAT	I^2C-bus data register	DAH										
I2SCLH	Serial clock generator/SCL duty cycle register high	DDH									00	0000 0000
I2SCLL	Serial clock generator/SCL duty cycle register low	DCH									00	0000 0000
I2STAT	I^2C-bus status register	D9H	STA.4	STA.3	STA.2	STA.1	STA.0	0	0	0	F8	1111 1000

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Table 4. Special function registers *…continued*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
		Bit address	**AF**	**AE**	**AD**	**AC**	**AB**	**AA**	**A9**	**A8**		
IEN0[1]	Interrupt enable 0	A8H	EA	EWDRT	EBO	ES/ESR	ET1	EX1	ET0	EX0	00	0000 0000
		Bit address	**EF**	**EE**	**ED**	**EC**	**EB**	**EA**	**E9**	**E8**		
IEN1[1]	Interrupt enable 1	E8H	-	EST	-	-	ESPI	EC	EKBI	EI2C	00[2]	00x0 0000
IEN2	Interrupt enable 2	D5H	-	-	-	-	EST1	ES1/ESR1	EADC	-	00[2]	00x0 0000
		Bit address	**BF**	**BE**	**BD**	**BC**	**BB**	**BA**	**B9**	**B8**		
IP0[1]	Interrupt priority 0	B8H	-	PWDRT	PBO	PS/PSR	PT1	PX1	PT0	PX0	00[2]	x000 0000
IP0H	Interrupt priority 0 high	B7H	-	PWDRTH	PBOH	PSH/ PSRH	PT1H	PX1H	PT0H	PX0H	00[2]	x000 0000
		Bit address	**FF**	**FE**	**FD**	**FC**	**FB**	**FA**	**F9**	**F8**		
IP1[1]	Interrupt priority 1	F8H	-	PST	-	-	PSPI	PC	PKBI	PI2C	00[2]	00x0 0000
IP1H	Interrupt priority 1 high	F7H	-	PSTH	-	-	PSPIH	PCH	PKBIH	PI2CH	00[2]	00x0 0000
IP2	Interrupt priority 2	D6H	-	-	-	-	PEST1	PES1/ PESR1	PADC	-	00[2]	00x0 0000
IP2H	Interrupt priority 2 high	D7H	-	-	-	-	PEST1H	PES1H/ PESR1H	PADCH	-	00[2]	00x0 0000
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN _SEL	KBIF	00[2]	xxxx xx00
KBMASK	Keypad interrupt mask register	86H									00	0000 0000
KBPATN	Keypad pattern register	93H									FF	1111 1111
		Bit address	**87**	**86**	**85**	**84**	**83**	**82**	**81**	**80**		
P0[1]	Port 0	80H	T1/KB7	CMP1 /KB6	CMPREF /KB5	CIN1A /KB4	CIN1B /KB3	CIN2A /KB2	CIN2B /KB1	CMP2 /KB0	[2]	
		Bit address	**97**	**96**	**95**	**94**	**93**	**92**	**91**	**90**		
P1[1]	Port 1	90H	-	-	$\overline{\text{RST}}$	$\overline{\text{INT1}}$	$\overline{\text{INT0}}$/SDA	T0/SCL	RXD0	TXD0	[2]	

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Table 4. Special function registers *...continued*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
		Bit address	97	96	95	94	93	92	91	90		
P2[1]	Port 2	A0H	-	-	SPICLK	$\overline{SS}$	MISO	MOSI	-	-	[2]	
		Bit address	B7	B6	B5	B4	B3	B2	B1	B0		
P3[1]	Port 3	B0H	-	-	-	-	-	-	XTAL1	XTAL2	[2]	
P4	Port 4	B3H	-	TMS	-	-	RXD1	TXD1	TRIG	T3EX	[2]	
P5	Port 5	B4H	T3	-	-	-	-	-	-	-	[2]	
P0M1	Port 0 output mode 1	84H	(P0M1.7)	(P0M1.6)	(P0M1.5)	(P0M1.4)	(P0M1.3)	(P0M1.2)	(P0M1.1)	(P0M1.0)	FF[2]	1111 1111
P0M2	Port 0 output mode 2	85H	(P0M2.7)	(P0M2.6)	(P0M2.5)	(P0M2.4)	(P0M2.3)	(P0M2.2)	(P0M2.1)	(P0M2.0)	00[2]	0000 0000
P1M1	Port 1 output mode 1	91H	(P1M1.7)	(P1M1.6)	-	(P1M1.4)	(P1M1.3)	(P1M1.2)	(P1M1.1)	(P1M1.0)	D3[2]	11x1 xx11
P1M2	Port 1 output mode 2	92H	(P1M2.7)	(P1M2.6)	-	(P1M2.4)	(P1M2.3)	(P1M2.2)	(P1M2.1)	(P1M2.0)	00[2]	00x0 xx00
P2M1	Port 2 output mode 1	A4H	(P2M1.7)	(P2M1.6)	(P2M1.5)	(P2M1.4)	(P2M1.3)	(P2M1.2)	(P2M1.1)	(P2M1.0)	FF[2]	1111 1111
P2M2	Port 2 output mode 2	A5H	(P2M2.7)	(P2M2.6)	(P2M2.5)	(P2M2.4)	(P2M2.3)	(P2M2.2)	(P2M2.1)	(P2M2.0)	00[2]	0000 0000
P3M1	Port 3 output mode 1	B1H	-	-	-	-	-	-	(P3M1.1)	(P3M1.0)	03[2]	xxxx xx11
P3M2	Port 3 output mode 2	B2H	-	-	-	-	-	-	(P3M2.1)	(P3M2.0)	00[2]	xxxx xx00
PCON	Power control register	87H	SMOD1	SMOD0	BOPD	BOI	GF1	GF0	PMOD1	PMOD0	00	0000 0000
PCONA	Power control register A	B5H	RTCPD	-	VCPD	ADPD	I2PD	SPPD	SPD	-	00[2]	0000 0000
		Bit address	D7	D6	D5	D4	D3	D2	D1	D0		
PSW[1]	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00	0000 0000
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	PT0AD.3	PT0AD.2	PT0AD.1	-	00	xx00 000x
RSTSRC	Reset source register	DFH	-	-	BOF	POF	R_BK	R_WD	R_SF	R_EX	[4]	

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Table 4. Special function registers *...continued*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
RTCCON	RTC control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60[2][7]	011x xx00
RTCH	RTC register high	D2H									00[7]	0000 0000
RTCL	RTC register low	D3H									00[7]	0000 0000
S0ADDR	Serial port address register	A9H									00	0000 0000
S0ADEN	Serial port address enable	B9H									00	0000 0000
S0BUF	Serial Port data buffer register	99H									xx	xxxx xxxx
	Bit address		**9F**	**9E**	**9D**	**9C**	**9B**	**9A**	**99**	**98**		
S0CON[1]	Serial port control	98H	SM0_0/FE_0	SM1_00	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	00	0000 0000
S0STAT	Serial port extended status register	BAH	DBMOD_0	INTLO_0	CIDIS_0	DBISEL_0	FE_0	BR_0	OE_0	STINT_0	00	0000 0000
SP	Stack pointer	81H									07	0000 0111
SPCTL	SPI control register	E2H	SSIG	SPEN	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	04	0000 0100
SPSTAT	SPI status register	E1H	SPIF	WCOL	-	-	-	-	-	-	00	00xx xxxx
SPDAT	SPI data register	E3H									00	0000 0000
S1CON	Serial port 1 control	B6H	SM0_1/FE_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1	00	0000 0000
S1STAT	Serial port 1 extended status register	D4H	DBMOD_1	INTLO_1	CIDIS_1	DBISEL_1	FE_1	BR_1	OE_1	STINT_1	00	0000 0000
TAMOD	Timer 0 and 1 auxiliary mode	8FH	-	-	-	T1M2	-	-	-	T0M2	00	xxx0 xxx0

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Table 4. Special function registers *…continued*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
	Bit address		8F	8E	8D	8C	8B	8A	89	88		
TCON[1]	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00	0000 0000
TH0	Timer 0 high	8CH									00	0000 0000
TH1	Timer 1 high	8DH									00	0000 0000
TL0	Timer 0 low	8AH									00	0000 0000
TL1	Timer 1 low	8BH									00	0000 0000
TMOD	Timer 0 and 1 mode	89H	T1GATE	T1C/T	T1M1	T1M0	T0GATE	T0C/T	T0M1	T0M0	00	0000 0000
TRIM	Internal oscillator trim register	96H	RCCLK	ENCLK	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1	TRIM.0	[6] [7]	
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF	WDCLK	[5] [7]	
WDL	Watchdog load	C1H									FF	1111 1111
WFEED1	Watchdog feed 1	C2H										
WFEED2	Watchdog feed 2	C3H										

[1] Indicates SFRs that are bit addressable.

[2] All ports are in input only (high-impedance) state after power-up.

[3] BRGR1_0 and BRGR0_0 must only be written if BRGEN_0 in BRGCON_0 SFR is logic 0. If any are written while BRGEN_0 = 1, the result is unpredictable.

[4] The RSTSRC register reflects the cause of the P89LPC952/954 reset. Upon a power-up reset, all reset source flags are cleared except POF and BOF; the power-on reset value is xx11 0000.

[5] After reset, the value is 1110 01x1, i.e., PRE2 to PRE0 are all logic 1, WDRUN = 1 and WDCLK = 1. WDTOF bit is logic 1 after watchdog reset and is logic 0 after power-on reset. Other resets will not affect WDTOF.

[6] On power-on reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.

[7] The only reset source that affects these SFRs is power-on reset.

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Table 5. Extended special function registers

Name	Description	SFR addr.	Bit functions and addresses		Reset value	
			MSB	LSB	Hex	Binary
ADC0HBND	ADC0 high_boundary register, left (MSB)	FFEFH			FF	1111 1111
ADC0LBND	ADC0 low_boundary register (MSB)	FFEEH			00	0000 0000
AD0DAT0R	ADC0 data register 0, right (LSB)	FFFEH	AD0DAT0[7:0]		00	0000 0000
AD0DAT0L	ADC0 data register 0, left (MSB)	FFFFH	AD0DAT0[9:2]		00	0000 0000
AD0DAT1R	ADC0 data register 1, right (LSB)	FFFCH	AD0DAT1[7:0]		00	0000 0000
AD0DAT1L	ADC0 data register 1, left (MSB)	FFFDH	AD0DAT1[9:2]		00	0000 0000
AD0DAT2R	ADC0 data register 2, right (LSB)	FFFAH	AD0DAT2[7:0]		00	0000 0000
AD0DAT2L	ADC0 data register 2, left (MSB)	FFFBH	AD0DAT2[9:2]		00	0000 0000
AD0DAT3R	ADC0 data register 3, right (LSB)	FFF8H	AD0DAT3[7:0]		00	0000 0000
AD0DAT3L	ADC0 data register 3, left (MSB)	FFF9H	AD0DAT3[9:2]		00	0000 0000
AD0DAT4R	ADC0 data register 4, right (LSB)	FFF6H	AD0DAT4[7:0]		00	0000 0000
AD0DAT4L	ADC0 data register 4, left (MSB)	FFF7H	AD0DAT4[9:2]		00	0000 0000
AD0DAT5R	ADC0 data register 5, right (LSB)	FFF4H	AD0DAT5[7:0]		00	0000 0000
AD0DAT5L	ADC0 data register 5, left (MSB)	FFF5H	AD0DAT5[9:2]		00	0000 0000
AD0DAT6R	ADC0 data register 6, right (LSB)	FFF2H	AD0DAT6[7:0]		00	0000 0000
AD0DAT6L	ADC0 data register 6, left (MSB)	FFF3H	AD0DAT6[9:2]		00	0000 0000
AD0DAT7R	ADC0 data register 7, right (LSB)	FFF0H	AD0DAT7[7:0]			

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Table 5. Extended special function registers *…continued*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
AD0DAT7L	ADC0 data register 7, left (MSB)	FFF1H	AD0DAT7[9:2]									
BNDSTA0	ADC0 boundary status register	FFEDH										
BRGCON_1	Baud rate generator 1 control	FFB3H	-	-	-	-	-	-	SBRGS_1	BRGEN_1	00[2]	xxxx xx00
BRG0_1	Baud rate generator 1 rate low	FFB4H										
BRG1_1	Baud rate generator 1 rate high	FFB5H										
FREEZE	Peripheral clock freeze	FFD0H	-	-	-	RTC_F	CCU_F	WDT_F	T1_F	T0_F	00	xxx0 0000
P4M1	Port 4 output mode 1	FFB8H	(P4M1.7)	(P4M1.6)	(P4M1.5)	(P4M1.4)	(P4M1.3)	(P4M1.2)	(P4M1.1)	(P4M1.0)	FF[1]	1111 1111
P4M2	Port 4 output mode 2	FFB9H	(P4M2.7)	(P4M2.6)	(P4M2.5)	(P4M2.4)	(P4M2.3)	(P4M2.2)	(P4M2.1)	(P4M2.0)	00[1]	0000 0000
P5M1	Port 5 output mode 1	FFBAH	(P5M1.7)	(P5M1.6)	(P5M1.5)	(P5M1.4)	(P5M1.3)	(P5M1.2)	(P5M1.1)	(P5M1.0)	FF[1]	1111 1111
P5M2	Port 5 output mode 3	FFBBH	(P5M2.7)	(P5M2.6)	(P5M2.5)	(P5M2.4)	(P5M2.3)	(P5M2.2)	(P5M2.1)	(P5M2.0)	00[1]	0000 0000
S1ADDR	Serial port 1 address register	FFB2H									00	0000 0000
S1ADEN	Serial port 1 address enable	FFB1H									00	0000 0000
S1BUF	Serial port 1 data buffer register	FFB0H									xx	xxxx xxxx

[1] Extended SFRs are physically located on-chip but logically located in external data memory address space (XDATA). The MOVX A,@DPTR and MOVX @DPTR,A instructions are used to access these extended SFRs.

[2] BRGR1_1 and BRGR0_1 must only be written if BRGEN_1 in BRGCON_1 SFR is logic 0. If any are written while BRGEN_1 = 1, the result is unpredictable.

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7.2 Enhanced CPU

The P89LPC952/954 uses an enhanced 80C51 CPU which runs at six times the speed of standard 80C51 devices. A machine cycle consists of two CPU clock cycles, and most instructions execute in one or two machine cycles.

7.3 Clocks

7.3.1 Clock definitions

The P89LPC952/954 device has several internal clocks as defined below:

OSCCLK — Input to the DIVM clock divider. OSCCLK is selected from one of four clock sources (see Figure 6) and can also be optionally divided to a slower frequency (see Section 7.8 “CCLK modification: DIVM register”).

Note: f_{osc} is defined as the OSCCLK frequency.

CCLK — CPU clock; output of the clock divider. There are two CCLK cycles per machine cycle, and most instructions are executed in one to two machine cycles (two or four CCLK cycles).

RCCLK — The internal 7.373 MHz RC oscillator output. The clock doubler option, when enabled, provides an output frequency of 14.746 MHz.

PCLK — Clock for the various peripheral devices and is $^{CCLK}/_{2}$.

7.3.2 CPU clock (OSCCLK)

The P89LPC952/954 provides several user-selectable oscillator options in generating the CPU clock. This allows optimization for a range of needs from high precision to lowest possible cost. These options are configured when the flash is programmed and include an on-chip watchdog oscillator, an on-chip RC oscillator, an oscillator using an external crystal, or an external clock source. The crystal oscillator can be optimized for low, medium, or high frequency crystals covering a range from 20 kHz to 18 MHz.

7.3.3 Low speed oscillator option

This option supports an external crystal in the range of 20 kHz to 100 kHz. Ceramic resonators are also supported in this configuration.

7.3.4 Medium speed oscillator option

This option supports an external crystal in the range of 100 kHz to 4 MHz. Ceramic resonators are also supported in this configuration.

7.3.5 High speed oscillator option

This option supports an external crystal in the range of 4 MHz to 18 MHz. Ceramic resonators are also supported in this configuration. **When using a clock frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using a clock frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device**

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in reset when V_{DD} falls below the minimum specified operating voltage. These requirements for clock frequencies above 12 MHz do not apply when using the internal RC oscillator in clock doubler mode.

7.3.6 Clock output

The P89LPC952/954 supports a user-selectable clock output function on the XTAL2/CLKOUT pin when crystal oscillator is not being used. This condition occurs if another clock source has been selected (on-chip RC oscillator, watchdog oscillator, external clock input on XTAL1) and if the RTC is not using the crystal oscillator as its clock source. This allows external devices to synchronize to the P89LPC952/954. This output is enabled by the ENCLK bit in the TRIM register.

The frequency of this clock output is $\frac{1}{2}$ that of the CCLK. If the clock output is not needed in Idle mode, it may be turned off prior to entering Idle, saving additional power.

7.4 On-chip RC oscillator option

The P89LPC952/954 has a 6-bit TRIM register that can be used to tune the frequency of the RC oscillator. During reset, the TRIM value is initialized to a factory pre-programmed value to adjust the oscillator frequency to 7.373 MHz ± 1 % at room temperature. End-user applications can write to the TRIM register to adjust the on-chip RC oscillator to other frequencies. When the clock doubler option is enabled (UCFG1.3 = 1), the output frequency is 14.746 MHz. If CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to logic 1 to reduce power consumption. On reset, CLKLP is logic 0 allowing highest performance access. This bit can then be set in software if CCLK is running at 8 MHz or slower.

The requirements in Section 7.3.5 “High speed oscillator option” for configuring P1.5 as an external reset input and using an external reset circuit when the clock frequency is greater than 12 MHz do **not** apply when using the internal RC oscillator’s clock doubler option.

7.5 Watchdog oscillator option

The watchdog has a separate oscillator which has a frequency of 400 kHz. This oscillator can be used to save power when a high clock frequency is not needed.

7.6 External clock input option

In this configuration, the processor clock is derived from an external source driving the P3.1/XTAL1 pin. The rate may be from 0 Hz up to 18 MHz. The P3.0/XTAL2 pin may be used as a standard port pin or a clock output.

When using an external clock input frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an external clock input frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage. These requirements for clock frequencies above 12 MHz do not apply when using the internal RC oscillator in clock doubler mode.

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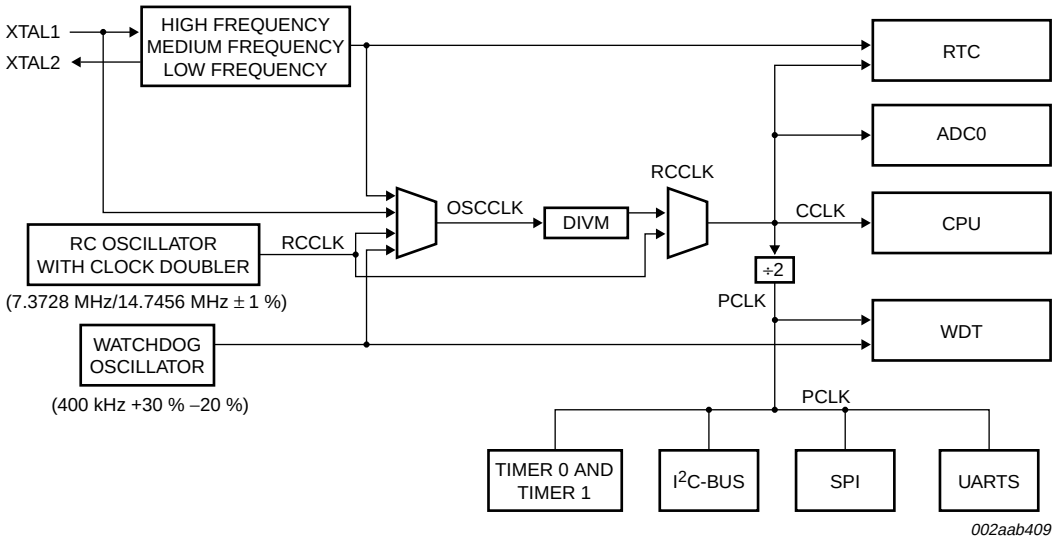


Fig 6. Block diagram of oscillator control

7.7 CCLK wake-up delay

The P89LPC952/954 has an internal wake-up timer that delays the clock until it stabilizes depending on the clock source used. If the clock source is any of the three crystal selections (low, medium and high frequencies) the delay is 992 OSCCLK cycles plus 60 μs to 100 μs. If the clock source is either the internal RC oscillator, watchdog oscillator, or external clock, the delay is 224 OSCCLK cycles plus 60 μs to 100 μs.

7.8 CCLK modification: DIVM register

The OSCCLK frequency can be divided down up to 510 times by configuring a dividing register, DIVM, to generate CCLK. This feature makes it possible to temporarily run the CPU at a lower rate, reducing power consumption. By dividing the clock, the CPU can retain the ability to respond to events that would not exit Idle mode by executing its normal program at a lower rate. This can also allow bypassing the oscillator start-up time in cases where Power-down mode would otherwise be used. The value of DIVM may be changed by the program at any time without interrupting code execution.

7.9 Low power select

The P89LPC952/954 is designed to run at 18 MHz (CCLK) maximum. However, if CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to ‘1’ to lower the power consumption further. On any reset, CLKLP is ‘0’ allowing highest performance access. This bit can then be set in software if CCLK is running at 8 MHz or slower.

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7.10 Memory organization

The various P89LPC952/954 memory spaces are as follows:

- DATA

  128 bytes of internal data memory space (00H:7FH) accessed via direct or indirect addressing, using instructions other than MOVX and MOVC. All or part of the Stack may be in this area.

- IDATA

  Indirect Data. 256 bytes of internal data memory space (00H:FFH) accessed via indirect addressing using instructions other than MOVX and MOVC. All or part of the Stack may be in this area. This area includes the DATA area and the 128 bytes immediately above it.

- SFR

  Special Function Registers. Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.

- XDATA

  'External' Data or Auxiliary RAM. Duplicates the classic 80C51 64 kB memory space addressed via the MOVX instruction using the SPTR, R0, or R1. All or part of this space could be implemented on-chip. The P89LPC952/954 has 256 bytes of on-chip XDATA memory, plus extended SFRs located in XDATA.

- CODE

  64 kB of Code memory space, accessed as part of program execution and via the MOVC instruction. The P89LPC952/954 has 8 kB/16 kB of on-chip Code memory.

7.11 Data RAM arrangement

The 768 bytes of on-chip RAM are organized as shown in Table 6.

Table 6. On-chip data memory usages

Type	Data RAM	Size (bytes)
DATA	Memory that can be addressed directly and indirectly	128
IDATA	Memory that can be addressed indirectly	256
XDATA	Auxiliary ('External Data') on-chip memory that is accessed using the MOVX instructions	256

7.12 Interrupts

The P89LPC952/954 uses a four priority level interrupt structure. This allows great flexibility in controlling the handling of the many interrupt sources. The P89LPC952/954 supports 17 interrupt sources: external interrupts 0 and 1, timers 0 and 1, serial port 0 TX, serial port 0 RX, combined serial port 0 RX/TX, serial port 1 TX, serial port 1 RX, combined serial port 1 RX/TX, brownout detect, watchdog/RTC, I^2C-bus, keyboard, comparators 1 and 2, SPI, and ADC completion.

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the interrupt enable registers IEN0, IEN1 or IEN2. The IEN0 register also contains a global disable bit, EA, which disables all interrupts.

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Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the interrupt priority registers IP0, IP0H, IP1, IP1H, IP2, and IP2H. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. If two requests of different priority levels are pending at the start of an instruction, the request of higher priority level is serviced.

If requests of the same priority level are pending at the start of an instruction, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve pending requests of the same priority level.

7.12.1 External interrupt inputs

The P89LPC952/954 has two external interrupt inputs as well as the Keypad Interrupt function. The two interrupt inputs are identical to those present on the standard 80C51 microcontrollers.

These external interrupts can be programmed to be level-triggered or edge-triggered by setting or clearing bit IT1 or IT0 in Register TCON.

In edge-triggered mode, if successive samples of the $\overline{\text{INTn}}$ pin show a HIGH in one cycle and a LOW in the next cycle, the interrupt request flag IEn in TCON is set, causing an interrupt request.

If an external interrupt is enabled when the P89LPC952/954 is put into Power-down or Idle mode, the interrupt will cause the processor to wake-up and resume operation. Refer to Section 7.15 “Power reduction modes” for details.

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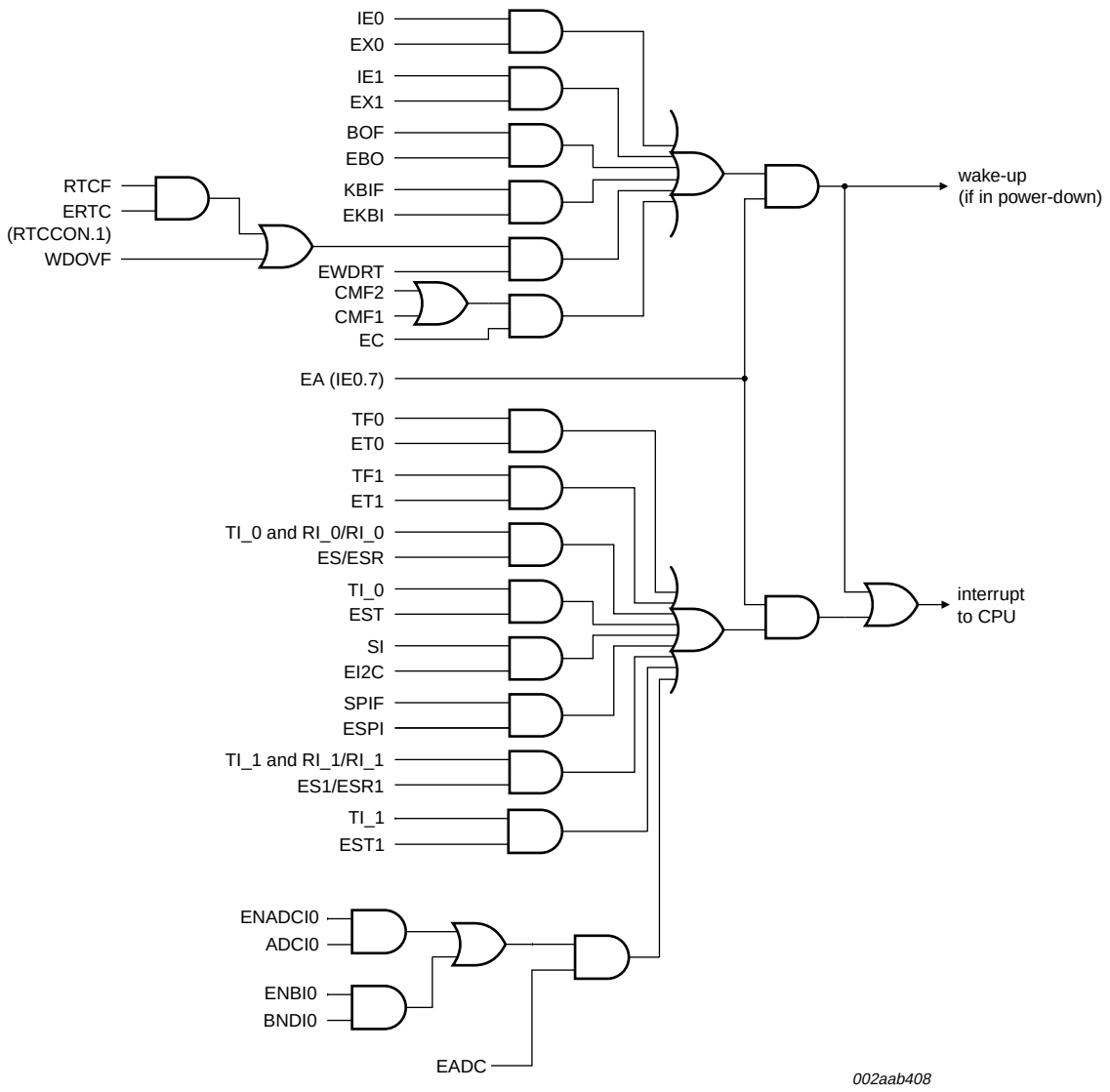


Fig 7. Interrupt sources, interrupt enables, and power-down wake-up sources

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7.13 I/O ports

The P89LPC952/954 has six I/O ports: Port 0, Port 1, Port 2, Port 3, Port 4, and Port 5. Ports 0, 1, 2, 4, and 5 are 8-bit ports, and Port 3 is a 2-bit port. The exact number of I/O pins available depends upon the clock and reset options and package chosen, as shown in Table 7.

Table 7. Number of I/O pins available

Clock source	Reset option	Number of I/O pins (48-pin package)	Number of I/O pins (44-pin package)
On-chip oscillator or watchdog oscillator	No external reset (except during power-up)	42	40
	External $\overline{RST}$ pin supported	41	39
External clock input	No external reset (except during power-up)	41	39
	External $\overline{RST}$ pin supported[1]	40	38
Low/medium/high speed oscillator (external crystal or resonator)	No external reset (except during power-up)	40	38
	External $\overline{RST}$ pin supported[1]	39	37

[1] Required for operation above 12 MHz.

7.13.1 Port configurations

All but three I/O port pins on the P89LPC952/954 may be configured by software to one of four types on a bit-by-bit basis. These are: quasi-bidirectional (standard 80C51 port outputs), push-pull, open drain, and input-only. Two configuration registers for each port select the output type for each port pin.

1. P1.5/$\overline{RST}$ can only be an input and cannot be configured.
2. P1.2/T0/SCL and P1.3/$\overline{INT0}$/SDA may only be configured to be either input-only or open-drain.

7.13.1.1 Quasi-bidirectional output configuration

Quasi-bidirectional output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic HIGH, it is weakly driven, allowing an external device to pull the pin LOW. When the pin is driven LOW, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open-drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

The P89LPC952/954 is a 3 V device, but the pins are 5 V-tolerant. In quasi-bidirectional mode, if a user applies 5 V on the pin, there will be a current flowing from the pin to V_{DD}, causing extra power consumption. Therefore, applying 5 V in quasi-bidirectional mode is discouraged.

A quasi-bidirectional port pin has a Schmitt triggered input that also has a glitch suppression circuit.

7.13.1.2 Open-drain output configuration

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic 0. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to V_{DD}.

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An open-drain port pin has a Schmitt triggered input that also has a glitch suppression circuit.

7.13.1.3 Input-only configuration

The input-only port configuration has no output drivers. It is a Schmitt triggered input that also has a glitch suppression circuit.

7.13.1.4 Push-pull output configuration

The push-pull output configuration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic 1. The push-pull mode may be used when more source current is needed from a port output. A push-pull port pin has a Schmitt triggered input that also has a glitch suppression circuit.

7.13.2 Port 0 analog functions

The P89LPC952/954 incorporates two Analog Comparators. In order to give the best analog function performance and to minimize power consumption, pins that are being used for analog functions must have the digital outputs and digital inputs disabled.

Digital outputs are disabled by putting the port output into the Input-Only (high-impedance) mode.

Digital inputs on Port 0 may be disabled through the use of the PT0AD register, bits 1:5. On any reset, PT0AD[1:5] defaults to ‘0’s to enable digital functions.

7.13.3 Additional port features

After power-up, all pins are in Input-Only mode. **Please note that this is different from the LPC76x series of devices.**

- After power-up, all I/O pins except P1.5, may be configured by software.
- Pin P1.5 is input only. Pins P1.2 and P1.3 are configurable for either input-only or open-drain.

Every output on the P89LPC952/954 has been designed to sink typical LED drive current. However, there is a maximum total output current for all ports which must not be exceeded. Please refer to Table 11 for detailed specifications.

All ports pins that can function as an output have slew rate controlled outputs to limit noise generated by quickly switching output signals. The slew rate is factory-set to approximately 10 ns rise and fall times.

7.14 Power monitoring functions

The P89LPC952/954 incorporates power monitoring functions designed to prevent incorrect operation during initial power-up and power loss or reduction during operation. This is accomplished with two hardware functions: Power-on detect and brownout detect.

7.14.1 Brownout detection

The brownout detect function determines if the power supply voltage drops below a certain level. The default operation is for a brownout detection to cause a processor reset, however it may alternatively be configured to generate an interrupt.

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Brownout detection may be enabled or disabled in software.

If brownout detection is enabled the brownout condition occurs when V_{DD} falls below the brownout trip voltage, V_{bo} (see Table 11 “Static characteristics”), and is negated when V_{DD} rises above V_{bo}. If the P89LPC952/954 device is to operate with a power supply that can be below 2.7 V, BOE should be left in the unprogrammed state so that the device can operate at 2.4 V, otherwise continuous brownout reset may prevent the device from operating.

For correct activation of brownout detect, the V_{DD} rise and fall times must be observed. Please see Table 11 “Static characteristics” for specifications.

7.14.2 Power-on detection

The Power-on detect has a function similar to the brownout detect, but is designed to work as power comes up initially, before the power supply voltage reaches a level where brownout detect can work. The POF flag in the RSTSRC register is set to indicate an initial power-up condition. The POF flag will remain set until cleared by software.

7.15 Power reduction modes

The P89LPC952/954 supports three different power reduction modes. These modes are Idle mode, Power-down mode, and total Power-down mode.

7.15.1 Idle mode

Idle mode leaves peripherals running in order to allow them to activate the processor when an interrupt is generated. Any enabled interrupt source or reset may terminate Idle mode.

7.15.2 Power-down mode

The Power-down mode stops the oscillator in order to minimize power consumption. The P89LPC952/954 exits Power-down mode via any reset, or certain interrupts. In Power-down mode, the power supply voltage may be reduced to the data retention supply voltage V_{DDR}. This retains the RAM contents at the point where Power-down mode was entered. SFR contents are not guaranteed after V_{DD} has been lowered to V_{DDR}, therefore it is highly recommended to wake-up the processor via reset in this case. V_{DD} must be raised to within the operating range before the Power-down mode is exited.

Some chip functions continue to operate and draw power during Power-down mode, increasing the total power used during power-down. These include: Brownout detect, watchdog timer, comparators (note that comparators can be powered down separately), and RTC/system timer. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock and the RTC is enabled.

7.15.3 Total Power-down mode

This is the same as Power-down mode except that the brownout detection circuitry and the voltage comparators are also disabled to conserve additional power. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock **and** the RTC is enabled. If the internal RC oscillator is used to clock the RTC during power-down, there will be high power consumption. Please use an external low frequency clock to achieve low power with the RTC running during power-down.

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7.16 Reset

The P1.5/$\overline{\text{RST}}$ pin can function as either a digital input (P1.5), an active-LOW reset input with an internal pull-up, a bidirectional reset input/output (open drain output with an internal pull-up), or as push-pull reset output. These modes are selected by the RPE (Reset Pin Enable) bit in UCFG1 and the RPE1 (Reset Pin Enable 1) bit in UCFG2.

Table 8. Reset pin modes

P1.5/$\overline{\text{RST}}$ mode	RPE1 (UCFG2.0)	RPE (UCFG1.6)
General purpose input	0	0
Reset input with pull-up	0	1
Bidirectional reset input/output (open drain with pull-up)	1	0
Reset output	1	1

Remark: During a power-up sequence, the RPE and RPE1 selection is overridden and this pin always functions as a reset input. **An external circuit connected to this pin should not hold this pin LOW during a power-on sequence as this will keep the device in reset.** After power-up this pin will function as defined by the RPE and RPE1 bits. Only a power-up reset will temporarily override the selection defined by RPE and RPE1 bits. Other sources of reset will not override the RPE and RPE1 bits.

Remark: During a power cycle, V_{DD} must fall below V_{POR} before power is reapplied, in order to ensure a power-on reset (see Table 11 “Static characteristics” on page 51).

Remark: When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.

Reset can be triggered from the following sources:

- External reset pin (during power-up or if user configured via UCFG1, UCGF2);
- Power-on detect;
- Brownout detect;
- Watchdog timer;
- Software reset;
- UART break character detect reset.

For every reset source, there is a flag in the Reset Register, RSTSRC. The user can read this register to determine the most recent reset source. These flag bits can be cleared in software by writing a ‘0’ to the corresponding bit. More than one flag bit may be set:

- During a power-on reset, both POF and BOF are set but the other flag bits are cleared.
- For any other reset, previously set flag bits that have not been cleared will remain set.

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7.16.1 Reset vector

Following reset, the P89LPC952/954 will fetch instructions from either address 0000H or the Boot address. The Boot address is formed by using the boot vector as the high byte of the address and the low byte of the address = 00H.

The Boot address will be used if a UART break reset occurs, or the non-volatile Boot Status bit (BOOTSTAT.0) = 1, or the device is forced into ISP mode during power-on (see P89LPC952/954 *User's Manual*). Otherwise, instructions will be fetched from address 0000H.

7.17 Timers/counters 0 and 1

The P89LPC952/954 has two general purpose counter/timers which are upward compatible with the standard 80C51 Timer 0 and Timer 1. Both can be configured to operate either as timers or event counters. An option to automatically toggle the T0 and/or T1 pins upon timer overflow has been added.

In the 'Timer' function, the register is incremented every machine cycle.

In the 'Counter' function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled once during every machine cycle.

Timer 0 and Timer 1 have five operating modes (Modes 0, 1, 2, 3 and 6). Modes 0, 1, 2 and 6 are the same for both Timers/Counters. Mode 3 is different.

7.17.1 Mode 0

Putting either Timer into Mode 0 makes it look like an 8048 Timer, which is an 8-bit Counter with a divide-by-32 prescaler. In this mode, the Timer register is configured as a 13-bit register. Mode 0 operation is the same for Timer 0 and Timer 1.

7.17.2 Mode 1

Mode 1 is the same as Mode 0, except that all 16 bits of the timer register are used.

7.17.3 Mode 2

Mode 2 configures the Timer register as an 8-bit Counter with automatic reload. Mode 2 operation is the same for Timer 0 and Timer 1.

7.17.4 Mode 3

When Timer 1 is in Mode 3 it is stopped. Timer 0 in Mode 3 forms two separate 8-bit counters and is provided for applications that require an extra 8-bit timer. When Timer 1 is in Mode 3 it can still be used by the serial port as a baud rate generator.

7.17.5 Mode 6

In this mode, the corresponding timer can be changed to a PWM with a full period of 256 timer clocks.

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7.17.6 Timer overflow toggle output

Timers 0 and 1 can be configured to automatically toggle a port output whenever a timer overflow occurs. The same device pins that are used for the T0 and T1 count inputs are also used for the timer toggle outputs. The port outputs will be a logic 1 prior to the first timer overflow when this mode is turned on.

7.18 RTC/system timer

The P89LPC952/954 has a simple RTC that allows a user to continue running an accurate timer while the rest of the device is powered down. The RTC can be a wake-up or an interrupt source. The RTC is a 23-bit down counter comprised of a 7-bit prescaler and a 16-bit loadable down counter. When it reaches all ‘0’s, the counter will be reloaded again and the RTCF flag will be set. The clock source for this counter can be either the CPU clock (CCLK) or the XTAL oscillator, provided that the XTAL oscillator is not being used as the CPU clock. If the XTAL oscillator is used as the CPU clock, then the RTC will use CCLK as its clock source. Only power-on reset will reset the RTC and its associated SFRs to the default state.

7.19 UARTs

The P89LPC952/954 has two enhanced UARTs that are compatible with the conventional 80C51 UART except that Timer 2 overflow cannot be used as a baud rate source. The P89LPC952/954 does include an independent Baud Rate Generator for each UART (BRG0 for UART 0 and BRG1 for UART 1). The baud rate can be selected from the oscillator (divided by a constant), Timer 1 overflow, or the independent Baud Rate Generator associated with the specific UART. In addition to the baud rate generation, enhancements over the standard 80C51 UART include Framing Error detection, automatic address recognition, selectable double buffering and several interrupt options. The UARTs can be operated in 4 modes: shift register, 8-bit UART, 9-bit UART, and CPU clock/32 or CPU clock/16.

7.19.1 Mode 0

Serial data enters and exits through RXDn. TXDn outputs the shift clock. 8 bits are transmitted or received, LSB first. The baud rate is fixed at $^{1}/_{16}$ of the CPU clock frequency.

7.19.2 Mode 1

10 bits are transmitted (through TXDn) or received (through RXDn): a start bit (logic 0), 8 data bits (LSB first), and a stop bit (logic 1). When data is received, the stop bit is stored in RB8_n in Special Function Register SnCON. The baud rate is variable and is determined by the Timer 1 overflow rate or the Baud Rate Generator (described in Section 7.19.5 “Baud rate generator and selection”).

7.19.3 Mode 2

11 bits are transmitted (through TXDn) or received (through RXDn): start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logic 1). When data is transmitted, the 9th data bit (TB8_n in SnCON) can be assigned the value of ‘0’ or ‘1’. Or, for example, the parity bit (P, in the PSW) could be moved into TB8_n. When data is received, the 9th data bit goes into RB8_n in Special Function Register SnCON, while the

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stop bit is not saved. The baud rate is programmable to either $^1/_{16}$ or $^1/_{32}$ of the CPU clock frequency, as determined by the SMOD1 bit in PCON. The SMOD1 bit controls the Timer 1 output rate available to both UARTs.

7.19.4 Mode 3

11 bits are transmitted (through TXDn) or received (through RXDn): a start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logic 1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable and is determined by the Timer 1 overflow rate or the Baud Rate Generator (described in Section 7.19.5 “Baud rate generator and selection”).

7.19.5 Baud rate generator and selection

Each enhanced UART has an independent Baud Rate Generator. The baud rate is determined by a baud-rate preprogrammed into the BRGR1_n and BRGR0_n SFRs which together form a 16-bit baud rate divisor value that works in a similar manner as Timer 1 but is much more accurate. If the baud rate generator is used, Timer 1 can be used for other timing functions.

The UARTs can use either Timer 1 or their respective baud rate generator output (see Figure 8). Note that Timer T1 is further divided by 2 if the SMOD1 bit (PCON.7) is cleared. The independent Baud Rate Generators use OSCCLK.

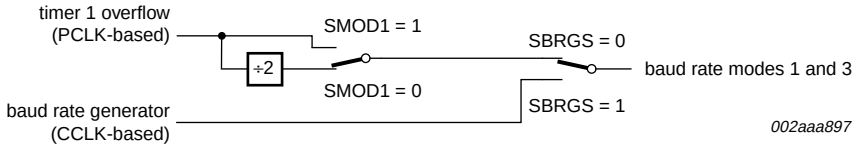


Fig 8. Baud rate sources for UART (Modes 1, 3)

7.19.6 Framing error

Framing error is reported in the status register (SnSTAT). In addition, if SMOD0 (PCON.6) is ‘1’, framing errors can be made available in SnCON.7 respectively. If SMOD0 is ‘0’, SnCON.7 is SM0_n. It is recommended that SM0_n and SM1_n (SnCON.7:6) are set up when SMOD0 is ‘0’.

7.19.7 Break detect

Break detect is reported in the status register (SnSTAT). A break is detected when 11 consecutive bits are sensed LOW. The break detect can be used to reset the device and force the device into ISP mode.

7.19.8 Double buffering

The UART has a transmit double buffer that allows buffering of the next character to be written to SnBUF while the first character is being transmitted. Double buffering allows transmission of a string of characters with only one stop bit between any two characters, as long as the next character is written between the start bit and the stop bit of the previous character.

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Double buffering can be disabled. If disabled (DBMOD_n, i.e., SnSTAT.7 = 0), the UART is compatible with the conventional 80C51 UART. If enabled, the UART allows writing to SnBUF while the previous data is being shifted out. Double buffering is only allowed in Modes 1, 2 and 3. When operated in Mode 0, double buffering must be disabled (DBMOD_n = 0).

7.19.9 Transmit interrupts with double buffering enabled (Modes 1, 2 and 3)

Unlike the conventional UART, in double buffering mode, the TI_n interrupt is generated when the double buffer is ready to receive new data.

7.19.10 The 9th bit (bit 8) in double buffering (Modes 1, 2 and 3)

If double buffering is disabled TB8_n can be written before or after SnBUF is written, as long as TB8_n is updated some time before that bit is shifted out. TB8_n must not be changed until the bit is shifted out, as indicated by the TI_n interrupt.

If double buffering is enabled, TB8_n **must** be updated before SnBUF is written, as TB8_n will be double-buffered together with SnBUF data.

7.20 I²C-bus serial interface

I²C-bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus, and it has the following features:

- Bidirectional data transfer between masters and slaves
- Multi master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- The I²C-bus may be used for test and diagnostic purposes.

A typical I²C-bus configuration is shown in Figure 9. The P89LPC952/954 device provides a byte-oriented I²C-bus interface that supports data transfers up to 400 kHz.

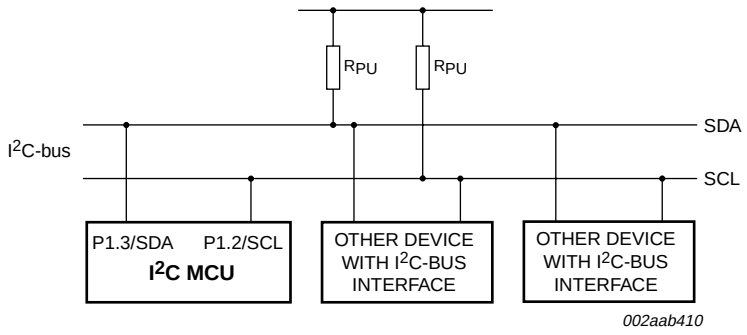


Fig 9. I²C-bus configuration

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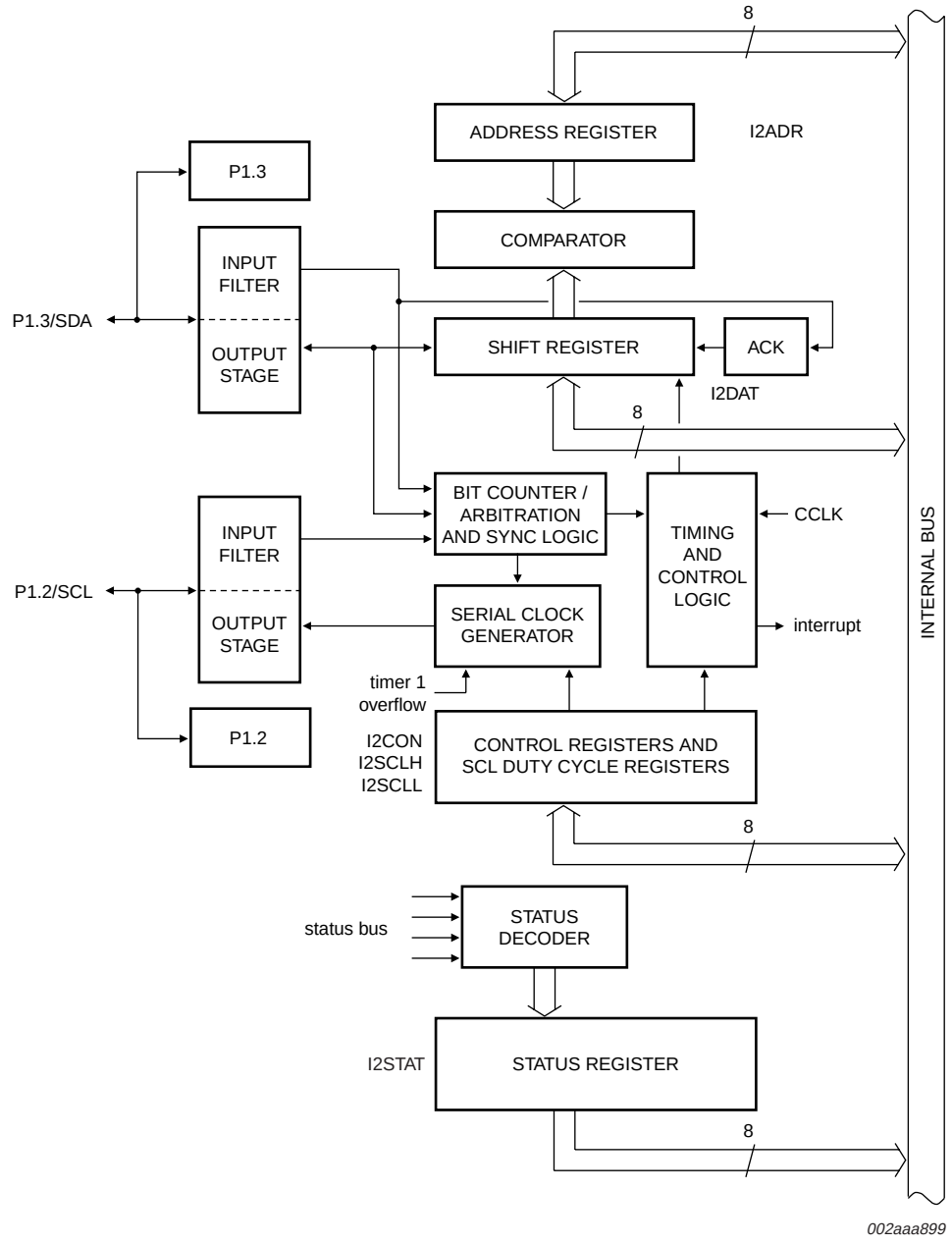


Fig 10. I²C-bus serial interface block diagram

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7.21 SPI

The P89LPC952/954 provides another high-speed serial communication interface — the SPI interface. SPI is a full-duplex, high-speed, synchronous communication bus with two operation modes: Master mode and Slave mode. Up to 3 Mbit/s can be supported in either Master or Slave mode. It has a Transfer Completion Flag and Write Collision Flag Protection.

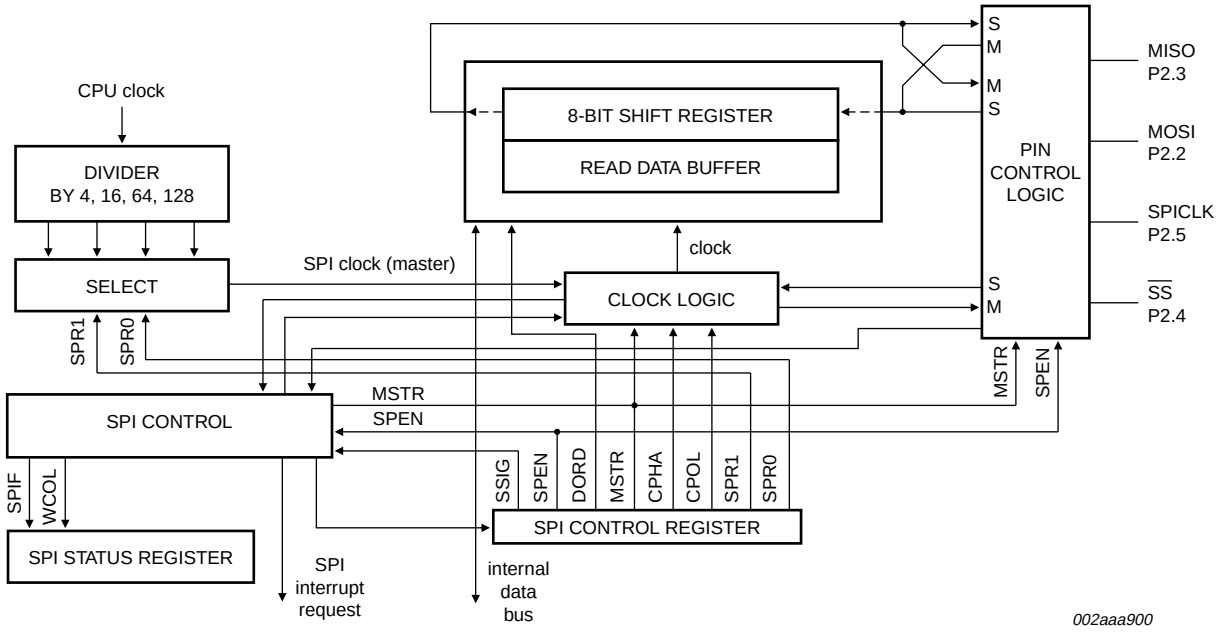


Fig 11. SPI block diagram

The SPI interface has four pins: SPICLK, MOSI, MISO and $\overline{SS}$:

- SPICLK, MOSI and MISO are typically tied together between two or more SPI devices. Data flows from master to slave on MOSI (Master Out Slave In) pin and flows from slave to master on MISO (Master In Slave Out) pin. The SPICLK signal is output in the Master mode and is input in the Slave mode. If the SPI system is disabled, i.e., SPEN (SPCTL.6) = 0 (reset value), these pins are configured for port functions.
- $\overline{SS}$ is the optional slave select pin. In a typical configuration, an SPI master asserts one of its port pins to select one SPI device as the current slave. An SPI slave device uses its $\overline{SS}$ pin to determine whether it is selected.

Typical connections are shown in Figure 12 through Figure 14.

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7.21.1 Typical SPI configurations

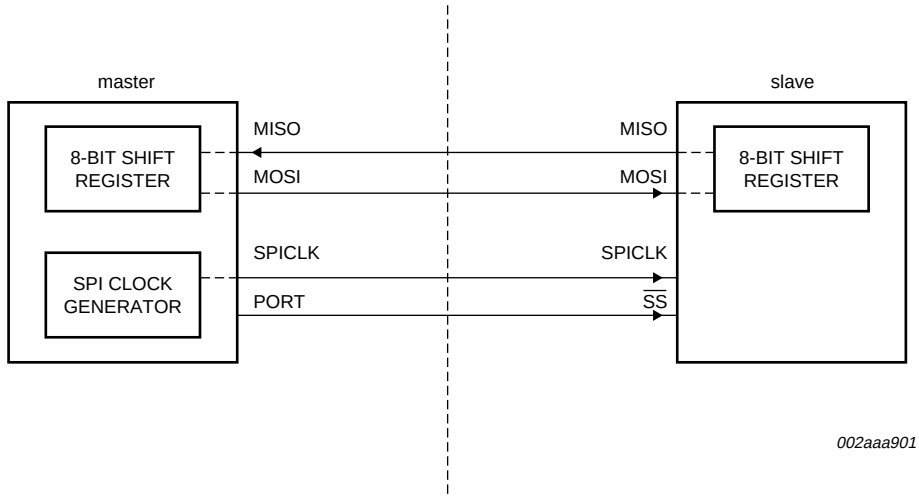


Fig 12. SPI single master single slave configuration

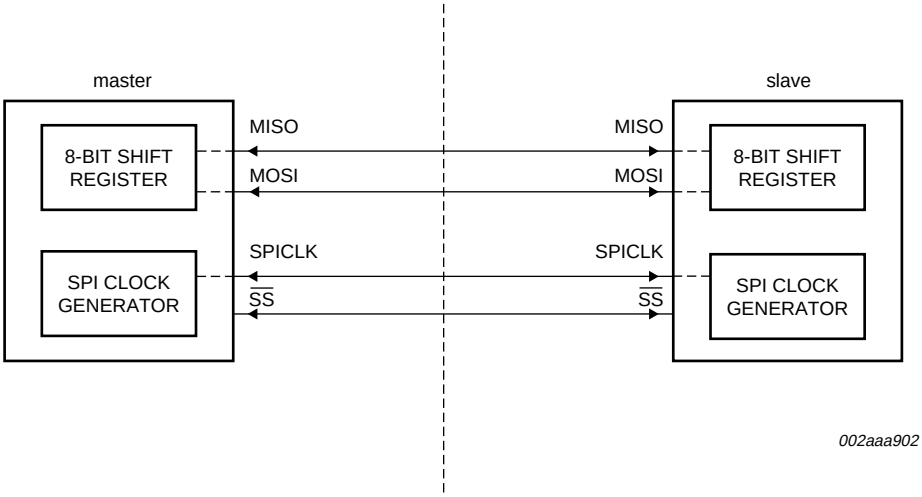


Fig 13. SPI dual device configuration, where either can be a master or a slave

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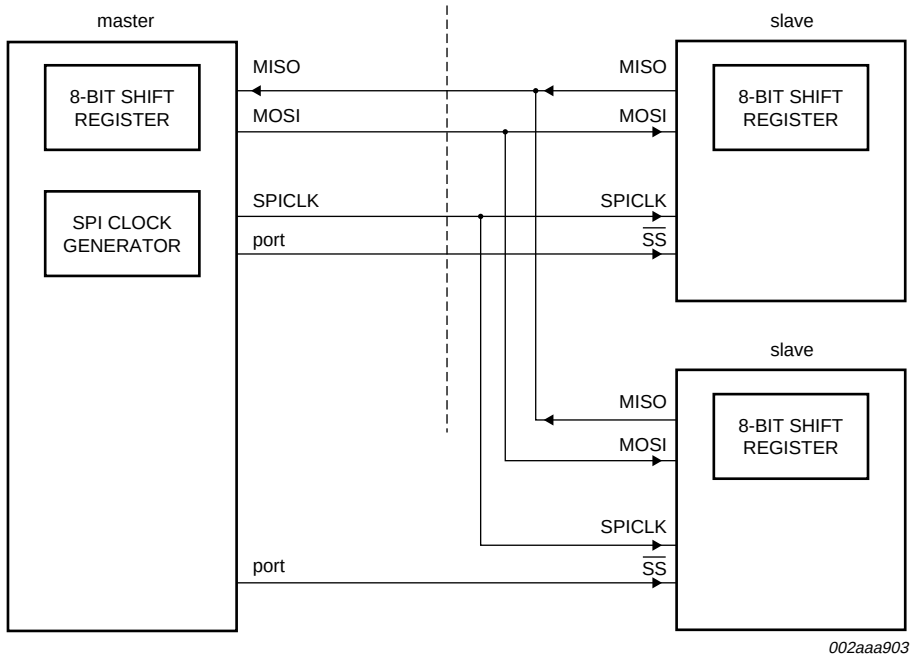


Fig 14. SPI single master multiple slaves configuration

7.22 Analog comparators

Two analog comparators are provided on the P89LPC952/954. Input and output options allow use of the comparators in a number of different configurations. Comparator operation is such that the output is a logical one (which may be read in a register and/or routed to a pin) when the positive input (one of two selectable pins) is greater than the negative input (selectable from a pin or an internal reference voltage). Otherwise the output is a zero. Each comparator may be configured to cause an interrupt when the output value changes.

The overall connections to both comparators are shown in Figure 15. The comparators function to V_{DD} = 2.4 V.

When each comparator is first enabled, the comparator output and interrupt flag are not guaranteed to be stable for 10 µs. The corresponding comparator interrupt should not be enabled during that time, and the comparator interrupt flag must be cleared before the interrupt is enabled in order to prevent an immediate interrupt service.

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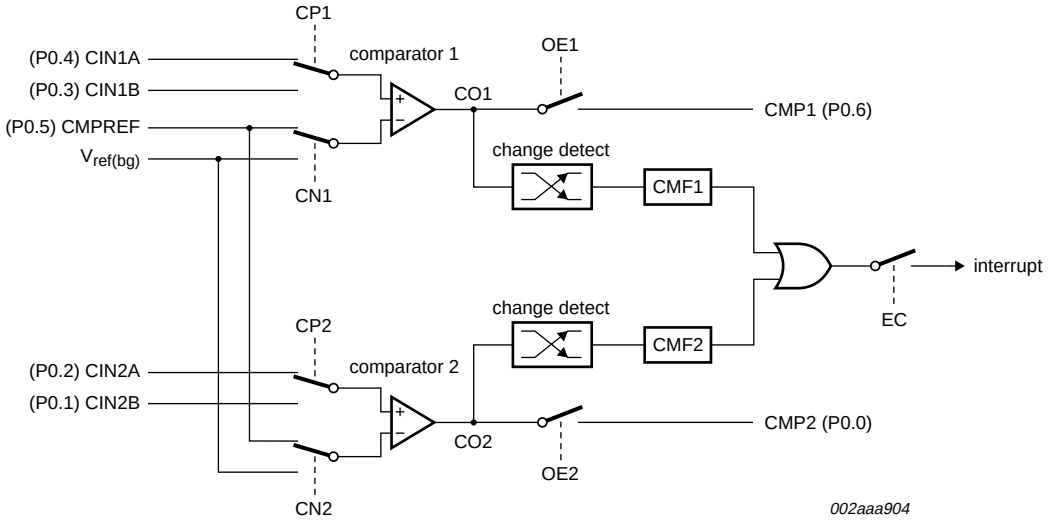


Fig 15. Comparator input and output connections

7.22.1 Internal reference voltage

An internal reference voltage generator may supply a default reference when a single comparator input pin is used. The value of the internal reference voltage, referred to as $V_{ref(bg)}$, is 1.23 V ± 10 %.

7.22.2 Comparator interrupt

Each comparator has an interrupt flag contained in its configuration register. This flag is set whenever the comparator output changes state. The flag may be polled by software or may be used to generate an interrupt. The two comparators use one common interrupt vector. If both comparators enable interrupts, after entering the interrupt service routine, the user needs to read the flags to determine which comparator caused the interrupt.

7.22.3 Comparators and power reduction modes

Either or both comparators may remain enabled when Power-down or Idle mode is activated, but both comparators are disabled automatically in Total Power-down mode.

If a comparator interrupt is enabled (except in Total Power-down mode), a change of the comparator output state will generate an interrupt and wake-up the processor. If the comparator output to a pin is enabled, the pin should be configured in the push-pull mode in order to obtain fast switching times while in Power-down mode. The reason is that with the **oscillator** stopped, the temporary strong pull-up that normally occurs during switching on a quasi-bidirectional port pin does not take place.

Comparators consume power in Power-down and Idle modes, as well as in the normal operating mode. This fact should be taken into account when system power consumption is an issue. To minimize power consumption, the user can disable the comparators via PCONA.5, or put the device in Total Power-down mode.

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7.23 KBI

The Keypad Interrupt function is intended primarily to allow a single interrupt to be generated when Port 0 is equal to or not equal to a certain pattern. This function can be used for bus address recognition or keypad recognition. The user can configure the port via SFRs for different tasks.

The Keypad Interrupt Mask Register (KBMASK) is used to define which input pins connected to Port 0 can trigger the interrupt. The Keypad Pattern Register (KBPATN) is used to define a pattern that is compared to the value of Port 0. The Keypad Interrupt Flag (KBIF) in the Keypad Interrupt Control Register (KBCON) is set when the condition is matched while the Keypad Interrupt function is active. An interrupt will be generated if enabled. The PATN_SEL bit in the Keypad Interrupt Control Register (KBCON) is used to define equal or not-equal for the comparison.

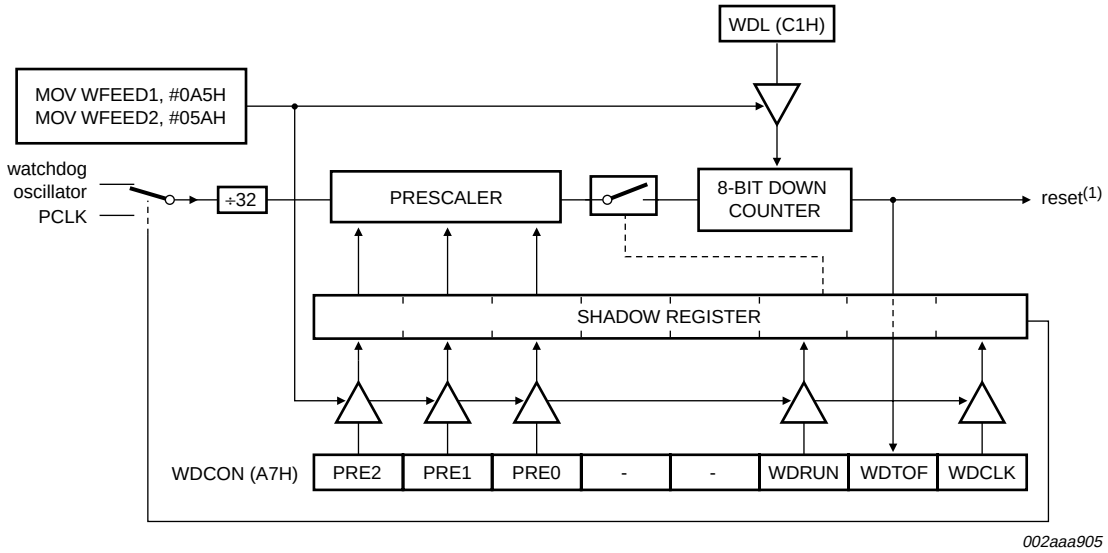
In order to use the Keypad Interrupt as an original KBI function like in 87LPC76x series, the user needs to set KBPATN = 0FFH and PATN_SEL = 1 (not equal), then any key connected to Port 0 which is enabled by the KBMASK register will cause the hardware to set KBIF and generate an interrupt if it has been enabled. The interrupt may be used to wake-up the CPU from Idle or Power-down modes. This feature is particularly useful in handheld, battery-powered systems that need to carefully manage power consumption yet also need to be convenient to use.

In order to set the flag and cause an interrupt, the pattern on Port 0 must be held longer than six CCLKs.

7.24 Watchdog timer

The watchdog timer causes a system reset when it underflows as a result of a failure to feed the timer prior to the timer reaching its terminal count. It consists of a programmable 12-bit prescaler, and an 8-bit down counter. The down counter is decremented by a tap taken from the prescaler. The clock source for the prescaler is either the PCLK or the nominal 400 kHz watchdog oscillator. The watchdog timer can only be reset by a power-on reset. When the watchdog feature is disabled, it can be used as an interval timer and may generate an interrupt. Figure 16 shows the watchdog timer in Watchdog mode. Feeding the watchdog requires a two-byte sequence. If PCLK is selected as the watchdog clock and the CPU is powered down, the watchdog is disabled. The watchdog timer has a time-out period that ranges from a few µs to a few seconds. Please refer to the P89LPC952/954 *User's Manual* for more details.

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(1) Watchdog reset can also be caused by an invalid feed sequence, or by writing to WDCON not immediately followed by a feed sequence.

Fig 16. Watchdog timer in Watchdog mode (WDTE = 1)

7.25 Additional features

7.25.1 Software reset

The SRST bit in AUXR1 gives software the opportunity to reset the processor completely, as if an external reset or watchdog reset had occurred. Care should be taken when writing to AUXR1 to avoid accidental software resets.

7.25.2 Dual data pointers

The dual Data Pointers (DPTR) provides two different Data Pointers to specify the address used with certain instructions. The DPS bit in the AUXR1 register selects one of the two Data Pointers. Bit 2 of AUXR1 is permanently wired as a logic 0 so that the DPS bit may be toggled (thereby switching Data Pointers) simply by incrementing the AUXR1 register, without the possibility of inadvertently altering other bits in the register.

7.25.3 Debugger interface

This device contains a two-wire serial debugger interface designed to be used with commercially available debugging tools. An additional trigger output is provided that maybe triggered using the two-wire debugger interface.

The Freeze register allows the user to selectively disable clocking of peripheral device timers while in the debugger mode.

The two-wire serial debugger interface can also be used be used to program the code memory of these devices.

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7.26 Flash program memory

7.26.1 General description

The P89LPC952/954 flash memory provides in-circuit electrical erasure and programming. The flash can be erased, read, and written as bytes. The Sector and Page Erase functions can erase any flash sector (1 kB) or page (64 bytes). The Chip Erase operation will erase the entire program memory. ICP using standard commercial programmers is available. In addition, IAP and byte-erase allows code memory to be used for non-volatile data storage. On-chip erase and write timing generation contribute to a user-friendly programming interface. The P89LPC952/954 flash reliably stores memory contents even after 400,000 erase and program cycles. The cell is designed to optimize the erase and programming mechanisms. The P89LPC952/954 uses V_{DD} as the supply voltage to perform the Program/Erase algorithms.

7.26.2 Features

- Programming and erase over the full operating voltage range.
- Byte erase allows code memory to be used for data storage.
- Read/Programming/Erase using ISP, IAP, ICP, or two-wire serial debugger.
- Internal fixed boot ROM, containing low-level IAP routines available to user code.
- Default loader providing ISP via the serial port, located in upper end of user program memory.
- Boot vector allows user-provided flash loader code to reside anywhere in the flash memory space, providing flexibility to the user.
- Any flash program/erase operation in 2 ms.
- Programming with industry-standard commercial programmers.
- Programmable security for the code in the flash for each sector.
- 400,000 typical erase/program cycles for each byte.
- 20 year minimum data retention.

7.26.3 Flash organization

The program memory consists of eight/sixteen 1 kB sectors on the P89LPC952/954 devices. Each sector can be further divided into 64-byte pages. In addition to sector erase, page erase, and byte erase, a 64-byte page register is included which allows from 1 to 64 bytes of a given page to be programmed at the same time, substantially reducing overall programming time.

7.26.4 Using flash as data storage

The flash code memory array of this device supports individual byte erasing and programming. Any byte in the code memory array may be read using the MOVC instruction, provided that the sector containing the byte has not been secured (a MOVC instruction is not allowed to read code memory contents of a secured sector). Thus any byte in a non-secured sector may be used for non-volatile data storage.

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7.26.5 Flash programming and erasing

Four different methods of erasing or programming of the flash are available. The flash may be programmed or erased in the end-user application (IAP) under control of the application's firmware. Another option is to use the ICP mechanism. This ICP system provides for programming through a serial clock/serial data interface. As shipped from the factory, the upper 512 bytes of user code space contains a serial ISP routine allowing for the device to be programmed in circuit through the serial port. The flash may also be programmed or erased using a commercially available EPROM programmer which supports this device. This device does not provide for direct verification of code memory contents. Instead, this device provides a 32-bit CRC result on either a sector or the entire user code space.

7.26.6 ICP

ICP is performed without removing the microcontroller from the system. The ICP facility consists of internal hardware resources to facilitate remote programming of the P89LPC952/954 through a two-wire serial interface. The Philips ICP facility has made in-circuit programming in an embedded application—using commercially available programmers—possible with a minimum of additional expense in components and circuit board area. The ICP function uses five pins. Only a small connector needs to be available to interface your application to a commercial programmer in order to use this feature. Additional details may be found in the P89LPC952/954 *User's Manual*.

7.26.7 IAP

IAP is performed in the application under the control of the microcontroller's firmware. The IAP facility consists of internal hardware resources to facilitate programming and erasing. The Philips IAP has made in-application programming in an embedded application possible without additional components. Two methods are available to accomplish IAP. A set of predefined IAP functions are provided in a Boot ROM and can be called through a common interface, PGM_MTP. Several IAP calls are available for use by an application program to permit selective erasing and programming of flash sectors, pages, security bits, configuration bytes, and device ID. These functions are selected by setting up the microcontroller's registers before making a call to PGM_MTP at FF03H. The Boot ROM occupies the program memory space at the top of the address space from FF00H to FEFFH, thereby not conflicting with the user program memory space.

In addition, IAP operations can be accomplished through the use of four SFRs consisting of a control/status register, a data register, and two address registers. Additional details may be found in the P89LPC952/954 *User's Manual*.

7.26.8 ISP

ISP is performed without removing the microcontroller from the system. The ISP facility consists of a series of internal hardware resources coupled with internal firmware to facilitate remote programming of the P89LPC952/954 through the serial port. This firmware is provided by Philips and embedded within each P89LPC952/954 device. The Philips ISP facility has made in-system programming in an embedded application possible with a minimum of additional expense in components and circuit board area. The ISP function uses five pins (V_{DD}, V_{SS}, TXD, RXD, and $\overline{RST}$). Only a small connector needs to be available to interface your application to an external circuit in order to use this feature.

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7.26.9 Power-on reset code execution

The P89LPC952/954 contains two special flash elements: the Boot Vector and the Boot Status bit. Following reset, the P89LPC952/954 examines the contents of the Boot Status bit. If the Boot Status bit is set to zero, power-up execution starts at location 0000H, which is the normal start address of the user's application code. When the Boot Status bit is set to a value other than zero, the contents of the Boot Vector are used as the high byte of the execution address and the low byte is set to 00H.

Table 9 shows the factory default Boot Vector setting for these devices. A factory-provided bootloader is pre-programmed into the address space indicated and uses the indicated bootloader entry point to perform ISP functions. This code can be erased by the user. **Users who wish to use this loader should take precautions to avoid erasing the 1 kB sector that contains this bootloader. Instead, the page erase function can be used to erase the first eight 64-byte pages located in this sector.** A custom bootloader can be written with the Boot Vector set to the custom bootloader, if desired.

Table 9. Default boot vector values and ISP entry points

Device	Default boot vector	Default bootloader entry point	Default bootloader code range	1 kB sector range
P89LPC952	1FH	1F00H	1E00H to 1FFFH	1C00H to 1FFFH
P89LPC954	3FH	3F00H	3E00H to 3FFFH	3C00H to 3FFFH

7.26.10 Hardware activation of the bootloader

The bootloader can also be executed by forcing the device into ISP mode during a power-on sequence (see the P89LPC952/954 *User's Manual* for specific information). This has the same effect as having a non-zero status byte. This allows an application to be built that will normally execute user code but can be manually forced into ISP operation. If the factory default setting for the boot vector (1FH/3FH) is changed, it will no longer point to the factory pre-programmed ISP bootloader code. After programming the flash, the status byte should be programmed to zero in order to allow execution of the user's application code beginning at address 0000H.

7.27 User configuration bytes

Some user-configurable features of the P89LPC952/954 must be defined at power-up and therefore cannot be set by the program after start of execution. These features are configured through the use of the flash byte UCFG1. Please see the P89LPC952/954 *User's Manual* for additional details.

7.28 User sector security bytes

There are eight/sixteen User Sector Security Bytes on the P89LPC952/954. Each byte corresponds to one sector. Please see the P89LPC952/954 *User's Manual* for additional details.

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8. ADC

8.1 General description

The P89LPC952/954 has a 10-bit, 8-channel multiplexed successive approximation ADC module. A block diagram of the ADC is shown in Figure 17. The ADC consists of an 8-input multiplexer which feeds a sample-and-hold circuit providing an input signal to one of two comparator inputs. The control logic in combination with the SAR drives a DAC which provides the other input to the comparator. The output of the comparator is fed to the SAR.

8.2 Features

- 10-bit, 8-channel multiplexed input, successive approximation ADC.
- Eight result register pairs.
- Six operating modes:
  - Fixed channel, single conversion mode.
  - Fixed channel, continuous conversion mode.
  - Auto scan, single conversion mode.
  - Auto scan, continuous conversion mode.
  - Dual channel, continuous conversion mode.
  - Single step mode.
- Three conversion start modes:
  - Timer triggered start.
  - Start immediately.
  - Edge triggered.
- 10-bit conversion time of 4 μs at an A/D clock of 9 MHz.
- Interrupt or polled operation.
- High and low boundary limits interrupt; selectable in or out-of-range.
- Clock divider.
- Power-down mode.

8.3 Block diagram

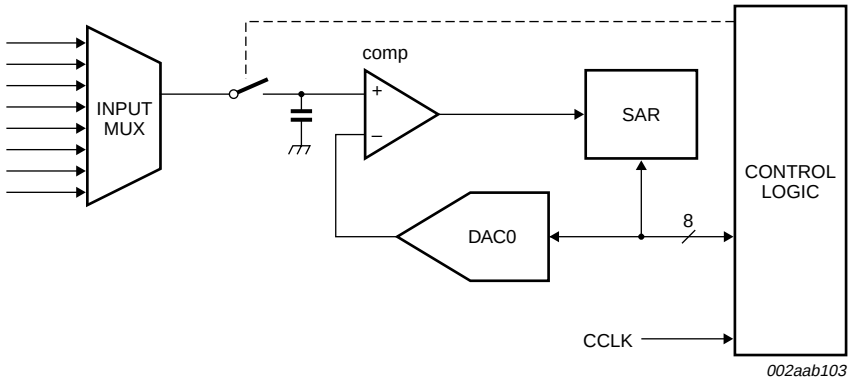


Fig 17. ADC block diagram

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8.4 ADC operating modes

8.4.1 Fixed channel, single conversion mode

A single input channel can be selected for conversion. A single conversion will be performed and the result placed in the result register pair which corresponds to the selected input channel. An interrupt, if enabled, will be generated after the conversion completes.

8.4.2 Fixed channel, continuous conversion mode

A single input channel can be selected for continuous conversion. The results of the conversions will be sequentially placed in the eight result register pairs. The user may select whether an interrupt can be generated after every four or every eight conversions. Additional conversion results will again cycle through the result register pairs, overwriting the previous results. Continuous conversions continue until terminated by the user.

8.4.3 Auto scan, single conversion mode

Any combination of the eight input channels can be selected for conversion. A single conversion of each selected input will be performed and the result placed in the result register pair which corresponds to the selected input channel. The user may select whether an interrupt, if enabled, will be generated after either the first four conversions have occurred or all selected channels have been converted. If the user selects to generate an interrupt after the four input channels have been converted, a second interrupt will be generated after the remaining input channels have been converted. If only a single channel is selected this is equivalent to single channel, single conversion mode.

8.4.4 Auto scan, continuous conversion mode

Any combination of the eight input channels can be selected for conversion. A conversion of each selected input will be performed and the result placed in the result register pair which corresponds to the selected input channel. The user may select whether an interrupt, if enabled, will be generated after either the first four conversions have occurred or all selected channels have been converted. If the user selects to generate an interrupt after the four input channels have been converted, a second interrupt will be generated after the remaining input channels have been converted. After all selected channels have been converted, the process will repeat starting with the first selected channel. Additional conversion results will again cycle through the eight result register pairs, overwriting the previous results. Continuous conversions continue until terminated by the user.

8.4.5 Dual channel, continuous conversion mode

This is a variation of the auto scan continuous conversion mode where conversion occurs on two user-selectable inputs. The result of the conversion of the first channel is placed in the result register pair, AD0DAT0R and AD0DAT0L. The result of the conversion of the second channel is placed in result register pair, AD0DAT1R and AD0DAT1L. The first channel is again converted and its result stored in AD0DAT2R and AD0DAT2L. The second channel is again converted and its result placed in AD0DAT3R and AD0DAT3L, etc. An interrupt is generated, if enabled, after every set of four or eight conversions (user selectable).

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8.4.6 Single step mode

This special mode allows ‘single-stepping’ in an auto scan conversion mode. Any combination of the eight input channels can be selected for conversion. After each channel is converted, an interrupt is generated, if enabled, and the ADC waits for the next start condition. May be used with any of the start modes.

8.5 Conversion start modes

8.5.1 Timer triggered start

An A/D conversion is started by the overflow of Timer 0. Once a conversion has started, additional Timer 0 triggers are ignored until the conversion has completed. The Timer triggered start mode is available in all ADC operating modes.

8.5.2 Start immediately

Programming this mode immediately starts a conversion. This start mode is available in all ADC operating modes.

8.5.3 Edge triggered

An A/D conversion is started by rising or falling edge of P1.4. Once a conversion has started, additional edge triggers are ignored until the conversion has completed. The edge triggered start mode is available in all ADC operating modes.

8.6 Boundary limits interrupt

The ADC has both a high and low boundary limit register. The user may select whether an interrupt is generated when the conversion result is within (or equal to) the high and low boundary limits or when the conversion result is outside the boundary limits. An interrupt will be generated, if enabled, if the result meets the selected interrupt criteria. The boundary limit may be disabled by clearing the boundary limit interrupt enable.

An early detection mechanism exists when the interrupt criteria has been selected to be outside the boundary limits. In this case, after the four MSBs have been converted, these four bits are compared with the four MSBs of the boundary high and low registers. If the four MSBs of the conversion meet the interrupt criteria (i.e., outside the boundary limits) an interrupt will be generated, if enabled. If the four MSBs do not meet the interrupt criteria, the boundary limits will again be compared after all 8 MSBs have been converted. A boundary status register (BNDSTA0) flags the channels which caused a boundary interrupt.

8.7 Clock divider

The ADC requires that its internal clock source be in the range of 320 kHz to 9 MHz to maintain accuracy. A programmable clock divider that divides the clock from 1 to 8 is provided for this purpose.

8.8 Power-down and Idle mode

In Idle mode the ADC, if enabled, will continue to function and can cause the device to exit Idle mode when the conversion is completed if the A/D interrupt is enabled. In Power-down mode or Total Power-down mode, the ADC does not function. If the ADC is enabled, it will consume power. Power can be reduced by disabling the ADC.

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9. Limiting values

Table 10. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
$T_{amb(bias)}$	bias ambient temperature		–55	+125	°C
T_{stg}	storage temperature		–65	+150	°C
$I_{OH(I/O)}$	HIGH-level output current per input/output pin		-	20	mA
$I_{OL(I/O)}$	LOW-level output current per input/output pin		-	20	mA
$I_{I/Otot(max)}$	maximum total input/output current		-	100	mA
V_n	voltage on any other pin	except V_{SS}, with respect to V_{DD}	-	3.5	V
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption	-	1.5	W

[1] The following applies to Table 10:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over ambient temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

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10. Static characteristics

Table 11. Static characteristics

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$I_{DD(oper)}$	operating supply current	V_{DD} = 3.6 V; f_{osc} = 12 MHz	[2]	-	11	18	mA
		V_{DD} = 3.6 V; f_{osc} = 18 MHz	[2]	-	14	23	mA
$I_{DD(idle)}$	Idle mode supply current	V_{DD} = 3.6 V; f_{osc} = 12 MHz	[2]	-	3.25	5	mA
		V_{DD} = 3.6 V; f_{osc} = 18 MHz	[2]	-	5	7	mA
$I_{DD(pd)}$	Power-down mode supply current	V_{DD} = 3.6 V; voltage comparators powered down	[2]	-	55	80	µA
$I_{DD(tpd)}$	total Power-down mode supply current	V_{DD} = 3.6 V	[3]	-	0.5	5	µA
$(dV/dt)_r$	rise rate	of V_{DD}		-	-	2	mV/µs
$(dV/dt)_f$	fall rate	of V_{DD}		-	-	50	mV/µs
V_{POR}	power-on reset voltage			-	-	0.5	V
V_{DDR}	data retention supply voltage			1.5	-	-	V
$V_{th(HL)}$	HIGH-LOW threshold voltage	except SCL, SDA		$0.22V_{DD}$	$0.4V_{DD}$	-	V
V_{IL}	LOW-level input voltage	SCL, SDA only		−0.5	-	$0.3V_{DD}$	V
$V_{th(LH)}$	LOW-HIGH threshold voltage	except SCL, SDA		-	$0.6V_{DD}$	$0.7V_{DD}$	V
V_{IH}	HIGH-level input voltage	SCL, SDA only		$0.7V_{DD}$	-	5.5	V
V_{hys}	hysteresis voltage	port 1		-	$0.2V_{DD}$	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 20 mA; V_{DD} = 2.4 V to 3.6 V all ports, all modes except high-Z	[4]	-	0.6	1.0	V
		I_{OL} = 3.2 mA; V_{DD} = 2.4 V to 3.6 V all ports, all modes except high-Z	[4]	-	0.2	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} = −20 µA; V_{DD} = 2.4 V to 3.6 V; all ports, quasi-bidirectional mode		V_{DD} − 0.3	V_{DD} − 0.2	-	V
		I_{OH} = −3.2 mA; V_{DD} = 2.4 V to 3.6 V; all ports, push-pull mode		V_{DD} − 0.7	V_{DD} − 0.4	-	V
		I_{OH} = −20 mA; V_{DD} = 2.4 V to 3.6 V; Port 5, push-pull mode		$0.8V_{DD}$	-	-	V
V_{xtal}	crystal voltage	on XTAL1, XTAL2 pins; with respect to V_{SS}		−0.5	-	+4.0	V
V_n	voltage on any other pin	except XTAL1, XTAL2, V_{DD}; with respect to V_{SS}	[5]	−0.5	-	+5.5	V

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Table 11. Static characteristics *…continued*

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
C_{iss}	input capacitance		[6]	-	-	15	pF
I_{IL}	LOW-level input current	V_I = 0.4 V	[7]	-	-	−80	µA
I_{LI}	input leakage current	$V_I = V_{IL}$, V_{IH}, or $V_{th(HL)}$	[8]	-	-	±1	µA
I_{THL}	HIGH-LOW transition current	all ports; V_I = 1.5 V at V_{DD} = 3.6 V	[9]	−30	-	−450	µA
$R_{RST_N(int)}$	internal pull-up resistance on pin $\overline{RST}$	pin $\overline{RST}$		10	-	30	kΩ
V_{bo}	brownout trip voltage	BOE = 1		2.4	-	2.7	V
$V_{ref(bg)}$	band gap reference voltage			1.19	1.23	1.27	V
TC_{bg}	band gap temperature coefficient			-	10	20	ppm/°C

[1] Typical ratings are not guaranteed. The values listed are at room temperature, 3 V.

[2] The $I_{DD(oper)}$, $I_{DD(idle)}$, and $I_{DD(pd)}$ specifications are measured using an external clock with the following functions disabled: comparators, real-time clock, and watchdog timer.

[3] The $I_{DD(tpd)}$ specification is measured using an external clock with the following functions disabled: comparators, real-time clock, brownout detect, and watchdog timer.

[4] See Section 9 “Limiting values” for steady state (non-transient) limits on I_{OL} or I_{OH}. If I_{OL}/I_{OH} exceeds the test condition, V_{OL}/V_{OH} may exceed the related specification.

[5] This specification can be applied to pins which have A/D input or analog comparator input functions when the pin is not being used for those analog functions. When the pin is being used as an analog input pin, the maximum voltage on the pin must be limited to 4.0 V with respect to V_{SS}.

[6] Pin capacitance is characterized but not tested.

[7] Measured with port in quasi-bidirectional mode.

[8] Measured with port in high-impedance mode.

[9] Port pins source a transition current when used in quasi-bidirectional mode and externally driven from logic 1 to logic 0. This current is highest when V_I is approximately 2 V.

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11. Dynamic characteristics

Table 12. Dynamic characteristics (12 MHz)

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 12 MHz		Unit
			Min	Max	Min	Max	
$f_{osc(RC)}$	internal RC oscillator frequency	nominal f = 7.3728 MHz trimmed to ± 1 % at T_{amb} = 25 °C; clock doubler option = OFF (default)	7.189	7.557	7.189	7.557	MHz
		nominal f = 14.7456 MHz; clock doubler option = ON, V_{DD} = 2.7 V to 3.6 V	14.378	15.114	14.378	15.114	MHz
$f_{osc(WD)}$	internal watchdog oscillator frequency		320	520	320	520	kHz
f_{osc}	oscillator frequency		0	12	-	-	MHz
$T_{cy(clk)}$	clock cycle time	see Figure 19	83	-	-	-	ns
f_{CLKLP}	low-power select clock frequency		0	8	-	-	MHz
Glitch filter							
t_{gr}	glitch rejection time	P1.5/$\overline{\text{RST}}$ pin	-	50	-	50	ns
		any pin except P1.5/$\overline{\text{RST}}$	-	15	-	15	ns
t_{sa}	signal acceptance time	P1.5/$\overline{\text{RST}}$ pin	125	-	125	-	ns
		any pin except P1.5/$\overline{\text{RST}}$	50	-	50	-	ns
External clock							
t_{CHCX}	clock HIGH time	see Figure 19	33	$T_{cy(clk)} - t_{CLCX}$	33	-	ns
t_{CLCX}	clock LOW time	see Figure 19	33	$T_{cy(clk)} - t_{CHCX}$	33	-	ns
t_{CLCH}	clock rise time	see Figure 19	-	8	-	8	ns
t_{CHCL}	clock fall time	see Figure 19	-	8	-	8	ns
Shift register (UART mode 0)							
T_{XLXL}	serial port clock cycle time	see Figure 18	$16T_{cy(clk)}$	-	1333	-	ns
t_{QVXH}	output data set-up to clock rising edge time	see Figure 18	$13T_{cy(clk)}$	-	1083	-	ns
t_{XHQX}	output data hold after clock rising edge time	see Figure 18	-	$T_{cy(clk)}$ + 20	-	103	ns
t_{XHDX}	input data hold after clock rising edge time	see Figure 18	-	0	-	0	ns
t_{XHDV}	input data valid to clock rising edge time	see Figure 18	150	-	150	-	ns
SPI interface							
f_{SPI}	SPI operating frequency						
	slave		0	CCLK/6	0	2.0	MHz
	master		-	CCLK/4	-	3.0	MHz

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Table 12. Dynamic characteristics (12 MHz) *…continued*

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.

T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 12 MHz		Unit
			Min	Max	Min	Max	
T_{SPICYC}	SPI cycle time	see Figure 20, 21, 22, 23					
	slave		$^{6}/_{CCLK}$	-	500	-	ns
	master		$^{4}/_{CCLK}$	-	333	-	ns
$t_{SPILEAD}$	SPI enable lead time	see Figure 22, 23					
	slave		250	-	250	-	ns
t_{SPILAG}	SPI enable lag time	see Figure 22, 23					
	slave		250	-	250	-	ns
$t_{SPICLKH}$	SPICLK HIGH time	see Figure 20, 21, 22, 23					
	master		$^{2}/_{CCLK}$	-	165	-	ns
	slave		$^{3}/_{CCLK}$	-	250	-	ns
$t_{SPICLKL}$	SPICLK LOW time	see Figure 20, 21, 22, 23					
	master		$^{2}/_{CCLK}$	-	165	-	ns
	slave		$^{3}/_{CCLK}$	-	250	-	ns
t_{SPIDSU}	SPI data set-up time	see Figure 20, 21, 22, 23					
	master or slave		100	-	100	-	ns
t_{SPIDH}	SPI data hold time	see Figure 20, 21, 22, 23					
	master or slave		100	-	100	-	ns
t_{SPIA}	SPI access time	see Figure 22, 23					
	slave		0	120	0	120	ns
t_{SPIDIS}	SPI disable time	see Figure 22, 23					
	slave		0	240	-	240	ns
t_{SPIDV}	SPI enable to output data valid time	see Figure 20, 21, 22, 23					
	slave		-	240	-	240	ns
	master		-	167	-	167	ns
t_{SPIOH}	SPI output data hold time	see Figure 20, 21, 22, 23	0	-	0	-	ns
t_{SPIR}	SPI rise time	see Figure 20, 21, 22, 23					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns
t_{SPIF}	SPI fall time	see Figure 20, 21, 22, 23					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

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Table 13. Dynamic characteristics (18 MHz)

V_{DD} = 3.0 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 18 MHz		Unit
			Min	Max	Min	Max	
$f_{osc(RC)}$	internal RC oscillator frequency	nominal f = 7.3728 MHz trimmed to ± 1 % at T_{amb} = 25 °C; clock doubler option = OFF (default)	7.189	7.557	7.189	7.557	MHz
		nominal f = 14.7456 MHz; clock doubler option = ON	14.378	15.114	14.378	15.114	MHz
$f_{osc(WD)}$	internal watchdog oscillator frequency		320	520	320	520	kHz
f_{osc}	oscillator frequency		0	18	-	-	MHz
$T_{cy(clk)}$	clock cycle time	see Figure 19	55	-	-	-	ns
f_{CLKLP}	low-power select clock frequency		0	8	-	-	MHz
Glitch filter							
t_{gr}	glitch rejection time	P1.5/$\overline{RST}$ pin	-	50	-	50	ns
		any pin except P1.5/$\overline{RST}$	-	15	-	15	ns
t_{sa}	signal acceptance time	P1.5/$\overline{RST}$ pin	125	-	125	-	ns
		any pin except P1.5/$\overline{RST}$	50	-	50	-	ns
External clock							
t_{CHCX}	clock HIGH time	see Figure 19	22	$T_{cy(clk)} - t_{CLCX}$	22	-	ns
t_{CLCX}	clock LOW time	see Figure 19	22	$T_{cy(clk)} - t_{CHCX}$	22	-	ns
t_{CLCH}	clock rise time	see Figure 19	-	5	-	5	ns
t_{CHCL}	clock fall time	see Figure 19	-	5	-	5	ns
Shift register (UART mode 0)							
T_{XLXL}	serial port clock cycle time	see Figure 18	$16T_{cy(clk)}$	-	888	-	ns
t_{QVXH}	output data set-up to clock rising edge time	see Figure 18	$13T_{cy(clk)}$	-	722	-	ns
t_{XHQX}	output data hold after clock rising edge time	see Figure 18	-	$T_{cy(clk)}$ + 20	-	75	ns
t_{XHDX}	input data hold after clock rising edge time	see Figure 18	-	0	-	0	ns
t_{XHDV}	input data valid to clock rising edge time	see Figure 18	150	-	150	-	ns
SPI interface							
f_{SPI}	SPI operating frequency						
	slave		0	$^{CCLK}/_{6}$	0	3.0	MHz
	master		-	$^{CCLK}/_{4}$	-	4.5	MHz
T_{SPICYC}	SPI cycle time	see Figure 20, 21, 22, 23					
	slave		$^{6}/_{CCLK}$	-	333	-	ns
	master		$^{4}/_{CCLK}$	-	222	-	ns

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Table 13. Dynamic characteristics (18 MHz) *…continued*

V_{DD} = 3.0 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 18 MHz		Unit
			Min	Max	Min	Max	
$t_{SPILEAD}$	SPI enable lead time	see Figure 22, 23					
	slave		250	-	250	-	ns
t_{SPILAG}	SPI enable lag time	see Figure 22, 23					
	slave		250	-	250	-	ns
$t_{SPICLKH}$	SPICLK HIGH time	see Figure 20, 21, 22, 23					
	slave		$^{3}/_{CCLK}$	-	167	-	ns
	master		$^{2}/_{CCLK}$	-	111	-	ns
$t_{SPICLKL}$	SPICLK LOW time	see Figure 20, 21, 22, 23					
	slave		$^{3}/_{CCLK}$	-	167	-	ns
	master		$^{2}/_{CCLK}$	-	111	-	ns
t_{SPIDSU}	SPI data set-up time	see Figure 20, 21, 22, 23					
	master or slave		100	-	100	-	ns
t_{SPIDH}	SPI data hold time	see Figure 20, 21, 22, 23					
	master or slave		100	-	100	-	ns
t_{SPIA}	SPI access time	see Figure 22, 23					
	slave		0	80	0	80	ns
t_{SPIDIS}	SPI disable time	see Figure 22, 23					
	slave		0	160	-	160	ns
t_{SPIDV}	SPI enable to output data valid time	see Figure 20, 21, 22, 23					
	slave		-	160	-	160	ns
	master		-	111	-	111	ns
t_{SPIOH}	SPI output data hold time	see Figure 20, 21, 22, 23	0	-	0	-	ns
t_{SPIR}	SPI rise time	see Figure 20, 21, 22, 23					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns
t_{SPIF}	SPI fall time	see Figure 20, 21, 22, 23					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

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11.1 Waveforms

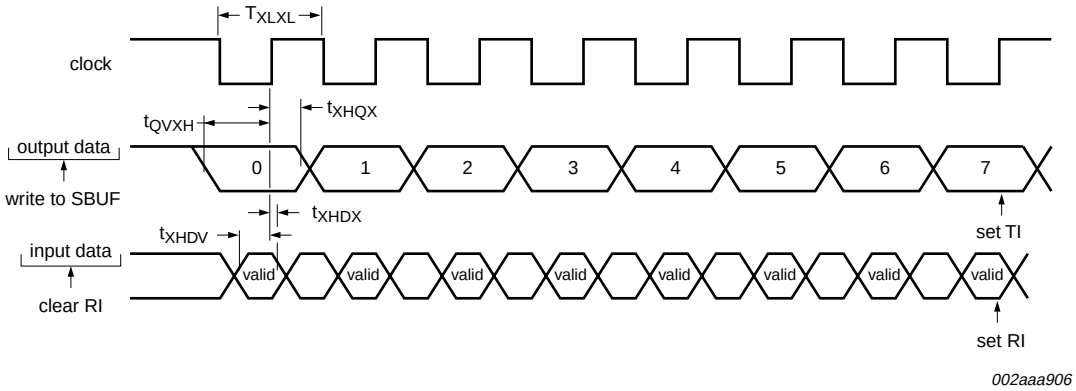


Fig 18. Shift register mode timing

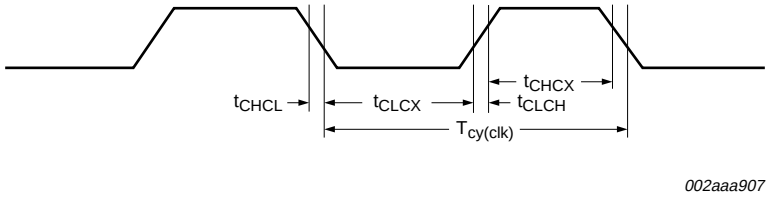


Fig 19. External clock timing

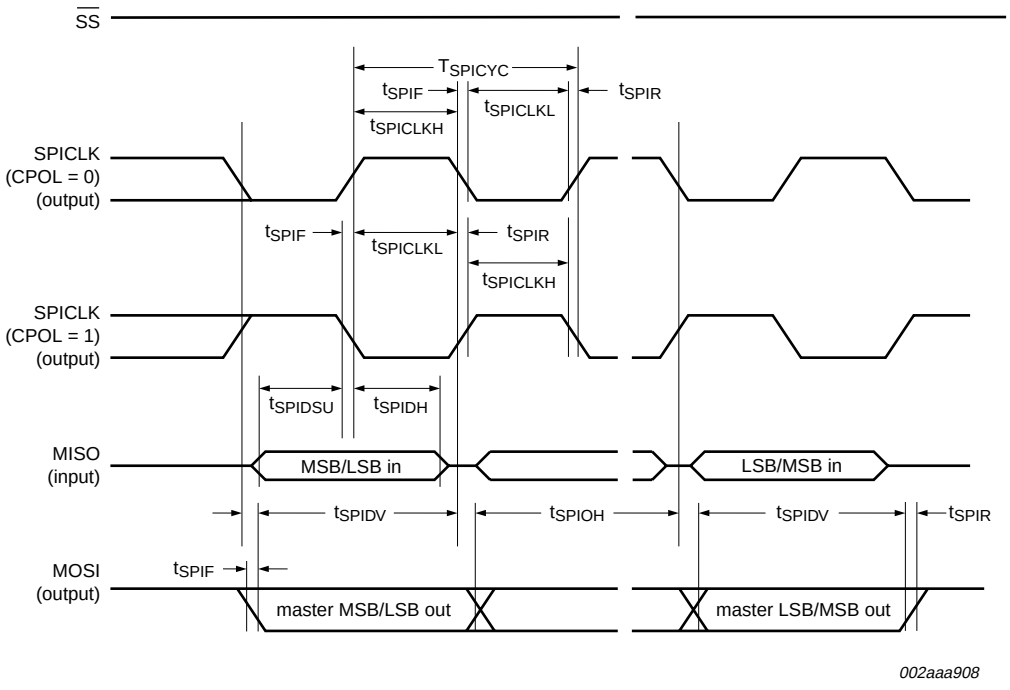


Fig 20. SPI master timing (CPHA = 0)

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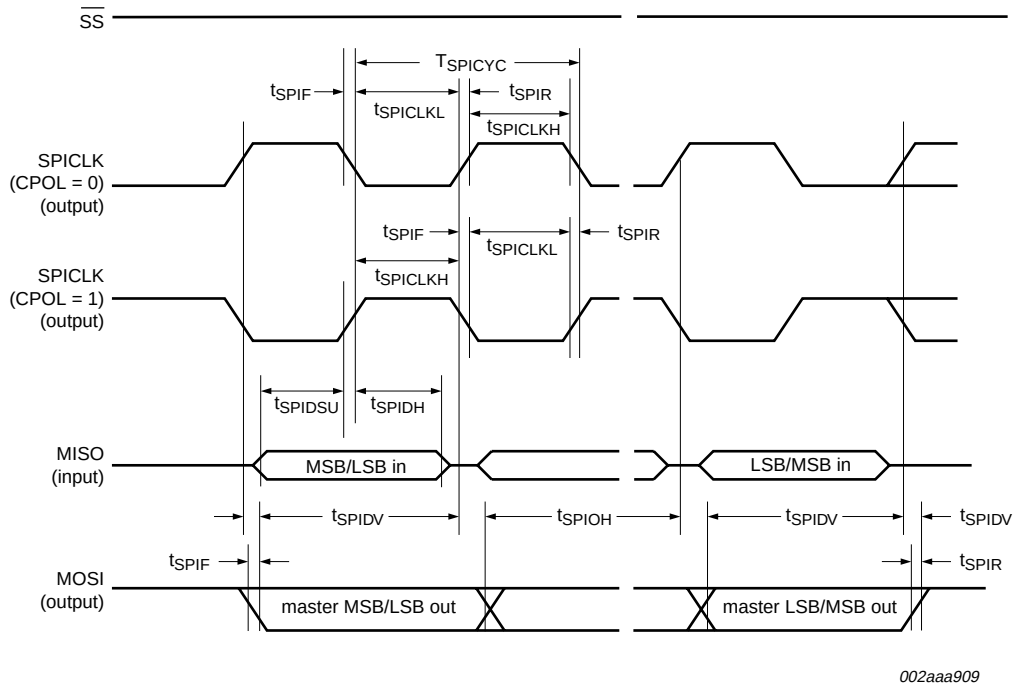


Fig 21. SPI master timing (CPHA = 1)

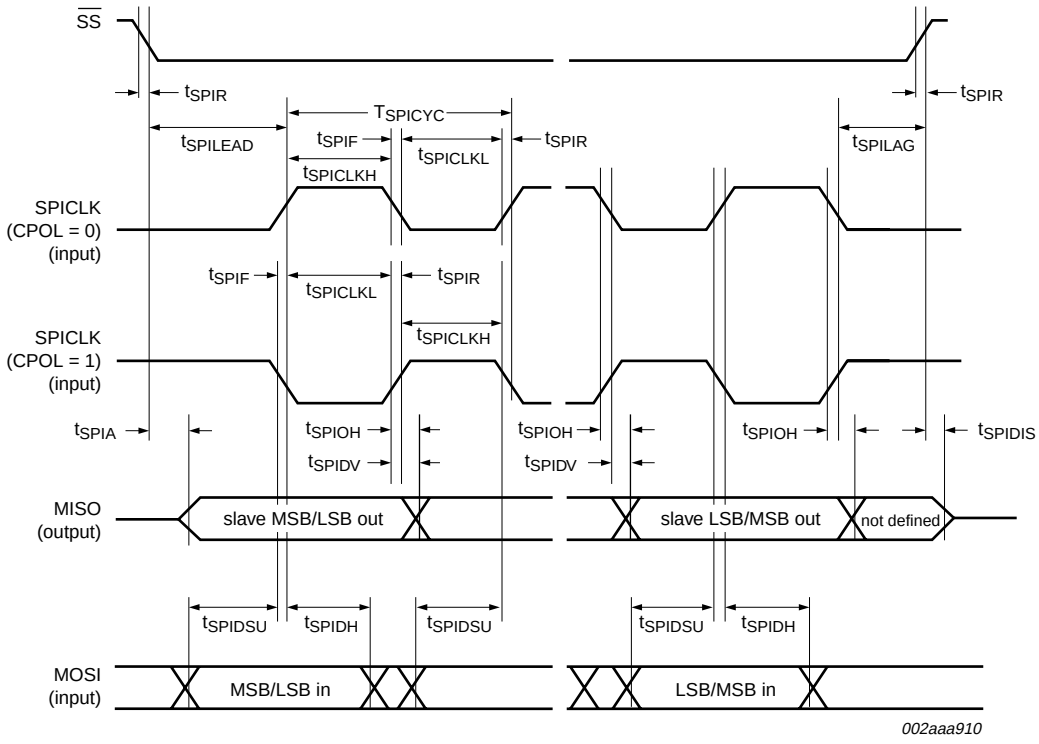


Fig 22. SPI slave timing (CPHA = 0)

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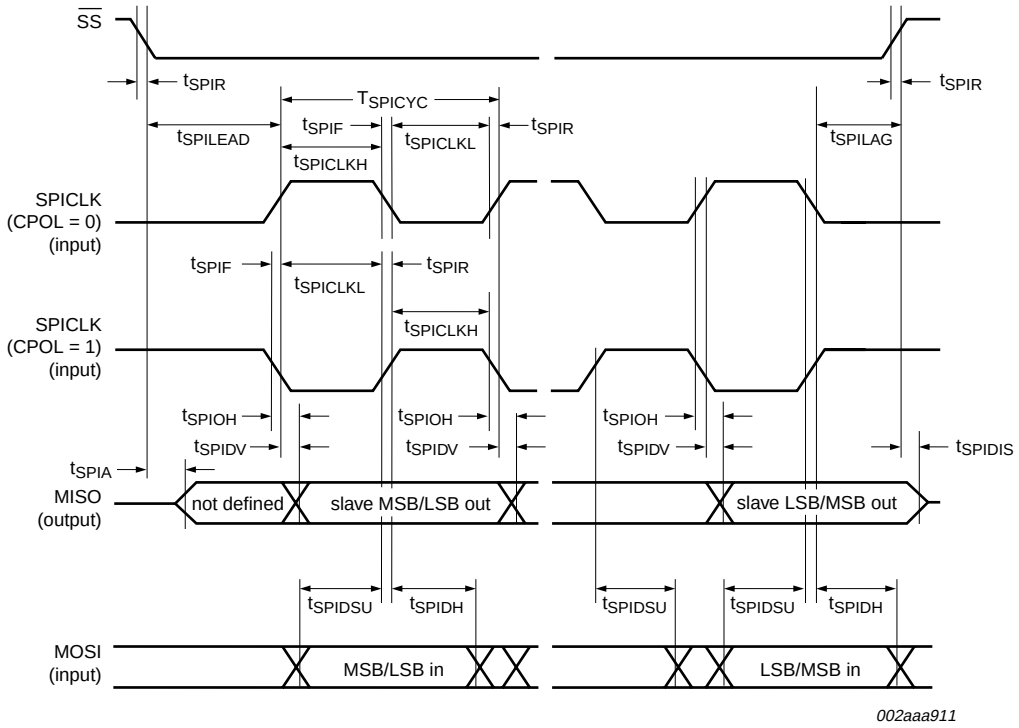


Fig 23. SPI slave timing (CPHA = 1)

11.2 ISP entry mode

Table 14. Dynamic characteristics, ISP entry mode

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VR}	V_{DD} active to $\overline{RST}$ active delay time	pin $\overline{RST}$	50	-	-	µs
t_{RH}	$\overline{RST}$ HIGH time	pin $\overline{RST}$	1	-	32	µs
t_{RL}	$\overline{RST}$ LOW time	pin $\overline{RST}$	1	-	-	µs

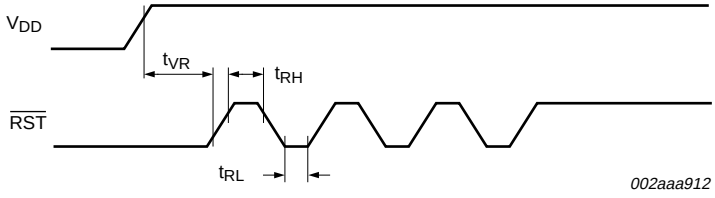


Fig 24. ISP entry waveform

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12. Other characteristics

12.1 Comparator electrical characteristics

Table 15. Comparator electrical characteristics

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IO}	input offset voltage		-	-	±10	mV
V_{IC}	common-mode input voltage		0	-	V_{DD} − 0.3	V
CMRR	common-mode rejection ratio	[1]	-	-	−50	dB
$t_{res(tot)}$	total response time		-	250	500	ns
$t_{(CE-OV)}$	chip enable to output valid time		-	-	10	µs
I_{LI}	input leakage current	0 V < V_I < V_{DD}	-	-	±10	µA

[1] This parameter is characterized, but not tested in production.

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12.2 ADC electrical characteristics

Table 16. ADC electrical characteristics

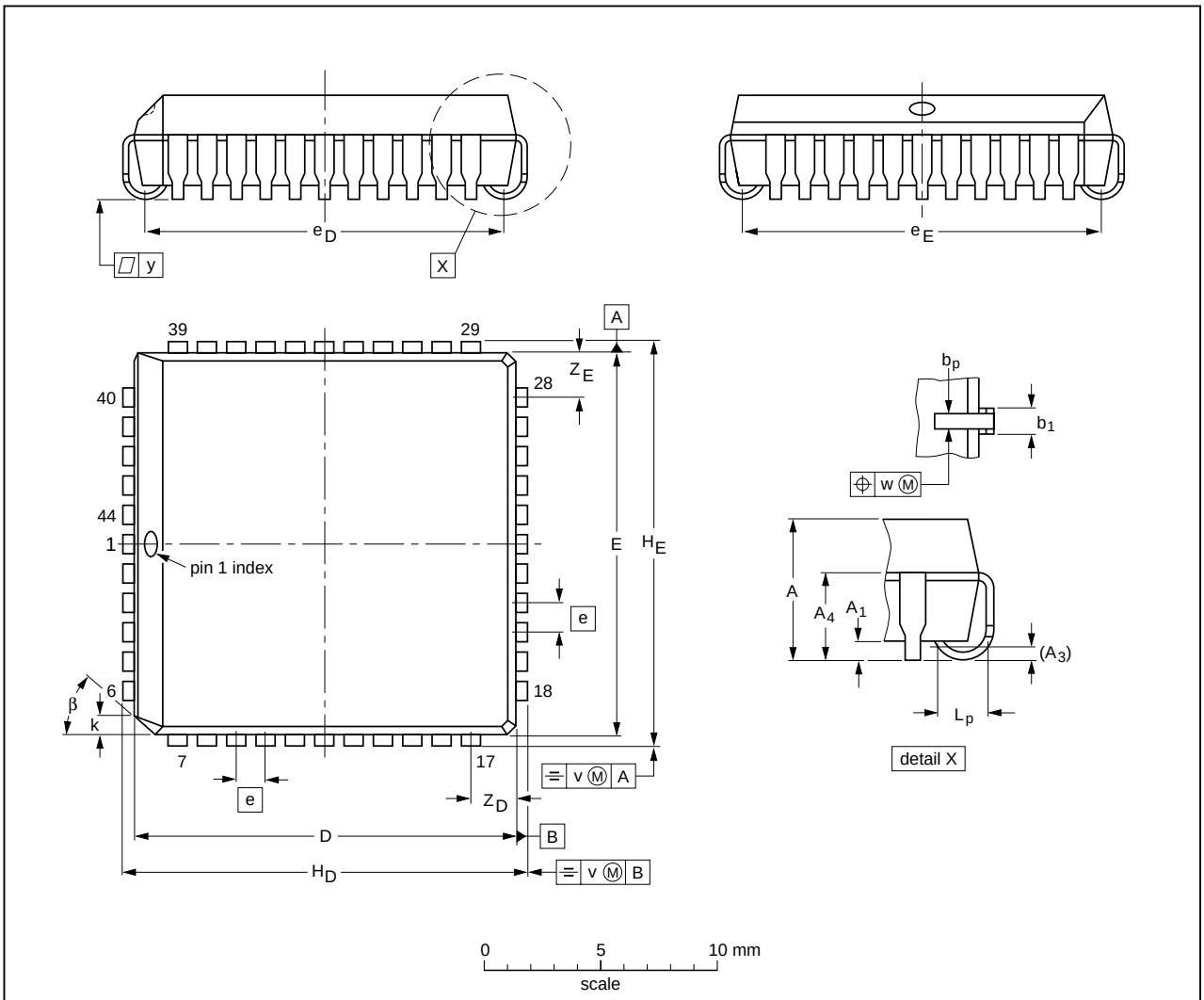
V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.
All limits valid for an external source impedance of less than 10 kΩ.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DDA(ADC)}$	ADC analog supply voltage		V_{DD} − 0.4	-	V_{DD} + 0.4	V
V_{SSA}	analog ground voltage		V_{SS} − 0.4	-	V_{SS} + 0.4	V
V_{VREFP}	voltage on pin VREFP		V_{DD} − 0.4	-	V_{DD} + 0.4	V
V_{VREFN}	voltage on pin VREFN		V_{SS} − 0.4	-	V_{SS} + 0.4	V
V_{IA}	analog input voltage		V_{SS} − 0.4	-	V_{DD} + 0.4	V
C_{ia}	analog input capacitance		-	-	15	pF
E_D	differential linearity error		-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity		-	-	±2	LSB
E_O	offset error		-	-	±2	LSB
E_G	gain error		-	-	±2	LSB
$E_{u(tot)}$	total unadjusted error		-	-	+4/–3	LSB
M_{CTC}	channel-to-channel matching		-	-	±1	LSB
$\alpha_{ct(port)}$	crosstalk between port inputs	0 kHz to 100 kHz	-	-	–60	dB
SR_{in}	input slew rate		-	-	100	V/ms
$T_{cy(ADC)}$	ADC clock cycle time		111	-	3125	ns
t_{ADC}	ADC conversion time	ADC enabled	-	-	$36T_{cy(ADC)}$	µs

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13. Package outline

PLCC44: plastic leaded chip carrier; 44 leads **SOT187-2**



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	1.44 1.02	0.18	0.18	0.1	2.16	2.16	45°
inches	0.180 0.165	0.02	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.63 0.59	0.63 0.59	0.695 0.685	0.695 0.685	0.048 0.042	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

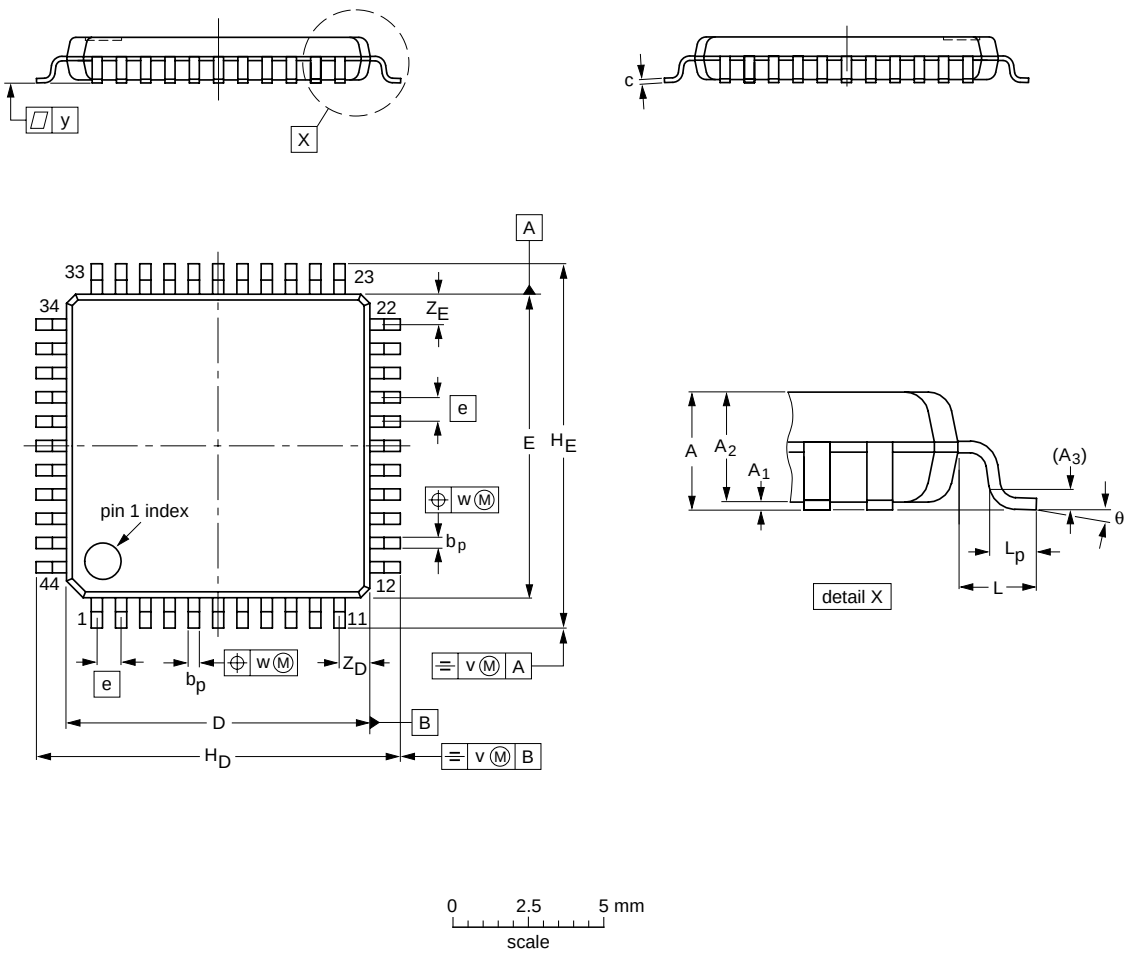
1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT187-2	112E10	MS-018	EDR-7319			~~99-12-27~~ 01-11-14

Fig 25. Package outline SOT187-2 (PLCC44)

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LQFP44: plastic low profile quad flat package; 44 leads; body 10 x 10 x 1.4 mm **SOT389-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.45 0.30	0.20 0.12	10.1 9.9	10.1 9.9	0.8	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.2	0.1	1.14 0.85	1.14 0.85	7^o 0^o

Note

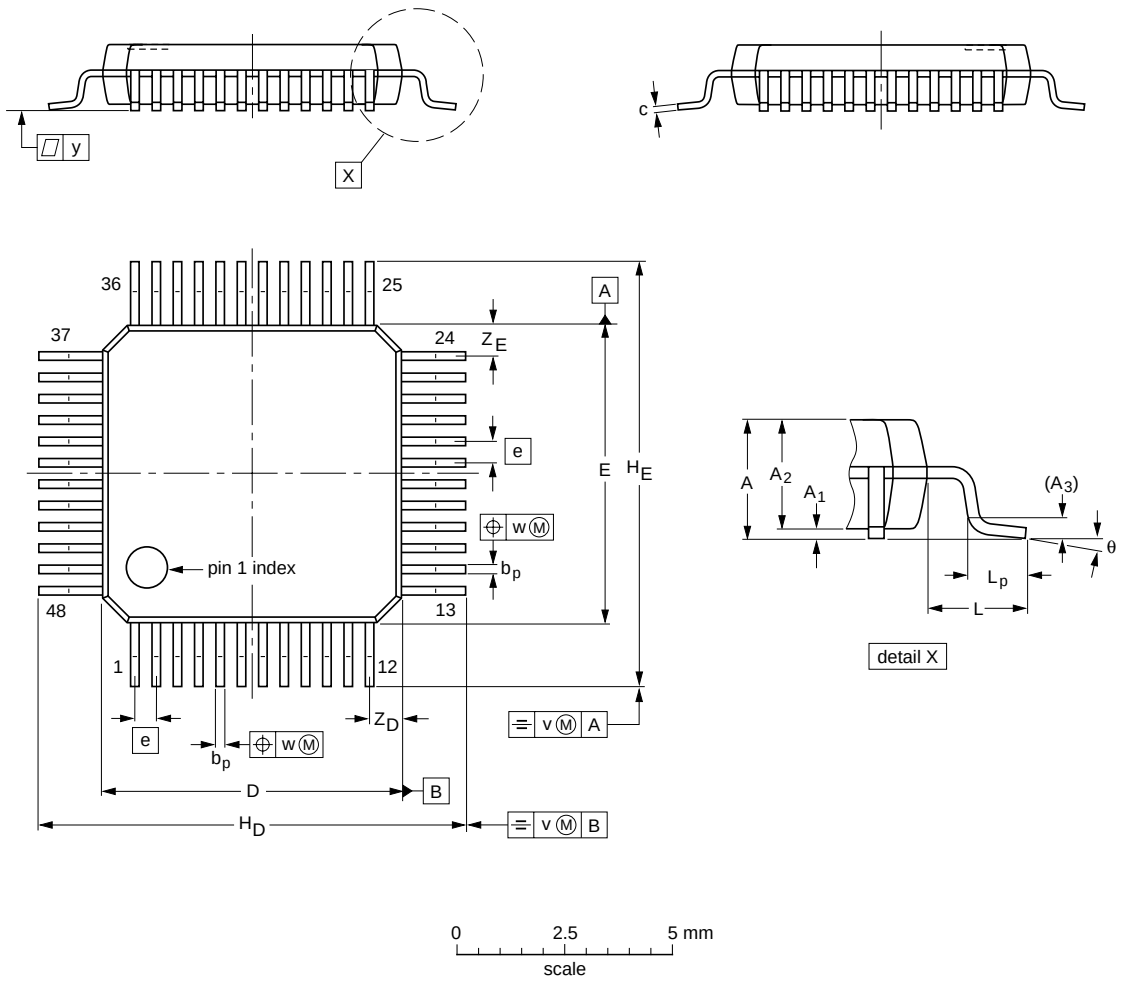
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT389-1	136E08	MS-026				~~00-01-19~~ 02-06-07

Fig 26. Package outline SOT389-1 (LQFP44)

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LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT313-2	136E05	MS-026				~~00-01-19~~ 03-02-25

Fig 27. Package outline SOT313-2 (LQFP48)

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14. Abbreviations

Table 17. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
BOE	BrownOut Enable
CPU	Central Processing Unit
CCU	Capture/Compare Unit
CRC	Cyclic Redundancy Check
DAC	Digital-to-Analog Converter
EPROM	Erasable Programmable Read-Only Memory
EMI	ElectroMagnetic Interference
IAP	In-Application Programming
LSB	Least Significant Bit
MSB	Most Significant Bit
PWM	Pulse Width Modulator
RAM	Random Access Memory
RC	Resistance-Capacitance
RTC	Real-Time Clock
SAR	Successive Approximation Register
SFR	Special Function Register
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter

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15. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
P89LPC952_954_4	20080724	Product data sheet	-	P89LPC952_954_3
Modifications:	• Figure 2 “Functional diagram”: Updated port 2 information.			
P89LPC952_954_3	20080605	Product data sheet	-	P89LPC952_954_2
P89LPC952_954_2	20071219	Preliminary data sheet	-	P89LPC952_1
P89LPC952_1	20050916	Preliminary data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 24 July 2008
Document identifier: P89LPC952_954_4

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