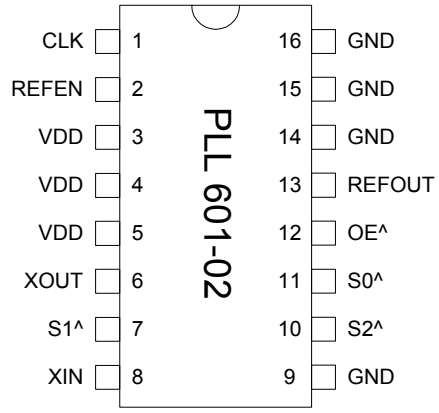
PLL601-02

Low Phase Noise PLL Clock Multiplier

FEATURES

- Low phase noise XO
- Input from crystal or clock at 10-27MHz.
- Integrated crystal load capacitor: no external load capacitor required.
- Output clocks up to 160MHz.
- Low phase noise (-125dBc/Hz @ 1kHz).
- Output Enable function.
- Low jitter (RMS): 6.4ps (period), 9.4ps (accum.)
- Advanced low power sub-micron CMOS process.
- 3.3V operation.
- Available in 16-Pin SOIC or TSSOP.

PIN CONFIGURATION



DESCRIPTION

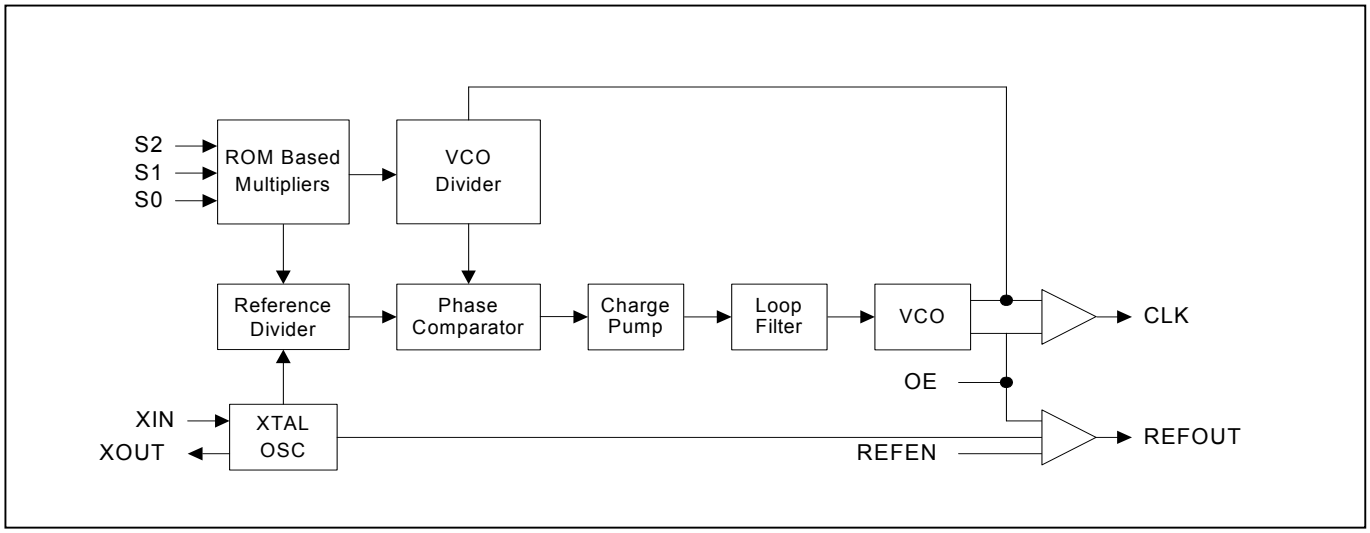
The PLL601-02 is a low cost, high performance and low phase noise clock synthesizer with 4x or 8x multiplier. Using PhaseLink's proprietary analog and digital Phase Locked Loop techniques, this IC can produce up to a 160MHz out put. Ideal for 155.52MHz applications.

MULTIPLIER SELECT TABLE

S2	S1	S0	CLK
0	0	0	Test
0	0	1	Reserved
0	1	0	4x Input (Low Frequency VCO*)
0	1	1	8x Input (Low Frequency VCO*)
1	0	0	Reserved
1	0	1	XO Frequency Pass through
1	1	0	4x Input (High Frequency VCO*)
1	1	1	8x Input (High Frequency VCO*)

*: Low Frequency VCO is advised for best performance at 155.52MHz

BLOCK DIAGRAM



PIN DESCRIPTIONS

Name	Number	Type	Description
CLK	1	O	Clock output from VCO. Equals the input frequency times multiplier.
REFEN	2	I	Reference clock enable. When Low, it disables REFOUT. When High, it enables REFOUT.
VDD	3,4,5	P	Power Supply.
XOUT	6	O	Crystal Connection.
S1	7	I	Multiplier Select Pin 1. Determines CLK output. Has internal pull-up.
XIN	8	I	Crystal input to be connected to 10-27MHz fundamental parallel mode crystal (C_L=15pF). On chip load capacitors: No external capacitor required.
GND	9,14,15,16	P	Ground.
S3	10	I	Multiplier Select Pin 3. Determines CLK output. Has internal pull-up.
S0	11	I	Multiplier Select Pin 0. Determines CLK output. Has internal pull-up.
OE	12	I	Output Enable. Tri-state CLK and REFOUT when low. Has internal pull-up.
REFOUT	13	O	Buffered crystal oscillator clock output. Controlled by REFEN.

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* **Note**: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

2. AC Specifications

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Frequency		10		27	MHz
Output Frequency	At 3.3V			160	MHz
Output Rise Time	0.8V to 2.0V with no load			1.5	ns
Output Fall Time	2.0V to 0.8V with no load			1.5	ns
Duty Cycle	@ 50% V_{DD}	45	50	55	%

3. DC Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operating Voltage	V_{DD}		2.97		3.63	V
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Input High Voltage	V_{IH}	For XIN pin	$(V_{DD}/2) + 1$	$V_{DD}/2$		V
Input Low Voltage	V_{IL}	For XIN pin		$V_{DD}/2$	$(V_{DD}/2) - 1$	V
Output High Voltage	V_{OH}	I_{OH} = -25mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 25mA			0.4	V
Output High Voltage At CMOS Level	V_{OH}	I_{OH} = -8mA	V_{DD}-0.4			V
Operating Supply Current	I_{DD}	No Load		35		mA
Short-circuit Current	I_S			±50		mA
Input Capacitance	C_{IN}	OE, Select Pins		5		pF

4. Crystal Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	F_{XIN}	Parallel Fundamental Mode	10		27	MHz
Crystal Loading Capacitance Rating	$C_{L\ (xtal)}$			15		pF

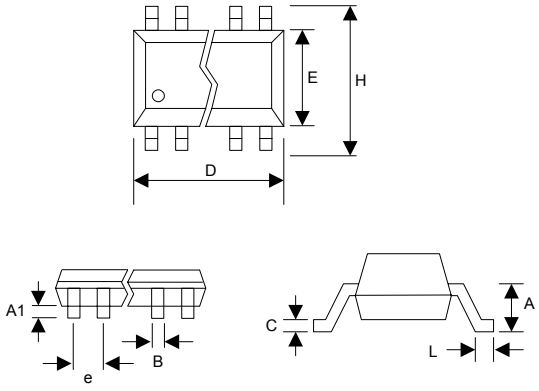
5. Jitter Specifications

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Period jitter RMS	With capacitive decoupling between VDD and GND		6.4		ps
Accumulated jitter RMS	With capacitive decoupling between VDD and GND		9.4		ps
Phase Noise, relative to carrier, 155Mhz(x8)	100Hz offset, 3.3V		-103		dBc/Hz
Phase Noise, relative to carrier, 155Mhz(x8)	1kHz offset, 3.3V		-126		dBc/Hz
Phase Noise, relative to carrier, 155Mhz(x8)	10kHz offset, 3.3V		-133		dBc/Hz
Phase Noise, relative to carrier, 155Mhz(x8)	100kHz offset, 3.3V		-128		dBc/Hz

PACKAGE INFORMATION

16 PIN Narrow SOIC, TSSOP (mm)

	SOIC		TSSOP	
Symbol	Min.	Max.	Min.	Max.
A	1.35	1.75	-	1.20
A1	0.10	0.25	0.05	0.15
B	0.33	0.51	0.19	0.30
C	0.19	0.25	0.09	0.20
D	9.80	10.00	4.90	5.10
E	3.80	4.00	4.30	4.50
H	5.80	6.20	6.40 BSC	
L	0.40	1.27	0.45	0.75
e	1.27 BSC		0.65 BSC	



ORDERING INFORMATION

For part ordering, please contact our Sales Department:
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER
The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range

PLL601-02 S C

PART NUMBER

TEMPERATURE
C=COMMERCIAL
I=INDUSTRAL

PACKAGE TYPE
S=SOIC,
O=TSSOP

Order Number	Marking	Package Option
PLL601-02OC	P601-02OC	16-Pin TSSOP (Tube)
PLL601-02OC-R	P601-02OC	16-Pin TSSOP (Tape & Reel)
PLL601-02SC	P601-02SC	16-Pin SOIC (Tube)
PLL601-02SC-R	P601-02SC	16-Pin SOIC (Tape & Reel)

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