## 320-640MHz Low Phase Noise VCXO

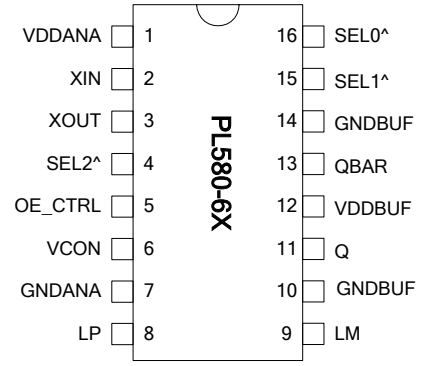
### FEATURES

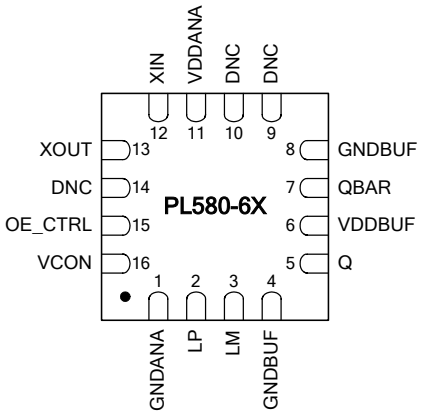
- Less than 0.4ps RMS (12KHz-20MHz) phase jitter for all frequencies.
- Low phase noise output (@ 1MHz frequency offset
  - * -140dBc/Hz for 320.0MHz,
  - * -131dBC/Hz for 622.08MHz
- 20MHz-40MHz crystal input.
- 320MHz-640MHz output.
- Available in PECL, or LVDS outputs.
- No external varicap required.
- Output Enable selector.
- Wide pull range (+/-200ppm).
- 3.3V operation.
- Available in 3x3 QFN or 16-pin TSSOP packages.

### DESCRIPTION

The PL580-6X is a monolithic low jitter and low phase noise VCXO, capable of 0.4ps RMS phase jitter and PECL or LVDS outputs, covering a wide frequency output range up to 640MHz. It allows the control of the output frequency with an input voltage (VCON), using a low cost crystal.
The PL580-6X is designed to address the demanding requirements of high performance applications such as SONET, GPS, Video, etc.

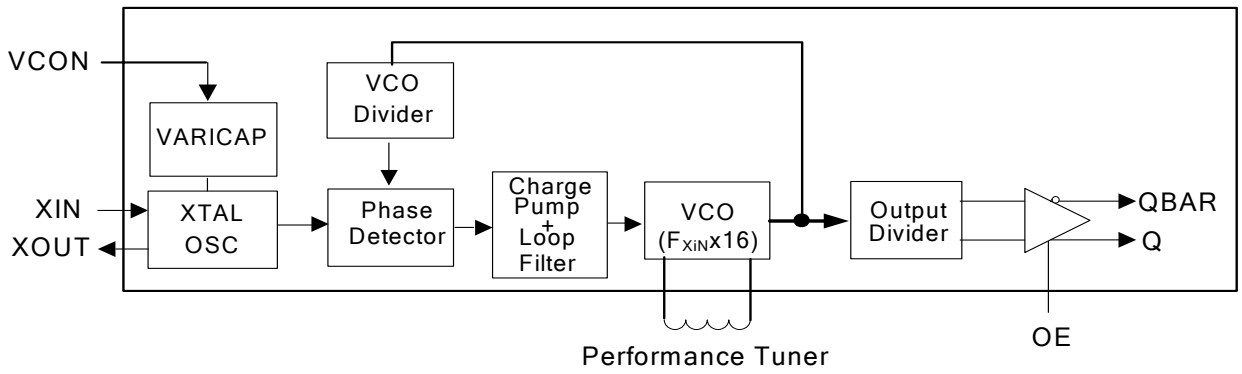
### PACKAGE PIN ASSIGNMENT




Note1: ^ Denotes internal pull up resistor.

### BLOCK DIAGRAM



## OUTPUT ENABLE LOGICAL LEVELS

| Part # | OE | State |
|---|---|---|
| PLL580-68 (PECL) | 0 (Default) | Output enabled |
| | 1 | Tri-state |
| PLL580-69 (LVDS) | 0 | Tri-state |
| | 1 (Default) | Output enabled |

## PIN DESCRIPTIONS

| Name | TSSOP Pin number | 3x3mm QFN Pin number | Type | Description |
|---|---|---|---|---|
| VDDANA | 1 | 11 | P | VDD for analog Circuitry. |
| XIN | 2 | 12 | I | Crystal input pin. (See Crystal Specifications on page 4). |
| XOUT | 3 | 13 | O | Crystal output pin. (See Crystal Specifications on page 4). |
| DNC | 4 | 14 | - | Do Not Connect |
| OE_CTRL | 5 | 15 | I | Output enable control pin. (See OE_CTRL Logic Levels above). |
| VCON | 6 | 16 | I | Voltage control input. |
| GNDANA | 7 | 1 | P | Ground for analog circuitry. |
| LP | 8 | 2 | - | Tuning inductor connection. The inductor is recommended to be a high Q small size 0402 or 0603 SMD component, and must be placed between LP and adjacent LM pin. Place inductor as close to the IC as possible to minimize parasitic effects and to maintain inductor Q. |
| LM | 9 | 3 | - | |
| GNDBUF | 10 | 4 | P | GND connection for output buffer circuitry. |
| Q | 11 | 5 | O | PECL or LVDS output. |
| VDDBUF | 12 | 6 | P | VDD connection for output buffer circuitry. VDDBUF should be separately decoupled from other VDDs whenever possible. |
| QBAR | 13 | 7 | O | Complementary PECL, LVDS output. |
| GNDBUF | 14 | 8 | P | GND connection for output buffer circuitry. |
| DNC | 15 | 9 | - | Do Not Connect |
| DNC | 16 | 10 | - | Do Not Connect |

## FREQUENCY SELECTION TABLE

| SEL2 | SEL1 | SEL0 | Selected Multiplier/Output Frequency |
|---|---|---|---|
| 0 | 0 | 0 | VCO Max* |
| 0 | 0 | 1 | VCO Min* |
| 1 | 1 | 1 | Fin x 16 |
| All Other Combinations | | | Reserved |

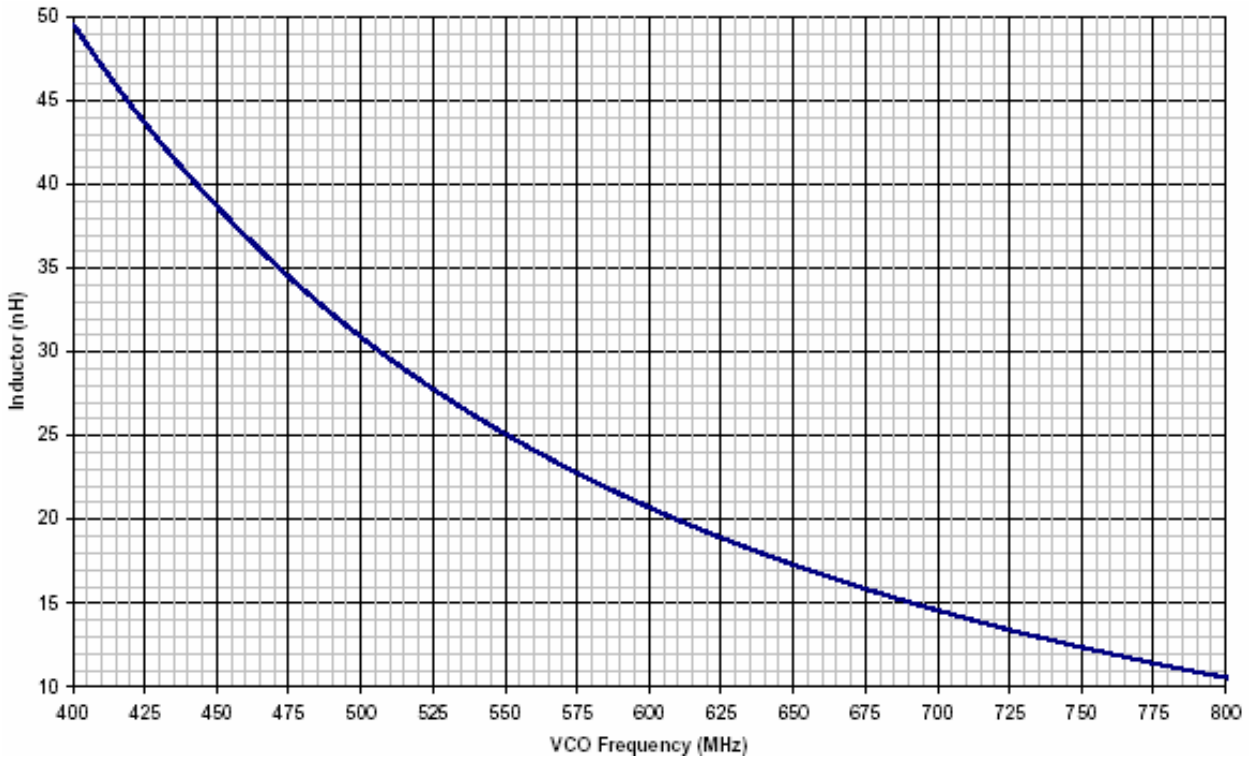
All SEL pads have internal pull-ups (default value is '1'). Bond to GND to set to 0.

* Special Test Modes to help selecting the inductor value for the target output frequency.

## PERFORMANCE TUNING & INDUCTOR VALUE SELECTION

Please refer to PhaseLink's 'PhasorV Tuning Assistance' software to automatically calculate the optimum inductor values for your application. In addition, the chart below could be used as a reference for quick inductor value selection. Please note that the inductor values mentioned in the table below, or when using 'PhasorV Tuning Assistance' are derived based on the parasitic values of PhaseLink's evaluation board. For performance enhancement of your custom board design, please follow the following instruction:

Use the special test modes "VCO Max" and "VCO Min" to determine the optimum inductor value. "VCO Max" represents the high end of the VCO range and "VCO Min" represents the low end of the VCO range. The output frequency in the "VCO Max" and "VCO Min" test modes is VCO/16. This means that the output frequencies are around the crystal frequency that will be used. The optimum inductor value is where the target crystal frequency is closest to the middle between the "VCO Max" and "VCO Min" output frequencies. In this case the VCO will lock in the middle of its tuning range with maximum margin on either side.



## ELECTRICAL SPECIFICATIONS

### 1. Absolute Maximum Ratings

| PARAMETERS | SYMBOL | MIN. | MAX. | UNITS |
|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | | 4.6 | V |
| Input Voltage, dc | $V_I$ | -0.5 | $V_{DD}$+0.5 | V |
| Output Voltage, dc | $V_O$ | -0.5 | $V_{DD}$+0.5 | V |
| Storage Temperature | $T_S$ | -65 | 150 | °C |
| Ambient Operating Temperature* | $T_A$ | -40 | 85 | °C |
| Junction Temperature | $T_J$ | | 125 | °C |
| Lead Temperature (soldering, 10s) | | | 260 | °C |
| ESD Protection, Human Body Model | | | 2 | kV |

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* **Note**: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

### 2. Crystal Specifications

| PARAMETERS | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| Crystal Resonator Frequency | $F_{XIN}$ | Parallel Fundamental Mode | 20 | | 40 | MHz |
| Crystal Loading Rating | $C_{L\ (xtal)}$ | at VCON = 0V | | 17.7 | | pF |
| | | at VCON = 1.65V | | 9.5 | | |
| | | at VCON = 3.3V | | 5.4 | | |
| Crystal Pullability | $C_0/C_{1\ (xtal)}$ | AT cut | | | 250 | - |
| Recommended ESR | $R_E$ | AT cut | | | 30 | Ω |

**Note**: Crystal Loading rating: The listed numbers are for the IC only. Specify the crystal for the value at VCON = 1.65V and add the PCB & package parasitic. A round number (i.e. 12pF) can be achieved by adding external capacitors. Try to add the same value to XIN and XOUT, and please note, that frequency pulling and oscillator gain may decrease.

### 3. Voltage Control Crystal Oscillator

| PARAMETERS | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| VCXO Stabilization Time * | $T_{VCXOSTB}$ | From power valid | | | 10 | ms |
| VCXO Tuning Range | | $F_{XIN}$ = 20 – 40MHz;<br>XTAL $C_0/C_1$ < 250<br>0V ≤ VCON ≤ 3.3V | | 500 | | ppm |
| CLK output pullability | | VCON=1.65V, ±1.65V | ±200 | | | ppm |
| VCXO Tuning Characteristic | | | | 150 | | ppm/V |
| Pull range linearity | | | | | 10 | % |
| VCON pin input impedance | | | 60 | | | kΩ |
| VCON modulation BW | | 0V ≤ VCON ≤ 3.3V, -3dB | 25 | | | kHz |

**Note:** Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits.

## 4. General Electrical Specifications

| PARAMETERS | SYMBOL | CONDITIONS | | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|---|
| Supply Current, Dynamic (with Loaded Outputs) | $I_{DD}$ | PECL/LVDS | 320MHz<Fout<640MHz | | | 90/70 | mA |
| Operating Voltage | $V_{DD}$ | | | 2.97 | | 3.63 | V |
| Output Clock Duty Cycle | | @ 50% $V_{DD}$ (CMOS)<br>@ 1.25V (LVDS)<br>@ $V_{DD}$ – 1.3V (PECL) | | 45<br>45<br>45 | 50<br>50<br>50 | 55<br>55<br>55 | % |
| Short Circuit Current | | | | | ±50 | | mA |

## 5. Jitter Specifications

| PARAMETERS | CONDITIONS | FREQUENCY | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| Integrated jitter RMS | Integrated 12 kHz to 20 MHz | 320.0MHz | | 0.4 | 0.5 | ps |
| | | 622.08MHz | | 0.4 | 0.6 | |
| Period jitter RMS | With capacitive decoupling between VDD and GND. Over 10,000 cycles. | 320.0MHz | | 3 | 5 | ps |
| | | 622.08MHz | | 6 | 8 | |
| Period jitter Peak-to-Peak | With capacitive decoupling between VDD and GND. Over 10,000 cycles. | 320.0MHz | | 25 | 30 | ps |
| | | 622.08MHz | | 40 | 50 | |

## 6. Phase Noise Specifications

| PARAMETERS | FREQ. | @10Hz | @100Hz | @1kHz | @10kHz | @100kHz | @1M | @10M | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| Phase Noise[2] relative to carrier (typical) | 320.0MHz | -59 | -86 | -116 | -129 | -124 | -140 | -148 | dBc/Hz |
| | 622.08MHz | -48 | -80 | -108 | -118 | -114 | -131 | -138 | |

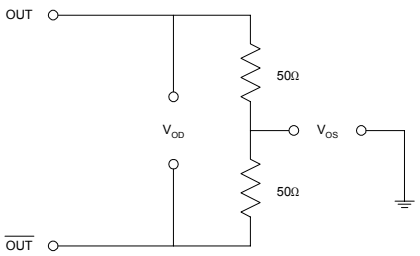
## 8. LVDS Electrical Characteristics

| PARAMETERS | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| Output Differential Voltage | $V_{OD}$ | $R_L$ = 100 Ω (see figure) | 247 | 355 | 454 | mV |
| $V_{DD}$ Magnitude Change | $\Delta V_{OD}$ | | -50 | | 50 | mV |
| Output High Voltage | $V_{OH}$ | | | 1.4 | 1.6 | V |
| Output Low Voltage | $V_{OL}$ | | 0.9 | 1.1 | | V |
| Offset Voltage | $V_{OS}$ | | 1.125 | 1.2 | 1.375 | V |
| Offset Magnitude Change | $\Delta V_{OS}$ | | 0 | 3 | 25 | mV |
| Power-off Leakage | $I_{OXD}$ | $V_{out}$ = $V_{DD}$ or GND, $V_{DD}$ = 0V | | ±1 | ±10 | uA |
| Output Short Circuit Current | $I_{OSD}$ | | | -5.7 | -8 | mA |

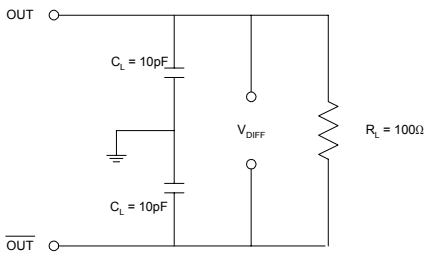
## 9. LVDS Switching Characteristics

| PARAMETERS | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| Differential Clock Rise Time | $t_r$ | $R_L$ = 100 Ω, $C_L$ = 10 pF (see figure) | 0.2 | 0.7 | 1.0 | ns |
| Differential Clock Fall Time | $t_f$ | | 0.2 | 0.7 | 1.0 | ns |

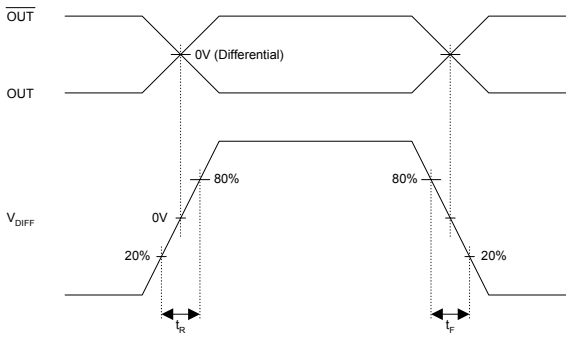
LVDS Levels Test Circuit




LVDS Switching Test Circuit




LVDS Transistion Time Waveform



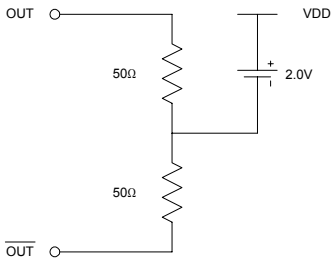
## 10. PECL Electrical Characteristics

| PARAMETERS | SYMBOL | CONDITIONS | MIN. | MAX. | UNITS |
|---|---|---|---|---|---|
| Output High Voltage | $V_{OH}$ | $R_L$ = 50 Ω to ($V_{DD}$ – 2V) (see figure) | $V_{DD}$ – 1.025 | | V |
| Output Low Voltage | $V_{OL}$ | | | $V_{DD}$ – 1.620 | V |

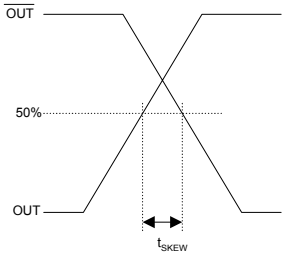
## 11. PECL Switching Characteristics

| PARAMETERS | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| Clock Rise Time | $t_r$ | @20/80% - PECL | 0.2 | 0.3 | 0.45 | ns |
| Clock Fall Time | $t_f$ | @80/20% - PECL | 0.2 | 0.3 | 0.45 | ns |

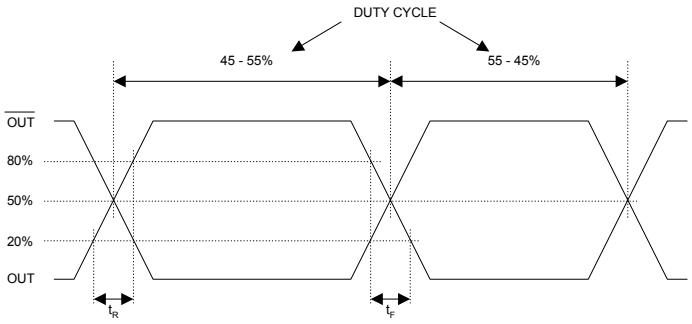
PECL Levels Test Circuit



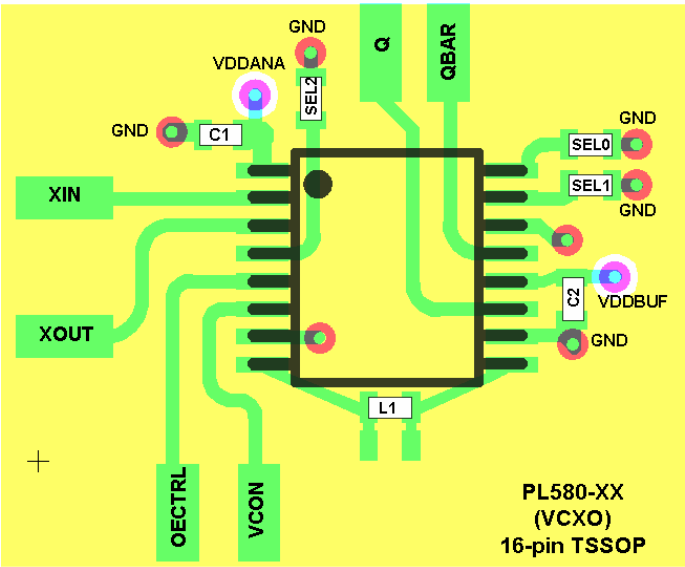

PECL Output Skew

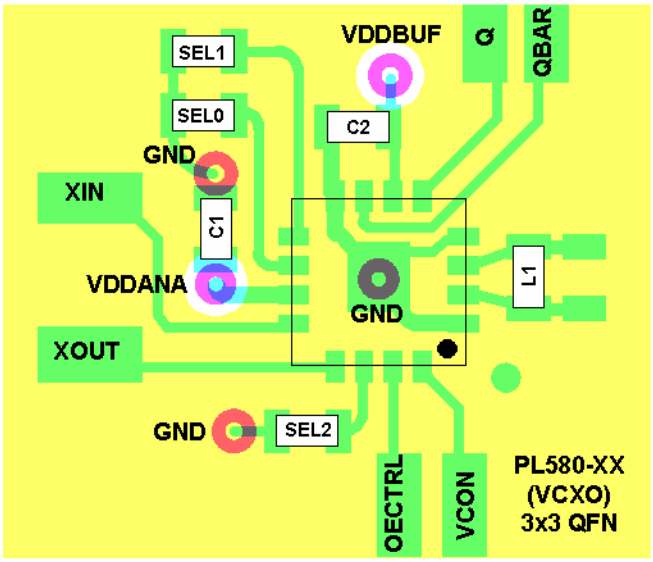



PECL Transistion Time Waveform



## LAYOUT RECOMMENDATIONS




## PCB LAYOUT CONSIDERATIONS FOR PERFORMANCE OPTIMIZATION

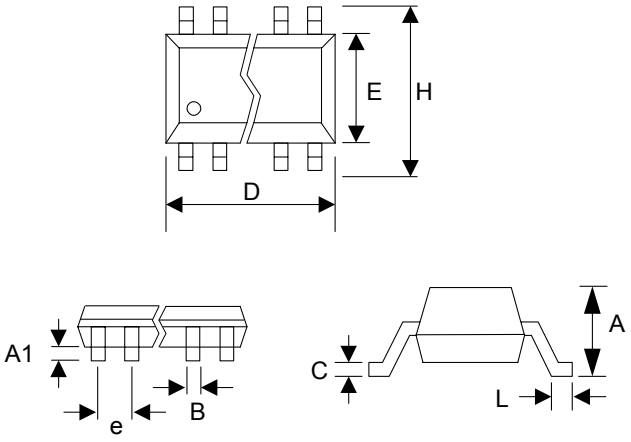
The following guidelines are to assist you with a performance optimized PCB design:

- Keep all the PCB traces to PL580 as short as possible, as well as keeping all other traces as far away from it as possible.
- Place the crystal as close as possible to both crystal pins of the device. This will reduce the cross-talk between the crystal and the other signals.
- Separate crystal pin traces from the other signals on the PCB, but allow ample distance between the two crystal pin traces.
- Place a 0.01µF~0.1µF decoupling capacitor between VDD and GND, on the component side of the PCB, close to the VDD pin. It is not recommended to place this component on the backside of the PCB. Going through vias will reduce the signal integrity, causing additional jitter and phase noise.
- It is highly recommended to keep the VDD and GND traces as short as possible.
- Please contact PhaseLink for the application note on how to design outputs driving long traces or the Gerber files for the PL580 layout.

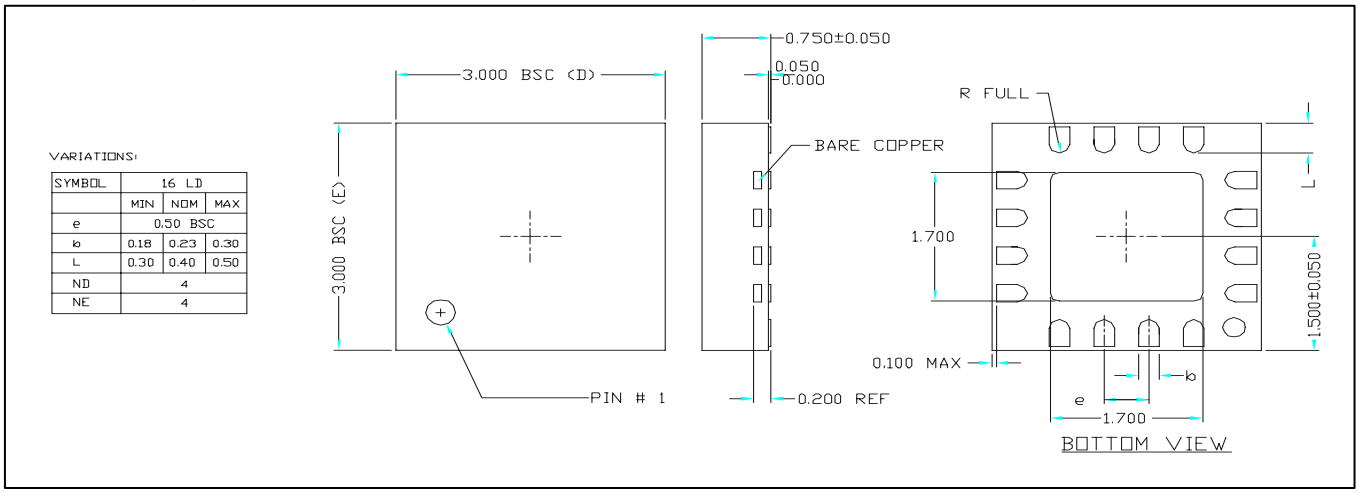
## PACKAGE INFORMATION

### 16-PIN SSOP

| 16 PIN TSSOP ( mm ) | | |
|---|---|---|
| Symbol | Min. | Max. |
| A | - | 1.20 |
| A1 | 0.05 | 0.15 |
| B | 0.19 | 0.30 |
| C | 0.09 | 0.20 |
| D | 4.90 | 5.10 |
| E | 4.30 | 4.50 |
| H | 6.40 BSC | |
| L | 0.45 | 0.75 |
| e | 0.65 BSC | |



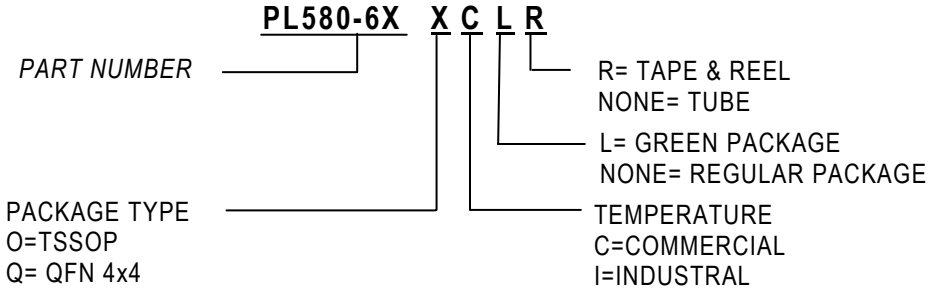

### 16-PIN 3x3 QFN



## ORDERING INFORMATION

***For part ordering, please contact our Sales Department:***
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

***PART NUMBER***
The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range




| Order Number | Marking | Package Option |
|---|---|---|
| PL580-68OC | P580-68OC | TSSOP - Tube |
| PL580-68OC-R | P580-68OC | TSSOP - Tape & Reel |
| PL580-68OCL | P580-68OCL | TSSOP - Tube (GREEN Package) |
| PL580-68OCL-R | P580-68OCL | TSSOP - Tape & Reel (GREEN Package) |
| PL580-68QC | P580-68QC | QFN - Tube |
| PL580-68QC-R | P580-68QC | QFN - Tape & Reel |
| PL580-68QCL | P580-68QCL | QFN - Tube (GREEN Package) |
| PL580-68QCL-R | P580-68QCL | QFN - Tape & Reel (GREEN Package) |
| PL580-69OC | P580-69OC | TSSOP - Tube |
| PL580-69OC-R | P580-69OC | TSSOP - Tape & Reel |
| PL580-69OCL | P580-69OCL | TSSOP - Tube (GREEN Package) |
| PL580-69OCL-R | P580-69OCL | TSSOP - Tape & Reel (GREEN Package) |
| PL580-69QC | P580-69QC | QFN - Tube |
| PL580-69QC-R | P580-69QC | QFN - Tape & Reel |
| PL580-69QCL | P580-69QCL | QFN - Tube (GREEN Package) |
| PL580-69QCL-R | P580-69QCL | QFN - Tape & Reel (GREEN Package) |

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