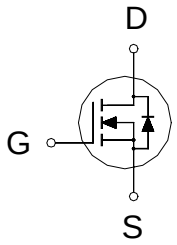
NIKO-SEM

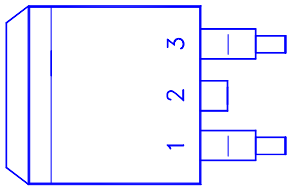
N-Channel Logic Level Enhancement Mode Field Effect Transistor

P50N02LS
TO-263 (D^2PAK)

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
25	12mΩ	55A





1. GATE
2. DRAIN
3. SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25 °C	I_D	55	A
	T_C = 100 °C		38	
Pulsed Drain Current[1]		I_{DM}	150	
Avalanche Current		I_{AR}	36	
Avalanche Energy	L = 0.1mH	E_{AS}	250	mJ
Repetitive Avalanche Energy[2]	L = 0.05mH	E_{AR}	8.6	
Power Dissipation	T_C = 25 °C	P_D	85	W
	T_C = 100 °C		46	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	275	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta JC}$		2.3	°C / W
Junction-to-Ambient	$R_{\theta JA}$		62.5	
Case-to-Heatsink	$R_{\theta CS}$	0.6		

[1]Pulse width limited by maximum junction temperature.
[2]Duty cycle ≤ 1%

ELECTRICAL CHARACTERISTICS (T_C = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250µA	25			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250µA	0.8	1.2	2.5	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±250	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20V, V_{GS} = 0V			25	µA
		V_{DS} = 20V, V_{GS} = 0V, T_C = 125 °C			250	

On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10V, V_{GS} = 10V	55			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 7V, I_D = 20A		13	16	mΩ
		V_{GS} = 10V, I_D = 30A		12	15	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15V, I_D = 40A		16		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 15V, f = 1MHz		1400		pF
Output Capacitance	C_{oss}			380		
Reverse Transfer Capacitance	C_{rss}			200		
Total Gate Charge[2]	Q_g	V_{DS} = 0.5$V_{(BR)DSS}$, V_{GS} = 10V, I_D = 30A		40		nC
Gate-Source Charge[2]	Q_{gs}			12		
Gate-Drain Charge[2]	Q_{gd}			25		
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DS} = 15V, R_L = 1Ω, I_D ≅ 35A, V_{GS} = 10V, R_{GS} = 2.5Ω		9		nS
Rise Time[2]	t_r			150		
Turn-Off Delay Time[2]	$t_{d(off)}$			20		
Fall Time[2]	t_f			30		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				55	A
Pulsed Current[3]	I_{SM}				170	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V			1.3	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100A / µS		70		nS
Peak Reverse Recovery Current	$I_{RM(REC)}$			200		A
Reverse Recovery Charge	Q_{rr}			0.043		µC

[1]Pulse test : Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature.

REMARK: THE PRODUCT MARKED WITH "P50N02LS", DATE CODE or LOT #

TO-263 (D^2PAK) MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	14.5	15	15.8	H	1.0	1.5	1.8
B	4.2		4.7	I	9.8		10.3
C	1.20		1.35	J		6.5	
D		2.8		K		1.5	
E	0.3	0.4	0.5	L	0.7		1.4
F	-0.102		0.203	M	4.83	5.08	5.33
G	8.5	9	9.5	N			

