

QorIQ Communications Platforms

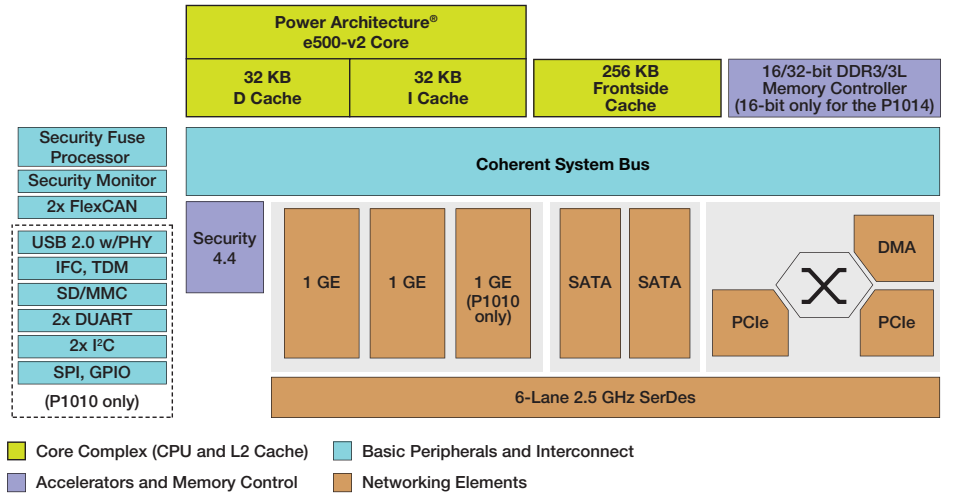
QorIQ P1010 and P1014 Communications Processors

BUILT ON Power

Target Markets and Applications

- Wireless LAN access points (802.11ac/802.11n)
- SOHO/SMB routers
- Controller for Ethernet switches
- Network attached storage
- Video surveillance
- Factory automation and industrial control

QorIQ P1010 and P1014 Processor Block Diagram



Overview

The QorIQ P1010 and P1014 processors are members of the value-perfomance tier, offering extensive integration and extreme power intelligence for a wide variety of applications in cost-sensitive networking, network attached storage, digital video surveillance and industrial segments. Based on 45 nm technology for low-power implementation, the P1010 and P1014 processors provide a single-core, low-power solution for the 533 to 1000 MHz performance range, along with a trusted security platform and a rich set of interfaces.

Secure Boot

The secure boot feature ensures that the processors only run authenticated code. Through a set of fuses that OEMs can program once but can never be read, secure boot prevents unauthorized parties from reverse engineering code to steal intellectual property, from loading illegitimate code to change system functionality or from extracting sensitive user information that may be stored in the system.

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Security Engine

The QorIQ security engine (SEC) is optimized to handle all the algorithms associated with IPSec, IEEE Std. 802.11i™ standard, and iSCSI. The security engine also supports booting to a known good state, untamperable boot code, key storage, I/O protection, and secure debug.

The SEC is a modular and scalable security core optimized to process all the algorithms associated with IPsec, IKE, SSL/TLS, iSCSI, SRTP, IEEE Std. 802.11i™, IEEE Std. 802.16™ (WiMAX), and IEEE Std. 802.1AE (MACSec). The SEC is designed to perform multi-algorithmic operations (for example, 3DES-HMAC-SHA-1) in a single pass of the data. The security coprocessor in the QorIQ P1010 processor is capable of performing single-pass security cryptographic processing for SSL 3.0, SSL 3.1/TLS 1.0, IPSec, SRTP, and IEEE Std. 802.11i.

SEC Features

- XOR engine for parity checking in RAID storage applications
- Four crypto-channels, each supporting multi-command descriptor chains

Cryptographic Execution Units:

- PKHA (public key hardware accelerator)
- DESA (DES accelerator)
- AESA (AES accelerator)
- MDHA (message digest hardware accelerator)
- RNG (random number generator)
- AFHA (ARC four hardware accelerator)
- STHA (SNOW 3G f8 and f9 hardware accelerators)
- CRCA (cyclic redundancy check accelerator)
- KFHA (Kasumi hardware accelerator)

Dual FlexCAN controllers

Two FlexCAN (revision 2.0B) controllers provide a standard interface for implementing industrial protocols. Each FlexCAN controller has the following features:

- Programmable bit rates up to 1 Mb/s
- Standard data and remote frames
- Extended data and remote frames
- Up to eight bytes data length
- Up to 64 message buffers (MB), each configurable as Rx or Tx
- Individual Rx mask registers per message buffers
- Rx FIFO with storage capacity of six frames and internal pointer handling
- Rx FIFO ID filtering
- Time stamp based on 16-bit free running timer

Technical Specifications

- Single e500 core, built on Power Architecture® technology
  - 36-bit physical addressing
  - Double-precision floating-point support
  - 32 KB L1 instruction cache and 32 KB L1 data cache
  - 533 MHz to 800 MHz core clock frequency
- 256 KB L2 cache with ECC, also configurable as SRAM and stashing memory
- Three 10/100/1000 Mb/s enhanced three-speed Ethernet controllers (eTSECs)
  - TCP/IP acceleration and classification capabilities
  - IEEE® 1588 support
  - Lossless flow control
  - RGMII, SGMII
- High-speed interfaces (not all available simultaneously)
  - Six SerDes to 3.125 GHz multiplexed across controllers
  - Two PCI Express controllers
  - Two SGMII interfaces
  - Two SATA interfaces
- One USB controller (USB 2.0) with integrated PHY, host, OTG and device support
- Serial peripheral interface
- Trusted boot platform, integrated security engine (SEC 4.0)
  - Crypto algorithm support includes 3DES, AES, RSA/ECC, MD5/SHA, ARC4, Snow 3G and FIPS deterministic RNG
  - Single pass encryption/message authentication for common security protocols (IPsec, SSL, SRTP, WiMAX)
  - XOR acceleration
- 16/32-bit DDR3/DDR3L SDRAM memory controller with ECC support
- Four-channel DMA controller
- Two I^2C controllers, two DUARTs, timers
- Integrated flash controller with enhanced capabilities to support large pages
- 32 general-purpose I/O signals
- Package: 425-pin TEPBGA1, 0.8 mm pitch, 19 mm x 19 mm

Software and Tools Support

- Enea®: Real-time operating system support
- Green Hills®: Complete portfolio of software and hardware development tools, trace tools and real-time operating systems
- Mentor Graphics®: Commercial grade Linux® solution
- P1010 reference design board (RDB)

QorIQ P1010 and P1014 Comparison

QorIQ Device	Top Core Frequency	L2 Size	DDR 3 Support	GE Ports	SATA	PCI Express®	Security	CAN
P1010	1000 MHz	256 KB	16/32-bit @ 800 MHz	3	2	2	Trusted	2
P1014	800 MHz	256 KB	16-bit @ 800 MHz	2	2	2	No	No

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