OPT9221 Time-of-Flight Controller

1 Features

- QVGA 3D ToF Controller: Up to 120 FPS
- Depth Data:
  - 12-Bit Phase
  - Up to 12-Bit Amplitude
  - Up to 4-Bit Ambient
  - Saturation Detection
- Chipset Interface:
  - Compatible with TI ToF Sensor (OPT8241)
- Output (CMOS, 8-Lane Data, 8 Control Signals, and Clock):
  - Digital Video Protocol (DVP)-Compatible:
    - Data, VD, HD, Clock
  - Synchronous Serial Interface (SSI)-Compatible
- Depth Engine:
  - Pixel Binning
  - Region of Interest (ROI)
  - De-Aliasing
  - Non-linearity Correction
  - Temperature Compensation
  - High Dynamic Range Operation
  - Spatial Filter
- Timing Coordinator:
  - Sensor Control
  - Master and Slave Sync Operation
- I^2C Slave Interface
- Power Supply: 1.2-V Core, 1.8-V I/O, 3.3-V I/O 2.5-V Analog
- Package: 256-Pin, 9-mm × 9-mm NFBGA
- Operating Temperature: 0°C to 85°C

2 Applications

- 3D Imaging:
  - Location and Proximity Sensing
  - 3D Scanning and 3D Machine Vision
  - Security and Surveillance
  - Gesture Controls

3 Description

The time-of-flight controller (TFC) is a high-performance, 3D time-of-flight (ToF) sensor companion device that computes the depth data from the digitized sensor data. Depth data are output via a programmable complementary metal-oxide-semiconductor (CMOS) parallel interface.

In addition to depth data, the TFC provides auxiliary information consisting of amplitude, ambient, and flags for each pixel. This information can be used to implement filters and masks and to dynamically control the system configuration for the intended performance.

The TFC supports a wide range of binning and ROI options that help optimize the data throughput that must be handled.

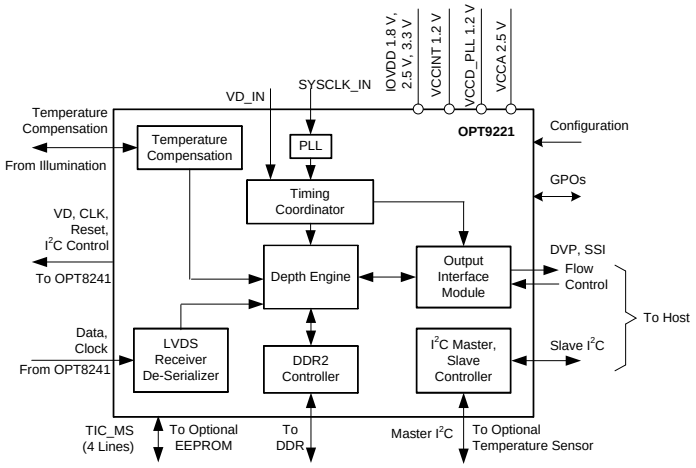
The 9-mm × 9-mm NFBGA package enables small form-factor, 3D, ToF systems that can be embedded into a variety of end equipment.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPT9221	NFBGA (256)	9.00 mm × 9.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Functional Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Original (June 2015) to Revision A	Page
• Changed from Product Preview to Production Data	1

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5 Pin Configuration and Functions

ZVM Package
256-Ball NFBGA
Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	VCCIO8	GPO_3	GPO_2	GPO_0	TIC_DATA_7	RSVD	VD_IN	RSVD_IN	RSVD_IN	VD_QD	HD_QD	VD_SF	VD_FR	SENSOR_DEMOD_CLK	VSYNC_OUT	VCCIO7
B	SLEEP	GND	GPO_1	RSVD	RSVD	RSVD	TIC_DATA_4	RSVD_IN	RSVD_IN	RSVD	RSVD	RSVD	RSVD	SENSOR_CLK	GND	ILLUM_FB
C	TIC_DATA_1/ASDO	RESETZ	RSVD	VCCIO8	GND	RSVD	VCCIO8	I2C_MAS_SDA	I2C_SDA_SENSOR	VCCIO7	RSVD	GND	VCCIO7	RSVD	ILLUM_SW_2	ILLUM_SW_1
D	DEBUG	TIC_CSOZ	RSVD	VCCD_PLL3	RSVD	RSVD	GND	I2C_MAS_SCL	I2C_SCL_SENSOR	GND	RSVD	RSVD	VCCD_PLL2	SENSOR_RSTZ	RSVD	RSVD
E	SYSCLK_IN	GND	VCCIO1	GND	GNDA3	TIC_DATA_6	TIC_DATA_5	TIC_DATA_2	GPI_1	RSVD	RSVD	GNDA2	GND	VCCIO6	ILLUM_MOD_FB	COMP_MOD_FB
F	I2C_SLV_SCL	I2C_SLV_SDA	RSVD	TIC_STATUSZ	VCCA3	GND	VCCINT	TIC_DATA_3	GPI_0	GND	VCCINT	VCCA2	ILLUM_REF	RSVD	IO_MOD_REF	COMP_MOD_REF
G	RSVD	INT_OUT	VCCIO1	GND	INT_PMIC	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	RSVD	BOOT_2	GND	VCCIO6	RSVD	TIC_INIT_DONE
H	TIC_CLK	TIC_DATA_0	TIC_C	TIC_I	TIC_CONFIGZ	VCCINT	GND	GND	GND	GND	VCCINT	BOOT_1	BOOT_0	TIC_CONF_DONE	GND	GND
J	RSVD	HD/BD	TIC_CEZ	TIC_O	TIC_S	VCCINT	GND	GND	GND	GND	GND	RSVD	RSVD	RSVD	CAP_DATA_SUM_P	CAP_DATA_SUM_M
K	VD	PHASE_AUX	VCCIO2	GND	OP_CLK	OP_CS	VCCINT	GND	DDR2_ADDR_3	DDR2_ADDR_2	VCCINT	RSVD	GND	VCCIO5	CAP_DATA_DIFF_1P	CAP_DATA_DIFF_1M
L	OP_DATA_5	OP_DATA_6	OVERFLOW	OP_DATA_7	VCCA1	FE	DDR2_DQ_0	DDR2_DQ_7	DDR2_ADDR_1	DDR2_ADDR_6	DDR2_ADDR_0	VCCA4	RSVD	RSVD_IN	RSVD_IN	RSVD
M	READY	RSVD_IN	VCCIO2	GND	GNDA1	RSVD	DDR2_DQS_0	DDR2_DM_1	DDR2_ADDR_5	DDR2_ADDR_11	DDR2_ADDR_4	GNDA4	GND	VCCIO5	CAP_BIT_CLKP	CAP_BIT_CLKM
N	OP_DATA_3	OP_DATA_4	DDR2_ADDR_10	VCCD_PLL1	DDR2_DQ_1	DDR2_DQ_3	GND	DDR2_DQ_14	DDR2_DQ_9	GND	DDR2_ADDR_8	DDR2_REF_3	VCCD_PLL4	RSVD	CAP_DATA_DIFF_0P	CAP_DATA_DIFF_0M
P	OP_DATA_1	OP_DATA_2	DDR2_DM_0	VCCIO3	GND	DDR2_REF_1	VCCIO3	DDR2_DQ_12	DDR2_ADDR_9	VCCIO4	DDR2_REF_2	GND	VCCIO4	DDR2_CLKz_0	RSVD	CAP_FRM_CLKM
R	OP_DATA_0	GND	DDR2_DQ_6	DDR2_BA_0	DDR2_DQ_4	DDR2_DQ_2	DDR2_DQ_5	RSVD_IN	RSVD_IN	DDR2_DQ_11	DDR2_DQ_10	DDR2_DQ_8	DDR2_CSZ	DDR2_CLK_0	GND	CAP_FRM_CLKP
T	VCCIO3	DDR2_CKE	DDR2_REF_0	DDR2_BA_1	DDR2_ADDR_12	DDR2_ADDR_7	DDR2_DQS_1	RSVD_IN	RSVD_IN	DDR2_WEZ	DDR2_CASZ	DDR2_RASZ	DDR2_DQ_15	DDR2_DQ_13	DDR2_ODT_0	VCCIO4

Pin Functions

PIN		I/O	I/O STANDARD	I/O BANK	DESCRIPTION
NAME	NO.				
BOOT_0	H13	Input	2.5 V	–	Boot configuration pin 0. Tie to VCC or to GND.
BOOT_1	H12	Input	2.5 V	–	Boot configuration pin 1. Tie to VCC or to GND.
BOOT_2	G12	Input	2.5 V	–	Boot configuration pin 2. Tie to VCC or to GND.

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Pin Functions (continued)

PIN		I/O	I/O STANDARD	I/O BANK	DESCRIPTION
NAME	NO.				
CAP_BIT_CLKM	M16	Input	LVDS	VCCIO5	Sensor data bit clk
CAP_BIT_CLKP	M15	Input	LVDS	VCCIO5	Sensor data bit clk
CAP_DATA_DIFF_0M	N16	Input	LVDS	VCCIO5	Sensor differential data ch 0
CAP_DATA_DIFF_0P	N15	Input	LVDS	VCCIO5	Sensor differential data ch 0
CAP_DATA_DIFF_1M	K16	Input	LVDS	VCCIO5	Sensor differential data ch 1
CAP_DATA_DIFF_1P	K15	Input	LVDS	VCCIO5	Sensor differential data ch 1
CAP_DATA_SUM_M	J16	Input	LVDS	VCCIO5	Sensor common mode data
CAP_DATA_SUM_P	J15	Input	LVDS	VCCIO5	Sensor common mode data
CAP_FRM_CLKM	P16	Input	LVDS	VCCIO5	Sensor sample clk
CAP_FRM_CLKP	R16	Input	LVDS	VCCIO5	Sensor sample clk
COMP_MOD_FB	E16	Input	3.3 V	VCCIO6	Feedback signal from the external illumination modulation feedback comparator.
COMP_MOD_REF	F16	Output	3.3 V	VCCIO6	Reference modulation signal for measuring external illumination modulation feedback comparator delay.
DDR2_ADDR_0	L11	Output	SSTL-18 Class I	VCCIO4	DDR address signal 0
DDR2_ADDR_1	L9	Output	SSTL-18 Class I	VCCIO4	DDR address signal 1
DDR2_ADDR_2	K10	Output	SSTL-18 Class I	VCCIO4	DDR address signal 2
DDR2_ADDR_3	K9	Output	SSTL-18 Class I	VCCIO4	DDR address signal 3
DDR2_ADDR_4	M11	Output	SSTL-18 Class I	VCCIO4	DDR address signal 4
DDR2_ADDR_5	M9	Output	SSTL-18 Class I	VCCIO4	DDR address signal 5
DDR2_ADDR_6	L10	Output	SSTL-18 Class I	VCCIO4	DDR address signal 6
DDR2_ADDR_7	T6	Output	SSTL-18 Class I	VCCIO3	DDR address signal 7
DDR2_ADDR_8	N11	Output	SSTL-18 Class I	VCCIO4	DDR address signal 8
DDR2_ADDR_9	P9	Output	SSTL-18 Class I	VCCIO4	DDR address signal 9
DDR2_ADDR_10	N3	Output	SSTL-18 Class I	VCCIO3	DDR address signal 10
DDR2_ADDR_11	M10	Output	SSTL-18 Class I	VCCIO4	DDR address signal 11
DDR2_ADDR_12	T5	Output	SSTL-18 Class I	VCCIO3	DDR address signal 12
DDR2_BA_0	R4	Output	SSTL-18 Class I	VCCIO3	DDR bank signal
DDR2_BA_1	T4	Output	SSTL-18 Class I	VCCIO3	DDR bank signal
DDR2_CASZ	T11	Output	SSTL-18 Class I	VCCIO4	DDR CAS
DDR2_CKE	T2	Output	SSTL-18 Class I	VCCIO3	DDR clock enable
DDR2_CLK_0	R14	Output	SSTL-18 Class I	VCCIO4	DDR clock
DDR2_CLKz_0	P14	Output	SSTL-18 Class I	VCCIO4	DDR clock

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Pin Functions (continued)

PIN		I/O	I/O STANDARD	I/O BANK	DESCRIPTION
NAME	NO.				
DDR2_CSZ	R13	Output	SSTL-18 Class I	VCCIO4	DDR chip select
DDR2_DM_0	P3	Output	SSTL-18 Class I	VCCIO3	DDR data mask 0
DDR2_DM_1	M8	Output	SSTL-18 Class I	VCCIO3	DDR data mask 1
DDR2_DQ_0	L7	Bidir	SSTL-18 Class I	VCCIO3	DDR data 15
DDR2_DQ_1	N5	Bidir	SSTL-18 Class I	VCCIO3	DDR data 14
DDR2_DQ_2	R6	Bidir	SSTL-18 Class I	VCCIO3	DDR data 13
DDR2_DQ_3	N6	Bidir	SSTL-18 Class I	VCCIO3	DDR data 12
DDR2_DQ_4	R5	Bidir	SSTL-18 Class I	VCCIO3	DDR data 11
DDR2_DQ_5	R7	Bidir	SSTL-18 Class I	VCCIO3	DDR data 10
DDR2_DQ_6	R3	Bidir	SSTL-18 Class I	VCCIO3	DDR data 9
DDR2_DQ_7	L8	Bidir	SSTL-18 Class I	VCCIO3	DDR data 8
DDR2_DQ_8	R12	Bidir	SSTL-18 Class I	VCCIO4	DDR data 7
DDR2_DQ_9	N9	Bidir	SSTL-18 Class I	VCCIO4	DDR data 6
DDR2_DQ_10	R11	Bidir	SSTL-18 Class I	VCCIO4	DDR data 5
DDR2_DQ_11	R10	Bidir	SSTL-18 Class I	VCCIO4	DDR data 4
DDR2_DQ_12	P8	Bidir	SSTL-18 Class I	VCCIO3	DDR data 3
DDR2_DQ_13	T14	Bidir	SSTL-18 Class I	VCCIO4	DDR data 2
DDR2_DQ_14	N8	Bidir	SSTL-18 Class I	VCCIO3	DDR data 1
DDR2_DQ_15	T13	Bidir	SSTL-18 Class I	VCCIO4	DDR data 0
DDR2_DQS_0	M7	Output	SSTL-18 Class I	VCCIO3	DDR data strobe
DDR2_DQS_1	T7	Output	SSTL-18 Class I	VCCIO3	DDR data strobe
DDR2_ODT_0	T15	Bidir	SSTL-18 Class I	VCCIO4	DDR on die termination
DDR2_RASZ	T12	Output	SSTL-18 Class I	VCCIO4	DDR RAS
DDR2_REF_0	T3	Input	Analog	–	DDR reference, tie to 0.9 V
DDR2_REF_1	P6	Input	Analog	–	DDR reference, tie to 0.9 V
DDR2_REF_2	P11	Input	Analog	–	DDR reference, tie to 0.9 V
DDR2_REF_3	N12	Input	Analog	–	DDR reference, tie to 0.9 V
DDR2_WEZ	T10	Output	SSTL-18 Class I	VCCIO4	DDR write enable
DEBUG	D1	Bidir	1.8 V	VCCIO1	TI proprietary debug port. Pullup by 10 kΩ.
FE	L6	Output	1.8 V	VCCIO2	Marks the end of a frame

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Pin Functions (continued)

PIN		I/O	I/O STANDARD	I/O BANK	DESCRIPTION
NAME	NO.				
GND	B2	Power	–	–	Digital ground
GND	B15	Power	–	–	Digital ground
GND	C5	Power	–	–	Digital ground
GND	C12	Power	–	–	Digital ground
GND	D7	Power	–	–	Digital ground
GND	D10	Power	–	–	Digital ground
GND	E2	Power	–	–	Digital ground
GND	E4	Power	–	–	Digital ground
GND	E13	Power	–	–	Digital ground
GND	F6	Power	–	–	Digital ground
GND	F10	Power	–	–	Digital ground
GND	G4	Power	–	–	Digital ground
GND	G13	Power	–	–	Digital ground
GND	H7	Power	–	–	Digital ground
GND	H8	Power	–	–	Digital ground
GND	H9	Power	–	–	Digital ground
GND	H10	Power	–	–	Digital ground
GND	H15	Power	–	–	Digital ground
GND	H16	Power	–	–	Digital ground
GND	J7	Power	–	–	Digital ground
GND	J8	Power	–	–	Digital ground
GND	J9	Power	–	–	Digital ground
GND	J10	Power	–	–	Digital ground
GND	J11	Power	–	–	Digital ground
GND	K4	Power	–	–	Digital ground
GND	K8	Power	–	–	Digital ground
GND	K13	Power	–	–	Digital ground
GND	M4	Power	–	–	Digital ground
GND	M13	Power	–	–	Digital ground
GND	N7	Power	–	–	Digital ground
GND	N10	Power	–	–	Digital ground
GND	P5	Power	–	–	Digital ground
GND	P12	Power	–	–	Digital ground
GND	R2	Power	–	–	Digital ground
GND	R15	Power	–	–	Digital ground
GNDA1	M5	Power	–	–	Analog ground
GNDA2	E12	Power	–	–	Analog ground
GNDA3	E5	Power	–	–	Analog ground
GNDA4	M12	Power	–	–	Analog ground
GPI_0	F9	Input	1.8 V	VCCIO7	Sensor general purpose pin
GPI_1	E9	Input	1.8 V	VCCIO7	Sensor general purpose pin
GPO_1	B3	Output	1.8 V	VCCIO8	General purpose output
GPO_2	A3	Output	1.8 V	VCCIO8	General purpose output
GPO_3	A2	Output	1.8 V	VCCIO8	General purpose output
GPO_0	A4	Output	1.8 V	VCCIO8	General purpose output
HD/BD	J2	Output	1.8 V	VCCIO2	Indicates the row boundary or block boundary

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Pin Functions (continued)

PIN		I/O	I/O STANDARD	I/O BANK	DESCRIPTION
NAME	NO.				
HD_QD	A11	Input	1.8 V	VCCIO7	Sensor HD
ILLUM_FB	B16	Input	3.3 V	VCCIO6	Comparator output feedback to TFC
ILLUM_MOD_FB	E15	Input	3.3 V	VCCIO6	Illumination modulation signal input. Connect to ILLUM_P/M of the OPT8241 sensor.
ILLUM_REF	F13	Output	3.3 V	VCCIO6	Comparator reference signal
ILLUM_SW_1	C16	Output	3.3 V	VCCIO6	DCDC control signal 1
ILLUM_SW_2	C15	Output	3.3 V	VCCIO6	DCDC control signal 2
INT_OUT	G2	Output	1.8 V	VCCIO1	Interrupt to external host
INT_PMIC	G5	Input	1.8 V	VCCIO1	Interrupt from PMIC
IO_MOD_REF	F15	Output	3.3 V	VCCIO6	Reference modulation signal from the TFC for measuring TFC I/O delay
I2C_MAS_SCL	D8	Output	1.8 V	VCCIO8	I^2C master clk
I2C_MAS_SDA	C8	Bidir	1.8 V	VCCIO8	I^2C master data
I2C_SCL_SENSOR	D9	Output	1.8 V	VCCIO7	Dedicated I^2C for sensor - clock
I2C_SDA_SENSOR	C9	Bidir	1.8 V	VCCIO7	Dedicated I^2C for sensor - data
I2C_SLV_SCL	F1	Input	1.8 V	VCCIO1	I^2C slave clk
I2C_SLV_SDA	F2	Bidir	1.8 V	VCCIO1	I^2C slave data
OP_CLK	K5	Output	1.8 V	VCCIO2	Output data clock
OP_CS	K6	Output	1.8 V	VCCIO2	Indicates the validity of the data output. Useful for SPI mode.
OP_DATA_0	R1	Output	1.8 V	VCCIO2	Output data bit 0
OP_DATA_1	P1	Output	1.8 V	VCCIO2	Output data bit 1
OP_DATA_2	P2	Output	1.8 V	VCCIO2	Output data bit 2
OP_DATA_3	N1	Output	1.8 V	VCCIO2	Output data bit 3
OP_DATA_4	N2	Output	1.8 V	VCCIO2	Output data bit 4
OP_DATA_5	L1	Output	1.8 V	VCCIO2	Output data bit 5
OP_DATA_6	L2	Output	1.8 V	VCCIO2	Output data bit 6
OP_DATA_7	L4	Output	1.8 V	VCCIO2	Output data bit 7
OVERFLOW	L3	Input	1.8 V	VCCIO2	Used to indicate failure in flow control.
PHASE_AUX	K2	Output	1.8 V	VCCIO2	Indicates the type of data on the output bus.
READY	M1	Input	1.8 V	VCCIO2	Used to achieve flow control of the output data.
RESETZ	C2	Input	1.8 V	VCCIO1	Global reset for the TFC
RSVD	A6	Bidir	1.8 V	VCCIO8	Reserved. Leave unconnected.
RSVD	B4	Bidir	3.3 V	VCCIO6	Leave unconnected
RSVD	B5	Bidir	1.8 V	VCCIO8	Reserved. Leave unconnected.
RSVD	B6	Bidir	1.8 V	VCCIO8	Reserved. Leave unconnected.
RSVD	B10	Bidir	1.8 V	VCCIO7	Leave unconnected
RSVD	B11	Bidir	1.8 V	VCCIO7	Leave unconnected
RSVD	B12	Bidir	1.8 V	VCCIO7	Leave unconnected
RSVD	B13	Bidir	1.8 V	VCCIO7	Leave unconnected
RSVD	C3	Bidir	1.8 V	VCCIO8	Leave unconnected
RSVD	C6	Bidir	1.8 V	VCCIO8	Reserved. Leave unconnected.
RSVD	C11	Bidir	1.8 V	VCCIO7	Leave unconnected
RSVD	C14	Bidir	1.8 V	VCCIO7	Leave unconnected
RSVD	D3	Bidir	1.8 V	VCCIO8	Reserved. Leave unconnected.
RSVD	D5	Bidir	1.8 V	VCCIO8	Reserved. Leave unconnected.
RSVD	D6	Bidir	1.8 V	VCCIO8	Reserved. Leave unconnected.

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Pin Functions (continued)

PIN		I/O	I/O STANDARD	I/O BANK	DESCRIPTION
NAME	NO.				
RSVD	D11	Bidir	1.8 V	VCCIO7	Leave unconnected
RSVD	D12	Bidir	1.8 V	VCCIO7	Leave unconnected
RSVD	D15	Bidir	3.3 V	VCCIO6	Leave unconnected
RSVD	D16	Bidir	3.3 V	VCCIO6	Leave unconnected
RSVD	E10	Bidir	1.8 V	VCCIO7	Leave unconnected
RSVD	E11	Bidir	1.8 V	VCCIO7	Leave unconnected
RSVD	F3	Bidir	1.8 V	VCCIO1	Leave unconnected
RSVD	F14	Bidir	3.3 V	VCCIO6	Leave unconnected
RSVD	G1	Bidir	1.8 V	VCCIO1	Leave unconnected
RSVD	G11	Bidir	3.3 V	VCCIO6	Leave unconnected
RSVD	G15	Bidir	3.3 V	VCCIO6	Leave unconnected
RSVD	J1	Output	1.8 V	VCCIO2	Reserved
RSVD	J12	Bidir	2.5 V	VCCIO5	Leave unconnected
RSVD	J13	Bidir	2.5 V	VCCIO5	Leave unconnected
RSVD	J14	Bidir	2.5 V	VCCIO5	Leave unconnected
RSVD	K12	Bidir	2.5 V	VCCIO5	Leave unconnected
RSVD	L13	Bidir	2.5 V	VCCIO5	Leave unconnected
RSVD	L16	Bidir	2.5 V	VCCIO5	Leave unconnected
RSVD	M6	Bidir	1.8 V	VCCIO3	Leave unconnected
RSVD	N14	Bidir	2.5 V	VCCIO5	Leave unconnected
RSVD	P15	Bidir	2.5 V	VCCIO5	Leave unconnected
RSVD_IN	A8	Input	1.8 V	VCCIO8	Tie to GND
RSVD_IN	A9	Input	1.8 V	VCCIO7	Tie to GND
RSVD_IN	B8	Input	1.8 V	VCCIO8	Tie to GND
RSVD_IN	B9	Input	1.8 V	VCCIO7	Tie to GND
RSVD_IN	L14	Input	Analog	VCCIO5	Tie to 2.5 V
RSVD_IN	L15	Input	Analog	VCCIO5	Tie to 2.5 V
RSVD_IN	M2	Input	1.8 V	VCCIO2	Tie to GND
RSVD_IN	R8	Input	1.8 V	VCCIO3	Tie to GND
RSVD_IN	R9	Input	1.8 V	VCCIO4	Tie to GND
RSVD_IN	T8	Input	1.8 V	VCCIO3	Tie to GND
RSVD_IN	T9	Input	1.8 V	VCCIO4	Tie to GND
SENSOR_CLK	B14	Output	1.8 V	VCCIO7	Sensor main clock
SENSOR_DEMOD_CLK	A14	Output	1.8 V	VCCIO7	Demod clock for test
SENSOR_RSTZ	D14	Output	1.8 V	VCCIO7	Sensor reset
SLEEP	B1	Input	1.8 V	VCCIO1	Puts the TFC in standby mode when enabled
SYSCLK_IN	E1	Input	1.8 V	VCCIO1	Main system clock input
TIC_C	H3	Input	2.5 V	–	Reserved. Needs external pull-down resistor of 10 kΩ
TIC_CEZ	J3	Input	1.8 V	VCCIO1	If high, TFC releases the control of configuration pins. In slave boot modes, tie to ground.
TIC_CLK	H1	Input	1.8 V	VCCIO1	Configuration data clock
TIC_CONFIGZ	H5	Input	1.8 V	VCCIO1	Used to start firmware load operation
TIC_CONF_DONE	H14	Output	Open Drain	VCCIO6	Used to indicate end of firmware load operation
TIC_CSOZ	D2	Output	1.8 V	VCCIO1	In master serial boot mode, Used by TFC to load firmware from EEPROM as chip select pin.
TIC_DATA_0	H2	Input	1.8 V	VCCIO1	Configuration data pin 0

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Pin Functions (continued)

PIN		I/O	I/O STANDARD	I/O BANK	DESCRIPTION
NAME	NO.				
TIC_DATA_1/ASDO	C1	Bidir	1.8 V	VCCIO1	Used as output in master serial boot mode to communicate to firmware EEPROM as data-out pin. Input in passive parallel boot mode.
TIC_DATA_2	E8	Input	1.8 V	VCCIO8	Used only in Passive Parallel Boot mode. Tie to GND otherwise.
TIC_DATA_3	F8	Input	1.8 V	VCCIO8	Used only in Passive Parallel Boot mode. Tie to GND otherwise.
TIC_DATA_4	B7	Input	1.8 V	VCCIO8	Used only in Passive Parallel Boot mode. Tie to GND otherwise.
TIC_DATA_5	E7	Input	1.8 V	VCCIO8	Used only in Passive Parallel Boot mode. Tie to GND otherwise.
TIC_DATA_6	E6	Input	1.8 V	VCCIO8	Used only in Passive Parallel Boot mode. Tie to GND otherwise.
TIC_DATA_7	A5	Input	1.8 V	VCCIO8	Used only in Passive Parallel Boot mode. Tie to GND otherwise.
TIC_I	H4	Input	2.5 V	–	Reserved. Needs external pull-up resistor of 10 kΩ to 2.5 V
TIC_INIT_DONE	G16	Output	Open Drain	VCCIO1	Used to indicate end of TFC initialization.
TIC_O	J4	Output	2.5 V	–	Reserved. Leave unconnected.
TIC_S	J5	Input	2.5 V	–	Reserved. Needs external pull-up resistor of 10 kΩ to 2.5 V
TIC_STATUSZ	F4	Output	Open Drain	VCCIO1	Used to indicate status of firmware load operation
VCCA1	L5	Power	–	–	2.5-V supply
VCCA2	F12	Power	–	–	2.5-V supply
VCCA3	F5	Power	–	–	2.5-V supply
VCCA4	L12	Power	–	–	2.5-V supply
VCCD_PLL1	N4	Power	–	–	1.2-V supply
VCCD_PLL2	D13	Power	–	–	1.2-V supply
VCCD_PLL3	D4	Power	–	–	1.2-V supply
VCCD_PLL4	N13	Power	–	–	1.2-V supply
VCCINT	F7	Power	–	–	1.2-V supply
VCCINT	F11	Power	–	–	1.2-V supply
VCCINT	G6	Power	–	–	1.2-V supply
VCCINT	G7	Power	–	–	1.2-V supply
VCCINT	G8	Power	–	–	1.2-V supply
VCCINT	G9	Power	–	–	1.2-V supply
VCCINT	G10	Power	–	–	1.2-V supply
VCCINT	H6	Power	–	–	1.2-V supply
VCCINT	H11	Power	–	–	1.2-V supply
VCCINT	J6	Power	–	–	1.2-V supply
VCCINT	K7	Power	–	–	1.2-V supply
VCCINT	K11	Power	–	–	1.2-V supply
VCCIO1	E3	Power	–	–	1.8-V supply
VCCIO1	G3	Power	–	–	1.8-V supply
VCCIO2	K3	Power	–	–	1.8-V supply
VCCIO2	M3	Power	–	–	1.8-V supply
VCCIO3	P4	Power	–	–	1.8-V supply
VCCIO3	P7	Power	–	–	1.8-V supply
VCCIO3	T1	Power	–	–	1.8-V supply

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Pin Functions (continued)

PIN		I/O	I/O STANDARD	I/O BANK	DESCRIPTION
NAME	NO.				
VCCIO4	P10	Power	–	–	1.8-V supply
VCCIO4	P13	Power	–	–	1.8-V supply
VCCIO4	T16	Power	–	–	1.8-V supply
VCCIO5	K14	Power	–	–	2.5-V supply
VCCIO5	M14	Power	–	–	2.5-V supply
VCCIO6	E14	Power	–	–	3.3-V supply
VCCIO6	G14	Power	–	–	3.3-V supply
VCCIO7	A16	Power	–	–	1.8-V supply
VCCIO7	C10	Power	–	–	1.8-V supply
VCCIO7	C13	Power	–	–	1.8-V supply
VCCIO8	A1	Power	–	–	1.8-V supply
VCCIO8	C4	Power	–	–	1.8-V supply
VCCIO8	C7	Power	–	–	1.8-V supply
VD	K1	Output	1.8 V	VCCIO2	Indicates the frame boundary
VD_FR	A13	Input	1.8 V	VCCIO7	Sensor Frame VD
VD_IN	A7	Input	1.8 V	VCCIO1	External Sync input
VD_QD	A10	Input	1.8 V	VCCIO7	Sensor Quad VD
VD_SF	A12	Input	1.8 V	VCCIO7	Sensor Sub-Frame VD
VSYNC_OUT	A15	Output	1.8 V	VCCIO7	Sensor Sync input

6 Specifications

6.1 Absolute Maximum Ratings

at GND = 0 V and all voltages related to ground (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
Core voltage	VCCINT	–0.5	1.8	V
I/O voltage	VCCIO	–0.5	3.75	V
PLL digital supply	VCCD_PLL	–0.5	4.5	V
PLL Analog supply	VCCA	–0.5	3.75	V
Input voltage at input pins, V_I		–0.5	4.2	V
Output current from output pins, I_{OUT}		–25	40	mA
Operating junction temperature, T_J		–40	125	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the device ground.

6.2 ESD Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)		2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)		500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

at GND = 0 V and all voltages related to ground (unless otherwise noted)

			MIN	NOM	MAX	UNIT
VCCINT	Core voltage		1.15	1.2	1.25	V
VCCIO	I/O voltage	1.8-V operation	1.71	1.8	1.89	V
		2.5-V operation	2.375	2.5	2.625	
		3.3-V operation	3.135	3.3	3.465	V
VCCD_PLL	PLL digital supply		1.16	1.2	1.24	V
VCCA	PLL Analog supply		2.375	2.5	2.625	V
V_I	Input voltage at input pins		–0.3		VCCIO(1) + 0.3	V
T_J	Operating junction temperature		0		85	°C
t_{RAMP}	Power-supply ramp time		50		3000	µs

(1) VCCIO is the corresponding bank voltage

6.4 Thermal Information

THERMAL METRIC(1)		OPT9221 ZVM (NFBGA) 256 BALLS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	7.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	16.0	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
1.8-V CMOS I/Os						
V_{IH}	High-level input threshold		0.65 × VCCIO(1)			V
V_{IL}	Low-level input threshold				0.35 × VCCIO	V
V_{OH}	High-level output voltage		VCCIO – 0.45			V
V_{OL}	Low-level output voltage				0.45	V
I_{lkg}	Input pin leakage current(2)		–10		10	µA
I_{OH}	High-level output current				–2	mA
I_{OL}	Low-level output current				2	mA
3.3-V LVCMOS I/Os						
V_{IH}	High-level input voltage		1.7			V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage		VCCIO – 0.2			V
V_{OL}	Low-level output voltage				0.2	V
I_{lkg}	Input pin leakage current(2)		–10		10	µA
I_{OH}	High-level output current				–2	mA
I_{OL}	Low-level output current				2	mA

(1) VCCIO is the corresponding bank voltage.
(2) For, 0 < Input voltage < VCCIO.

6.6 Timing Requirements

PARAMETER			MIN	TYP	MAX	UNIT
SYSCLK_IN	System input clock frequency			6		MHz
				12		MHz
				24		MHz
				48		MHz
	Duty cycle		40%		60%	
SYSCLK_FREQ	Internal system clock frequency			48		MHz
VD_IN	VD_IN pulse duration		40			ns
$\overline{\text{RESET}}$	RESET pulse duration		40			ns
I^2C clock	Slave I^2C interface clock frequency			400		KHz
	Master I^2C interface clock frequency			400		KHz
	Sensor I^2C interface clock frequency			400		KHz
PARALLEL CMOS MODE (Assuming default OP_CLK polarity)						
t_{su}	Data setup time	Data valid to zero crossing of CLKOUT	5			ns
t_h	Data hold time	Zero crossing of CLKOUT to data becoming invalid	20			ns

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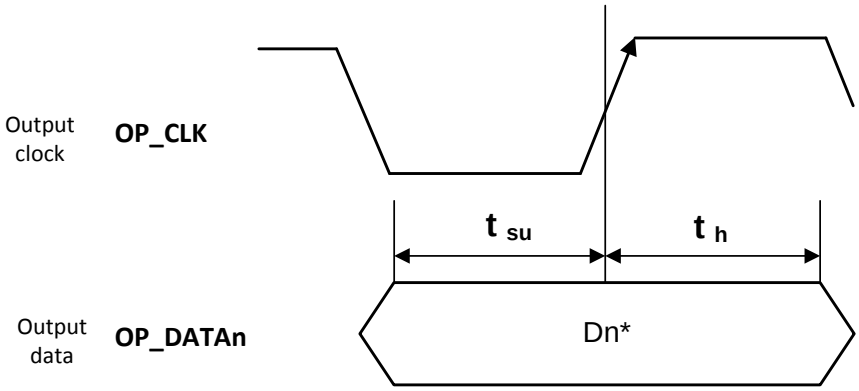


Figure 1. Timing Diagram

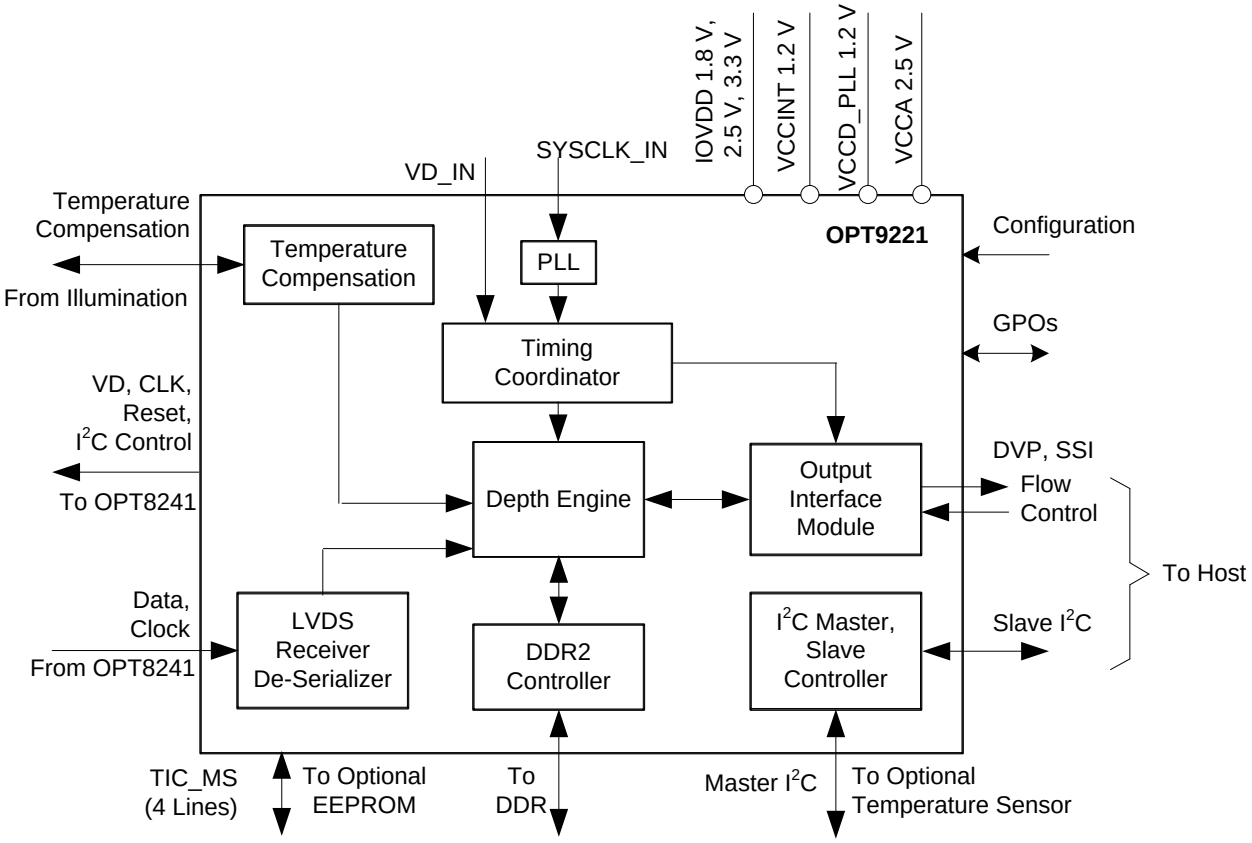
7 Detailed Description

7.1 Overview

The TFC has the following blocks:

- Timing generator – Generates the sequencing signals for sensor, illumination and depth processor
- Input LVDS receiver and de-serializer
- Depth engine - Calculates phase and amplitude
- Output data interface module
- DDR2 memory controller for external DDR memory
- I^2C slave - for configuration of TFC registers by the host processor
- I^2C master – for temperature sensing
- I^2C sensor interface – for controlling the OPT8241 sensor

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 DDR2 Interface

The TFC has a DDR2 controller that allows connection to an external DDR2 RAM. The TFC can support up to 300-MHz DDR2 (150-MHz clock operation). The TFC stores the readout sensor data for all the quads and sub-frames in the DDR. Once all the necessary data is available, the stored sensor data is retrieved from the DDR to calculate depth data. A minimum of 128 mbits of DDR memory is recommended for correct functionality. The recommended DDR part is Micron MT47H32M16NF-25E:H.

7.3.2 I^2C Master Interface

The I^2C master interface is used for reading temperature from an off-chip temperature sensor on the board. The temperature sensor is used for calibrating the phase offset with temperature changes. The external temperature sensor has to placed in close proximity to the illumination driver. The related programmable parameters and status registers are listed in Table 1.

Table 1. I^2C Master Interface

PARAMETER OR STATUS REGISTER	DESCRIPTION
tillum_slv_addr	I^2C address of the temperature sensor next to the illumination driver.
tillum	Status registers. Indicates the temperature readout from the temperature sensor next to the illumination driver.

The temperature readings are refreshed every frame. A single byte read operation is performed on the temperature sensor to read the temperature. It is expected that the temperature sensor returns the temperature in a single unsigned byte. The TI TMP103 series temperature sensors conform to this behavior. For temperature calibration of phase, the value read from the temperature sensor is assumed to be linear with the actual temperature.

7.3.3 Timing Coordinator

The timing coordinator programs the OPT8241 timing generator (TG). The OPT8241 timing signals consist of the modulation signals for the sensor and the illumination and the readout signals for the sensor. The TG has the following features:

- Frame rate control
- Sensor addressing
- Integration time control
- Modulation clock generation

7.3.3.1 Basic Frame Structure

Each frame is divided into sub-frames used for internal averaging.

FRAME				
Sub-frame-1	Sub-frame-2	…….	Sub-frame-n	Frame dead time

Each sub-frame is divided into quads. Each quad can have a different phase between illumination and sensor modulation signals.

SUBFRAME				
Quad-1	Quad-2	Quad-3	…….	Quad-n

Each quad is further split into 4 stages.

QUAD			
Reset	Integration	Readout	Quad dead time

QUAD STAGE	DESCRIPTION
Reset	Sensor is reset to clear the accumulated signal
Integration	The pixel array and illumination are modulated by the TFC. The sensor captures the raw ToF signal.
Readout	The raw pixel data in the selected region of interest is readout from the sensor by the TFC.
Dead	The sensor is inactive. The TFC and the sensor enter a low power mode.

7.3.3.2 Frame Rate Control and Sub Frames

OPT9221 supports master and slave modes of operation for the start of frame timing. The parameters shown in Table 2 control the master and slave behavior.

Table 2. Master and Slave Parameters

PARAMETER	DEFAULT	DESCRIPTION
tg_dis	1	Start the timing generator and hence the full chipset operation. '0' : Enable the timing generator. '1' : Disable the timing generator
slave_mode	0	Puts the timing controller in slave mode. The timing controller waits for external sync through VD_IN pin for the start of frames. By default the timing controller is in master mode.
sync_mode	0	Puts the timing controller in sync mode. The timing controller synchronizes with external input through VD_IN pin for the start of frames, but does not depend on it. If both slave_mode and sync_mode are enabled, sync_mode takes higher priority. By default, this mode is disabled.
frame_sync_delay	1	The programmable delay between external VD_IN pulse and internal start of frame. The delay has to be at the least 1 cycle..

In the slave mode or sync mode, a positive pulse on the VD_IN pin can be used for synchronization. The pulse has to be a minimum of 2 system clocks cycles wide in order to be recognized correctly. In slave mode, if another pulse is received before the end of the previous frame, the pulse is ignored. In sync mode, since a pulse can be received by the TFC anytime within a frame, the frame during which the pulse was received is aborted and therefore there is a possibility disruption of output data and hence loss of information.

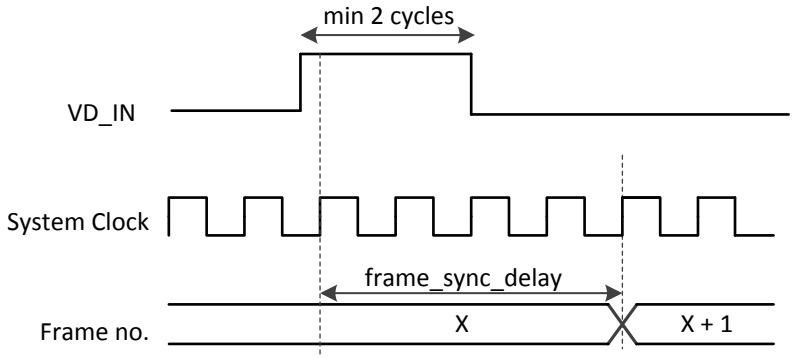

Figure 2. Timing Diagram

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When OPT9221 is operated in master mode or sync mode, frame rate is controlled using the parameters shown in Table 3.

Table 3. Frame-Rate Parameters

PARAMETER	DEFAULT	DESCRIPTION
quad_cnt_max	4	The number of quads in each sub-frame. Number of quads can be currently programmed to 4 and 6 only. Behavior is not determined for other values.
sub_frame_cnt_max	4	The number of sub-frames in each frame. Sub-frames can be currently programmed to values of 1, 2, 4 and 8 only. Behavior is not determined for other values.
pix_cnt_max	100000	The number of system clock cycles in one frame divided by the product of quad_cnt_max and sub_frame_cnt _max.
pix_cnt_max_set_failed	0	Read-only flag that indicates if the setting of pix_cnt_max value was successful. If the pix_cnt_max is smaller than the minimum size needed to accommodate reset and readout time, pix_cnt_max_set_failed is set.
lumped_dead_time	0	Dead time can be either distributed equally among all quads or it can be lumped at the end of each frame. Distributed quad dead time is typically better for phase offset cancellation. Lumped frame dead time is typically better for reducing motion artefacts and power consumption. By default, distributed dead time is used.

Dead time is automatically calculated by the device based on the values of integration duty cycle and readout time. If *lumped_dead_time* is set to '0', dead time for each quad in terms of number of system clocks is given by Equation 1:

$$quad\ dead\ time = pix_cnt_max \times (1 - integration\ duty\ cycle) - (sensor\ reset\ time + readout\ time) \quad (1)$$

If *lumped_dead_time* is set to '1', dead time for each frame in terms of number of system clocks is given by Equation 2:

$$\text{frame dead time} = sub_frame_cnt_\max \times quad_cnt_max \times (pix_cnt_max \times (1 - integration\ duty\ cycle) - (sensor\ reset\ time + readout\ time)) \quad (2)$$

Sensor reset time is equal to 768 system clock cycles. The readout time is given by Equation 5:

Calculation of *pix_cnt_max* is given by Equation 3:

$$\text{pix_cnt_max} = \frac{sys_clk_freq}{frame_rate \times quad_cnt_\max \times sub_frame_cnt_max} \quad (3)$$

7.3.3.3 Input Clock Generation

The system clock frequency of the TFC should be always set to 48 MHz. The input clock multiplier is set to '0' by default. Therefore, the expected input clock frequency on the SYSCLK_IN pin is 48 MHz. The TFC provides a mechanism for multiplying the input clock frequency so that a lower input clock frequency can be used. The related parameter is shown in Table 4.

Table 4. Input Clock Generation

PARAMETER	DEFAULT	DESCRIPTION
sysclk_in_freq	0	0 : 48 MHz
		1 : 24 MHz
		2 : 12 MHz
		3 : 6 MHz

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7.3.3.4 Sensor Addressing Engine

The sensor addressing engine generates the row and column address signals for the sensor. The addressing sequence can be configured to allow custom sensor readouts as per the requirements of the system.

7.3.3.4.1 Region of Interest (ROI)

A subset of the sensor array can be readout to enhance frame-rate or to reduce the power consumption of the ToF system. An ROI comprises of a set of row and column limits. The row and column counts start from zero. Row limits can be any of the valid row numbers for a given sensor size. The column beginning is always a multiple of 16 and column end is one less than a multiple of 16. The relevant parameters are listed in Table 5.

Table 5. ROI Parameters

PARAMETER	DEFAULT	DESCRIPTION
row_start	0	Start address for row address bus
col_start	0	Start address for column address bus col_start = (start address) >> 4
row_end	239	End address for row address bus
col_end	19	End address for column address bus col_end = (end address) >> 4

Sensor readout time is affected by ROI. A minimum row to row switching time of half the row readout time is enforced internally. Hence, reducing the column count to less than half of the total no. of columns for a given sensor will not lead to reduction in sensor readout time. For number of columns greater than total number of columns divided by 2:

$$\text{read out time} = preparation\ time + \frac{no.of\ rows \times no.of\ columns}{2}\ (Measured\ in\ system\ clock\ cycles) \quad (4)$$

For number of columns lesser than half of the total number of columns:

$$\text{read out time} = preparation\ time + \frac{no.of\ rows \times total\ number\ of\ columns}{4}\ (Measured\ in\ system\ clock\ cycles) \quad (5)$$

where:

- Preparation time = 401 + total number of columns (Measured in system clock cycles)

7.3.3.4.2 Readout Sequence

Readout sequence can be controlled to achieve mirroring along vertical axis. The programmable parameters are listed in Table 6.

Table 6. Readout Sequence Parameters

PARAMETER	DEFAULT	DESCRIPTION
col_rdout_dir	1	0: Horizontal inversion disabled
		1: Horizontal inversion enabled

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7.3.3.5 Integration Time

Integration time is the time during which the sensor demodulation and the illumination modulation are active. The configurable parameters are listed in Table 7.

Table 7. Integration Time Parameters

PARAMETER	DEFAULT	DESCRIPTION
intg_duty_cycle	6	This parameter controls the ratio of integration time to total frame time.
intg_duty_cycle_set_failed	0	This flag indicates if the intg_duty_cycle setting has taken effect. If the intg_duty_cycle is not feasible for a given set of conditions, this flag is set. It is cleared when a feasible value of intg_duty_cycle is programmed. If this flag is set, a lower value of intg_duty_cycle has to be programmed and the value of the flag checked again. This process has to be repeated till the flag clears.
normal_frm_intg_scale	0	Scaling of integration time.

The *intg_duty_cycle* registers allows 64 settings from 0 to 63. The relation between effective integration duty cycle and the register value is given by Equation 6:

$$\frac{Intg_duty_cycle}{2^{normal\ _frm_intg_scale}} = \frac{Integration\ duty\ cycle\ \times 64}{100} \tag{6}$$

Internally, integration time is set to a minimum of 1024 system clock cycles. Maximum integration duty cycle is given by Equation 7:

$$maximum\ integration\ duty\ cycle\ = \frac{pix_cnt_\max - (reset\ time + readout\ time)}{pix_cnt_max} \tag{7}$$

The intg_duty_cycle parameter has to be reprogrammed whenever any of the registers related to frame rate control or region of interest are programmed. The related registers are:

- quad_cnt_max
- sub_frame_cnt_max
- pix_cnt_max
- lumped_dead_time
- row_start
- col_start
- row_end
- col_end

When OPT9221 is in slave mode, the duty cycle will still correspond to the frame length calculated as per the internal registers and not as per the period of the external sync signal. The sync signal period should be large enough to make sure that the frame data is streamed successfully. When the sync signal period is larger than the internal frame period, actual integration duty cycle will be lesser than the programmed value.

7.3.3.5.1 High Dynamic Range Functionality

When high dynamic range functionality is enabled, alternate frames can use different integration times. The HDR frame's integration time is scaled down as compared to a normal frame by a factor. The relevant parameters are listed in Table 8.

Table 8. High Dynamic Range Functionality Parameter

PARAMETER NAME	DEFAULT	DESCRIPTION
hdr_frm_intg_scale	0	Additional scaling of integration time during the HDR frame

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$$HDR\ \ frame\ integration\ time = \frac{normal\ \ frame\ integration\ time}{2^{hdr_frm_intg_scale}} \quad (8)$$

7.3.3.6 Modulation Clock Generator

The sensor (OPT8241) modulation block provides the high frequency demodulation to the pixels as well as the illumination module. The sensor controls the phase between the modulation signals connected to the pixels and the illumination module from quad to quad.

7.3.3.6.1 Sensor Output Signals

Table 9. Sensor Output signals

PIN NAME	DESCRIPTION
ILLUM_P	High frequency input to the illumination driver – Non-inverting. Modulates during integration time. Low by default during rest of the time.
ILLUM_N	High frequency input to the illumination driver – Inverting. Modulates during integration time. High by default during rest of the time.
ILLUM_EN	If an external driver is used for driving the illumination current, this signal can be used to switch the driver between active and standby mode. Normally, it goes active just before the integration time and goes inactive just after the integration time. The polarities and the position of the pulse are programmable.

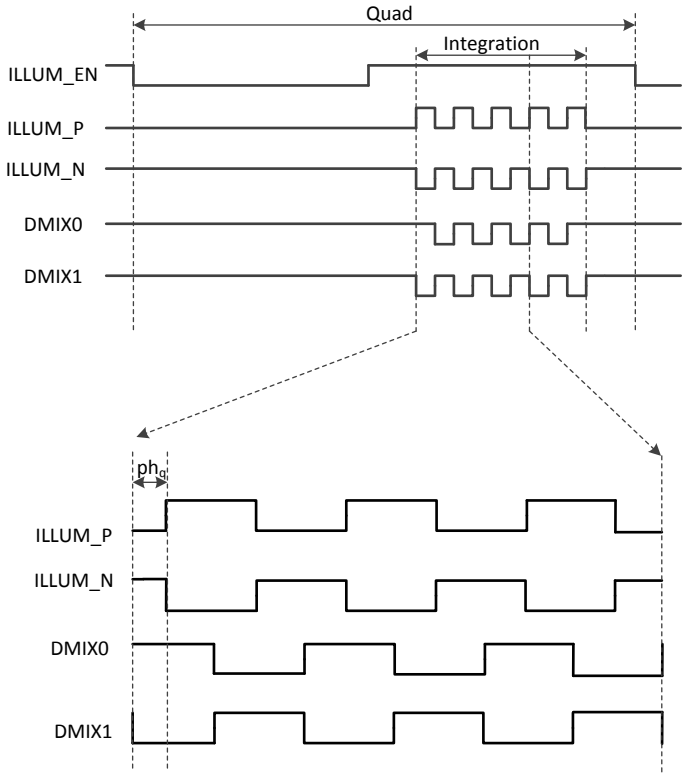

Figure 3. Timing Diagram

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The phase between illumination modulation and the sensor demodulation signals is stepped automatically as per the quad number. For example, in the case of one sub-frame having 4 quads, the phase is typically stepped between 0º, 90º, 180º and 270º. The phase stepping sequence of the sensor is programmable through TFC registers. A different sequence can be enabled for odd and even sub-frames. Also, the phase registers for base frequency and de-aliasing frequency are separately programmable. The programmable parameters are listed in Table 10 and Table 11.

Table 10. Pin Programmability

PARAMETER	DEFAULT	DESCRIPTION
modulation_hold	0	Disable modulation during integration period. Set to '0' for normal operation.
demod_static_pol	0	DC state of illumination pins during integration period if mod_static='1'.
illum_static_pol	0	DC state of illumination pins during integration period if mod_static='1'. ILLUM_P = illum_static , ILLUM_N = not (illum_static)
illum_en_early	0	Activates the illumination enable signal 15 µs before integration period starts when set to '1'.
illum_mod_early	0	Activates the illumination modulation 15 µs before integration period starts when set to '1'.
Illum_dc_corr_dir	0	Sets the direction of duty cycle correction for illumination output waveforms. Note that when duty cycle is increased, ILLUM_P duty cycle increases and ILLUM_N duty cycle decreases. 0: Increase the duty cycle 1: Reduce the duty cycle
Illum_dc_corr	0	Illumination duty cycle can be corrected in steps of about 450 ps. The maximum value of this register is 11 which results into a total correction of about +/-5 ns.

Table 11. Phase Sequence Programmability

PARAMETER	DEFAULT	DESCRIPTION
quad_hop_en	0	Enables a different sequence of quads for odd and even frames.
quad_hop_offset_f1	0	The offset of the quad sequence for alternate frames for base frequency.
quad_hop_offset_f2	0	The offset of the quad sequence for alternate frames for de-aliasing frequency
quad_cnt_max	0	The number of quads in each sub-frame

The relative phase of illumination modulation with respect to sensor modulation, phq for any quad, can be calculated as shown in Equation 9:

$$Ph_q = 360 \times \frac{quad\ number}{quad_cnt_max} \tag{9}$$

Note that the quad number is offset by the flicker cancel offset for that sub-frame.

effective quad number = quad number + quad hop offset

7.3.4 Output Interface

The TFC has a programmable parallel CMOS output interface module, which gives an option to connect the TFC to wide variety of host processors.

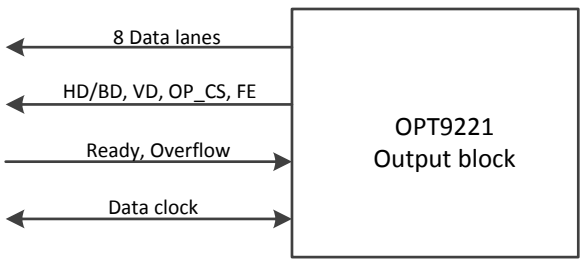

Figure 4. Output Interface Module

Table 12. Output Interface Pins

PIN NAME	FUNCTIONALITY
OP_CLK	Output interface clock. The clk frequency is controlled internally to meet the frame-rate requirement. Alternatively, clock can be supplied from an external host. All the output interface signals transition on the configured (positive/negative) edge of this clock. By default, the output signals transition on the negative edge of this clock.
OP_DATA [7:0]	Output CMOS data pins. By default, all the pins are used for transfer of data. In the 4-lane mode, only Data[3:0] are used. In the 1-lane mode, only Data[0] is used.
HD/BD	This signal is used as horizontal sync in the DVP mode to indicate row data transfer. In 8-lane generic CMOS mode, it is used to indicate the validity of the data available on output bus.
VD	Frame sync. It used to indicate the beginning of a new frame.
OP_CS	Chip select. This signal is used to indicate the validity of the data on the data bus. It can be used in the TI SSI mode as SSIFss.
FE	Frame-end. This signal pulses for a single clock cycle to indicate frame end.
Ready	This signal is used for flow control when enabled. Output data is buffered when the ready signal is not active.
Overflow	This signal is used by host processor to indicate buffer overflow. This is used for debug only.

7.3.4.1 Output Data Format

The depth information can be obtained with varying degrees of detail as per the host application's requirements using register control. The two options available are listed below:

7.3.4.1.1 4-Byte Mode (default)

- 12 bits amplitude (C)
- 4 bits ambient (A)
- 12 bits phase (P)
- 4 bits flags (F)

Byte 3								**Byte 2**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Flags[3:0]				Phase[11:0]											

Byte 1								**Byte 0**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Ambient[3:0]				Amplitude[11:0]											

Ambient and amplitude information together form a 16-bit word with ambient in the MSBs. Flags and phase information together form a 16-bit word with flags in the MSBs.

There are two modes of arrangement possible :

Contiguous

C0, A0	**P0, F0**	**C2, A2**	**P2, F2**	**C3, A3**	**P3, F3**	**…….**
Pixel0		Pixel1		Pixel3		……

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Group by 8 (default)

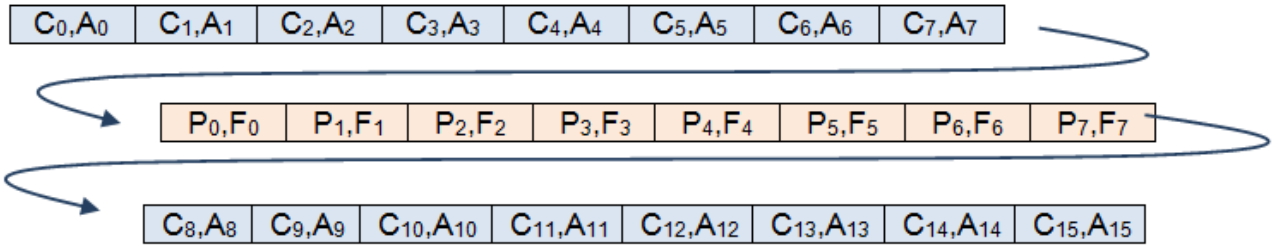

Figure 5.

7.3.4.1.2 2-Byte Mode

- 4 bits amplitude (C)
- 12 bits phase (P)

Byte 1								Byte 0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Amplitude [3:0]				Phase[11:0]											

Amplitude and phase information together form a 16-bit word with confidence in the MSBs

P0	C0	P1	C1	P2	C2	P3	C3	P4	C4	P5	C5	…….

7.3.4.1.3 Register Controls

Table 13. Register Controls

PARAMETER	DESCRIPTION
pixel_data_size	0: 2 byte mode 1: 4 byte mode(default)
op_data_arrange_mode	0: continuous 1: reserved 2: rearrange in groups of 8 (Default) 3: reserved Needs to be explicitly set to 0 when not using 4-byte mode

7.3.4.2 Frame Fragmentation

Every frame of data can be broken into blocks before being sent out. The block size is controlled using register settings. In DVP mode, the block size matches the row size of the ROI. In other modes, block size can take any value between 1 byte and the total frame-size. The blanking period between the blocks is also configurable. If the last block is smaller than the block size, padding can be enabled to append the data with data zeros. Frame and block level headers can be enabled to get UVC compatible data stream. An external parallel to USB conversion can be employed to achieve UVC streaming on to a USB host.

7.3.4.3 Data Output Waveforms

The output VD/CS toggle after the end of last quad's readout in every frame. Depending on the configured output mode, the relation of VD/CS with data output changes. This sub-section describes the output waveforms for the supported output modes.

7.3.4.3.1 8-Lane Mode – DVP

DVP mode outputs the array data row by row. A frame marker and a row marker are used to indicate the frame and row boundaries respectively. Output data order is least significant byte first.

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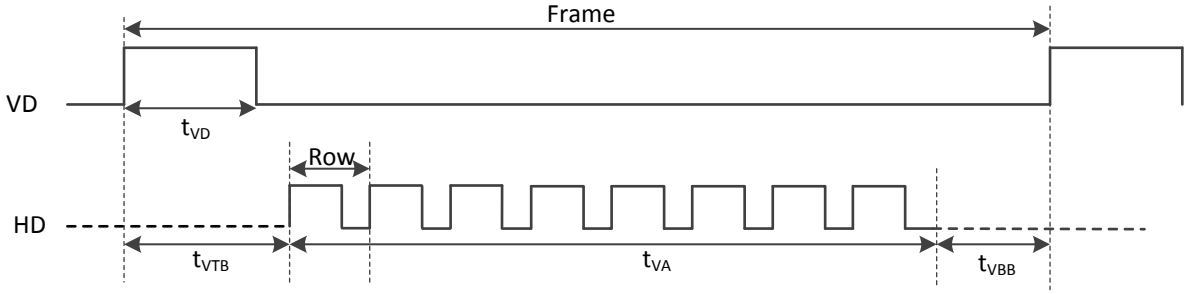

Figure 6.

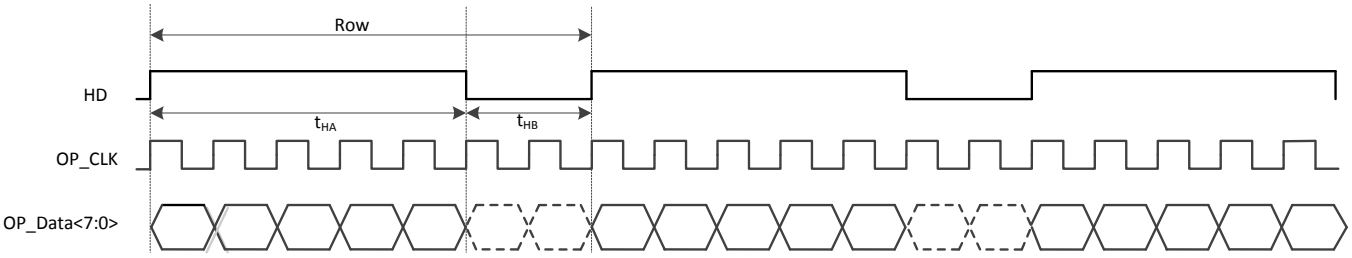

Figure 7.

Table 14. Timing Notations

TIMING NOTATION	DESCRIPTION (number of OP_CLK cycles)	PROGRAMMABLE OR CALCULATED
t_{VD}	Vertical sync time	Programmable using vd_active paramater
t_{VTB}	Vertical top blanking time	Programmable using frm_blank_size parameter
t_{VA}	Vertical active time	Calculated from ROI and binning settings
t_{VBB}	Vertical bottom blanking time	Derived from other settings in order to meet the required frame-rate
t_{HA}	Horizontal active time	Calculated from ROI and binning settings
t_{HB}	Horizontal blanking time	Programmable using blk_blank_size parameter

Table 15. Parameters

PARAMETER	DESCRIPTION
hd_pol	Polarity of HD signal. The default polarity is '1' (active high)
vd_pol	Polarity of the VD signal. The default polarity is '1' (active high)
fe_pol	Polarity of the FE signal. The default polarity is '1' (active high)
fe_last_cycle	0: Activate frame end signal along with the last byte of data. 1: Activate frame end signal one output clock cycle after the last byte of data.

7.3.4.3.2 8-Lane Mode – Generic Parallel Interface

In addition to the features available in the DVP mode, the HD/BD width is independent of the sensor readout image width and is programmable as per the requirements of the host in this mode. The FE signal can be used for indicating the transfer of the last byte. Therefore, it is one clock wide. DVP mode outputs the array data row by row. Output data order is least significant byte first.

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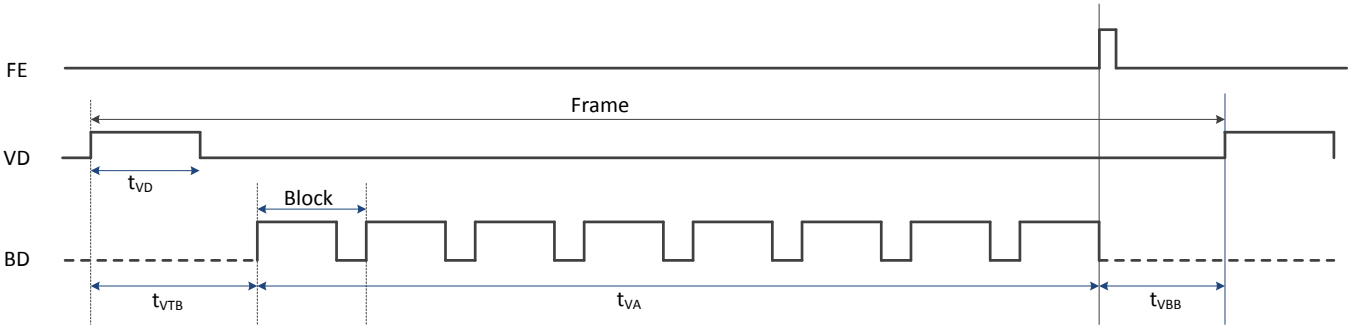

Figure 8.

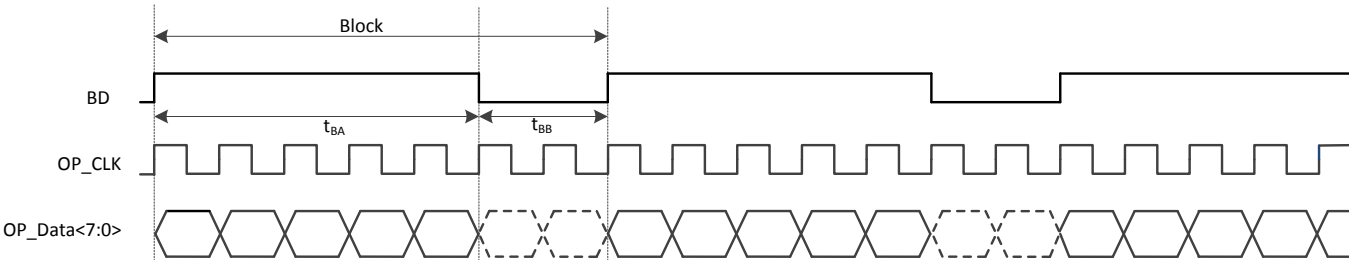

Figure 9.

Most of the timing controls are the same as in the case of DVP mode. The changes are listed in Table 16.

Table 16.

TIMING NOTATION	DESCRIPTION (number of OP_CLK cycles)	PROGRAMMABLE OR CALCULATED
t_{BA}	Block active time	Programmable using the blk_size parameter
t_{BB}	Block blanking time	Programmable using blk_blank_size parameter

Most of the programmable parameters are common with the DVP mode. The changes are listed in Table 17.

Table 17.

PARAMETER	DESCRIPTION
fb_ready_en	Ready feedback signal enable. When ready is inactive, the TFC stops sending out data till the line goes active. This is useful for cases where the host may be temporarily busy.
fb_ready_pol	Sets the polarity of the ready signal. 0: active low 1: active high(default)

The FE signal can be programmed to come along with the last byte or one clock cycle later. By default, it comes one clock cycle later.

7.3.4.3.3 4-Lane Mode – SSI

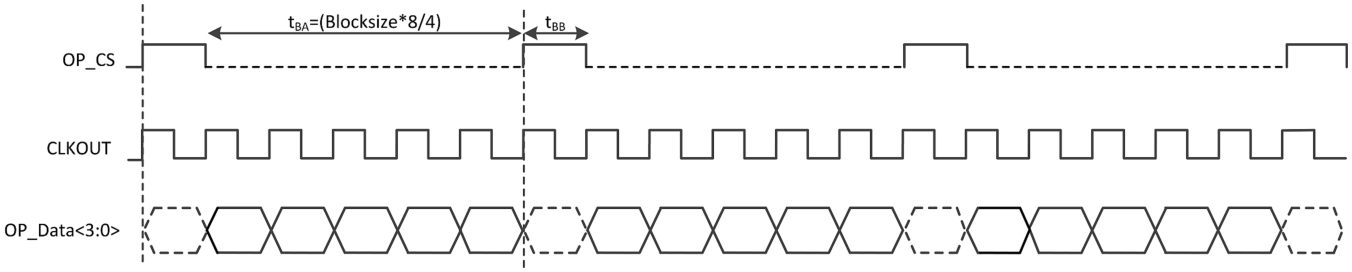

Figure 10.

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Table 18.

TIMING NOTATION	DESCRIPTION (Number of OP_CLK cycles)	PROGRAMMABLE OR CALCULATED
t_{BA}	Block active time	Programmable using the blk_size parameter. t_{BA}= blk_size × 2
t_{BB}	Block blanking time	Programmable using blk_blank_size parameter

Chip-select (OP_CS) signal indicates the validity of the data presented on Data[3:0]. For example, if a block-blanking period of 2 clocks and a block-size of 4 bytes are programmed, OP_CS remains inactive of 2 clocks and become active for 8 clock cycles. Chip-select polarity is programmable using the op_cs_pol parameter.

A 4-byte header containing a unique sequence – 0xFF, 0xFF, 0xFF, 0xFF is inserted in the beginning of each frame to indicate the start of frame in this mode.

Serialization Logic in 4-Lane Mode

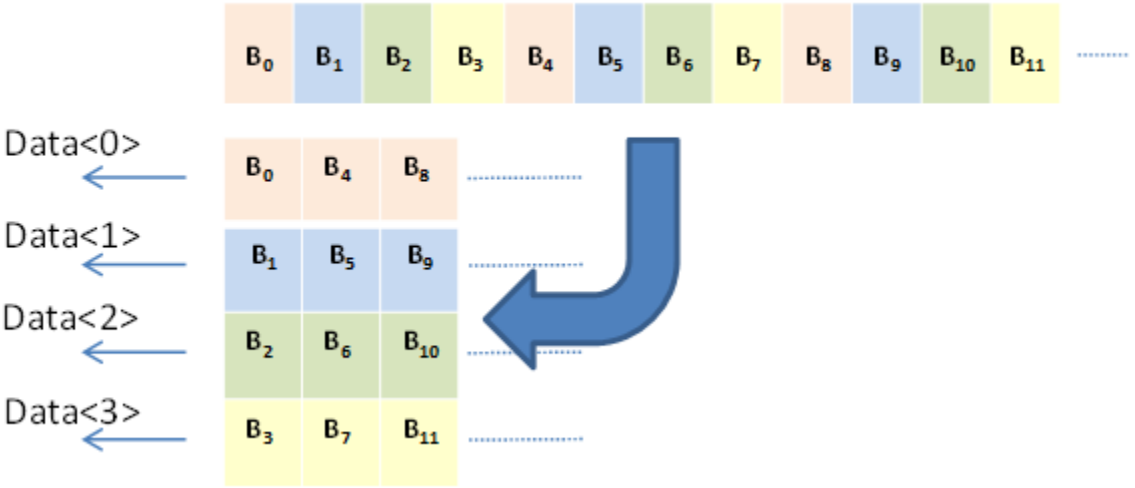

Figure 11.

Each chunk of 4-byte data is serialized and sent out on Data[3:0]. While the 1st byte is being sent out on Data[0], the successive bytes are sent on the other data lanes simultaneously. Within each byte, the LSB is sent out first.

7.3.4.3.4 1-Lane Mode – SSI

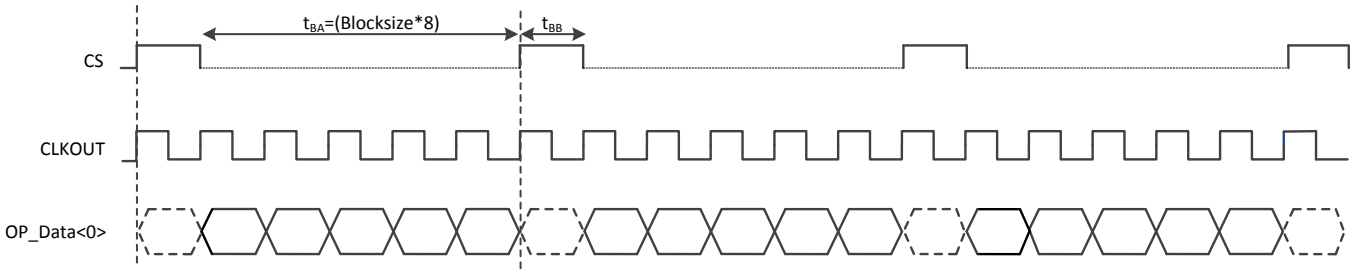

Figure 12.

Table 19.

TIMING NOTATION	DESCRIPTION (Number of OP_CLK cycles)	PROGRAMMABLE OR CALCULATED
t_{BA}	Block active time	Programmable using the blk_size parameter. t_{BA}= blk_size × 8
t_{BB}	Block blanking time	Programmable using blk_blank_size parameter

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Chip-select (OP_CS) indicates the validity of the data presented on Data[0]. For example, if a block-blanking period of 2 clocks and a block size of 4 bytes are programmed, OP_CS remains inactive of 2 clocks and remain active for 32 clock cycles. Chip-select polarity is programmable using the op_cs_pol parameter.

A 4-byte header containing a unique sequence – 0xFF, 0xFF, 0xFF, 0xFF is inserted in the beginning of each frame to indicate the start of frame in this mode .

Serialization Logic in 1-Lane Mode

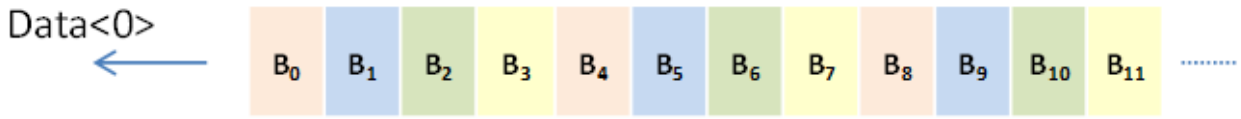

Figure 13.

Each byte of data is serialized and sent out on Data[0]. Within each byte, the LSB is sent out first.

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7.3.4.3.5 Register Controls

Table 20. Register Control Parameters

PARAMETER	DESCRIPTION
op_mode	0: Generic parallel mode(default) 1: DVP mode 2: Serial mode
op_cs_pol	Polarity of op_cs signal 0: active low 1: active high
op_serial_width	0: 1-lane SSI 1: 4-lane SSI
padding_en	In modes other than the DVP mode, enables padding of zeros at the end of the frame if the last packet is smaller than the set packet size. In DVP mode, padding is always enabled and this parameter has no effect.
frm_header_en	Enables frame level header. In the generic parallel and DVP modes, this is a 12 byte UVC header (for bulk transfers). In the serial modes, a 4 byte pattern (0xFF, 0xFF, 0xFF, 0xFF) is always enabled and this parameter has no effect.
blk_header_en	When enabled, a 12 byte UVC header for every packet is inserted.
op_clk_freq	Output clock frequency. 0: 24MHz 1: 12MHz 2: 6MHz 3: 3MHz
op_clk_edge	Data transitions on the configured edge of the output clock. 0: Falling edge(default) 1: Rising edge

Output timing parameters have to be programmed so that all the data in each frame is transferred out within one frame time. Also, the output clock frequency has to be programmed to make sure that the output data rate demand is met by the depth engine. The equation for maximum output clock rate is given by Equation 10:

$$output\ clock\ frequency \leq \frac{96 \times pixel\ data\ size}{sub_frame_cnt_max \times quad_cnt_max} \tag{10}$$

where

- Where, pixel data size is set by the pixel_data_size register.

7.3.5 Modulation Frequency

The OPT8241 sensor has 2 PLLs internally for generating the base modulation frequency (MOD_F1) and the de-aliasing frequency (MOD_F2). The formula for calculating the modulation frequency is given in Equation 11:

$$MOD_Fx = \frac{MOD_Mx \times 48\ MHz}{2^{(MOD_Nx-1)} \times quad_cnt_\max \times (1+MOD_PSx)} \tag{11}$$

Internal VCO frequency is given by Equation 12:

$$VCO_freq = \frac{MOD_{Mx} \times 48\ MHz}{2^{(MOD_Nx-1)}} \tag{12}$$

MOD_M and MOD_N should be chosen to meet the internal VCO frequency range limitation. The internal VCO can operate between 300 MHz and 600 MHz. The PLL block diagram is shown in Figure 14:

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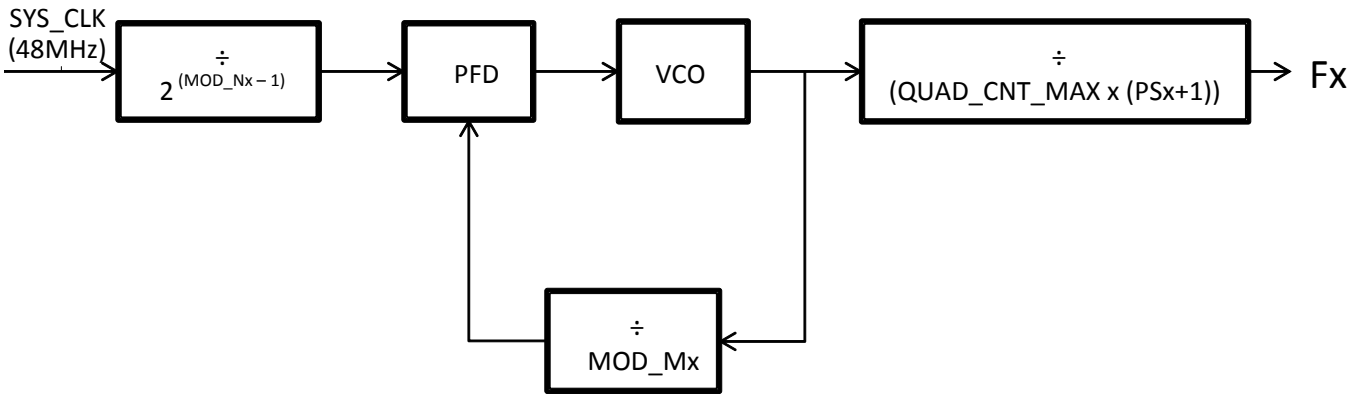

Figure 14. Modulation PLL Block Diagram

To enable accurate setting of desired modulation frequency, Mod_m is split into an integer and a fractional part. The effective mod_m is given by Equation 13:

$$effective\ MOD_M = mod_m + \frac{mod_m_frac}{2^{16}} \tag{13}$$

The programmable parameters are listed in Table 21. The default modulation frequency on start-up is 48 MHz.

Table 21. Programmable Parameters

PARAMETER	DEFAULT	DESCRIPTION
mod_m1, mod_m2	16	VCO multiplier
mod_m_frac1, mod_m_frac2	0	VCO multiplier
mod_n1, mod_n2	2	VCO divider
mod_ps1, mod_ps2	1	Divider for generation of base modulation frequency
mod_pll_update	0	Set this bit to 1 and back to 0 for updating any modulation frequency setting. The update starts on the positive edge.

7.3.6 LVDS Receiver and Deserializer

The data input interface has standard LVDS receivers with external terminations. It consists of 3 data lanes, 1 frame-clk lane and 1 bit-clk lane. Each data lane expects 12-bit serialized data. The input interface is compatible with the TI ToF integrated ADC+TG+sensor - OPT8241.

The raw data is de-serialized and preprocessed before it gets supplied to the depth engine

7.3.7 Depth Engine

The depth engine calculates the phase and amplitude information using the data obtained from the input block. It uses the DDR memory to temporarily store data obtained and processes it. It has the following features :

- Phase/amplitude calculation
- Temperature calibration
- Binning
- De-aliasing
- Histogram

7.3.7.1 Phase Data

The computed phase for each pixel is proportional to the distance of the corresponding object in the scene. For a phase varying from 0 to 2π, the distance varies from 0 to R where R is the unambiguous range.

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$$d = \frac{phase \times R}{2\pi} \tag{14}$$

$$R = \frac{C}{2F} \tag{15}$$

where

- C is speed of light
- F is the modulation frequency

At the output of the depth processor block, phase of 2π is typically represented by a full 12-bit code. That is, 2^{12}. If the application requires knowledge of the distance (in meters) of the points in the scene, it must be calculated from the TFC output using the following formula:

$$d = \frac{phase \times R}{2^{12}} \tag{16}$$

The above formula assumes that the phase has no offset. If offset correction is not done within the TFC, the formula is:

$$d = \frac{(phase - offset) \times R}{2^{12}} \tag{17}$$

The sensor data collected in the quads is used to compute the phase information. The quad information is then used to compute in-phase and quadrature components as shown in Equation 18:

$$I = \sum_{n=0}^{n=N} Q_n Cos\left(\frac{2\pi n}{N}\right)$$

$$Q = \sum_{n=0}^{n=N} Q_n Sin\left(\frac{2\pi n}{N}\right)$$

$$Phase = tan^{-1}\frac{Q}{I} \tag{18}$$

where

- 'N' is the number of quads in each sub-frame and 'n' is the quad index. The Cos and Sin coefficients need to be programmed into the TFC as per the number of quads. The default coefficients are programmed for 4 quads.

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Each parameter in the register set is a coefficient represented in 16-bits signed representation. The formula for calculating the parameter is shown in Equation 19:

$$cos_fx_qn_coeff = 32767 \times Cos\left(\frac{2\pi n}{N}\right)$$

$$sin_fx_qn_coeff = 32767 \times Sin\left(\frac{2\pi n}{N}\right)$$

where

- n is the index of the coefficient, 'x' represents the frequency (base or de-aliasing frequency). N is the number of quads (same as quad_cnt_max). (19)

When de-aliasing is not enabled, the default number of quads is 4. To use 6 quads without de-aliasing, the following configuration has to be programmed.

- Reduce the number of sub-frames (sub_frame_cnt_max) to 2 or reduce the output clock to 12 MHz (op_clk_freq).
- Program base frequency (f1) to desired value.
- Set the number of quads (quad_cnt_max) to 6.
- Set ind_freq_data_sel to '1' to use the alternate set of coefficients to process the obtained data.
- Set cos_f2_qn_coeff and sin_f2_qn_coeff registers to the appropriate values.

7.3.7.2 De-Aliasing

Unambiguous range of a ToF system is defined by the modulation frequency (F). It is given by the equation Equation 20:

$$R = \frac{C}{2F}$$

where

- C is the speed of light in the medium. (20)

For example, for a modulation frequency of 50 MHz, R = 3m in open air. If the total range of the application is beyond the unambiguous range for a given modulation frequency, de-aliasing can be enabled to extend the unambiguous range. This technique employs two modulation frequencies.

The unambiguous range is given by Equation 21:

$$R = \frac{C}{2 \times GCD(F1, F2)} \quad (21)$$

The de-aliasing filter implemented in the depth processor computes the unambiguous phase automatically when de-aliasing is enabled.

7.3.7.2.1 Procedure for Enabling the De-Aliasing Mode

1. Disable the timing generator using the *tg_dis* parameter.
2. set *quad_cnt_max* parameter to 6.
3. Set the base frequency and de-aliasing modulation frequency as described in Modulation Clock Generator section. Always ensure that base frequency is lower than the de-aliasing frequency.

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4. Set the de-aliasing coefficients as shown in Setting the De-Aliasing Coefficients.
5. Set the phase calibration parameters for each frequency as described in Phase Offset Correction section.
6. Set *sub_frame_cnt_max* count to meet the relation (refer Equation 10) between *sub_frame_cnt_max* and *quad_cnt_max.*
7. Set *pix_cnt_max* to meet frame rate requirements.
8. Set *dealias_en* parameter to 1.
9. Enable the timing generator using the *tg_enable* parameter.

When de-aliasing is enabled, for the purpose of calibration, streaming of individual frequency data can be enabled in place of de-aliased data using the parameters in Table 22.

Table 22.

PARAMETER	DEFAULT	DESCRIPTION
ind_freq_data_en	0	Enables streaming of output data corresponding to individual frequencies. 0: disabled 1: enabled
ind_freq_data_sel	0	0: Stream output data corresponding to base frequency 1: Stream output data corresponding to de-aliasing frequency

7.3.7.2.2 Procedure for Disabling the De-Aliasing Mode

1. Disable the timing generator using the tg_dis parameter.
2. Set the *pix_cnt_max*, *sub_frame_cnt_max* and *quad_cnt_max* parameters to meet the frame rate requirements and satisfy Equation 10.
3. Set the base frequency as described in Modulation Clock Generator section.
4. Set the phase calibration parameter for base frequency as described in Phase Offset Correction section.
5. Set dealias_en parameter to 0.
6. Enable the timing generator using the tg_dis parameter.

7.3.7.2.3 Setting the De-Aliasing Coefficients

The parameters *ma* and *mb* have to be chosen such that the following conditions are met:

$$\frac{ma}{mb} = \frac{f1}{f2} \quad and \quad GCD(ma, mb) = 1 \tag{22}$$

And the parameter *freq_ratio* has to be programmed to match the ratio between the two frequencies as shown in Equation 23:

$$freq_ratio = \frac{f1 \times 4096}{f2} \tag{23}$$

Where, f1 is the base frequency and f2 is the de-aliasing frequency. The coefficients *ka* and *kb* have to be chosen such that (ka × ma) - (kb × mb) = 1

7.3.7.2.4 Scaling of Phase

The de-aliased phase is internally masked. The mask is programmable using a register configuration as shown by Equation 24:

$$phase\ output = ((dealiased\ phase \times ma \times mb) \gg (5 - dealiased_ph_mask)) \,\&\, 0FFFh \tag{24}$$

Where,

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$$dealiased\ phase = \frac{d \times 2^{12}}{R} \tag{25}$$

Where, R is the total unambiguous range.

The internal de-aliased phase is 16-bit wide. But the final phase output is only 12 bit. The application of the mask leads to a scaling in the output. Therefore, to correctly calculate the distance, Equation 26 should be used in the external host.

$$d = \frac{phase \times R \times 2^{(5-dealiased_ph_mask)}}{ma \times mb \times 2^{12}} \tag{26}$$

Programmable parameters are listed in Table 23.

Table 23.

PARAMETER	DEFAULT	DESCRIPTION
dealiased_ph_mask	0	The mask for the getting the output phase from the calculated de-aliased phase. The mask is 16bits wide. The least significant bit of the mask is given by the following relation. LSB=5-dealiased_ph_mask.

Example:

Table 24.

F1 = 18 MHz	F2 = 24 MHz
ma = 3	mb = 4
Unambiguous range = 8.33 m	Unambiguous range= 6.25 m

Therefore, the total unambiguous range with de-aliasing is given by Equation 27:

$$R = \frac{C}{2 \times GCD(18MHz, 24MHz)} = 25m \tag{27}$$

For a value of 20m, the value of de-aliased phase is given by Equation 28:

$$\text{dealiased phase} = \frac{20 \times 2^{12}}{25} = 3276 \tag{28}$$

If the default value of *dealised_ph_mask* is used, the phase output for 20m will be given by Equation 29:

$$phase\ output = ((3276 \times 3 \times 4) \gg (5))\ \&\ 0FFFh = 1228 \tag{29}$$

At the host, the original distance value can be calculated as shown by Equation 30:

$$d = \frac{1228 \times 25 \times 2^5}{3 \times 4 \times 2^{12}} = 19.99 \tag{30}$$

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7.3.7.2.5 LSBs in the De-Aliased Phase

In some applications, it is desirable to get range extension without losing the least significant bits. As explained in the above sub-section, by default only 12 bits of phase output are available. To get additional 4 LSBs of the phase output, the following parameter can bet set as shown in Table 25.

Table 25.

PARAMETER	DEFAULT	DESCRIPTION
dealias_16bit_op_enable	0	Enables 16-bit output of de-aliased data. This mode is available only if pixel_data_size is set to 4-byte mode.

LSBs of de-aliased phase are available in-place of ambient data. Therefore, ambient data will not be available when using 16-bit de-aliased phase output.

7.3.7.3 Binning

Multiple pixel data can be averaged to form a single large pixel data. This feature is useful in cases where the application requires lesser pixel resolution but needs better phase noise performance. Any number of rows/columns can be binned. The programmable parameters are listed in Table 26.

Table 26. Binning Parameters

PARAMETER	DEFAULT	DESCRIPTION
rows_to_merge	1	Number of rows to merge
cols_to_merge	1	Number of columns to merge
bin_row_count	240	Number of rows after binning.
bin_col_count	320	Number of rows after binning

Note that *bin_row_count* and *bin_col_count* need to be programmed explicitly. For example, if the *rows_to_merge*=7, *bin_row_count* = floor(total no of rows / 7) = floor(240/7) = 34.

7.3.7.4 Spatial Filter

A simple 3 x 3 spatial filter is implemented inside the TFC. The filter operates on the phase vectors represented by I + jQ. The spatial filter coefficients are arranged as shown in Table 27.

Table 27.

0 + 0j	Y coefficient	0 + 0j
X coefficient	1 + 0j	X coefficient
0 + 0j	Y coefficient	0 + 0i

The relevant parameters are listed in Table 28.

Table 28.

PARAMETER	DESCRIPTION
filt_en	Enable spatial filter
filt_scale	Filters are scaled down by $2^{(2 + \text{filt_scale})}$.
filt_coeff_x_re _f1, filt_coeff_x_im _f1, filt_coeff_y_re _f1, filt_coeff_y_im _f1, filt_coeff_x_re _f2, filt_coeff_x_im _f2, filt_coeff_y_re _f2, filt_coeff_y_im _f2,	Filter Coefficients. Represented as 8-bit signed numbers

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7.3.7.5 Auxiliary Depth Data

Amplitude data represents the amplitude of the received signal at each pixel. If the amplitude is higher, signal amplitude is higher and hence the phase SNR is higher. The value of amplitude output is given by Equation 31.

$$\text{Amplitude} = 2^{12} \times \text{Signal Amplitude} \times 1.65 \quad (31)$$

Where, the signal amplitude is the amplitude of the single ended modulating signal (A or B) generated on the pixel in each quad. When binning is enabled, signal amplitude is the vector sum of the signals of all the binned pixels divided by the nearest power of two which is greater than the number of pixels binned together.

Ambient data is an indicator of the non-modulating component of voltage on the pixels. It is the sum of the ambient light, pixel offsets and the non-demodulated component of ToF illumination. The output ambient data values decrease with increase in voltage. Therefore, near zero values indicate pixel saturation.

The TFC provides masking of data based on the value of amplitude and single ended voltage in a pixel for the purpose of basic filtering. The related parameters are listed in Table 29.

Table 29. Auxiliary Depth Data Parameters

PARAMETER	DEFAULT	DESCRIPTION
amplitude_threshold	0	If the amplitude of the pixel is lower than this number, the pixel phase data is set to FFFh.
iq_scale	0	Left shifts the acquired sensor data by the configured value. The scaling results into an equivalent scaling in amplitude. Care must be taken to avoid bit overflow in the depth processor as this scaling is done before the computation of phase and amplitude. If a bit overflow occurs, it is indicated by digital saturation flag in the flags part of the data stream.
amplitude_post_scale	0	Left shifts the computed amplitude by the configured value. If the amplitude of any pixel exceeds the full scale value, the amplitude is clipped to FFFh.
saturation_threshold	0	Saturation flag is set if the ambient value of the pixel is lesser than or equal to this value. Also, pixel phase data is set to 000h.

Flags[3:0] indicate important pixel data reliability parameters. The flags are described in Table 30.

Table 30. Pixel Data

FLAG BIT	DESCRIPTION
Flag[3]	0 : No pixel saturation 1 : Pixel is saturated
Flag[2]	For the first pixel in the frame : 0 : Normal frame 1 : HDR frame Remaining pixels: 0 : No digital saturation detected 1 : Digital pipeline saturated
Flag[1]	Reserved
Flag[0]	Reserved

7.3.8 Calibration

7.3.8.1 Phase Offset Correction

Time delay between sensor modulation and the illumination modulation manifests itself as a phase offset. Since it may vary from one system to another, the offset has to be calibrated individually for each system. The measured offset can be programmed into a phase_corr parameter in the TFC registers. The TFC subtracts the phase_corr parameter to the computed phase. The programmable parameters are listed in Table 31.

Table 31. Phase Offset Correction Parameters

PARAMETER	DESCRIPTION
phase_corr_1	Phase offset correction for base frequency
phase_corr_2	Phase offset correction for de-aliasing frequency

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Table 31. Phase Offset Correction Parameters (continued)

hdr_phase_corr_1	Phase offset correction for base frequency during HDR frame
hdr_phase_corr_2	Phase offset correction for de-aliasing frequency during HDR frame
disable_offset_corr	Disables phase offset correction in the TFC. Phase offset correction is enabled by default.

Due to temperature variations, system delays in the illumination and sensor modulation path can vary differently. This variation leads to a change in the measured phase. To compensate for phase change vs temperature, the TFC uses two programmable temperature coefficients. The built-in temperature sensor in OPT8241 is used for measuring the ToF sensor temperature and an external I2C interface based temperature sensor is used for measuring the illumination driver temperature. The programmable parameters are listed in Table 32.

Table 32. Temperature Coefficient Parameters

PARAMETER	DESCRIPTION
tillum_calib	Illumination driver temperature when phase_corr was measured.
tsensor_calib	Sensor temperature when phase_corr was measured.
coeff_illum	Phase vs temperature coefficients for illumination driver for the base frequency.
coeff_sensor	Phase vs temperature coefficients for sensor for the base frequency.
disable_temp_corr	Disables phase offset correction due to temperature. (Temperature correction is enabled by default)
calib_prec	Scales the co-efficients. Default scaling of 16 is applied to the temperature coefficients 0 : Scaling by 1 1 : Scaling by 16

The phase correction due to temperature variation is calculated by the TFC as shown in Equation 32:

$$phase_corr_temp = \frac{coeff_illum \times (T_{illum} - T_{illum_calib}) \; + \; coeff_sensor \times (T_{sensor} - T_{sensor_calib})}{calibration\ scale} \tag{32}$$

Where, calibration scale is 1 when *calib_prec* = 0 and 16 when *calib_prec* = 1 .

When de-aliasing is not used, the final value of phase given out by the TFC is calculated as shown in Equation 33:

$$\text{Corrected phase} = Computed\ phase - (phase_corr_1 \; + \; phase_corr_temp) \tag{33}$$

When de-aliasing is used, phase correction on individual frequency measurements is applied before combining the phase information to compute the final unambiguous phase. Since individual frequency measurements may have different offsets and temperature co-efficients, the TFC provides separate correction blocks for measurements using each frequency. The temperature coefficients for the de-aliasing frequency are internally computed using the coefficients for base frequency. When de-aliasing is enabled, for the purpose of calibration, streaming of individual frequency data can be enabled in place of de-aliased data using the parameters of Table 33.

Table 33.

PARAMETER	DEFAULT	DESCRIPTION
ind_freq_data_en	0	Enables streaming of output data corresponding to individual frequencies. 0: disabled 1: enabled
ind_freq_data_sel	0	0: Stream output data corresponding to base frequency 1: Stream output data corresponding to second frequency

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7.3.8.2 Illumination Path Delay Correction Using Feedback

The illumination modulation path delay can be compensated to reduce the absolute and temperature dependent phase offsets. The illumination modulation path delay is measured using feedback from the sensor and the illumination modulation. The appropriate feedback has to be implemented in the system. A typical block diagram of such a feedback system is shown in Figure 15.

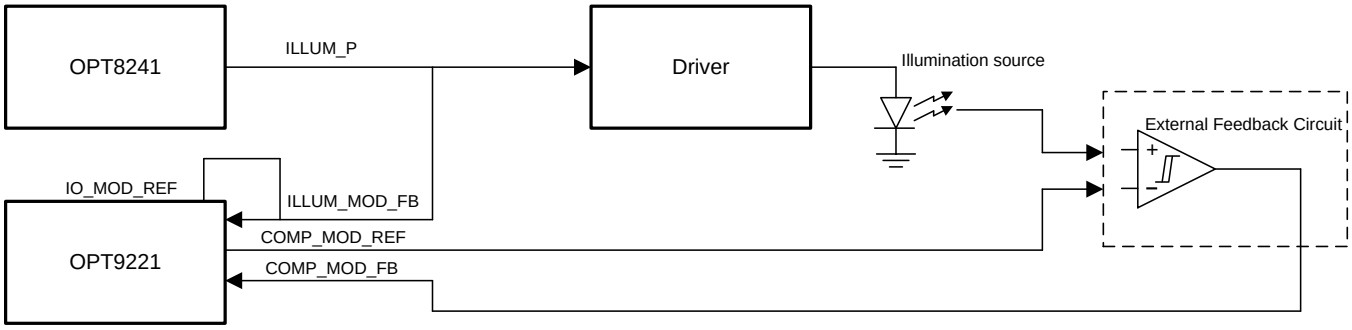

Figure 15.

The delay compensation circuit measures the delay from ILLUM_P to COMP_MOD_FB during the integration time and measures the delay of the external feedback circuit from COMP_MOD_REF to COMP_MOD_FB during sensor readout. For measuring the delay, an internal uncorrelated clock (with a frequency between 10 MHz to 50 MHz) is used to sample the feedback waveforms. The difference between the two delays measured is used as a phase offset that is used to correct the obtained phase.

Functional requirements of the feedback circuit:

- ILLUM_P output from OPT8241 should be connected to ILLUM_MOD_REF input pin of OPT9221
- The output of a feedback ckt that converts illumination current waveform to a square wave must be connected to COMP_MOD_FB pin.
- The same feedback ckt or a replica with similar delays must be driven by COMP_MOD_REF and the output must be fed back to COMP_MOD_FB pin
- The feedback circuit must have a minimum frequency of operation of 48 MHz or the operating modulation frequency (whichever is higher)

The relevant parameters for configuring the delay correction block are listed in Table 34.

Table 34.

PARAMETER	DESCRIPTION
delay_fb_corr_mode	Enabled phase correction using illumination path delay feedback and set the direction of correction.
delay_fb_dc_corr_mode	Enable using the duty cycle of the obtained feedback signal for calculating the phase compensation and set the direction of correction.
comp_mod_ref_inv	Enable inversion of feedback signal in the signal chain before evaluating the delay.
Illum_fb_inv	Enable inversion of the signal at ILLUM_FB pin in the signal chain before evaluating the delay.
fb_error_cnt_threshold	Number of errors that can be tolerated in sampling the pulses per 4096 samples.
comp_fb_error_cnt	Number of pulses not sampled correctly on the COMP_FB pin.
illum_fb_error_cnt	Number of pulses not sampled correctly on the ILLUM_FB pin.
delay_fb_coeff	Ratio of modulation frequency to 24MHz. Refer to Equation 34

The delay coefficients have to be calculated as per the below equations .

When de-aliasing is not enabled:

$$delay_fb_coeff = \frac{f1 \times 2^{10}}{24MHz} \quad (34)$$

When de-aliasing is enabled:

$$delay_fb_coeff = \frac{f2 \times 2^{10}}{24MHz} \quad (35)$$

7.3.8.3 Phase Non-Linearity Correction

Obtained phase vs distance should be ideally a straight line. But in practice, the function of phase to distance may be non-linear. To linearize the obtained phase, a lookup table can be programmed into the TFC. The lookup table is used for converting the obtained phase to linearized phase. The relevant registers are listed in Table 35.

Table 35.

PARAMETER	DESCRIPTION
phase_lin_corr_enable	Enable phase to distance non-linearity correction
phase_lin_corr_period	The period after which the non-linearity function repeats.
phase_lin_coeff1_x, phase_lin_coeff2_x	The lookup table. phase_lin_corr_coeff1_x registers correspond to the lookup table for the base frequency and the phase_lin_corr_coeff2_x registers correspond to the lookup table for the de-aliasing frequency.

The lookup table provides 16 points that are evenly spread across a period. The 16 points can be spread over 90/180/360 degrees. The first entry in the lookup table corresponds to an obtained phase value of zero. The last point in the lookup table corresponds to an obtained phase value of period × (15/16) . The spread of the points in degrees is controlled by the phase_lin_corr_period register. If the period is less than 360 degrees, the same lookup table is repeated for rest of the angles.

7.4 Device Functional Modes

7.4.1 Standby and Low-Power Modes

Various blocks of the ToF chipset can be put in low power mode using the standby functionality. The TFC has a standby pin which when asserted activates the low power operation of the chipset. The same can also be achieved using register settings. The parameters that control the low power operation are listed inTable 36.

Table 36. Parameter Description

PARAMETER	DESCRIPTION
standby_pin_en	Enables the functionality of standby pin when set to ‘1’
standby_pin_pol	Selects the active polarity of standby pin. For example, when set to ‘1’ the chipset enters low-power mode when standby pin is pulled high. Active only when standby_pin_en is set.
standby	0: Chipset is in normal operation 1: Chipset is in standby mode

7.5 Programming

7.5.1 Boot Sequence

After power up, an internal POR is asserted to reset the TFC. Once the POR is complete, the TFC enters the configuration stage. During the configuration stage, the TFC firmware is loaded through one of the configuration methods. Once the configuration is complete, INT_OUT pin is pulled low to indicate that the TFC is ready for normal operation.

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Programming (continued)

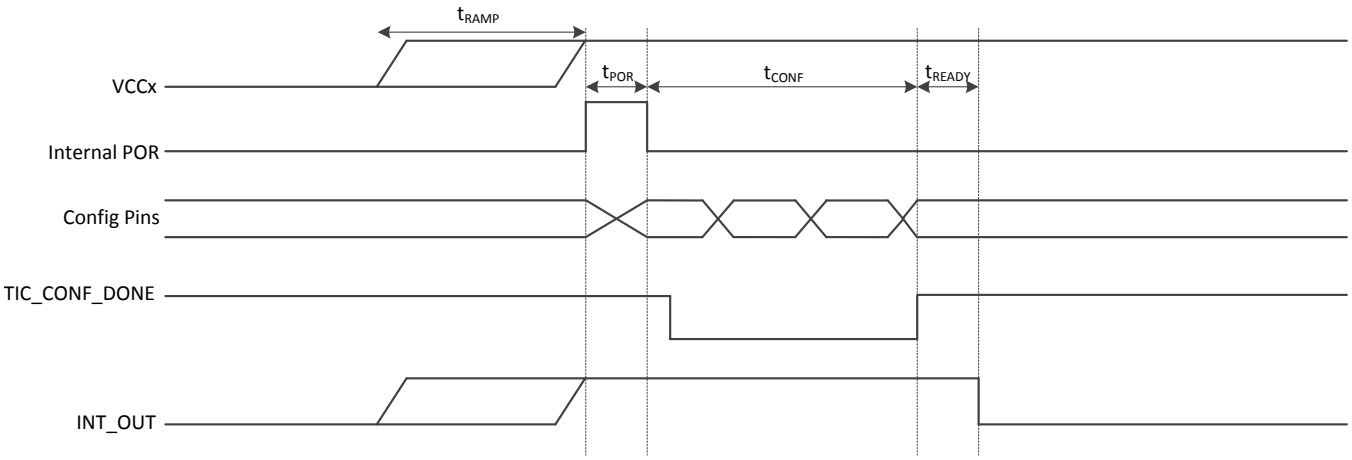

Figure 16. Boot Sequence Timing Diagram

Table 37. Boot Sequence Timing Parameters(1)

PARAMETER		MIN	MAX	UNIT
t_{RAMP}	Supply voltage ramp	50	3000	µs
t_{POR}	Reset time	50	200	ms
t_{CONF}	Configuration time. Depends on the mode of configuration and the clock rates.	-	-	
t_{READY}	Time required for TFC to be in operational state after configuration		2	ms

(1) Configuration time (t_{CONF}) depends on the mode of the configuration.

7.5.1.1 Configuration

After the POR is complete, one of the configuration methods is chosen as per the state of the BOOT[2:0] pins.

The recommended modes are listed in Table 38.

Table 38. Recommended Boot Modes

BOOT[2:0]	MODE	DESCRIPTION
011	Master serial configuration	Firmware is loaded from an external EEPROM
000	Slave serial configuration	External host loads the firmware using single data pin
111	Slave parallel configuration	External host loads the firmware using 8 data pins.

After the configuration is complete and the TFC is ready for operation the TFC pulls the INT_OUT pin low.

7.5.1.1.1 Master Serial Configuration

An external SPI EEPROM can be used to store the TFC firmware. On power-up, if the boot modes are configured for master serial configuration, the TFC reads loads the firmware from the EEPROM. During the configuration, the TIC_CONF_DONE pin is held low. Once the configuration is done, the TIC_CONF_DONE pin is released.

The recommended connections between TFC and EEPROM are shown in Figure 17. For programming the EEPROM, the TIC_CONFIGZ pin has to be pulled low and TIC_CEz has to be pulled high. This causes the TFC to put its pins in tri-state and the EEPROM can be programmed using the SPI lines. The SPI EEPROM size should be sufficient to hold the firmware. The minimum size required for storing the firmware is 4mbits. The firmware has to be programmed in the least significant bit first order into the EEPROM for proper functionality. The recommended EEPROM is W25Q04DWSSIG.

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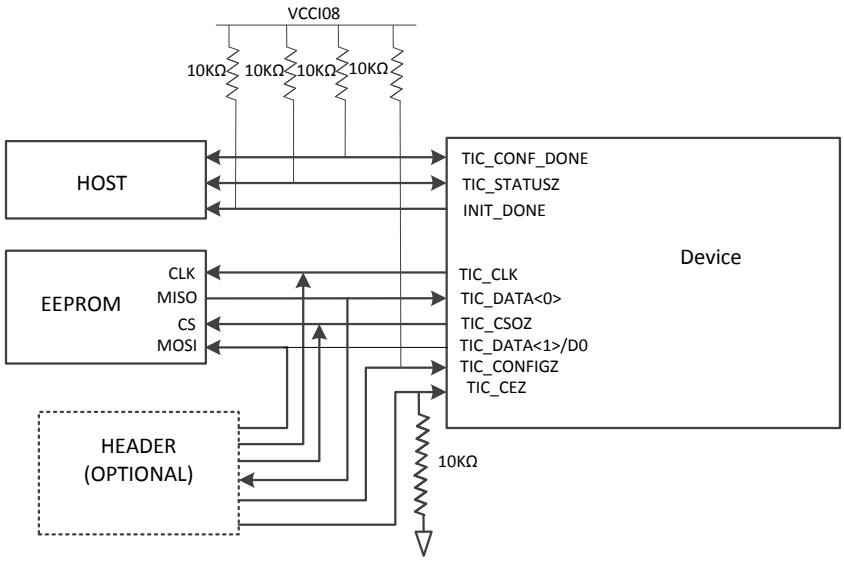

Figure 17. Recommended Connections

7.5.1.1.2 Slave Serial Configuration (SS mode)

This mode of configuration can be used to program the TFC firmware dynamically. The host processor can program the firmware after very power cycle. This method alleviates the need for a dedicated EEPROM to store the TFC firmware.

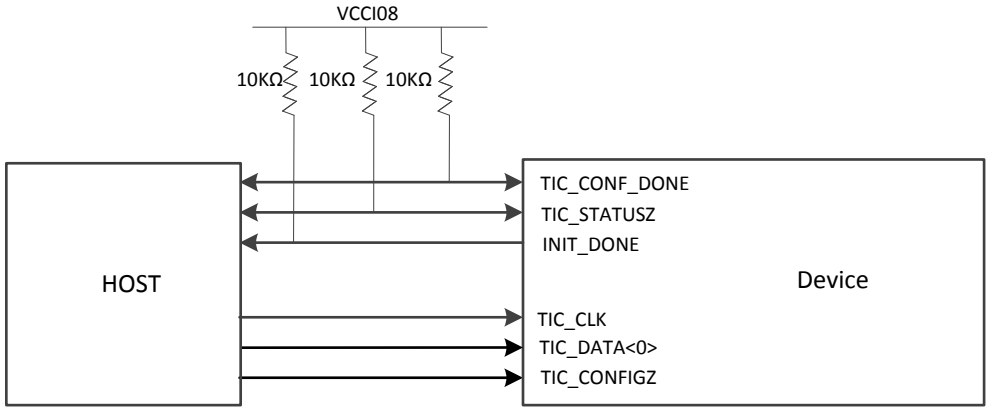

Figure 18. Connection Diagram

7.5.1.1.3 Slave Parallel Configuration (SP mode)

Slave parallel configuration is similar to the slave serial mode, but it is a faster alternative. It involves the use of 8 data lanes instead of a single lane in the SS mode.

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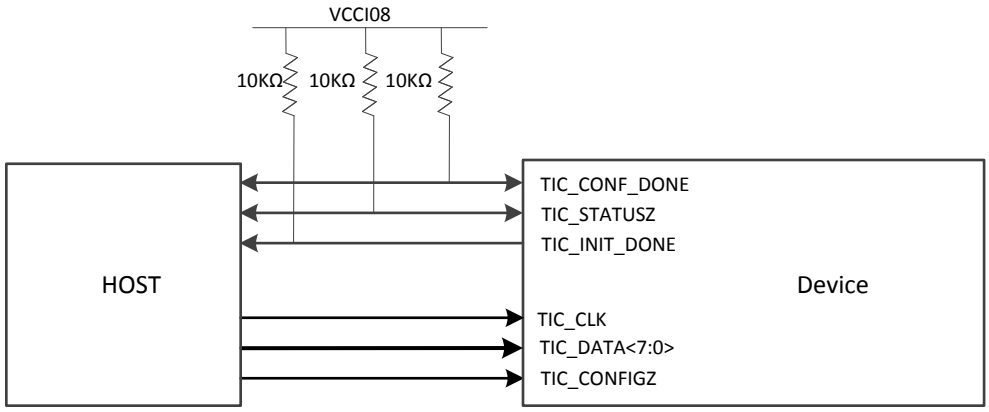

Figure 19.

7.5.1.1.4 Slave Parallel and Serial Timing

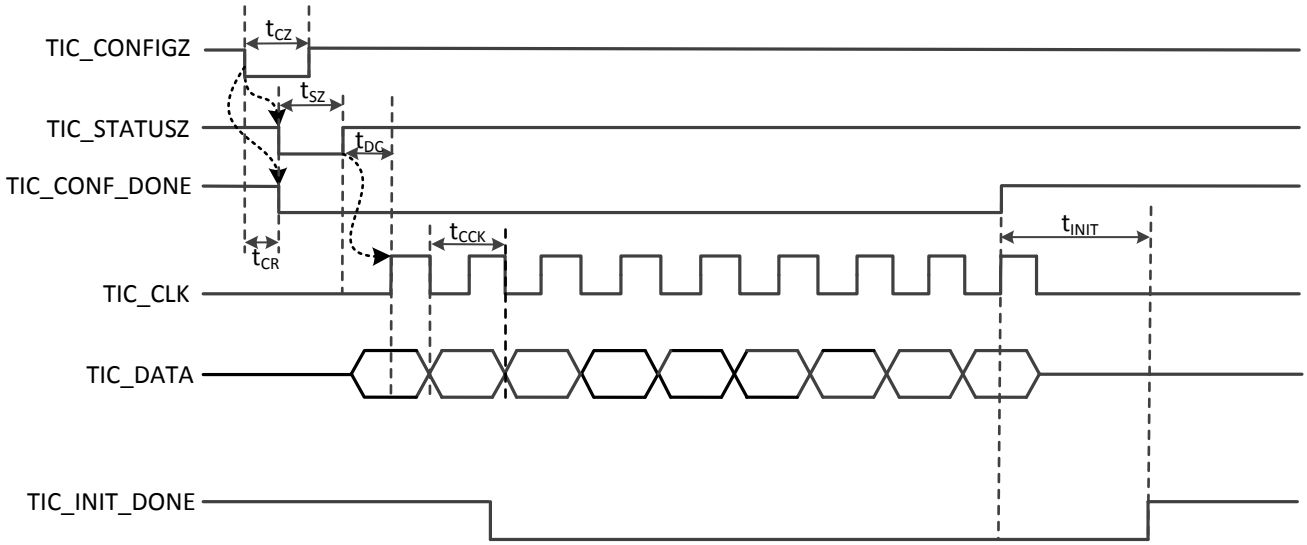

Figure 20. Slave Parallel and Serial Timing Diagram

Table 39. Slave Parallel and Serial Timing Characteristics

PARAMETER		MIN	MAX	UNIT
t_{CZ}	$\overline{\text{TIC_CONFIG}}$ low pulse duration	500		ns
t_{CR}	Delay from $\overline{\text{TIC_CONFIG}}$ falling edge to TIC_CONF_DONE falling edge		500	ns
t_{SZ}	$\overline{\text{TIC_STATUS}}$ low pulse duration	45	230	µs
t_{DC}	$\overline{\text{TIC_STATUS}}$ rising edge to configuration clock's first rising edge		2	µs
t_{CCK}	Configuration clock period	15		ns
t_{INIT}	End of configuration to start of firmware execution	300	650	µs
Duty cycle,	configuration clock duty cycle	40%	60%	
t_{CH}	Data hold time	0		ns
t_{CS}	Data setup time	8		ns
Clock edge	Configuration data is captured by the TFC on every rising edge of the configuration clock. It is recommended to clock out configuration data from the host on every falling edge of the clock.			

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To initiate the configuration, the host must pull the TIC_CONFIG pin low. The host then waits for TIC_STATUS to pulse. After the TIC_STATUS line goes high, a minimum gap of t_{DC} has to be observed before clocking out the complete configuration data. For the slave serial mode, clock out the LSB first. At the end of the configuration, TIC_CONF_DONE signal goes high again. TIC_CLK and TIC_DATA_0 are held to ground or the rail voltage after the configuration is complete. Hold the TIC_CONFIG pin high after the configuration.

7.5.2 Slave I²C Interface

The TFC can be configured by the host processor through an I²C interface. All the registers have update mechanism controls. For example, the registers that affect the frame-size such as ROI are updated only on frame VD. This feature makes the register write easy as the write operation can happen at any point of time without taking into account the state of the TFC.

The device has two slave addresses – 1011000 (0x58) and 1011100 (0x5C). The register access can be single read/write or continuous read/write with auto-increment of register address. In continuous read/write mode the appropriate register settings in I²C control register is necessary.

The individual registers are 24 bit length in this device. However, the register read/write is in chunks of eight bits. After every 8-bit transfer the slave expects an acknowledgment from the master in the case of read or gives out an acknowledgment in the case of write. The following figures explain the I²C format.



Figure 21. I²C Write Example

Table 40. I²C Register Write

Start	Slave Addr	W	Ack	Reg Addr	Ack	Reg Data(0:7)	Ack	Reg Data(8:15)	Ack	Reg Data(16:23)	Ack	Stop

For example to write X"654321" to any register, the split the data into three bytes and order as follows, X"21", X"43", X"65". The same ordering is true for read mode. The first byte of data received corresponds to (7:0), followed by (15:8) and then followed by (23:16). In the subsequent diagrams split up of data (with ack in between) is shown.

Table 41. I²C Register Read

Start	Slave Addr	W	Ack	Reg Addr	Ack	Start	Slave Addr	R	Ack	Reg Data(0:7)	Ack	Reg Data(8:15)	Ack	Reg Data(16:23)	Ack	Stop

Table 42. I²C Register Write (Continuous mode)

Start	Slave Addr	W	Ack	Reg Addr	Ack	Reg(1) Data	Ack	…	Reg(n) Data	Ack	Stop

Table 43. I²C Register Read (Continuous mode)

Start	Slave Addr	W	Ack	Reg Addr	Ack	Start	Slave Addr	R	Ack	Reg(1) Data Read	Ack	…	Reg(n) Data Read	Ack	Stop

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7.6 Register Maps

7.6.1 Serial Interface Register Map

Table 44. DE Register Map

ADDRESS (Hex)	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SOFTWARE_RESET
01h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DEVICE	MAJOR				MINOR			
02h	DEALIAS_EN	IND_FREQ_DATA_EN	0	1	0	0	0	0	0	0	MB				0	MA				0	KA			
03h	KB				0	0	0	0	0	DEALIASED_PH_MASK				0	0	0	0	0	0	0	0	0	0	0	0
04h	0	0	0	0	0	0	0	0	SIN_F1_Q0_COEFF															
05h	0	0	0	0	0	0	0	0	SIN_F1_Q1_COEFF															
06h	0	0	0	0	0	0	0	0	SIN_F1_Q2_COEFF															
07h	0	0	0	0	0	0	0	0	SIN_F1_Q3_COEFF															
08h	0	0	0	0	0	0	0	0	SIN_F1_Q4_COEFF															
09h	0	0	0	0	0	0	0	0	SIN_F1_Q5_COEFF															
0Ah	0	0	0	0	0	0	0	0	COS_F1_Q0_COEFF															
0Bh	0	0	0	0	0	0	0	0	COS_F1_Q1_COEFF															
0Ch	0	0	0	0	0	0	0	0	COS_F1_Q2_COEFF															
0Dh	0	0	0	0	0	0	0	0	COS_F1_Q3_COEFF															
0Eh	0	0	0	0	0	0	0	0	COS_F1_Q4_COEFF															
0Fh	0	0	0	0	0	0	0	0	COS_F1_Q5_COEFF															
10h	0	0	0	0	0	0	0	0	SIN_F2_Q0_COEFF															
11h	0	0	0	0	0	0	0	0	SIN_F2_Q1_COEFF															
12h	0	0	0	0	0	0	0	0	SIN_F2_Q2_COEFF															
13h	0	0	0	0	0	0	0	0	SIN_F2_Q3_COEFF															
14h	0	0	0	0	0	0	0	0	SIN_F2_Q4_COEFF															
15h	0	0	0	0	0	0	0	0	SIN_F2_Q5_COEFF															
16h	0	0	0	0	0	0	0	0	COS_F2_Q0_COEFF															
17h	0	0	0	0	0	0	0	0	COS_F2_Q1_COEFF															
18h	0	0	0	0	0	0	0	0	COS_F2_Q2_COEFF															
19h	0	0	0	0	0	0	0	0	COS_F2_Q3_COEFF															
1Ah	0	0	0	0	0	0	0	0	COS_F2_Q4_COEFF															
1Bh	0	0	0	0	0	0	0	0	COS_F2_Q5_COEFF															
1Fh	0	IQ_SCALE			0	1	0	1	0	1	0	0	0	0	1	1	0	0	1	0	0	0	0	1
25h	0	0	0	0	OP_DATA_ARRANGE_MODE		0	0	0	0	0	0	OUTPUT_MODE				0	0	0	0	0	0	0	1
27h	0	0	0	0	0	0	0	0	0	PIXEL_DATA_SIZE				0	0	0	0	0	0	0	0	0	0	0
28h	DEALIAS_16BIT_OP_ENABLE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
29h	0	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	IND_FREQ_DATA_SEL	0	PHY_TEST_ENABLE	0
2Eh	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	TILLUM_SLV_ADDR						

Register Maps (continued)

Table 44. DE Register Map (continued)

ADDRESS (Hex)	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
2Fh	BIN_ROW_COUNT										0	BINNING_EN	0	0	ROWS_TO_MERGE									
30h	BIN_COL_COUNT										0	0	0	0	COLS_TO_MERGE									
31h	0	0	0	0	0	0	0	0	0	0	FREQUENCY_SCALE				AMPLITUDE_SCALE						RAMP_PAT			MAC_TEST_ENABLE
33h	SYSCLK_IN_FREQ								0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0
35h	1	ILLUM_MOD_EARLY	ILLUM_EN_EARLY	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
36h	SATURATION_THRESHOLD												AMPLITUDE_THRESHOLD											
37h	0	0	0	0	0	0	0	0	PHASE_CORR_1												0	0	0	0
38h	0	0	0	0	0	0	0	0	PHASE_CORR_2												0	0	0	0
39h	0	0	0	0	0	0	0	0	0	0	0	DEBUG_FRAME_NUMBER_EN	0	OP_SERIAL_WIDTH	OP_MODE		0	0	OP_CLK_EDGE	0	0	OP_CLK_FREQ		0
3Ah	0	0	0	0	0	0	0	0	HDR_PHASE_CORR_1												0	0	0	0
3Bh	0	0	0	0	0	0	0	0	HDR_PHASE_CORR_2												0	0	0	0
3Ch	BLK_SIZE																				FRM_TRAILER_EN	BLK_HEADER_EN	FRM_HEADER_EN	PADDING_EN
3Dh	BLK_BLANK_SIZE																				BLK_BLANK_SKIP			
3Eh	VD_ACTIVE																				0	0	0	0
3Fh	FRM_BLANK_SIZE																				1	0	FB_READY_POL	FB_READY_EN
40h	0	0	0	FE_LAST_CYCLE	0	FE_POL	0	1	0	OP_CS_POL	0	0	0	PHASE_AUX_POL	0	PHASE_AUX_EN	0	VD_POL	0	1	0	HD_POL	0	1
47h	0	0	0	0	0	0	0	0	0	0	0	0	COEFF_ILLUM											
48h	0	0	0	0	0	0	0	0	0	0	0	0	COEFF_SENSOR											
4Ch	EASY_CONF_EN	LUMPED_DEAD_TIME	STANDBY_PIN_EN	STANDBY_PIN_POL	STANDBY	0	0	0	0	0	0	0	0	0	0	HDR_SCALE			INTG_DUTY_CYCLE					
4Dh	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	NORMAL_FRM_INTG_SCALE			0	0	0	0	0	0
51h	0	0	0	CALIB_PREC	0	1	DISABLE_TEMP_COR	DISABLE_OFFSET_CORR	TSENSOR_CALIB							TILLUM_CALIB								
52h	0	0	0	0	AMPLITUDE_POST_SCALE			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
61h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TSENSOR							
62h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TILLUM							

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Register Maps (continued)

Table 44. DE Register Map (continued)

ADDRESS (Hex)	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
63h	INTG_DUTY_CYCLE_SET_FAILED	PIX_CNT_MAX_SET_FAILED	OP_UNDERFLOW	OP_OVERFLOW	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	MASTER_PLL_LOCK	LVDS_PLL_LOCK	DDR_CALIBRATION_FLAG	DDR_CONTROLLER_FLAG	0
65h	ILLUM_FB_ERROR_CNT												0	0	0	0	0	0	0	0	0	0	0	0
66h	COMP_FB_ERROR_CNT												0	0	0	0	0	0	0	0	0	0	0	0
80h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PHASE_LIN_CORR_PERIOD		PHASE_LIN_CORR_EN
81h	PHASE_LIN_COEFF0_1												PHASE_LIN_COEFF0_0											
82h	PHASE_LIN_COEFF0_3												PHASE_LIN_COEFF0_2											
83h	PHASE_LIN_COEFF0_5												PHASE_LIN_COEFF0_4											
84h	PHASE_LIN_COEFF0_7												PHASE_LIN_COEFF0_6											
85h	PHASE_LIN_COEFF0_9												PHASE_LIN_COEFF0_8											
86h	PHASE_LIN_COEFF0_11												PHASE_LIN_COEFF0_10											
87h	PHASE_LIN_COEFF0_13												PHASE_LIN_COEFF0_12											
88h	PHASE_LIN_COEFF0_15												PHASE_LIN_COEFF0_14											
91h	PHASE_LIN_COEFF1_1												PHASE_LIN_COEFF1_0											
92h	PHASE_LIN_COEFF1_3												PHASE_LIN_COEFF1_2											
93h	PHASE_LIN_COEFF1_5												PHASE_LIN_COEFF1_4											
94h	PHASE_LIN_COEFF1_7												PHASE_LIN_COEFF1_6											
95h	PHASE_LIN_COEFF1_9												PHASE_LIN_COEFF1_8											
96h	PHASE_LIN_COEFF1_11												PHASE_LIN_COEFF1_10											
97h	PHASE_LIN_COEFF1_13												PHASE_LIN_COEFF1_12											
98h	PHASE_LIN_COEFF1_15												PHASE_LIN_COEFF1_14											
ABh	FILT_COEF_Y_IM_F2								FILT_COEF_Y_RE_F2								0	0	0	0	0	0	0	0
ACh	FILT_COEF_X_RE_F2								FILT_COEF_X_IM_F2								0	0	0	0	0	0	0	0
ADh	FILT_COEF_Y_IM_F1								FILT_COEF_Y_RE_F1								0	0	0	0	0	0	0	0
AEh	FILT_COEF_X_IM_F1								FILT_COEF_X_RE_F1								0	0	0	0	0	0	0	0
AFh	0	0	OP_UNDERFLOW_INTR_DIS	OP_OVERFLOW_INTR_DIS	ILLUM_OVTEMP_INTR_DIS	SENSOR_OVTEMP_INTR_DIS	0	0	0	0	0	0	0	0	0	0	0	0	0	MASTER_PLL_LOCK_INTR_DIS	LVDS_PLL_LOCK_INTR_DIS	DDR_CALIBRATION_INTR_DIS	DDR_CONTROLLER_INTR_DIS	0
B0h	0	0	0	0	0	0	0	0	ILLUM_OVTEMP_THRESH								SENSOR_OVTEMP_THRESH							
B1h	0	DELAY_FB_CORR_MODE		DELAY_FB_DC_CORR_MODE		FB_ERROR_CNT_THRESHOLD								MOD_FB_INV		MOD_REF_INV	0	0	0	0	1	0	0	
B2h	0	0	0	0	0	0	0	0	0	0	0	0	FREQ_RATIO											
B3h	0	0	0	0	0	0	0	0	0	0	0	0	DELAY_FB_COEFF											
B6h	0	0	0	0	FILT_EN	0	FILT_SCALE		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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7.6.2 Register Descriptions

7.6.2.1 Register 0h (offset = 0h) [reset = 0h]

Figure 22. Register 0h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	SOFTWARE_RESET

Table 45. Register 00 Field Descriptions

Bit	Field	Type	Reset	Description
Bit D0	SOFTWARE_RESET	R/W	0h	Resets all registers to default values. Resets the TFC and the sensor.

7.6.2.2 Register 1h (offset = 1h) [reset = 1XXh]

Figure 23. Register 1h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	DEVICE
7	6	5	4	3	2	1	0
MAJOR			MINOR				

Table 46. Register 01 Field Descriptions

Bit	Field	Type	Reset	Description
Bit D8	DEVICE	R/W	1h	0 : Gen1 1 : Gen2
Bits[7:5]	MAJOR	R/W	NA	Firmware version major number
Bits[4:0]	MINOR	R/W	NA	Firmware version minor number

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7.6.2.3 Register 2h (offset = 2h) [reset = 100C81h]

Figure 24. Register 2h

23	22	21	20	19	18	17	16
DEALIAS_EN	IND_FREQ_DATA_EN	0	1	0	0	0	0
15	14	13	12	11	10	9	8
0	0	MB				0	MA
7	6	5	4	3	2	1	0
MA			0	KA			

Table 47. Register 02 Field Descriptions

Bit	Field	Type	Reset	Description
Bit D23	DEALIAS_EN	R/W	0h	Enables de-aliasing when set to '1'.
Bit D22	IND_FREQ_DATA_EN	R/W	0h	When set to '1', enables selection of individual frequency data instead of dealiased data when dealiasing is enabled. Refer to ind_freq_data_sel for details.
Bits[13:10]	MB	R/W	3h	De-aliasing frequencies : fA and fB feff = GCD(fA,fB) ma = fA/feff mb = fB/feff ma and mb have to be co-prime.
Bits[8:5]	MA	R/W	4h	De-aliasing frequencies : fA and fB feff = GCD(fA,fB) ma = fA/feff mb = fB/feff ma and mb have to be co-prime.
Bits[3:0]	KA	R/W	1h	ka should be such that following equation is met for given frequency selection : ka*MA-kb*MB = 1

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7.6.2.4 Register 3h (offset = 3h) [reset = 100000h]

Figure 25. Register 3h

23	22	21	20	19	18	17	16
KB				0	0	0	0
15	14	13	12	11	10	9	8
0	DEALIASED_PH_MASK				0	0	0
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Table 48. Register 03 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[23:20]	KB	R/W	1h	kb should be such that following equation is met for given frequency selection : ka*MA-kb*MB = 1
Bits[14:11]	DEALIASED_PH_MASK	R/W	0h	The mask for the getting the output phase from the calculated dealiased phase. Signed 2's complement representation. The mask is 16bits wide. The lsb of the mask is given by the following relation. lsb=5-dealiased_ph_mask.

7.6.2.5 Register 4h (offset = 4h) [reset = 0h]

Figure 26. Register 4h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
SIN_F1_Q0_COEFF							
7	6	5	4	3	2	1	0
SIN_F1_Q0_COEFF							

Table 49. Register 04 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[15:0]	SIN_F1_Q0_COEFF	R/W	0h	sin(quadcount*2*pi/quad_cnt_max)

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7.6.2.6 Register 5h (offset = 5h) [reset = 7FFFh]

Figure 27. Register 5h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
SIN_F1_Q1_COEFF							
7	6	5	4	3	2	1	0
SIN_F1_Q1_COEFF							

Table 50. Register 05 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[15:0]	SIN_F1_Q1_COEFF	R/W	7FFFh	sin(quadcount*2*pi/quad_cnt_max)

7.6.2.7 Register 6h (offset = 6h) [reset = 0h]

Figure 28. Register 6h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
SIN_F1_Q2_COEFF							
7	6	5	4	3	2	1	0
SIN_F1_Q2_COEFF							

Table 51. Register 06 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[15:0]	SIN_F1_Q2_COEFF	R/W	0h	sin(quadcount*2*pi/quad_cnt_max)

7.6.2.8 Register 7h (offset = 7h) [reset = 8001h]

Figure 29. Register 7h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
SIN_F1_Q3_COEFF							
7	6	5	4	3	2	1	0
SIN_F1_Q3_COEFF							

Table 52. Register 07 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[15:0]	SIN_F1_Q3_COEFF	R/W	8001h	sin(quadcount*2*pi/quad_cnt_max)

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7.6.2.9 Register 8h (offset = 8h) [reset = 0h]

Figure 30. Register 8h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
SIN_F1_Q4_COEFF							
7	6	5	4	3	2	1	0
SIN_F1_Q4_COEFF							

Table 53. Register 08 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[15:0]	SIN_F1_Q4_COEFF	R/W	0h	sin(quadcount*2*pi/quad_cnt_max)

7.6.2.10 Register 9h (offset = 9h) [reset = 0h]

Figure 31. Register 9h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
SIN_F1_Q5_COEFF							
7	6	5	4	3	2	1	0
SIN_F1_Q5_COEFF							

Table 54. Register 09 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[15:0]	SIN_F1_Q5_COEFF	R/W	0h	sin(quadcount*2*pi/quad_cnt_max)

7.6.2.11 Register Ah (offset = Ah) [reset = 7FFFh]

Figure 32. Register Ah

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
COS_F1_Q0_COEFF							
7	6	5	4	3	2	1	0
COS_F1_Q0_COEFF							

Table 55. Register 0A Field Descriptions

Bit	Field	Type	Reset	Description
Bits[15:0]	COS_F1_Q0_COEFF	R/W	7FFFh	cos(quadcount*2*pi/quad_cnt_max)

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7.6.2.12 Register Bh (offset = Bh) [reset = 0h]

Figure 33. Register Bh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
COS_F1_Q1_COEFF							
7	6	5	4	3	2	1	0
COS_F1_Q1_COEFF							

Table 56. Register 0B Field Descriptions

Bit	Field	Type	Reset	Description
Bits[15:0]	COS_F1_Q1_COEFF	R/W	0h	cos(quadcount*2*pi/quad_cnt_max)

7.6.2.13 Register Ch (offset = Ch) [reset = 8001h]

Figure 34. Register Ch

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
COS_F1_Q2_COEFF							
7	6	5	4	3	2	1	0
COS_F1_Q2_COEFF							

Table 57. Register 0C Field Descriptions

Bit	Field	Type	Reset	Description
Bits[15:0]	COS_F1_Q2_COEFF	R/W	8001h	cos(quadcount*2*pi/quad_cnt_max)

7.6.2.14 Register Dh (offset = Dh) [reset = 0h]

Figure 35. Register Dh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
COS_F1_Q3_COEFF							
7	6	5	4	3	2	1	0
COS_F1_Q3_COEFF							

Table 58. Register 0D Field Descriptions

Bit	Field	Type	Reset	Description
Bits[15:0]	COS_F1_Q3_COEFF	R/W	0h	cos(quadcount*2*pi/quad_cnt_max)

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7.6.2.15 Register Eh (offset = Eh) [reset = 0h]

Figure 36. Register Eh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
COS_F1_Q4_COEFF							
7	6	5	4	3	2	1	0
COS_F1_Q4_COEFF							

Table 59. Register 0E Field Descriptions

Bit	Field	Type	Reset	Description
Bits[15:0]	COS_F1_Q4_COEFF	R/W	0h	cos(quadcount*2*pi/quad_cnt_max)

7.6.2.16 Register Fh (offset = Fh) [reset = 0h]

Figure 37. Register Fh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
COS_F1_Q5_COEFF							
7	6	5	4	3	2	1	0
COS_F1_Q5_COEFF							

Table 60. Register 0F Field Descriptions

Bit	Field	Type	Reset	Description
Bits[15:0]	COS_F1_Q5_COEFF	R/W	0h	cos(quadcount*2*pi/quad_cnt_max)

7.6.2.17 Register 10h (offset = 10h) [reset = 0h]

Figure 38. Register 10h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
SIN_F2_Q0_COEFF							
7	6	5	4	3	2	1	0
SIN_F2_Q0_COEFF							

Table 61. Register 10 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[15:0]	SIN_F2_Q0_COEFF	R/W	0h	sin(quadcount*2*pi/quad_cnt_max)

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7.6.2.18 Register 11h (offset = 11h) [reset = 6ED9h]

Figure 39. Register 11h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
SIN_F2_Q1_COEFF							
7	6	5	4	3	2	1	0
SIN_F2_Q1_COEFF							

Table 62. Register 11 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[15:0]	SIN_F2_Q1_COEFF	R/W	6ED9h	sin(quadcount*2*pi/quad_cnt_max)

7.6.2.19 Register 12h (offset = 12h) [reset = 9127h]

Figure 40. Register 12h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
SIN_F2_Q2_COEFF							
7	6	5	4	3	2	1	0
SIN_F2_Q2_COEFF							

Table 63. Register 12 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[15:0]	SIN_F2_Q2_COEFF	R/W	9127h	sin(quadcount*2*pi/quad_cnt_max)

7.6.2.20 Register 13h (offset = 13h) [reset = 0h]

Figure 41. Register 13h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
SIN_F2_Q3_COEFF							
7	6	5	4	3	2	1	0
SIN_F2_Q3_COEFF							

Table 64. Register 13 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[15:0]	SIN_F2_Q3_COEFF	R/W	0h	sin(quadcount*2*pi/quad_cnt_max)

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7.6.2.21 Register 14h (offset = 14h) [reset = 6ED9h]

Figure 42. Register 14h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
SIN_F2_Q4_COEFF							
7	6	5	4	3	2	1	0
SIN_F2_Q4_COEFF							

Table 65. Register 14 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[15:0]	SIN_F2_Q4_COEFF	R/W	6ED9h	sin(quadcount*2*pi/quad_cnt_max)

7.6.2.22 Register 15h (offset = 15h) [reset = 9127h]

Figure 43. Register 15h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
SIN_F2_Q5_COEFF							
7	6	5	4	3	2	1	0
SIN_F2_Q5_COEFF							

Table 66. Register 15 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[15:0]	SIN_F2_Q5_COEFF	R/W	9127h	sin(quadcount*2*pi/quad_cnt_max)

7.6.2.23 Register 16h (offset = 16h) [reset = 7FFFh]

Figure 44. Register 16h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
COS_F2_Q0_COEFF							
7	6	5	4	3	2	1	0
COS_F2_Q0_COEFF							

Table 67. Register 16 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[15:0]	COS_F2_Q0_COEFF	R/W	7FFFh	cos(quadcount*2*pi/quad_cnt_max)

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7.6.2.24 Register 17h (offset = 17h) [reset = C000h]

Figure 45. Register 17h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
COS_F2_Q1_COEFF							
7	6	5	4	3	2	1	0
COS_F2_Q1_COEFF							

Table 68. Register 17 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[15:0]	COS_F2_Q1_COEFF	R/W	C000h	cos(quadcount*2*pi/quad_cnt_max)

7.6.2.25 Register 18h (offset = 18h) [reset = C000h]

Figure 46. Register 18h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
COS_F2_Q2_COEFF							
7	6	5	4	3	2	1	0
COS_F2_Q2_COEFF							

Table 69. Register 18 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[15:0]	COS_F2_Q2_COEFF	R/W	C000h	cos(quadcount*2*pi/quad_cnt_max)

7.6.2.26 Register 19h (offset = 19h) [reset = 7FFFh]

Figure 47. Register 19h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
COS_F2_Q3_COEFF							
7	6	5	4	3	2	1	0
COS_F2_Q3_COEFF							

Table 70. Register 19 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[15:0]	COS_F2_Q3_COEFF	R/W	7FFFh	cos(quadcount*2*pi/quad_cnt_max)

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7.6.2.27 Register 1Ah (offset = 1Ah) [reset = C000h]

Figure 48. Register 1Ah

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
COS_F2_Q4_COEFF							
7	6	5	4	3	2	1	0
COS_F2_Q4_COEFF							

Table 71. Register 1A Field Descriptions

Bit	Field	Type	Reset	Description
Bits[15:0]	COS_F2_Q4_COEFF	R/W	C000h	cos(quadcount*2*pi/quad_cnt_max)

7.6.2.28 Register 1Bh (offset = 1Bh) [reset = C000h]

Figure 49. Register 1Bh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
COS_F2_Q5_COEFF							
7	6	5	4	3	2	1	0
COS_F2_Q5_COEFF							

Table 72. Register 1B Field Descriptions

Bit	Field	Type	Reset	Description
Bits[15:0]	COS_F2_Q5_COEFF	R/W	C000h	cos(quadcount*2*pi/quad_cnt_max)

7.6.2.29 Register 1Fh (offset = 1Fh) [reset = 54321h]

Figure 50. Register 1Fh

23	22	21	20	19	18	17	16
0	IQ_SCALE			0	1	0	1
15	14	13	12	11	10	9	8
0	1	0	0	0	0	1	1
7	6	5	4	3	2	1	0
0	0	1	0	0	0	0	1

Table 73. Register 1F Field Descriptions

Bit	Field	Type	Reset	Description
Bits[22:20]	IQ_SCALE	R/W	0h	The computed internal I/Q are left shifted by this value before computation of phase and amplitude.

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7.6.2.30 Register 25h (offset = 25h) [reset = 80001h]

Figure 51. Register 25h

23	22	21	20	19	18	17	16
0	0	0	0	OP_DATA_ARRANGE_MODE		0	0
15	14	13	12	11	10	9	8
0	0	0	0	OUTPUT_MODE			
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1

Table 74. Register 25 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[19:18]	OP_DATA_ARRANGE_MODE	R/W	2h	Applicable in 4-byte depth data output mode. 0 : Continuous 1 : Continuous 2 : rearrange_8
Bits[11:8]	OUTPUT_MODE	R/W	0h	Selects the output data. 0 : depth data 1 : raw IQ data 15 : raw quad data

7.6.2.31 Register 27h (offset = 27h) [reset = 2000h]

Figure 52. Register 27h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
0	PIXEL_DATA_SIZE				0	0	0
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Table 75. Register 27 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[14:11]	PIXEL_DATA_SIZE	R/W	4h	Number of bytes per pixel. 0 : should not be used 1 : should not be used 2 : 2 byte mode 3 : reserved 4 : 4 bytes

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7.6.2.32 Register 28h (offset = 28h) [reset = 0h]

Figure 53. Register 28h

23	22	21	20	19	18	17	16
DEALIAS_16BIT_OP_ENABLE	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Table 76. Register 28 Field Descriptions

Bit	Field	Type	Reset	Description
Bit D23	DEALIAS_16BIT_OP_ENABLE	R/W	0h	Enables 16-bit output of dealiased data. Ambient will not be available in this mode. This mode is available only if pixel_data_size is set to 4 byte mode.

7.6.2.33 Register 29h (offset = 29h) [reset = 304000h]

Figure 54. Register 29h

23	22	21	20	19	18	17	16
0	0	1	1	0	0	0	0
15	14	13	12	11	10	9	8
0	1	0	0	0	0	0	0
7	6	5	4	3	2	1	0
0	0	0	0	IND_FREQ_DATA_SEL	0	PHY_TEST_ENABLE	0

Table 77. Register 29 Field Descriptions

Bit	Field	Type	Reset	Description
Bit D3	IND_FREQ_DATA_SEL	R/W	0h	Select individual frequency data when dealiasing is enabled. ind_freq_data_en should be set so that this bit has any effect. 0 : freq1 data 1 : freq2 data
Bit D1	PHY_TEST_ENABLE	R/W	0h	Useful for debugging. Outputs an 8-bit ramp. 0,0,1,2,3.....255,0,1,2,..

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7.6.2.34 Register 2Eh (offset = 2Eh) [reset = 871h]

Figure 55. Register 2Eh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
0	0	0	0	1	0	0	0
7	6	5	4	3	2	1	0
0	TILLUM_SLV_ADDR						

Table 78. Register 2E Field Descriptions

Bit	Field	Type	Reset	Description
Bits[6:0]	TILLUM_SLV_ADDR	R/W	71h	The illumination temperature sensor's I2C slave address. This temperature sensor is assumed to be near the ToF illumination driver for calibration.

7.6.2.35 Register 2Fh (offset = 2Fh) [reset = 3C0001h]

Figure 56. Register 2Fh

23	22	21	20	19	18	17	16
BIN_ROW_COUNT							
15	14	13	12	11	10	9	8
BIN_ROW_COUNT		0	BINNING_EN	0	0	ROWS_TO_MERGE	
7	6	5	4	3	2	1	0
ROWS_TO_MERGE							

Table 79. Register 2F Field Descriptions

Bit	Field	Type	Reset	Description
Bits[23:14]	BIN_ROW_COUNT	R/W	F0h	Must be programmed to floor(total_rows/rows_to_merge)
Bit D12	BINNING_EN	R/W	0h	When set to '1', enables binning of output data. Number of rows merged = rows_to_merge Number of columns merged = cols_to_merge
Bits[9:0]	ROWS_TO_MERGE	R/W	1h	Refer to binning_en description

7.6.2.36 Register 30h (offset = 30h) [reset = 500001h]

Figure 57. Register 30h

23	22	21	20	19	18	17	16
BIN_COL_COUNT							
15	14	13	12	11	10	9	8
BIN_COL_COUNT		0	0	0	0	COLS_TO_MERGE	
7	6	5	4	3	2	1	0
COLS_TO_MERGE							

Table 80. Register 30 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[23:14]	BIN_COL_COUNT	R/W	140h	Must be programmed to floor(total_rows/cols_to_merge)
Bits[9:0]	COLS_TO_MERGE	R/W	1h	Refer to binning_en description

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7.6.2.37 Register 31h (offset = 31h) [reset = 1802h]

Figure 58. Register 31h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
0	0	FREQUENCY_SCALE					AMPLITUDE_SCALE
7	6	5	4	3	2	1	0
AMPLITUDE_SCALE				RAMP_PAT			MAC_TEST_ENABLE

Table 81. Register 31 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[13:9]	FREQUENCY_SCALE	R/W	Ch	If this 0, the phase period is 4096. The period is scaled down by power of 2 of the value of this register. If the register's value is 3, the period is scaled down by 8 times. i.e. the period is right shifted by 3.
Bits[8:4]	AMPLITUDE_SCALE	R/W	0h	Default amplitude of the (A-B) is 2048. The amplitude is scaled down by power of 2 of the value of this register. If the register's value is 3, the amplitude is scaled down by 8 times. i.e. the amplitude is right shifted by 3.
Bits[3:1]	RAMP_PAT	R/W	1h	Chooses the type of ramp pattern 0 : No ramp 1 : Row ramp 2 : Column ramp 3 : Frame ramp
Bit D0	MAC_TEST_ENABLE	R/W	0h	Enables the test patterns within amplitude and phase data. Various ramp patterns can be configured. The patterns can be used to verify the decoding logic of the data received from the TFC.

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7.6.2.38 Register 33h (offset = 33h) [reset = 30h]

Figure 59. Register 33h

23	22	21	20	19	18	17	16
SYSCLK_IN_FREQ							
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
0	0	1	1	0	0	0	0

Table 82. Register 33 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[23:16]	SYSCLK_IN_FREQ	R/W	0h	Selects the system input clock frequency. Programs the PLL accordingly to generate 48MHz system clock. 0 : 48 1 : 24 2 : 12 3 : 6

7.6.2.39 Register 35h (offset = 35h) [reset = 800000h]

Figure 60. Register 35h

23	22	21	20	19	18	17	16
1	ILLUM_MOD_EARLY	ILLUM_EN_EARLY	0	0	0	0	0
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Table 83. Register 35 Field Descriptions

Bit	Field	Type	Reset	Description
Bit D22	ILLUM_MOD_EARLY	R/W	0h	Activates the illumination modulation before integration starts by 15us when set to '1'. 0 : synced 1 : early
Bit D21	ILLUM_EN_EARLY	R/W	0h	Activates the illumination enable signal before integration starts by 15us when set to '1' 0 : synced 1 : early

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7.6.2.40 Register 36h (offset = 36h) [reset = 0h]

Figure 61. Register 36h

23	22	21	20	19	18	17	16
SATURATION_THRESHOLD							
15	14	13	12	11	10	9	8
SATURATION_THRESHOLD				AMPLITUDE_THRESHOLD			
7	6	5	4	3	2	1	0
AMPLITUDE_THRESHOLD							

Table 84. Register 36 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[23:12]	SATURATION_THRESHOLD	R/W	0h	Saturation detection flag in the datastream will be set if the pixel voltage on A/B nodes falls below this set level.
Bits[11:0]	AMPLITUDE_THRESHOLD	R/W	0h	Phase will be made '0xFFF' when amplitude is lower than this threshold.

7.6.2.41 Register 37h (offset = 37h) [reset = 0h]

Figure 62. Register 37h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
PHASE_CORR_1							
7	6	5	4	3	2	1	0
PHASE_CORR_1				0	0	0	0

Table 85. Register 37 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[15:4]	PHASE_CORR_1	R/W	0h	Phase correction for base frequency. This value is subtracted from the obtained phase.

7.6.2.42 Register 38h (offset = 38h) [reset = 0h]

Figure 63. Register 38h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
PHASE_CORR_2							
7	6	5	4	3	2	1	0
PHASE_CORR_2				0	0	0	0

Table 86. Register 38 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[15:4]	PHASE_CORR_2	R/W	0h	Phase correction for de-aliasing frequency. This value is subtracted from the obtained phase.

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7.6.2.43 Register 39h (offset = 39h) [reset = 0h]

Figure 64. Register 39h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
0	0	0	DEBUG_FRAME_NUMBER_EN	0	OP_SERIAL_WIDTH	OP_MODE	
7	6	5	4	3	2	1	0
0	0	OP_CLK_EDGE	0	0	OP_CLK_FREQ		0

Table 87. Register 39 Field Descriptions

Bit	Field	Type	Reset	Description
Bit D12	DEBUG_FRAME_NUMBER_EN	R/W	0h	Debug. Replaces first byte of each frame with the current frame number when set to '1'.
Bit D10	OP_SERIAL_WIDTH	R/W	0h	1-lane or 4-lane serial mode selection 0 : 1-lane serial mode 1 : 4-lane serial mode
Bits[9:8]	OP_MODE	R/W	0h	Serial vs Parallel Mode 0 : DVP Mode 1 : Generic Parallel Mode 2 : Serial Mode
Bit D5	OP_CLK_EDGE	R/W	0h	Data/Control signal transition edge. 0 : Falling edge 1 : Rising Edge
Bits[2:1]	OP_CLK_FREQ	R/W	0h	Sets the ouput data clock rate. Applicable only in master mode. Note that it is the host's responsibility to ensure that the rate is sufficient to attain the required frame-rate without dropping any data. 0 : 24 1 : 12 2 : 6 3 : 3

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7.6.2.44 Register 3Ah (offset = 3Ah) [reset = 0h]

Figure 65. Register 3Ah

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
HDR_PHASE_CORR_1							
7	6	5	4	3	2	1	0
HDR_PHASE_CORR_1				0	0	0	0

Table 88. Register 3A Field Descriptions

Bit	Field	Type	Reset	Description
Bits[15:4]	HDR_PHASE_CORR_1	R/W	0h	Phase correction to be applied in HDR frame on the base frequency data. This value is subtracted from the obtained phase.

7.6.2.45 Register 3Bh (offset = 3Bh) [reset = 0h]

Figure 66. Register 3Bh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
HDR_PHASE_CORR_2							
7	6	5	4	3	2	1	0
HDR_PHASE_CORR_2				0	0	0	0

Table 89. Register 3B Field Descriptions

Bit	Field	Type	Reset	Description
Bits[15:4]	HDR_PHASE_CORR_2	R/W	0h	Phase correction to be applied in HDR frame on the de-aliasing frequency data. This value is subtracted from the obtained phase.

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7.6.2.46 Register 3Ch (offset = 3Ch) [reset = 4000h]

Figure 67. Register 3Ch

23	22	21	20	19	18	17	16
BLK_SIZE							
15	14	13	12	11	10	9	8
BLK_SIZE							
7	6	5	4	3	2	1	0
BLK_SIZE				FRM_TRAILER_EN	BLK_HEADER_EN	FRM_HEADER_EN	PADDING_EN

Table 90. Register 3C Field Descriptions

Bit	Field	Type	Reset	Description
Bits[23:4]	BLK_SIZE	R/W	400h	Includes the header if any and the data size. Each frame is sent to the host in blocks of the this size in terms of the number of output clock cycles. This is also equal to the horizontal active period in DVP mode. (tHA/tBA in the datasheet)
Bit D3	FRM_TRAILER_EN	R/W	0h	Enable a fixed pattern trailer at the end of every frame when set to '1'. Debug only - this inserts a 12-byte constant pattern at the end of every frame.
Bit D2	BLK_HEADER_EN	R/W	0h	When set to '1', enables block level header. This inserts a 12 byte UVC header for every block.
Bit D1	FRM_HEADER_EN	R/W	0h	Enables frame level header when set to '1'. In normal/DVP modes, this is a 12 byte UVC header (for bulk transfers). In serial modes, this is a 4 byte pattern (0xFF, 0xFF, 0xFF, 0xFF).
Bit D0	PADDING_EN	R/W	0h	When set to '1', enables padding of zeros at the end of the frame if the last packet is smaller than the set packet size.

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7.6.2.47 Register 3Dh (offset = 3Dh) [reset = 0h]

Figure 68. Register 3Dh

23	22	21	20	19	18	17	16
BLK_BLANK_SIZE							
15	14	13	12	11	10	9	8
BLK_BLANK_SIZE							
7	6	5	4	3	2	1	0
BLK_BLANK_SIZE				BLK_BLANK_SKIP			

Table 91. Register 3D Field Descriptions

Bit	Field	Type	Reset	Description
Bits[23:4]	BLK_BLANK_SIZE	R/W	0h	The blanking period after each block in terms of number of output clock cycles. This is also equal to the horizontal blank period in DVP mode. (tHB/tBB in the datasheet)
Bits[3:0]	BLK_BLANK_SKIP	R/W	0h	This is the number of block blank periods to skip after the first line. This is useful for interfacing to microcontrollers with multiple packet buffering.

7.6.2.48 Register 3Eh (offset = 3Eh) [reset = 80h]

Figure 69. Register 3Eh

23	22	21	20	19	18	17	16
VD_ACTIVE							
15	14	13	12	11	10	9	8
VD_ACTIVE							
7	6	5	4	3	2	1	0
VD_ACTIVE				0	0	0	0

Table 92. Register 3E Field Descriptions

Bit	Field	Type	Reset	Description
Bits[23:4]	VD_ACTIVE	R/W	8h	The width of the VD signal in terms of number of pixel clock cycles (tVD in the datasheet)

7.6.2.49 Register 3Fh (offset = 3Fh) [reset = Bh]

Figure 70. Register 3Fh

23	22	21	20	19	18	17	16
FRM_BLANK_SIZE							
15	14	13	12	11	10	9	8
FRM_BLANK_SIZE							
7	6	5	4	3	2	1	0
FRM_BLANK_SIZE				1	0	FB_READY_POL	FB_READY_EN

Table 93. Register 3F Field Descriptions

Bit	Field	Type	Reset	Description
Bits[23:4]	FRM_BLANK_SIZE	R/W	0h	The vertical top blanking period from start of VD to the start of the first HD in terms of number of pixel clock cycles (tVTB in the datasheet).
Bit D1	FB_READY_POL	R/W	1h	Decides the polarity of the ready signal 0 : active_low 1 : active_high
Bit D0	FB_READY_EN	R/W	1h	Ready feedback signal enable. When ready is inactive, the TFC stops sending out data till the line goes active. This is useful for cases where the host may be temporarily busy. Set to '1' to enable feedback. 0 : disable 1 : enable

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7.6.2.50 Register 40h (offset = 40h) [reset = 50455h]

Figure 71. Register 40h

23	22	21	20	19	18	17	16
0	0	0	FE_LAST_CYCLE	0	FE_POL	0	1
15	14	13	12	11	10	9	8
0	OP_CS_POL	0	0	0	PHASE_AUX_POL	0	PHASE_AUX_EN
7	6	5	4	3	2	1	0
0	VD_POL	0	1	0	HD_POL	0	1

Table 94. Register 40 Field Descriptions

Bit	Field	Type	Reset	Description
Bit D20	FE_LAST_CYCLE	R/W	0h	Activate frame end signal with last byte of data or one cycle later 0 : Frame end is asserted one cycle after the last byte 1 : Frame end is asserted along with last byte of frame
Bit D18	FE_POL	R/W	1h	Controls the polarity of the FE signal when active. 0 : active low 1 : active high
Bit D14	OP_CS_POL	R/W	0h	Controls the polarity of the OP/CS line when active. 0 : active low 1 : active high
Bit D10	PHASE_AUX_POL	R/W	1h	Controls the polarity of the phase/aux signal when active. 0 : active low 1 : active high
Bit D8	PHASE_AUX_EN	R/W	0h	Enables Phase/Aux selection when set to '1' 0 : disable 1 : enable
Bit D6	VD_POL	R/W	1h	Controls the polarity of the VD signal when active. 0 : active low 1 : active high
Bit D2	HD_POL	R/W	1h	Controls the polarity of the HD/BD signal when active. 0 : active low 1 : active high

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7.6.2.51 Register 47h (offset = 47h) [reset = 0h]

Figure 72. Register 47h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
0	0	0	0	COEFF_ILLUM			
7	6	5	4	3	2	1	0
COEFF_ILLUM							

Table 95. Register 47 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[11:0]	COEFF_ILLUM	R/W	0h	phase correction = phase_offset + coeff_illum*(tillum-tillum_calib) + coeff_sensor*(tsensor-tsensor_calib) phase correction is subtracted from the phase output.

7.6.2.52 Register 48h (offset = 48h) [reset = 0h]

Figure 73. Register 48h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
0	0	0	0	COEFF_SENSOR			
7	6	5	4	3	2	1	0
COEFF_SENSOR							

Table 96. Register 48 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[11:0]	COEFF_SENSOR	R/W	0h	phase correction = phase_offset + coeff_illum*(tillum-tillum_calib) + coeff_sensor*(tsensor-tsensor_calib) phase correction is subtracted from the phase output.

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7.6.2.53 Register 4Ch (offset = 4Ch) [reset = 800006h]

Figure 74. Register 4Ch

23	22	21	20	19	18	17	16
EASY_CONF_EN	LUMPED_DEAD_TIME	STANDBY_PIN_EN	STANDBY_PIN_POL	STANDBY	0	0	0
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	HDR_SCALE
7	6	5	4	3	2	1	0
HDR_SCALE		INTG_DUTY_CYCLE					

Table 97. Register 4C Field Descriptions

Bit	Field	Type	Reset	Description	
Bit D23	EASY_CONF_EN	R/W	1h	When set to '1', enables simple configuration of timings which covers most of the usual scenarios.	
Bit D22	LUMPED_DEAD_TIME	R/W	0h	In the easy configuration mode, dead time can be either distributed equally among all quads or it can be lumped at the end of each frame. 0 : uniform quad dead time 1 : lumped frame dead time	
Bit D21	STANDBY_PIN_EN	R/W	0h	When set to '1', standby pin functionality is enabled.	
Bit D20	STANDBY_PIN_POL	R/W	0h	Selects the active polarity of standby pin. Active only when standby_pin_en is set. 0 : active low 1 : active high	
Bit D19	STANDBY	R/W	0h	Put the device in standby	
Bits[8:6]	HDR_SCALE	R/W	0h	Enables scaling of integration time on alternate frames. If HDR scale is set to 0, no scaling happens (The default case). Scaling is given by the formula : integration time (scaled) = integration time >> hdr_frm_intg_scale. Note that this scaling is in addition to the scaling of the normal integration duty cycle set using the normal_frm_intg_scale register.	
Bits[5:0]	INTG_DUTY_CYCLE	R/W	6h	If no scaling is used, Integration time = intg_duty_cycle * 100/64.0.	

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7.6.2.54 Register 4Dh (offset = 4Dh) [reset = 0h]

Figure 75. Register 4Dh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	NORMAL_FRM_INTG_SCALE
7	6	5	4	3	2	1	0
NORMAL_FRM_INTG_SCALE	0	0	0	0	0	0	0

Table 98. Register 4D Field Descriptions

Bit	Field	Type	Reset	Description
Bits[8:6]	NORMAL_FRM_INTG_SCALE	R/W	0h	Integration duty cycle is scaled by down this value. Scaling is given by the formula : integration time (scaled) = integration time >> normal_frm_intg_scale

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7.6.2.55 Register 51h (offset = 51h) [reset = 140000h]

Figure 76. Register 51h

23	22	21	20	19	18	17	16
0	0	0	CALIB_PREC	0	1	DISABLE_TEMP_CORR	DISABLE_OFFSET_CORR
15	14	13	12	11	10	9	8
TSENSOR_CALIB							
7	6	5	4	3	2	1	0
TILLUM_CALIB							

Table 99. Register 51 Field Descriptions

Bit	Field	Type	Reset	Description
Bit D20	CALIB_PREC	R/W	1h	Adjusts the precision of temperature correction. coefficients are scaled down by calib_prec. coeff = coeff / calib_prec 0 : 1 1 : 16
Bit D17	DISABLE_TEMP_CORR	R/W	0h	Disables temperature calibration of phase when set to '1'.
Bit D16	DISABLE_OFFSET_CORR	R/W	0h	Disables phase calibration completely when set to '1'.
Bits[15:8]	TSENSOR_CALIB	R/W	0h	phase correction = phase_offset + coeff_illum*(tillum-tillum_calib) + coeff_sensor*(tsensor-tsensor_calib) phase correction is subtracted from the phase output.
Bits[7:0]	TILLUM_CALIB	R/W	0h	phase correction = phase_offset + coeff_illum*(tillum-tillum_calib) + coeff_sensor*(tsensor-tsensor_calib) phase correction is subtracted from the phase output.

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7.6.2.56 Register 52h (offset = 52h) [reset = 0h]

Figure 77. Register 52h

23	22	21	20	19	18	17	16
0	0	0	0	AMPLITUDE_POST_SCALE			0
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Table 100. Register 52 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[19:17]	AMPLITUDE_POST_SCALE	R/W	0h	Scales the amplitude values. amplitude = amplitude << amplitude_post_scale. If a bit overflow occurs, amplitude will be clipped to a maximum 12-bit value of 0xFFF.

7.6.2.57 Register 61h (offset = 61h) [reset = 0h]

Figure 78. Register 61h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
TSENSOR							

Table 101. Register 61 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[7:0]	TSENSOR	R	0h	temperature output from OPT8241's builtin temp sensor

7.6.2.58 Register 62h (offset = 62h) [reset = 0h]

Figure 79. Register 62h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
TILLUM							

Table 102. Register 62 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[7:0]	TILLUM	R	0h	temperature output from temp sensor with slave address = TILLUM_SLV_ADDR. If the slave address is invalid, it reads FFh.

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7.6.2.59 Register 63h (offset = 63h) [reset = 0h]

Figure 80. Register 63h

23	22	21	20	19	18	17	16
INTG_DUTY_CYCLE_SET_FAILED	PIX_CNT_MAX_SET_FAILED	OP_UNDERFLOW	OP_OVERFLOW	0	0	0	0
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
0	0	0	MASTER_PLL_LOCK	LVDS_PLL_LOCK	DDR_CALIBRATION_FLAG	DDR_CONTROLLER_FLAG	0

Table 103. Register 63 Field Descriptions

Bit	Field	Type	Reset	Description
Bit D23	INTG_DUTY_CYCLE_SET_FAILED	R	0h	Indicates that the integration duty cycle is too high.
Bit D22	PIX_CNT_MAX_SET_FAILED	R	0h	indicates the pix_cnt_max setting is too low.
Bit D21	OP_UNDERFLOW	R/W	0h	Indicates that the output data rate is too high. Write a '0' to reset the state.
Bit D20	OP_OVERFLOW	R/W	0h	Indicates that the output data rate is too low. Write a '0' to reset the state.
Bit D4	MASTER_PLL_LOCK	R	0h	Master PLL lock flag
Bit D3	LVDS_PLL_LOCK	R	0h	LVDS PLL lock flag
Bit D2	DDR_CALIBRATION_FLAG	R	0h	DDR calibration done flag
Bit D1	DDR_CONTROLLER_FLAG	R	0h	DDR controller initialization done flag

7.6.2.60 Register 65h (offset = 65h) [reset = 0h]

Figure 81. Register 65h

23	22	21	20	19	18	17	16
ILLUM_FB_ERROR_CNT							
15	14	13	12	11	10	9	8
ILLUM_FB_ERROR_CNT				0	0	0	0
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Table 104. Register 65 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[23:12]	ILLUM_FB_ERROR_CNT	R	0h	Number of phase inversions of divider in measurements in 4096 cycles

7.6.2.61 Register 66h (offset = 66h) [reset = 0h]

Figure 82. Register 66h

23	22	21	20	19	18	17	16
COMP_FB_ERROR_CNT							
15	14	13	12	11	10	9	8
COMP_FB_ERROR_CNT				0	0	0	0
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Table 105. Register 66 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[23:12]	COMP_FB_ERROR_CNT	R	0h	Number of phase inversions of divider in measurements in 4096 cycles

7.6.2.62 Register 80h (offset = 80h) [reset = 0h]

Figure 83. Register 80h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
0	0	0	0	0	PHASE_LIN_CORR_PERIOD		PHASE_LIN_CORR_EN

Table 106. Register 80 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[2:1]	PHASE_LIN_CORR_PERIOD	R/W	0h	Represents the repetition period of non-linearity. The 16 LUT values are spread over this period. The remaining periods in 360 degrees are a repeat of this period. 0 : 90 1 : 180 2 : 360
Bit D0	PHASE_LIN_CORR_EN	R/W	0h	Enable phase non-linearity correction. The linearity coefficients represent the lookup table for converting the obtained phase to actual phase.

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7.6.2.63 Register 81h (offset = 81h) [reset = 0h]

Figure 84. Register 81h

23	22	21	20	19	18	17	16
PHASE_LIN_COEFF0_1							
15	14	13	12	11	10	9	8
PHASE_LIN_COEFF0_1				PHASE_LIN_COEFF0_0			
7	6	5	4	3	2	1	0
PHASE_LIN_COEFF0_0							

Table 107. Register 81 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[23:12]	PHASE_LIN_COEFF0_1	R/W	0h	
Bits[11:0]	PHASE_LIN_COEFF0_0	R/W	0h	

7.6.2.64 Register 82h (offset = 82h) [reset = 0h]

Figure 85. Register 82h

23	22	21	20	19	18	17	16
PHASE_LIN_COEFF0_3							
15	14	13	12	11	10	9	8
PHASE_LIN_COEFF0_3				PHASE_LIN_COEFF0_2			
7	6	5	4	3	2	1	0
PHASE_LIN_COEFF0_2							

Table 108. Register 82 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[23:12]	PHASE_LIN_COEFF0_3	R/W	0h	
Bits[11:0]	PHASE_LIN_COEFF0_2	R/W	0h	

7.6.2.65 Register 83h (offset = 83h) [reset = 0h]

Figure 86. Register 83h

23	22	21	20	19	18	17	16
PHASE_LIN_COEFF0_5							
15	14	13	12	11	10	9	8
PHASE_LIN_COEFF0_5				PHASE_LIN_COEFF0_4			
7	6	5	4	3	2	1	0
PHASE_LIN_COEFF0_4							

Table 109. Register 83 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[23:12]	PHASE_LIN_COEFF0_5	R/W	0h	
Bits[11:0]	PHASE_LIN_COEFF0_4	R/W	0h	

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7.6.2.66 Register 84h (offset = 84h) [reset = 0h]

Figure 87. Register 84h

23	22	21	20	19	18	17	16
PHASE_LIN_COEFF0_7							
15	14	13	12	11	10	9	8
PHASE_LIN_COEFF0_7				PHASE_LIN_COEFF0_6			
7	6	5	4	3	2	1	0
PHASE_LIN_COEFF0_6							

Table 110. Register 84 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[23:12]	PHASE_LIN_COEFF0_7	R/W	0h	
Bits[11:0]	PHASE_LIN_COEFF0_6	R/W	0h	

7.6.2.67 Register 85h (offset = 85h) [reset = 0h]

Figure 88. Register 85h

23	22	21	20	19	18	17	16
PHASE_LIN_COEFF0_9							
15	14	13	12	11	10	9	8
PHASE_LIN_COEFF0_9				PHASE_LIN_COEFF0_8			
7	6	5	4	3	2	1	0
PHASE_LIN_COEFF0_8							

Table 111. Register 85 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[23:12]	PHASE_LIN_COEFF0_9	R/W	0h	
Bits[11:0]	PHASE_LIN_COEFF0_8	R/W	0h	

7.6.2.68 Register 86h (offset = 86h) [reset = 0h]

Figure 89. Register 86h

23	22	21	20	19	18	17	16
PHASE_LIN_COEFF0_11							
15	14	13	12	11	10	9	8
PHASE_LIN_COEFF0_11				PHASE_LIN_COEFF0_10			
7	6	5	4	3	2	1	0
PHASE_LIN_COEFF0_10							

Table 112. Register 86 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[23:12]	PHASE_LIN_COEFF0_11	R/W	0h	
Bits[11:0]	PHASE_LIN_COEFF0_10	R/W	0h	

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7.6.2.69 Register 87h (offset = 87h) [reset = 0h]

Figure 90. Register 87h

23	22	21	20	19	18	17	16
PHASE_LIN_COEFF0_13							
15	14	13	12	11	10	9	8
PHASE_LIN_COEFF0_13				PHASE_LIN_COEFF0_12			
7	6	5	4	3	2	1	0
PHASE_LIN_COEFF0_12							

Table 113. Register 87 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[23:12]	PHASE_LIN_COEFF0_13	R/W	0h	
Bits[11:0]	PHASE_LIN_COEFF0_12	R/W	0h	

7.6.2.70 Register 88h (offset = 88h) [reset = 0h]

Figure 91. Register 88h

23	22	21	20	19	18	17	16
PHASE_LIN_COEFF0_15							
15	14	13	12	11	10	9	8
PHASE_LIN_COEFF0_15				PHASE_LIN_COEFF0_14			
7	6	5	4	3	2	1	0
PHASE_LIN_COEFF0_14							

Table 114. Register 88 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[23:12]	PHASE_LIN_COEFF0_15	R/W	0h	
Bits[11:0]	PHASE_LIN_COEFF0_14	R/W	0h	

7.6.2.71 Register 91h (offset = 91h) [reset = 0h]

Figure 92. Register 91h

23	22	21	20	19	18	17	16
PHASE_LIN_COEFF1_1							
15	14	13	12	11	10	9	8
PHASE_LIN_COEFF1_1				PHASE_LIN_COEFF1_0			
7	6	5	4	3	2	1	0
PHASE_LIN_COEFF1_0							

Table 115. Register 91 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[23:12]	PHASE_LIN_COEFF1_1	R/W	0h	
Bits[11:0]	PHASE_LIN_COEFF1_0	R/W	0h	

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7.6.2.72 Register 92h (offset = 92h) [reset = 0h]

Figure 93. Register 92h

23	22	21	20	19	18	17	16
PHASE_LIN_COEFF1_3							
15	14	13	12	11	10	9	8
PHASE_LIN_COEFF1_3				PHASE_LIN_COEFF1_2			
7	6	5	4	3	2	1	0
PHASE_LIN_COEFF1_2							

Table 116. Register 92 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[23:12]	PHASE_LIN_COEFF1_3	R/W	0h	
Bits[11:0]	PHASE_LIN_COEFF1_2	R/W	0h	

7.6.2.73 Register 93h (offset = 93h) [reset = 0h]

Figure 94. Register 93h

23	22	21	20	19	18	17	16
PHASE_LIN_COEFF1_5							
15	14	13	12	11	10	9	8
PHASE_LIN_COEFF1_5				PHASE_LIN_COEFF1_4			
7	6	5	4	3	2	1	0
PHASE_LIN_COEFF1_4							

Table 117. Register 93 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[23:12]	PHASE_LIN_COEFF1_5	R/W	0h	
Bits[11:0]	PHASE_LIN_COEFF1_4	R/W	0h	

7.6.2.74 Register 94h (offset = 94h) [reset = 0h]

Figure 95. Register 94h

23	22	21	20	19	18	17	16
PHASE_LIN_COEFF1_7							
15	14	13	12	11	10	9	8
PHASE_LIN_COEFF1_7				PHASE_LIN_COEFF1_6			
7	6	5	4	3	2	1	0
PHASE_LIN_COEFF1_6							

Table 118. Register 94 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[23:12]	PHASE_LIN_COEFF1_7	R/W	0h	
Bits[11:0]	PHASE_LIN_COEFF1_6	R/W	0h	

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7.6.2.75 Register 95h (offset = 95h) [reset = 0h]

Figure 96. Register 95h

23	22	21	20	19	18	17	16
PHASE_LIN_COEFF1_9							
15	14	13	12	11	10	9	8
PHASE_LIN_COEFF1_9				PHASE_LIN_COEFF1_8			
7	6	5	4	3	2	1	0
PHASE_LIN_COEFF1_8							

Table 119. Register 95 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[23:12]	PHASE_LIN_COEFF1_9	R/W	0h	
Bits[11:0]	PHASE_LIN_COEFF1_8	R/W	0h	

7.6.2.76 Register 96h (offset = 96h) [reset = 0h]

Figure 97. Register 96h

23	22	21	20	19	18	17	16
PHASE_LIN_COEFF1_11							
15	14	13	12	11	10	9	8
PHASE_LIN_COEFF1_11				PHASE_LIN_COEFF1_10			
7	6	5	4	3	2	1	0
PHASE_LIN_COEFF1_10							

Table 120. Register 96 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[23:12]	PHASE_LIN_COEFF1_11	R/W	0h	
Bits[11:0]	PHASE_LIN_COEFF1_10	R/W	0h	

7.6.2.77 Register 97h (offset = 97h) [reset = 0h]

Figure 98. Register 97h

23	22	21	20	19	18	17	16
PHASE_LIN_COEFF1_13							
15	14	13	12	11	10	9	8
PHASE_LIN_COEFF1_13				PHASE_LIN_COEFF1_12			
7	6	5	4	3	2	1	0
PHASE_LIN_COEFF1_12							

Table 121. Register 97 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[23:12]	PHASE_LIN_COEFF1_13	R/W	0h	
Bits[11:0]	PHASE_LIN_COEFF1_12	R/W	0h	

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7.6.2.78 Register 98h (offset = 98h) [reset = 0h]

Figure 99. Register 98h

23	22	21	20	19	18	17	16
PHASE_LIN_COEFF1_15							
15	14	13	12	11	10	9	8
PHASE_LIN_COEFF1_15				PHASE_LIN_COEFF1_14			
7	6	5	4	3	2	1	0
PHASE_LIN_COEFF1_14							

Table 122. Register 98 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[23:12]	PHASE_LIN_COEFF1_15	R/W	0h	
Bits[11:0]	PHASE_LIN_COEFF1_14	R/W	0h	

7.6.2.79 Register ABh (offset = ABh) [reset = 0h]

Figure 100. Register ABh

23	22	21	20	19	18	17	16
FILT_COEF_Y_IM_F2							
15	14	13	12	11	10	9	8
FILT_COEF_Y_RE_F2							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Table 123. Register AB Field Descriptions

Bit	Field	Type	Reset	Description
Bits[23:16]	FILT_COEF_Y_IM_F2	R/W	0h	Spatial filter coefficient. Used if filt_en is set to '1'. Location : Above or below the center pixel. Frequency : f2 Component : Imaginary
Bits[15:8]	FILT_COEF_Y_RE_F2	R/W	0h	Spatial filter coefficient. Used if filt_en is set to '1'. Location : Above or below the center pixel. Frequency : f1 Component : Real

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7.6.2.80 Register ACh (offset = ACh) [reset = 0h]

Figure 101. Register ACh

23	22	21	20	19	18	17	16
FILT_COEF_X_RE_F2							
15	14	13	12	11	10	9	8
FILT_COEF_X_IM_F2							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Table 124. Register AC Field Descriptions

Bit	Field	Type	Reset	Description
Bits[23:16]	FILT_COEF_X_RE_F2	R/W	0h	Spatial filter coefficient. Used if filt_en is set to '1'. Location : Left or Right of the center pixel. Frequency : f2 Component : Real
Bits[15:8]	FILT_COEF_X_IM_F2	R/W	0h	Spatial filter coefficient. Used if filt_en is set to '1'. Location : Left or Right of the center pixel. Frequency : f2 Component : Imaginary

7.6.2.81 Register ADh (offset = ADh) [reset = 0h]

Figure 102. Register ADh

23	22	21	20	19	18	17	16
FILT_COEF_Y_IM_F1							
15	14	13	12	11	10	9	8
FILT_COEF_Y_RE_F1							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Table 125. Register AD Field Descriptions

Bit	Field	Type	Reset	Description
Bits[23:16]	FILT_COEF_Y_IM_F1	R/W	0h	Spatial filter coefficient. Used if filt_en is set to '1'. Location : Above or below the center pixel. Frequency : f1 Component : Imaginary
Bits[15:8]	FILT_COEF_Y_RE_F1	R/W	0h	Spatial filter coefficient. Used if filt_en is set to '1'. Location : Above or below the center pixel. Frequency : f1 Component : Real

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7.6.2.82 Register AEh (offset = AEh) [reset = 0h]

Figure 103. Register AEh

23	22	21	20	19	18	17	16
FILT_COEF_X_IM_F1							
15	14	13	12	11	10	9	8
FILT_COEF_X_RE_F1							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Table 126. Register AE Field Descriptions

Bit	Field	Type	Reset	Description
Bits[23:16]	FILT_COEF_X_IM_F1	R/W	0h	Spatial filter coefficient. Used if filt_en is set to '1'. Location : Left or Right of the center pixel. Frequency : f1 Component : Imaginary
Bits[15:8]	FILT_COEF_X_RE_F1	R/W	0h	Spatial filter coefficient. Used if filt_en is set to '1'. Location : Left or Right of the center pixel. Frequency : f1 Component : Real

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7.6.2.83 Register AFh (offset = AFh) [reset = 0h]

Figure 104. Register AFh

23	22	21	20	19	18	17	16
0	0	OP_UNDERFLOW_INTR_DIS	OP_OVERFLOW_INTR_DIS	ILLUM_OVTEMP_INTR_DIS	SENSOR_OVTEMP_INTR_DIS	0	0
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
0	0	0	MASTER_PLL_LOCK_INTR_DIS	LVDS_PLL_LOCK_INTR_DIS	DDR_CALIBRATION_INTR_DIS	DDR_CONTROLLER_INTR_DIS	0

Table 127. Register AF Field Descriptions

Bit	Field	Type	Reset	Description
Bit D21	OP_UNDERFLOW_INTR_DIS	R/W	0h	disable the interrupt on output data path underflow failure
Bit D20	OP_OVERFLOW_INTR_DIS	R/W	0h	disable the interrupt on output data path overflow failure
Bit D19	ILLUM_OVTEMP_INTR_DIS	R/W	0h	disable the interrupt on illumination overtemperature
Bit D18	SENSOR_OVTEMP_INTR_DIS	R/W	0h	disable the interrupt on sensor overtemperature
Bit D4	MASTER_PLL_LOCK_INTR_DIS	R/W	0h	disable the interrupt on master PLL lock failure
Bit D3	LVDS_PLL_LOCK_INTR_DIS	R/W	0h	disable the interrupt on LVDS PLL lock failure
Bit D2	DDR_CALIBRATION_INTR_DIS	R/W	0h	disable the interrupt on DDR calibration failure
Bit D1	DDR_CONTROLLER_INTR_DIS	R/W	0h	disable the interrupt on DDR initialization failure

7.6.2.84 Register B0h (offset = B0h) [reset = 0h]

Figure 105. Register B0h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
ILLUM_OVTEMP_THRESH							
7	6	5	4	3	2	1	0
SENSOR_OVTEMP_THRESH							

Table 128. Register B0 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[15:8]	ILLUM_OVTEMP_THRESH	R/W	0h	
Bits[7:0]	SENSOR_OVTEMP_THRESH	R/W	0h	

7.6.2.85 Register B1h (offset = B1h) [reset = 5004h]

Figure 106. Register B1h

23	22	21	20	19	18	17	16
0	DELAY_FB_CORR_MODE		DELAY_FB_DC_CORR_MODE		FB_ERROR_CNT_THRESHOLD		
15	14	13	12	11	10	9	8
FB_ERROR_CNT_THRESHOLD					MOD_FB_INV		MOD_REF_INV
7	6	5	4	3	2	1	0
ILLUM_FB_INV	0	0	0	0	1	0	0

Table 129. Register B1 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[22:21]	DELAY_FB_CORR_MODE	R/W	0h	delay correction : delay_fb_corr = (delay_fb_corr_mode*delay_fb_coeff*(delay_fb_illum-delay_fb_comp)/256
Bits[20:19]	DELAY_FB_DC_CORR_MODE	R/W	0h	delay correction : delay_fb_dc_corr = (delay_fb_dc_corr_mode*0.5*delay_fb_coeff*(dc_fb_illum-0.5))/256
Bits[18:11]	FB_ERROR_CNT_THRESHOLD	R/W	Ah	Threshold for maximum number of errors in measurements in 4096 cycles
Bits[10:9]	MOD_FB_INV	R/W	3h	Invert feedback signals before measurement
Bits[8:7]	MOD_REF_INV	R/W	0h	Invert reference pins before measurements

7.6.2.86 Register B2h (offset = B2h) [reset = C00h]

Figure 107. Register B2h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
0	0	0	0	FREQ_RATIO			
7	6	5	4	3	2	1	0
FREQ_RATIO							

Table 130. Register B2 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[11:0]	FREQ_RATIO	R/W	C00h	freq_ratio = f1*4096/f2

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7.6.2.87 Register B3h (offset = B3h) [reset = 800h]

Figure 108. Register B3h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
0	0	0	0	DELAY_FB_COEFF			
7	6	5	4	3	2	1	0
DELAY_FB_COEFF							

Table 131. Register B3 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[11:0]	DELAY_FB_COEFF	R/W	800h	delay_fb_coeff=f*1024/24 MHz. f is equal to base frequency when not using de-aliasing and equal to de-aliasing frequency when using de-aliasing.

7.6.2.88 Register B6h (offset = B6h) [reset = 0h]

Figure 109. Register B6h

23	22	21	20	19	18	17	16
0	0	0	0	FILT_EN	0	FILT_SCALE	
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Table 132. Register B6 Field Descriptions

Bit	Field	Type	Reset	Description
Bit D19	FILT_EN	R/W	0h	Enable spatial filter. The filter acts on the complex representation of phase data at each pixel given by I+jQ. Only the adjacent pixels are used in the filter. Diagonal elements are not taken into consideration. The filter's center has a coefficient of 1+0j.
Bits[17:16]	FILT_SCALE	R/W	0h	Filter coefficients will be scaled by this number. filt_coeff (programmed) = 128 * 2^(2+filt_scale) * coeff where coeff is the complex coefficient with absolute value between 0 and 1.

7.6.3 Serial Interface Register Map

Table 133. TG Register Map

ADDRESS (Hex)	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
02h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	MOD_PLL_UPDATE	1	1
0Bh	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0Ch	0	0	MOD_M1						MOD_M_FRAC1															
0Dh	0	0	MOD_M2						MOD_M_FRAC2															
0Eh	0	0	0	0	0	0	ILLUM_DC_CORR_DIR	ILLUM_DC_CORR				0	0	0	0	0	0	0	0	0	0	1	0	0
0Fh	0	0	0	ILLUM_STATIC_POL	DEMOD_STATIC_POL	MODULATION_HOLD	0	0	0	0	0	0	0	1	MOD_PS2			MOD_PS1			MOD_N2		MOD_N1	
12h	0	0	0	0	0	0	0	0	0	0	QUAD_HOP_OFFSET_F2			QUAD_HOP_OFFSET_F1			QUAD_HOP_EN	0	0	0	0	0	0	0
1Fh	ROW_END								0	0	0	0	0	0	0	0	ROW_START							
20h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	COL_START					0	0	0
21h	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	COL_END					1	1	1
22h	0	0	0	0	0	0	0	COL_RDOUT_DIR	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0
80h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TG_DIS
81h	0	0	0	0	0	0	0	0	0	0	0	SYNC_MODE	0	0	0	0	1	0	1	0	0	0	0	SLAVE_MODE
82h	0	0	PIX_CNT_MAX																					
83h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SUB_FRAME_CNT_MAX				QUAD_CNT_MAX			
CCh	SHUTTER_DIS	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
D6h	0	0	FRAME_SYNC_DELAY																					

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7.6.3.1 Register 2h (offset = 2h) [reset = 0h]

Figure 110. Register 2h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
0	0	0	0	0	MOD_PLL_UPDATE	1	1

Table 134. Register 02 Field Descriptions

Bit	Field	Type	Reset	Description
Bit D2	MOD_PLL_UPDATE	R/W	0h	After updating the PLL registers, set this register to 1 and then back to 0 to update the PLL frequency.

7.6.3.2 Register Ch (offset = Ch) [reset = 100000h]

Figure 111. Register Ch

23	22	21	20	19	18	17	16
0	0	MOD_M1					
15	14	13	12	11	10	9	8
MOD_M_FRAC1							
7	6	5	4	3	2	1	0
MOD_M_FRAC1							

Table 135. Register 0C Field Descriptions

Bit	Field	Type	Reset	Description
Bits[21:16]	MOD_M1	R/W	10h	
Bits[15:0]	MOD_M_FRAC1			

7.6.3.3 Register Dh (offset = Dh) [reset = 100000h]

Figure 112. Register Dh

23	22	21	20	19	18	17	16
0	0	MOD_M2					
15	14	13	12	11	10	9	8
MOD_M_FRAC2							
7	6	5	4	3	2	1	0
MOD_M_FRAC2							

Table 136. Register 0D Field Descriptions

Bit	Field	Type	Reset	Description
Bits[21:16]	MOD_M2	R/W	10h	
Bits[15:0]	MOD_M_FRAC2			

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7.6.3.4 Register Eh (offset = Eh) [reset = 04h]

Figure 113. Register Eh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	ILLUM_DC_CORR_DIR	ILLUM_DC_CORR
15	14	13	12	11	10	9	8
ILLUM_DC_CORR			0	0	0	0	0
7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0

Table 137. Register 0E Field Descriptions

Bit	Field	Type	Reset	Description
Bit D17	ILLUM_DC_CORR_DIR	R/W	0h	Sets the direction of duty cycle correction for illumination output waveforms. Note that when duty cycle is increased, ILLUM_P duty cycle increases and ILLUM_N duty cycle decreases. 0 : Increase the duty cycle of ILLUM_P 1 : Reduce the duty cycle of ILLUM_P
Bits[16:13]	ILLUM_DC_CORR	R/W	0h	Illumination duty cycle can be corrected in steps of about 360ps. The maximum value of this register is 11 which results into a total correction of about +/-4ns.

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7.6.3.5 Register Fh (offset = Fh) [reset = 49Ah]

Figure 114. Register Fh

23	22	21	20	19	18	17	16
0	0	0	ILLUM_STATIC_POL	DEMOD_STATIC_POL	MODULATION_HOLD	0	0
15	14	13	12	11	10	9	8
0	0	0	0	0	1	MOD_PS2	
7	6	5	4	3	2	1	0
MOD_PS2	MOD_PS1			MOD_N2		MOD_N1	

Table 138. Register 0F Field Descriptions

Bit	Field	Type	Reset	Description
Bit D20	ILLUM_STATIC_POL	R/W	0h	Holds illumination pins in static state during the integration time. Set modulation_hold='1' for this register to take effect. 0 : Hold low 1 : Hold high
Bit D19	DEMOD_STATIC_POL	R/W	0h	Holds the pixel demodulation in a static state during the integration time. Set modulation_hold='1' for this register to take effect. 0 : Hold low 1 : Hold high
Bit D18	MODULATION_HOLD	R/W	0h	Hold the demodulation and modulation waveforms to a static state.
Bits [9:7]	MOD_PS2	R/W	0h	
Bits [6:4]	MOD_PS1	R/W	0h	
Bits [3:2]	MOD_N2	R/W	0h	
Bits [1:0]	MOD_N1	R/W	0h	

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7.6.3.6 Register 12h (offset = 12h) [reset = 0h]

Figure 115. Register 12h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
0	0	QUAD_HOP_OFFSET_F2			QUAD_HOP_OFFSET_F1		
7	6	5	4	3	2	1	0
QUAD_HOP_EN	0	0	0	0	0	0	0

Table 139. Register 12 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[13:11]	QUAD_HOP_OFFSET_F2	R/W	0h	The offset of the quad sequence for alternate frames for de-aliasing frequency
Bits[10:8]	QUAD_HOP_OFFSET_F1	R/W	0h	The offset of the quad sequence for alternate frames for base frequency
Bit D7	QUAD_HOP_EN	R/W	0h	Enables a different sequence of quads for odd and even frames

7.6.3.7 Register 1Fh (offset = 1Fh) [reset = EF0000h]

Figure 116. Register 1Fh

23	22	21	20	19	18	17	16
ROW_END							
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
ROW_START							

Table 140. Register 1F Field Descriptions

Bit	Field	Type	Reset	Description
Bits[23:16]	ROW_END	R/W	EFh	end address for row addr bus for default ROI.
Bits[7:0]	ROW_START	R/W	0h	start address for row address bus for the default ROI

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7.6.3.8 Register 20h (offset = 20h) [reset = 0h]

Figure 117. Register 20h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
COL_START					0	0	0

Table 141. Register 20 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[7:3]	COL_START	R/W	0h	start address for col addr bus for default ROI. col_start = (start address) >> 4

7.6.3.9 Register 21h (offset = 21h) [reset = 40009Fh]

Figure 118. Register 21h

23	22	21	20	19	18	17	16
0	1	0	0	0	0	0	0
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
COL_END					1	1	1

Table 142. Register 21 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[7:3]	COL_END	R/W	13h	end address for col address bus for default ROI. col_end = (end address) >> 4

7.6.3.10 Register 22h (offset = 22h) [reset = 12020h]

Figure 119. Register 22h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	COL_RDOUT_DIR
15	14	13	12	11	10	9	8
0	0	1	0	0	0	0	0
7	6	5	4	3	2	1	0
0	0	1	0	0	0	0	0

Table 143. Register 22 Field Descriptions

Bit	Field	Type	Reset	Description
Bit D16	COL_RDOUT_DIR	R/W	1h	Used for mirroring the image along vertical axis (left-right mirroring) 0 : count up 1 : count down

7.6.3.11 Register 80h (offset = 80h) [reset = 1h]

Figure 120. Register 80h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	TG_DIS

Table 144. Register 80 Field Descriptions

Bit	Field	Type	Reset	Description
Bit D0	TG_DIS	R/W	1h	'0' : Normal operation '1' : TFC stops all processing. Streaming comes to a halt. The sensor operation is also halted.

7.6.3.12 Register 81h (offset = 81h) [reset = A0h]

Figure 121. Register 81h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
0	0	0	SYNC_MODE	0	0	0	0
7	6	5	4	3	2	1	0
1	0	1	0	0	0	0	SLAVE_MODE

Table 145. Register 81 Field Descriptions

Bit	Field	Type	Reset	Description
Bit D12	SYNC_MODE	R/W	0h	Puts the TG in sync mode. The TG synchronizes with external input through VD_IN pin for the start of frames, but does not depend on it. If both slave_mode and sync_mode are enabled, sync_mode takes higher priority.
Bit D0	SLAVE_MODE	R/W	0h	Puts the TFC in slave mode. The TFC waits for external sync through VD_IN pin for the start of frames.

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7.6.3.13 Register 82h (offset = 82h) [reset = 186A0h]

Figure 122. Register 82h

23	22	21	20	19	18	17	16
0	0	PIX_CNT_MAX					
15	14	13	12	11	10	9	8
PIX_CNT_MAX							
7	6	5	4	3	2	1	0
PIX_CNT_MAX							

Table 146. Register 82 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[21:0]	PIX_CNT_MAX	R/W	186A0h	Total frame time divided by the number of subframes and quads in terms of system clock cycles.

7.6.3.14 Register 83h (offset = 83h) [reset = 44h]

Figure 123. Register 83h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
SUB_FRAME_CNT_MAX				QUAD_CNT_MAX			

Table 147. Register 83 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[7:4]	SUB_FRAME_CNT_MAX	R/W	4h	Total number of sub frames in each frame. Only values of 1,2,4 and 8 are valid. The behavior is unpredicatable when set to other values. 1 : 1 2 : 2 4 : 4 8 : 8
Bits[3:0]	QUAD_CNT_MAX	R/W	4h	This indicates the total number of quads in each subframe. Only values of 4 and 6 are valid.

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7.6.3.15 Register CCh (offset = CCh) [reset = 400003h]

Figure 124. Register CCh

23	22	21	20	19	18	17	16
SHUTTER_DIS	1	0	0	0	0	0	0
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1

Table 148. Register CC Field Descriptions

Bit	Field	Type	Reset	Description
Bit D23	SHUTTER_DIS	R/W	0h	If set to '1', shutter functionality is disabled. If shutter functionality is disabled, the pixel charge continues to transfer to the storage node during the sensor readout.

7.6.3.16 Register D6h (offset = D6h) [reset = 1h]

Figure 125. Register D6h

23	22	21	20	19	18	17	16
0	0	FRAME_SYNC_DELAY					
15	14	13	12	11	10	9	8
FRAME_SYNC_DELAY							
7	6	5	4	3	2	1	0
FRAME_SYNC_DELAY							

Table 149. Register D6 Field Descriptions

Bit	Field	Type	Reset	Description
Bits[21:0]	FRAME_SYNC_DELAY	R/W	1h	The programmable delay between external vd and synced vd. The minimum value of programmable delay is 1 cycle.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPT9221 is the companion ToF controller IC for the ToF sensor OPT8241. Standalone use of OPT9221 is not recommended. Application information is covered as part of the OPT8241 data sheet.

8.2 Typical Application

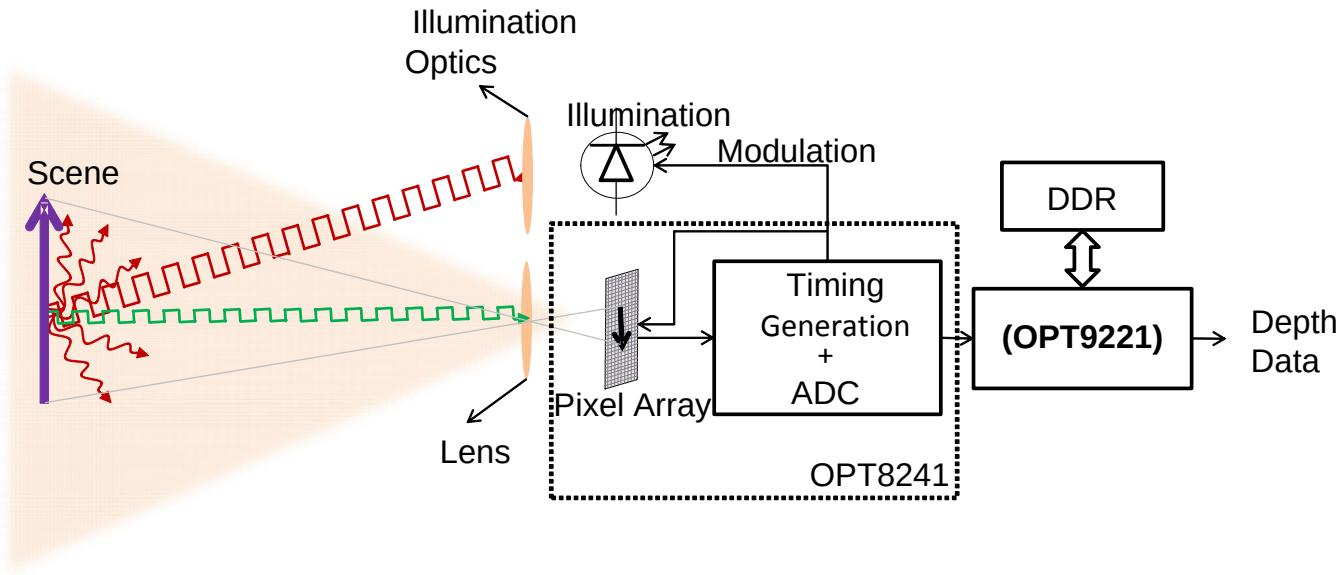

Figure 126. TFC Application Diagram

9 Power Supply Recommendations

9.1 Power-Up Sequence

The power rails VCCA, VCCIO, VCCD_PLL, and VCC_INT can come up in any order. All the rails have to rise monotonically to the recommended voltage levels within t_{RAMP} time (see Figure 16). A power on reset (POR) is internally generated as soon as all the power rails are within the recommended levels.

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10 Layout

10.1 Layout Guidelines

10.1.1 DDR Placement and Routing

The DDR2 interface on the OPT9221 device works at a frequency of 144 MHz. It is recommended to place the DDR2 memory IC as close as possible to the device to avoid any signal integrity issues. All the nets between OPT9221 and the DDR2 memory IC must have a trace length lesser than 50 mm to avoid using terminations. Considering the relatively lower frequency of operation of DDR2 interface and the short trace lengths, termination resistors on data or address pins may not be necessary for proper functioning of the DDR2 interface.

10.1.2 LVDS Receiver

The sensor data receiver pins (named CAP_) are LVDS pairs. The OPT9221 device does not have internal 100-Ω differential termination. Termination resistors need to be placed externally as close as possible to the OPT9221 device.

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10.2 Layout Example

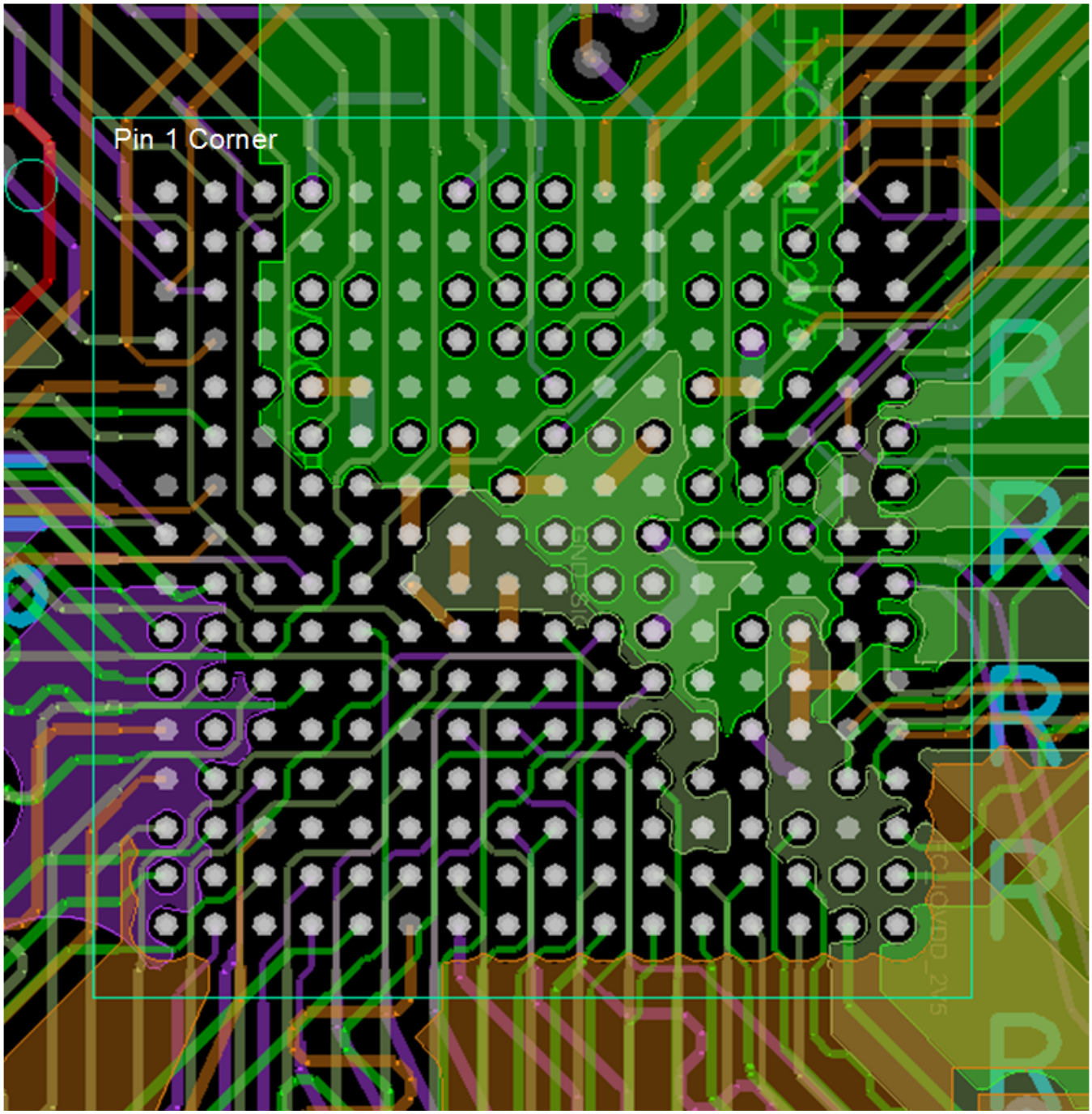

Figure 127.

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

OPT8241 3D Time-of-Flight Sensor Data Sheet, SBAS704

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPT9221ZVM	ACTIVE	NFBGA	ZVM	256	250	TBD	Call TI	Call TI	0 to 70		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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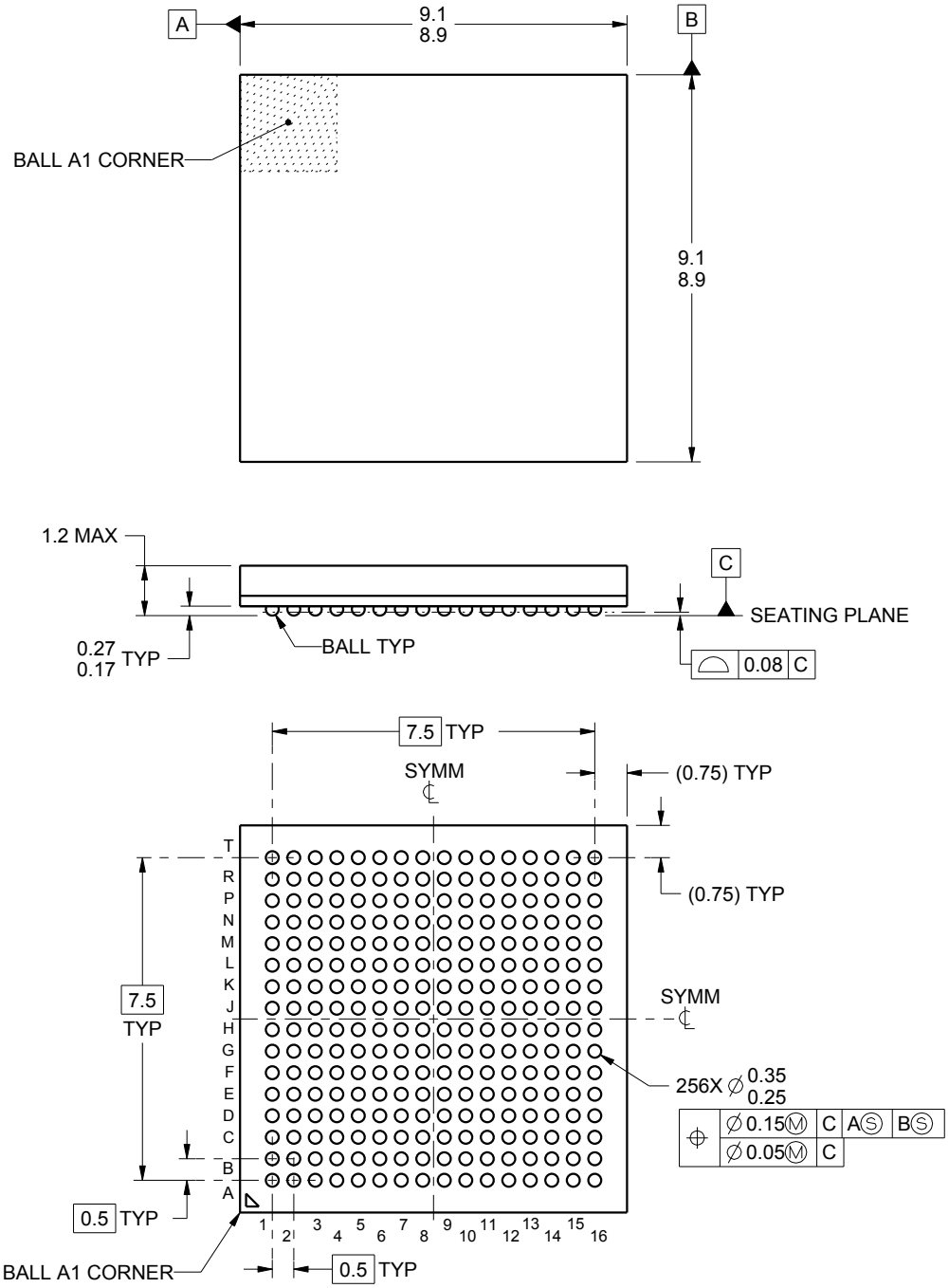
PACKAGE OUTLINE

ZVM0256A

NFBGA - 1.2 mm max height

PLASTIC BALL GRID ARRAY



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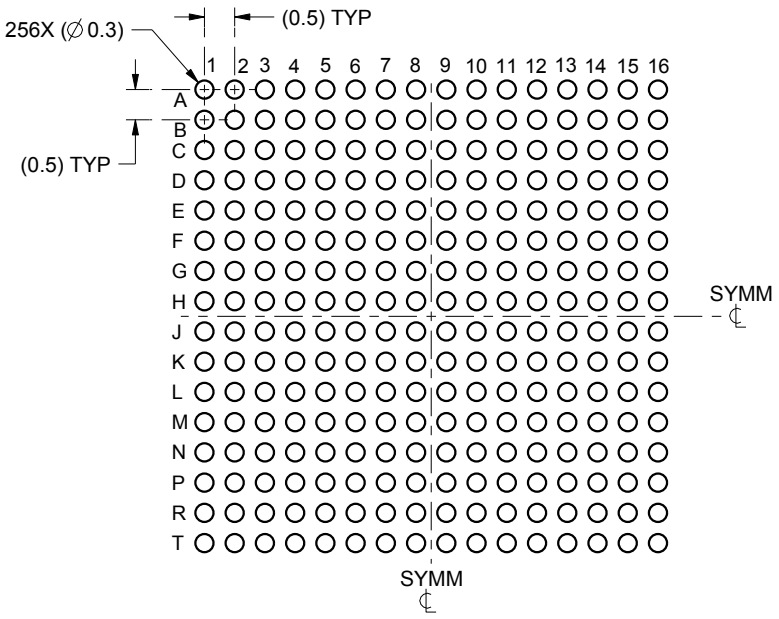
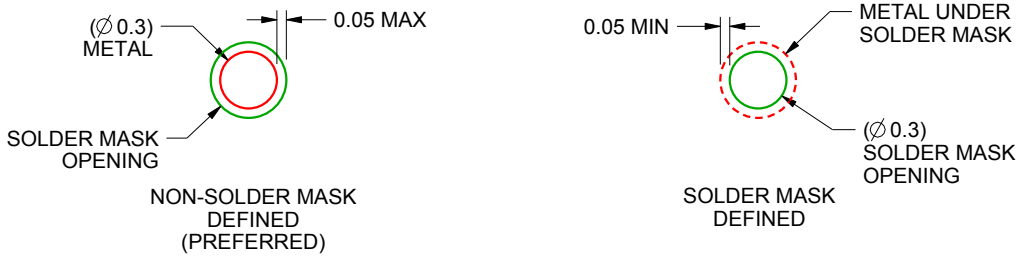
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS
NOT TO SCALE

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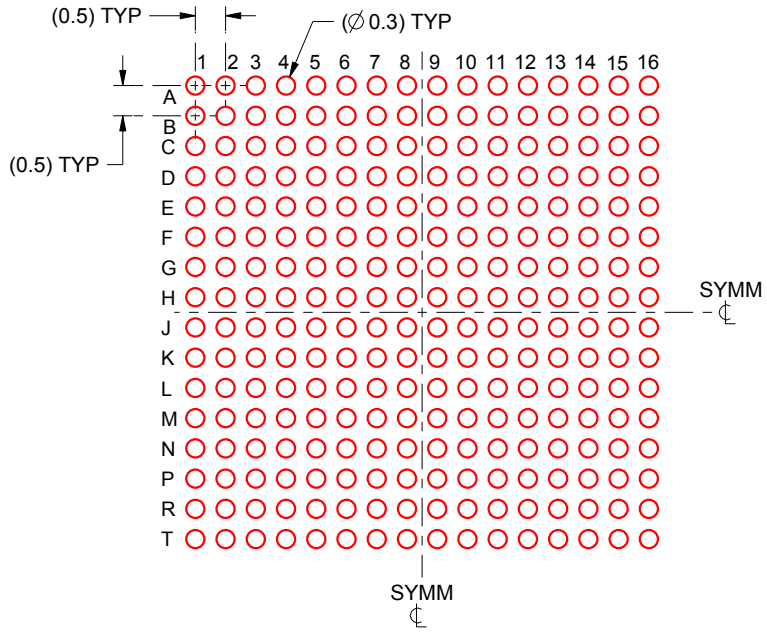
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:8X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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