# OPAx990 40-V rail-to-rail input/output, low offset voltage, low power op amp

## 1 Features

- Low offset voltage: ±250 µV
- Low offset voltage drift: ±0.5 µV/°C
- Low noise: 28 nV/√Hz at 1 kHz
- High common-mode rejection: 120 dB
- Low bias current: ±5 pA
- Rail-to-rail input and output
- MUX-friendly/comparator inputs
  - Amplifier operates with differential inputs up to supply rail
  - Amplifier can be used in open-loop or as comparator
- Wide bandwidth: 1.25-MHz GBW
- High slew rate: 5 V/µs
- Low quiescent current: 125 µA per amplifier
- Wide supply: ±1.35 V to ±20 V, 2.7 V to 40 V
- Robust EMIRR performance: EMI/RFI filters on input and supply pins
- Differential and common-mode input voltage range to supply rail

## 2 Applications

- Multiplexed data-acquisition systems
- Test and measurement equipment
- ADC driver and reference buffer amplifier
- Programmable logic controllers
- High-side and low-side current sensing
- High precision comparator

## 3 Description

The OPAx990 family (OPA990, OPA2990, and OPA4990) is a family of high voltage (40-V) general purpose operational amplifiers. These devices offer excellent DC precision and AC performance, including rail-to-rail input/output, low offset (±250 µV, typ), and low offset drift (±0.5 µV/°C, typ).

Unique features such as differential and common-mode input voltage range to the supply rail, high output current (±80 mA), high slew rate (5 V/µs), and shutdown make the OPAx990 an extremely flexible, robust, and high-performance operational amplifier for high-voltage industrial applications.

The OPAx990 family of op amps is available in *micro*-size packages (such as X2QFN, WSON, and SOT-553), as well as standard packages (such as SOT-23, SOIC, and TSSOP), and is specified from –40°C to 125°C.

**Device Information(1)**

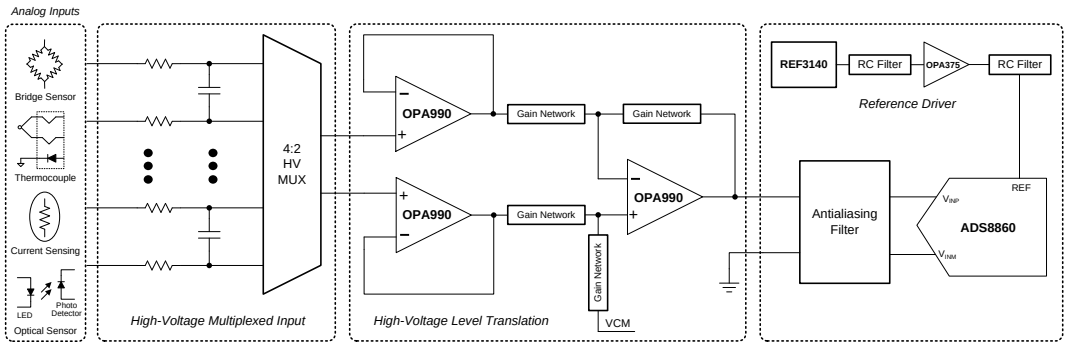
| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| OPA990 | SOT-23 (5)(2) | 2.90 mm × 1.60 mm |
| | SOT-23 (6)(2) | 2.90 mm × 1.60 mm |
| | SC70 (5)(2) | 2.00 mm × 1.25 mm |
| | SOT-553 (5)(2) | 1.60 mm × 1.20 mm |
| OPA2990 | SOIC (8)(2) | 4.90 mm × 3.90 mm |
| | TSSOP (8)(2) | 3.00 mm × 4.40 mm |
| | VSSOP (8)(2) | 3.00 mm × 3.00 mm |
| | WSON (8)(2) | 2.00 mm × 2.00 mm |
| | X2QFN (10)(2) | 2.00 mm × 1.50 mm |
| OPA4990 | SOIC (14)(2) | 8.65 mm × 3.90 mm |
| | TSSOP (14)(2) | 5.00 mm × 4.40 mm |
| | WQFN (16)(2) | 3.00 mm × 3.00 mm |
| | X2QFN (14)(2) | 2.00 mm × 2.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) This package is preview only.

ADVANCE INFORMATION

**OPAx990 in a High-Voltage, Multiplexed, Data-Acquisition System**

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---|---|---|
| February 2019 | * | Initial release. |


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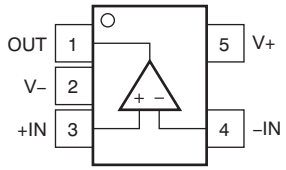
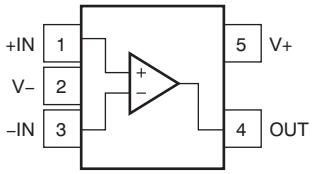
# 5 Pin Configuration and Functions

**OPA990 DBV and DRL Package(1)**
**5-Pin SOT-23 and SOT-553**
**Top View**




(1) Package is preview only.

**OPA990 DCK Package(1)**
**5-Pin SC70**
**Top View**

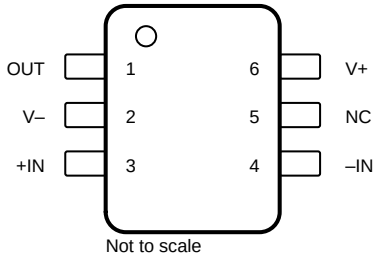



(1) Package is preview only.

**Pin Functions: OPA990**

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | DBV, DCK, and DRL | DCK | | |
| +IN | 3 | 1 | I | Noninverting input |
| –IN | 4 | 3 | I | Inverting input |
| OUT | 1 | 4 | O | Output |
| V+ | 5 | 5 | — | Positive (highest) power supply |
| V– | 2 | 2 | — | Negative (lowest) power supply |

**OPA990S DBV and DRL Package(1)**
**6-Pin SOT-23 and SOT-563**
**Top View**




Not to scale

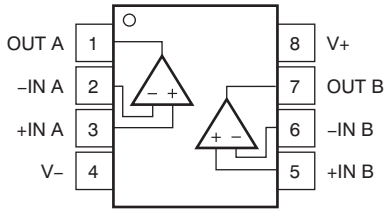
(1) Package is preview only.

**Pin Functions: OPA990S**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | DBV and DRL | | |
| +IN | 3 | I | Noninverting input |
| –IN | 4 | I | Inverting input |
| OUT | 1 | O | Output |
| $\overline{\text{SHDN}}$ | 5 | I | Shutdown (active low) logic input |
| V+ | 6 | — | Positive (highest) power supply |
| V– | 2 | — | Negative (lowest) power supply |

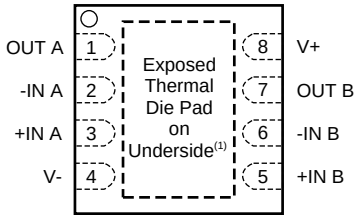
ADVANCE INFORMATION

**OPA2990 D, DGK, and PW Packages(1)**
**8-Pin SOIC, TSSOP, and VSSOP**
**Top View**




(1) Package is preview only.

**OPA2990 DSG Package(1)(2)**
**8-Pin WSON With Exposed Thermal Pad**
**Top View**




(1) Connect thermal pad to V–.
(2) Package is preview only.

## Pin Functions: OPA2990

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | SOIC, TSSOP, VSSOP, and WSON | | |
| +IN A | 3 | I | Noninverting input, channel A |
| +IN B | 5 | I | Noninverting input, channel B |
| –IN A | 2 | I | Inverting input, channel A |
| –IN B | 6 | I | Inverting input, channel B |
| OUT A | 1 | O | Output, channel A |
| OUT B | 7 | O | Output, channel B |
| V+ | 8 | — | Positive (highest) power supply |
| V– | 4 | — | Negative (lowest) power supply |

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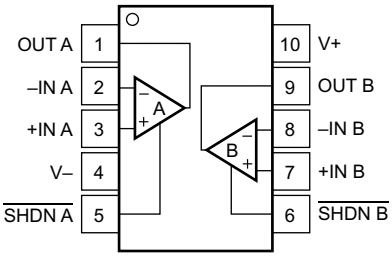
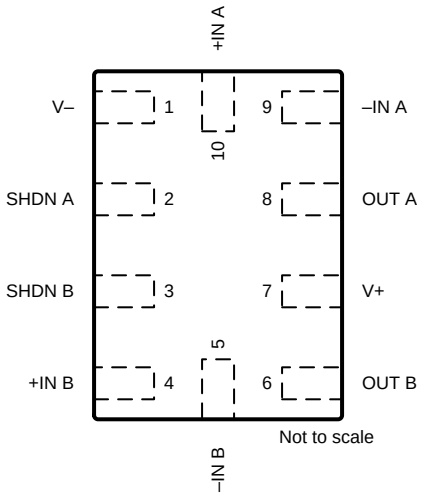
**OPA2990S DGS Package(1)**
**10-Pin VSSOP**
**Top View**




(1) Package is preview only.

**OPA2990S RUG Package(1)**
**10-Pin X2QFN**
**Top View**




(1) Package is preview only.

**Pin Functions: OPA2990S**

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | VSSOP | X2QFN | | |
| +IN A | 3 | 10 | I | Noninverting input, channel A |
| +IN B | 7 | 4 | I | Noninverting input, channel B |
| –IN A | 2 | 9 | I | Inverting input, channel A |
| –IN B | 8 | 5 | I | Inverting input, channel B |
| OUT A | 1 | 8 | O | Output, channel A |
| OUT B | 9 | 6 | O | Output, channel B |
| $\overline{\text{SHDN A}}$ | 5 | 2 | I | Shutdown (active low), channel A, logic input |
| $\overline{\text{SHDN B}}$ | 6 | 3 | I | Shutdown (active low), channel B, logic input |
| V+ | 10 | 7 | — | Positive (highest) power supply |
| V– | 4 | 1 | — | Negative (lowest) power supply |

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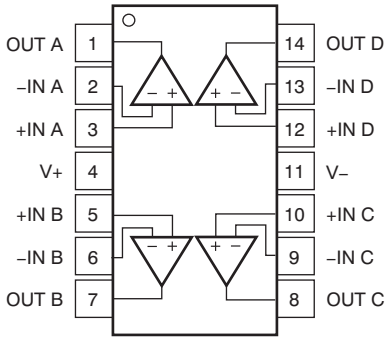
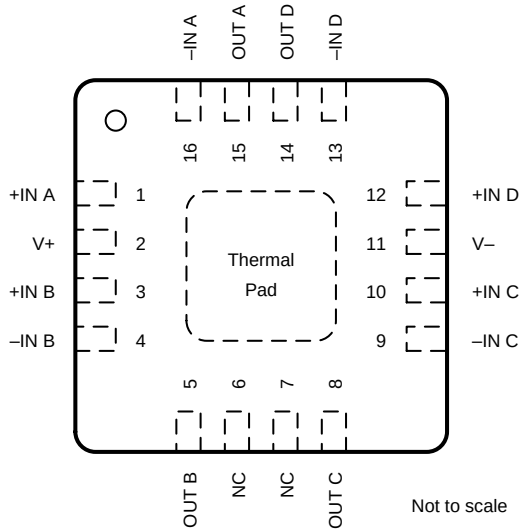
**OPA4990 D and PW Packages(1)**
**14-Pin SOIC and TSSOP**
**Top View**




(1) Package is preview only.

**OPA4990 RTE Package(2)**
**16-Pin WQFN With Exposed Thermal Pad**
**Top View**




(1) Connect thermal pad to V–.
(2) Package is preview only.

**Pin Functions: OPA4990**

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | SOIC and TSSOP | WQFN | | |
| +IN A | 3 | 1 | I | Noninverting input, channel A |
| +IN B | 5 | 3 | I | Noninverting input, channel B |
| +IN C | 10 | 10 | I | Noninverting input, channel C |
| +IN D | 12 | 12 | I | Noninverting input, channel D |
| –IN A | 2 | 16 | I | Inverting input, channel A |
| –IN B | 6 | 4 | I | Inverting input, channel B |
| –IN C | 9 | 9 | I | Inverting input, channel C |
| –IN D | 13 | 12 | I | Inverting input, channel D |
| NC | — | 6, 7 | — | Do not connect |
| OUT A | 1 | 15 | O | Output, channel A |
| OUT B | 7 | 5 | O | Output, channel B |
| OUT C | 8 | 8 | O | Output, channel C |
| OUT D | 14 | 14 | O | Output, channel D |
| V+ | 4 | 2 | — | Positive (highest) power supply |
| V– | 11 | 11 | — | Negative (lowest) power supply |

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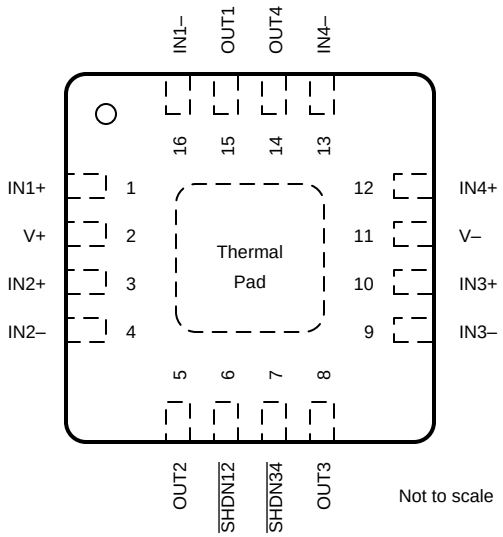
**OPA4990S RTE Package(1)**
**16-Pin WQFN With Exposed Thermal Pad**
**Top View**




(1) Package is preview only.

## Pin Functions: OPA4990S

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | WQFN | | |
| IN1+ | 1 | I | Noninverting input, channel 1 |
| IN1– | 16 | I | Inverting input, channel 1 |
| IN2+ | 3 | I | Noninverting input, channel 2 |
| IN2– | 4 | I | Inverting input, channel 2 |
| IN3+ | 10 | I | Noninverting input, channel 3 |
| IN3– | 9 | I | Inverting input, channel 3 |
| IN4+ | 12 | I | Noninverting input, channel 4 |
| IN4– | 13 | I | Inverting input, channel 4 |
| OUT1 | 15 | O | Output, channel 1 |
| OUT2 | 5 | O | Output, channel 2 |
| OUT3 | 8 | O | Output, channel 3 |
| OUT4 | 14 | O | Output, channel 4 |
| $\overline{\text{SHDN12}}$ | 6 | I | Shutdown (active low), channel 1 and 2, logic input |
| $\overline{\text{SHDN34}}$ | 7 | I | Shutdown (active low), channel 3 and 4, logic input |
| VCC+ | 2 | — | Positive (highest) power supply |
| VCC– | 11 | — | Negative (lowest) power supply |

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_S$ = (V+) – (V–) | | 0 | 42 | V |
| Signal input pins | Common-mode voltage(2) | (V–) – 0.5 | (V+) + 0.5 | V |
| | Differential voltage(2) | | $V_S$ + 0.2 | V |
| | Current(2) | –10 | 10 | mA |
| Output short-circuit(3) | | Continuous | | |
| Operating ambient temperature, $T_A$ | | –55 | 150 | °C |
| Junction temperature, $T_J$ | | | 150 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_S$ | Supply voltage, (V+) – (V–) | 2.7 | 40 | V |
| $V_I$ | Input voltage range | (V–) – 0.1 | (V+) + 0.1 | V |
| $T_A$ | Specified temperature | –40 | 125 | °C |

## 6.4 Thermal Information for Single Channel

| THERMAL METRIC(1) | | OPA990, OPA990S | | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | DBV(2) (SOT-23) | | DCK(2) (SC70) | DRL(2) (SOT-553) | | |
| | | 5 PINS | 6 PINS | 5 PINS | 5 PINS | 6 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | TBD | TBD | TBD | TBD | TBD | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | TBD | TBD | TBD | TBD | TBD | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | TBD | TBD | TBD | TBD | TBD | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | TBD | TBD | TBD | TBD | TBD | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | TBD | TBD | TBD | TBD | TBD | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | TBD | TBD | TBD | TBD | TBD | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) This package option is preview for OPA990.

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## 6.5 Thermal Information for Dual Channel

| THERMAL METRIC(1) | | OPA2990, OPA2990S | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | D(2) (SOIC) | DDF(2) (SOT-23-8) | DGK(2) (VSSOP) | DGS(2) (VSSOP) | DSG(2) (WSON) | PW(2) (TSSOP) | RUG(2) (X2QFN) | |
| | | 8 PINS | 8 PINS | 8 PINS | 10 PINS | 8 PINS | 8 PINS | 10 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 138.7 | TBD | TBD | TBD | TBD | TBD | TBD | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 78.7 | TBD | TBD | TBD | TBD | TBD | TBD | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 82.2 | TBD | TBD | TBD | TBD | TBD | TBD | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 27.8 | TBD | TBD | TBD | TBD | TBD | TBD | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 81.4 | TBD | TBD | TBD | TBD | TBD | TBD | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | TBD | TBD | TBD | TBD | TBD | TBD | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) This package option is preview for OPA2990.

## 6.6 Thermal Information for Quad Channel

| THERMAL METRIC(1) | | OPA4990, OPA4990S | | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | D(2) (SOIC) | PW(2) (TSSOP) | | RTE(2) (WQFN) | RUC(2) (WQFN) | |
| | | 14 PINS | 14 PINS | 16 PINS | 16 PINS | 14 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | TBD | TBD | TBD | TBD | TBD | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | TBD | TBD | TBD | TBD | TBD | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | TBD | TBD | TBD | TBD | TBD | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | TBD | TBD | TBD | TBD | TBD | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | TBD | TBD | TBD | TBD | TBD | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | TBD | TBD | TBD | TBD | TBD | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) This package option is preview for OPA4990.

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## 6.7 Electrical Characteristics

For $V_S$ = (V+) – (V–) = 2.7 V to 40 V (±1.35 V to ±20 V) at $T_A$ = 25°C, $R_L$ = 10 kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{OUT}$ = $V_S$ / 2, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | | |
| $V_{OS}$ | Input offset voltage | | | | ±0.25 | ±1.6 | mV |
| | | | $T_A$ = –40°C to 125°C | | | ±1.75 | |
| $dV_{OS}/dT$ | Input offset voltage drift | | $T_A$ = –40°C to 125°C | | ±0.5 | | µV/°C |
| PSRR | Input offset voltage versus power supply | $V_{CM}$ = V– | $T_A$ = –40°C to 125°C | | ±0.7 | ±5 | µV/V |
| | Channel separation | f = 0 Hz | | | 5 | | µV/V |
| **INPUT BIAS CURRENT** | | | | | | | |
| $I_B$ | Input bias current | | | | ±10 | ±100 | pA |
| | | | $T_A$ = –40°C to 125°C | | | ±3.5 | nA |
| $I_{OS}$ | Input offset current | | | | ±0.1 | ±100 | pA |
| | | | $T_A$ = –40°C to 125°C | | | ±3.5 | nA |
| **NOISE** | | | | | | | |
| $E_N$ | Input voltage noise | f = 0.1 Hz to 10 Hz | | | 6 | | $\mu V_{PP}$ |
| | | | | | 2.1 | | $\mu V_{RMS}$ |
| $e_N$ | Input voltage noise density | f = 1 kHz | | | 33 | | nV/√Hz |
| | | f = 10 kHz | | | 28 | | |
| $i_N$ | Input current noise | f = 1 kHz | | | 2 | | fA/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | | | |
| $V_{CM}$ | Common-mode voltage range | | | (V–) – 0.2 | | (V+) + 0.2 | V |
| CMRR | Common-mode rejection ratio | $V_S$ = 40 V, (V–) – 0.1 V < $V_{CM}$ < (V+) – 2 V (Main input pair) | $T_A$ = –40°C to 125°C | 104 | 120 | | dB |
| | | $V_S$ = 4 V, (V–) – 0.1 V < $V_{CM}$ < (V+) – 2 V (Main input pair) | | 80 | 95 | | |
| | | $V_S$ = 4 – 40 V, (V+) – 1 V < $V_{CM}$ < (V+) + 0.1 V (Aux input pair) | | | 80 | | |
| **INPUT CAPACITANCE** | | | | | | | |
| $Z_{ID}$ | Differential | | | | 100 \|\| 3 | | MΩ \|\| pF |
| $Z_{ICM}$ | Common-mode | | | | 6 \|\| 1 | | TΩ \|\| pF |
| **OPEN-LOOP GAIN** | | | | | | | |
| $A_{OL}$ | Open-loop voltage gain | $V_S$ = 40 V, $V_{CM}$ = V– (V–) + 0.1 V < $V_O$ < (V+) – 0.1 V | | 130 | 145 | | dB |
| | | | $T_A$ = –40°C to 125°C | 126 | 142 | | |
| | | $V_S$ = 4 V, $V_{CM}$ = V– (V–) + 0.1 V < $V_O$ < (V+) – 0.1 V | | 115 | 130 | | |
| | | | $T_A$ = –40°C to 125°C | 110 | 125 | | |
| **FREQUENCY RESPONSE** | | | | | | | |
| GBW | Gain-bandwidth product | | | | 1.25 | | MHz |
| SR | Slew rate | $V_S$ = 40 V, G = +1, $C_L$ = 20 pF | | | 4.5 | | V/µs |
| $t_S$ | Settling time | To 0.1%, $V_S$ = 40 V, $V_{STEP}$ = 10 V , G = +1, CL = 20 pF | | | 4 | | µs |
| | | To 0.1%, $V_S$ = 40 V, $V_{STEP}$ = 2 V , G = +1, CL = 20 pF | | | 2 | | |
| | | To 0.01%, $V_S$ = 40 V, $V_{STEP}$ = 10 V , G = +1, CL = 20 pF | | | 5 | | |
| | | To 0.01%, $V_S$ = 40 V, $V_{STEP}$ = 2 V , G = +1, CL = 20 pF | | | 3 | | |
| | Phase margin | G = +1, $R_L$ = 10 kΩ, $C_L$ = 20 pF | | | 60 | | ° |
| | Overload recovery time | $V_{IN}$ × gain > $V_S$ | | | 1 | | µs |
| THD+N | Total harmonic distortion + noise | $V_S$ = 40 V, $V_O$ = 1 $V_{RMS}$, G = -1, f = 1 kHz | | | 0.001% | | |

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## Electrical Characteristics (continued)

For $V_S$ = (V+) – (V–) = 2.7 V to 40 V (±1.35 V to ±20 V) at $T_A$ = 25°C, $R_L$ = 10 kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{OUT}$ = $V_S$ / 2, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **OUTPUT** | | | | | | | |
| | Voltage output swing from rail | Positive rail headroom | $V_S$ = 4 V to 40 V, $R_L$ = no load | | 25 | 50 | mV |
| | | | $V_S$ = 4 V to 40 V, $R_L$ = 10 kΩ | | 50 | 100 | |
| | | | $V_S$ = 4 V to 40 V, $R_L$ = 2 kΩ | | 200 | 500 | |
| | | Negative rail headroom | $V_S$ = 4 V to 40 V, $R_L$ = no load | | 25 | 50 | |
| | | | $V_S$ = 4 V to 40 V, $R_L$ = 10 kΩ | | 50 | 100 | |
| | | | $V_S$ = 4 V to 40 V, $R_L$ = 2 kΩ | | 200 | 500 | |
| $I_{SC}$ | Short-circuit current | | | | ±80 | | mA |
| $C_{LOAD}$ | Capacitive load drive | | | | 100 | | pF |
| $Z_O$ | Open-loop output impedance | f = 1 MHz, $I_O$ = 0 A | | | 900 | | Ω |
| **POWER SUPPLY** | | | | | | | |
| $I_Q$ | Quiescent current per amplifier | $I_O$ = 0 A | | | 120 | 150 | µA |
| | | | $T_A$ = –40°C to 125°C | | | 150 | |
| | Turn-on time | At $T_A$ = 25°C, $V_S$ = 40 V, $V_S$ ramp rate > 0.3 V/µs | | | 1 | | µs |

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# 7 Detailed Description

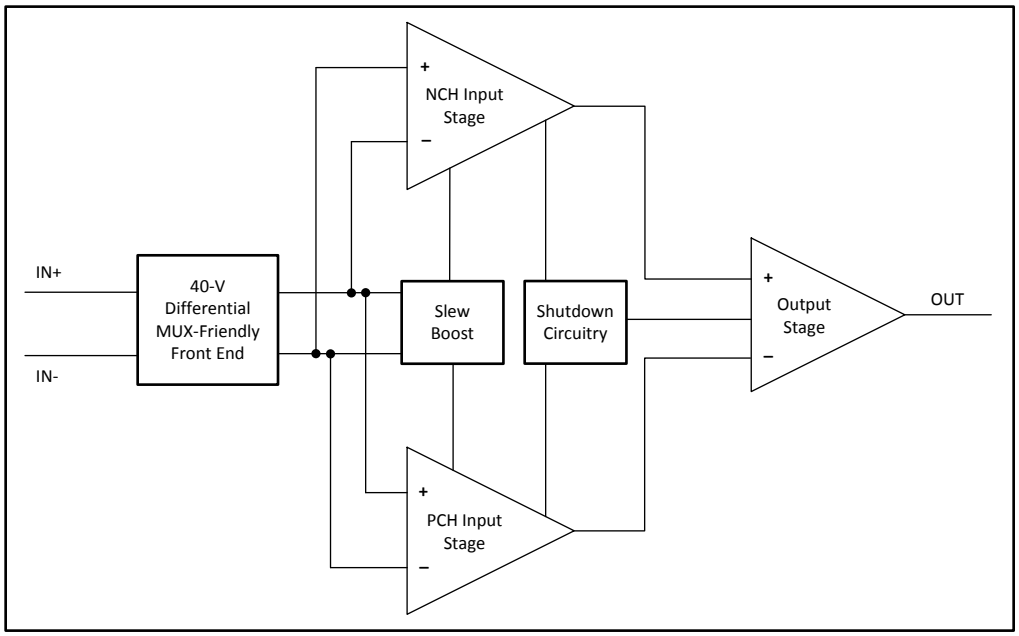
## 7.1 Overview

The OPAx990 family (OPA990, OPA2990, and OPA4990) is a new generation of 40-V general purpose operational amplifiers.

These devices offer excellent DC precision and AC performance, including rail-to-rail input/output, low offset (±250 µV, typ), low offset drift (±0.5 µV/°C, typ), and 1.25-MHz bandwidth.

Unique features such as differential and common-mode input-voltage range to the supply rail, high output current (±80 mA), high slew rate (5 V/µs), and shutdown make the OPAx990 a robust, high-performance operational amplifier for high-voltage industrial applications.

## 7.2 Functional Block Diagram

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## 7.3 Feature Description

### 7.3.1 Input Protection Circuitry

The OPAx990 uses a unique input architecture to eliminate the requirement for input protection diodes but still provides robust input protection under transient conditions. Figure 1 shows conventional input diode protection schemes that are activated by fast transient step responses and introduce signal distortion and settling time delays because of alternate current paths, as shown in Figure 2. For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes, causing an increase in input current and resulting in extended settling time, as Figure 3 shows.

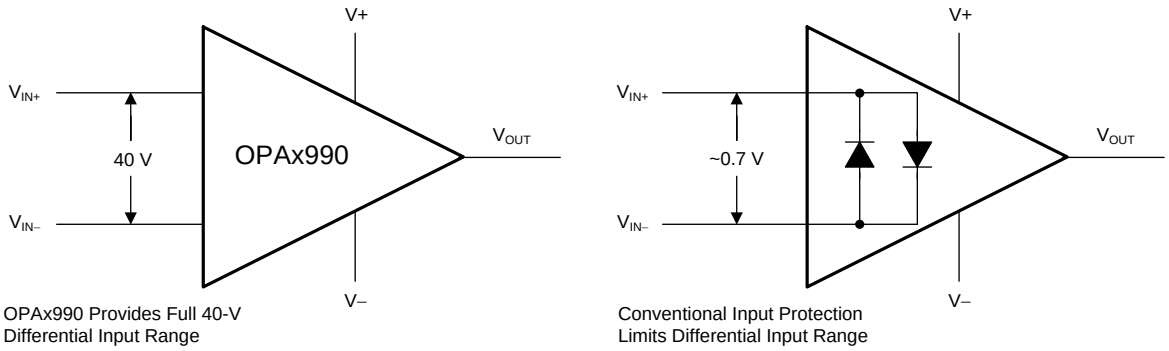


**Figure 1. OPAx990 Input Protection Does Not Limit Differential Input Capability**

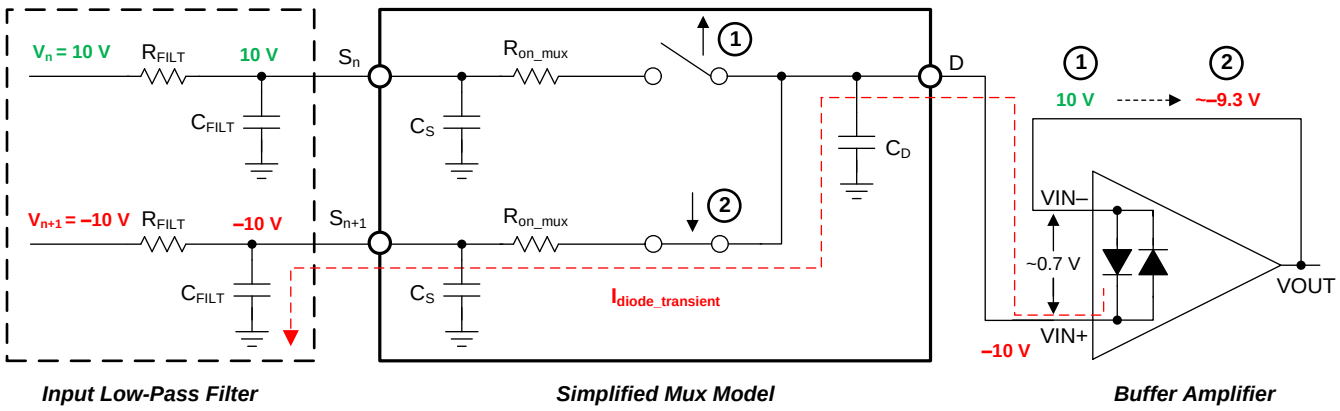


**Figure 2. Back-to-Back Diodes Create Settling Issues**

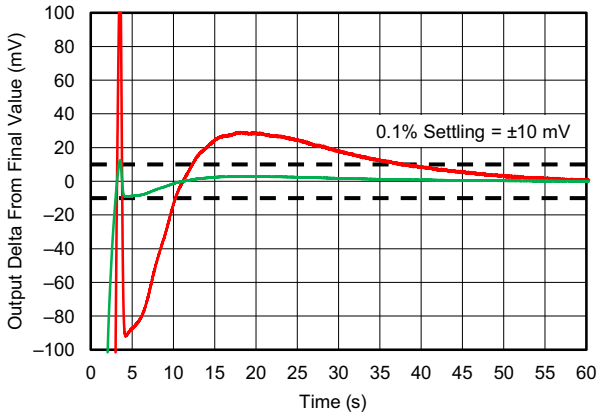


**Figure 3. OPAx990 Protection Circuit Maintains Fast-Settling Transient Response**

ADVANCE INFORMATION

## Feature Description (continued)

The OPAx990 family of operational amplifiers provides a true high-impedance differential input capability for high-voltage applications. This patented input protection architecture does not introduce additional signal distortion or delayed settling time, making the device an optimal op amp for multichannel, high-switched, input applications. The OPA990 tolerates a maximum differential swing (voltage between inverting and non-inverting pins of the op amp) of up to 40 V, making the device suitable for use as a comparator or in applications with fast-ramping input signals such as multiplexed data-acquisition systems.

### 7.3.2 EMI Rejection

The OPAx990 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx990 benefits from these design improvements. The *EMI Rejection Ratio of Operational Amplifiers* application report contains detailed information on the topic of EMIRR performance as it relates to op amps and is available for download from www.ti.com.

### 7.3.3 Phase Reversal Protection

The OPAx990 family has internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in non-inverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPAx990 is a rail-to-rail input op amp; therefore, the common-mode range can extend up to the rails. Input signals beyond the rails do not cause phase reversal; instead, the output limits into the appropriate rail.

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## Feature Description (continued)

### 7.3.4 Thermal Protection

The internal power dissipation of any amplifier causes its internal (junction) temperature to rise. This phenomenon is called *self heating*. The absolute maximum junction temperature of the OPAx990 is 150°C. Exceeding this temperature causes damage to the device. The OPAx990 has a thermal protection feature that prevents damage from self heating. The protection works by monitoring the temperature of the device and turning off the op amp output drive for temperatures above 140°C. Figure 4 shows an application example for the OPA990 that has significant self heating (159°C) because of its power dissipation (0.81 W). Thermal calculations indicate that for an ambient temperature of 65°C the device junction temperature must reach 187°C. The actual device, however, turns off the output drive to maintain a safe junction temperature. Figure 4 shows how the circuit behaves during thermal protection. During normal operation, the device acts as a buffer so the output is 3 V. When self heating causes the device junction temperature to increase above 140°C, the thermal protection forces the output to a high-impedance state and the output is pulled to ground through resistor RL.

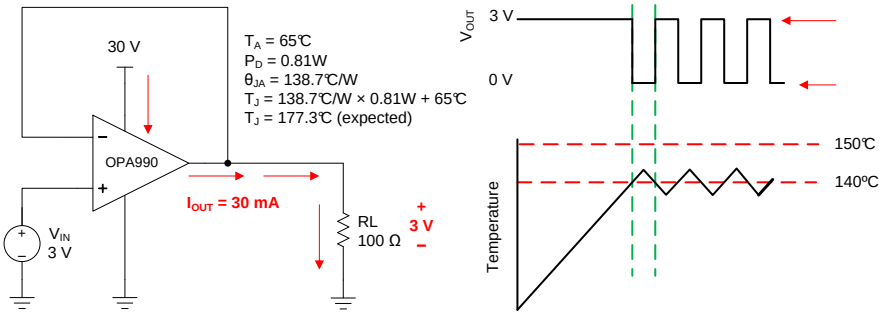


**Figure 4. Thermal Protection**

### 7.3.5 Capacitive Load and Stability

The OPAx990 features a resistive output stage capable of driving moderate capacitive loads, and by leveraging an isolation resistor, the device can easily be configured to drive large capacitive loads. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier will be stable in operation.

For additional drive capability in unity-gain configurations, improve capacitive load drive by inserting a small (10 Ω to 20 Ω) resistor, $R_{ISO}$, in series with the output, as shown in Figure 5. This resistor significantly reduces ringing and maintains DC performance for purely capacitive loads. However, if a resistive load is in parallel with the capacitive load, then a voltage divider is created, thus introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio $R_{ISO}$ / $R_L$, and is generally negligible at low output levels. A high capacitive load drive makes the OPAx990 well suited for applications such as reference buffers, MOSFET gate drives, and cable-shield drives. The circuit shown in Figure 5 uses an isolation resistor, $R_{ISO}$, to stabilize the output of an op amp. $R_{ISO}$ modifies the open-loop gain of the system for increased phase margin.

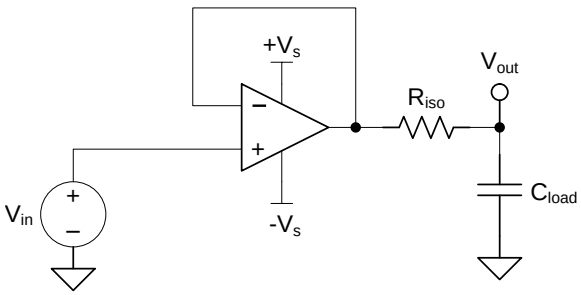


**Figure 5. Extending Capacitive Load Drive with the OPA990**

ADVANCE INFORMATION

## Feature Description (continued)

### 7.3.6 Common-Mode Voltage Range

The OPAx990 is a 40-V, true rail-to-rail input operational amplifier with an input common-mode range that extends 100 mV beyond either supply rail. This wide range is achieved with paralleled complementary N-channel and P-channel differential input pairs, as shown in Figure 6. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1 V to 100 mV above the positive supply. The P-channel pair is active for inputs from 100 mV below the negative supply to approximately (V+) – 2 V. There is a small transition region, typically (V+) – 2 V to (V+) – 1 V in which both input pairs are on. This transition region can vary modestly with process variation, and within this region PSRR, CMRR, offset voltage, offset drift, noise and THD performance may be degraded compared to operation outside this region. To achieve best performance for the OPAx990 family, avoid this transition region when possible.

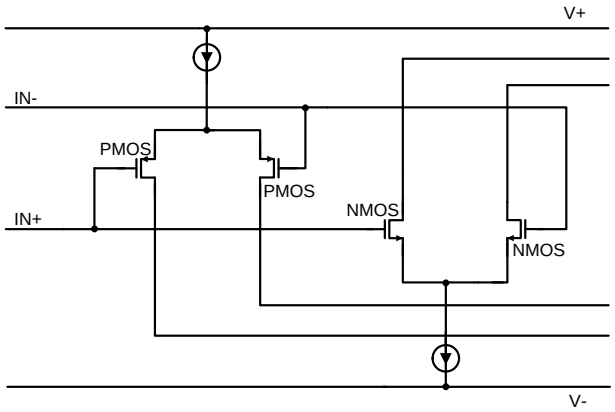


**Figure 6. Rail-to-Rail Input Stage**

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## Feature Description (continued)

### 7.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. Figure 7 shows an illustration of the ESD circuits contained in the OPAx990 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

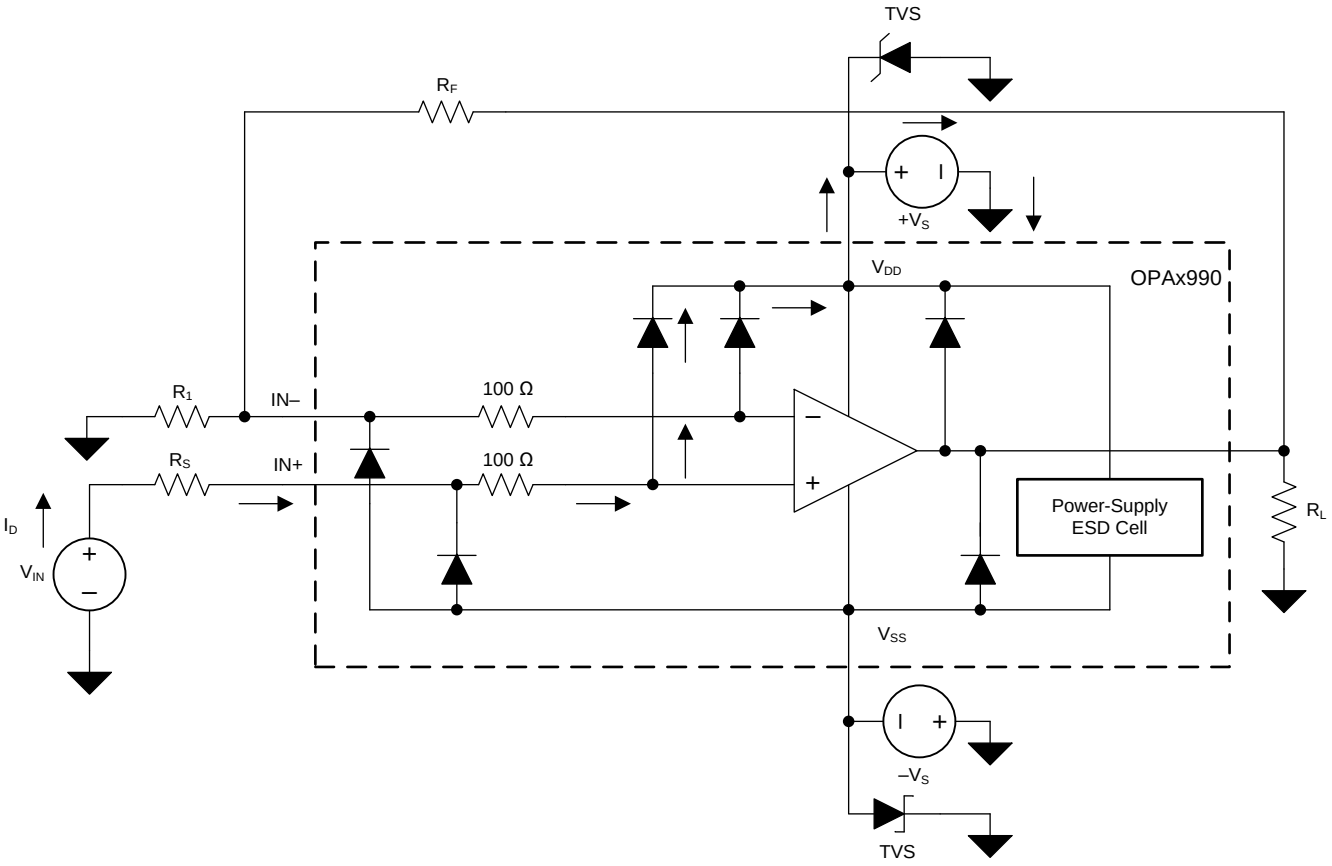


**Figure 7. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application**

ADVANCE INFORMATION

## Feature Description (continued)

An ESD event is very short in duration and very high voltage (for example, 1 kV, 100 ns), whereas an EOS event is long duration and lower voltage (for example, 50 V, 100 ms). The ESD diodes are designed for out-of-circuit ESD protection (that is, during assembly, test, and storage of the device before being soldered to the PCB). During an ESD event, the ESD signal is passed through the ESD steering diodes to an absorption circuit (labeled ESD power-supply circuit). The ESD absorption circuit clamps the supplies to a safe level.

Although this behavior is necessary for out-of-circuit protection, excessive current and damage is caused if activated in-circuit. A transient voltage suppressors (TVS) can be used to prevent against damage caused by turning on the ESD absorption circuit during an in-circuit ESD event. Using the appropriate current limiting resistors and TVS diodes allows for the use of device ESD diodes to protect against EOS events.

### 7.3.8 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the OPAx990 is approximately 1 µs.

## 7.4 Device Functional Modes

The OPAx990 has a single functional mode and is operational when the power-supply voltage is greater than or equal to 2.7 V (±1.35 V). The maximum power supply voltage for the OPAx990 is 40 V (±20 V).

The OPAx990S devices feature a shutdown pin, which can be used to place the op amp into a low-power mode.

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# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The OPAx990 family offers excellent DC precision and AC performance. These devices operate up to 40-V supply rails and offer true rail-to-rail input/output, low offset voltage and offset voltage drift, as well as 1.25-MHz bandwidth and high output drive. These features make the OPAx990 a robust, high-performance operational amplifier for high-voltage industrial applications.

## 8.2 Typical Applications

### 8.2.1 Slew Rate Limit for Input Protection

In control systems for valves or motors, abrupt changes in voltages or currents can cause mechanical damages. By controlling the slew rate of the command voltages into the drive circuits, the load voltages ramps up and down at a safe rate. For symmetrical slew-rate applications (positive slew rate equals negative slew rate), one additional op amp provides slew-rate control for a given analog gain stage. The unique input protection and high output current and slew rate of the OPAx990 make the device an optimal amplifier to achieve slew rate control for both dual- and single-supply systems. Figure 8 shows the OPA990 in a slew-rate limit design.

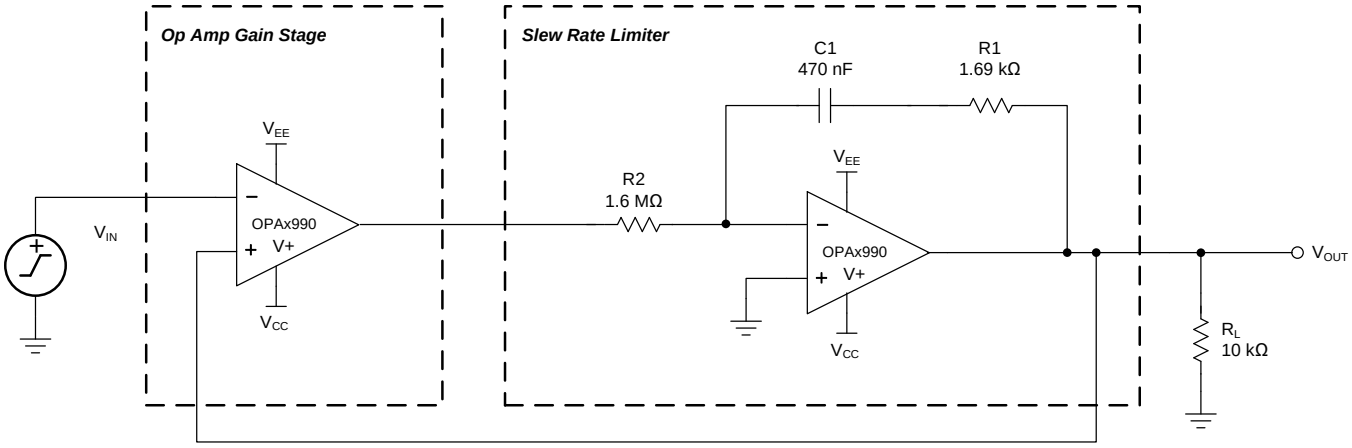


**Figure 8. Slew Rate Limiter Uses One Op Amp**

ADVANCE INFORMATION

# 9 Power-Supply Recommendations

The OPAx990 is specified for operation from 2.7 V to 40 V (±1.35 V to ±20 V); many specifications apply from –40°C to 125°C or with specific supply voltages and test conditions.

**CAUTION**

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings*.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout* section.

# 10 Layout

## 10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information refer to *Circuit board layout techniques* (SLOA089).
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in Figure 10, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

## 10.2 Layout Example

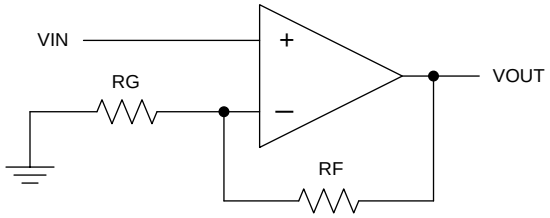


**Figure 9. Schematic Representation**


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## Layout Example (continued)

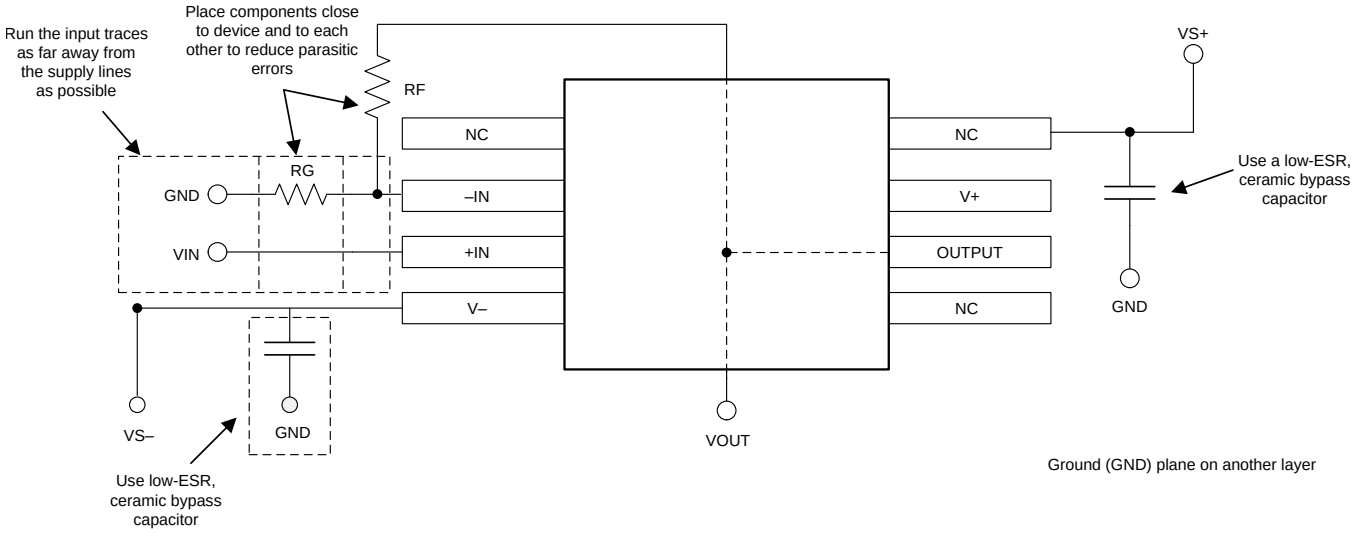


**Figure 10. Operational Amplifier Board Layout for Noninverting Configuration**

ADVANCE INFORMATION

# 11 Device and Documentation Support

## 11.1 Device Support

### 11.1.1 Development Support

#### *11.1.1.1 TINA-TI™ (Free Software Download)*

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

**NOTE**

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

## 11.2 Documentation Support

### 11.2.1 Related Documentation

Texas Instruments, *Circuit board layout techniques*

Texas Instruments, *Op amps for everyone*

## 11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

**Table 1. Related Links**

| PARTS | PRODUCT FOLDER | ORDER NOW | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| OPA2990 | Click here | Click here | Click here | Click here | Click here |

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### 11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.5 Trademarks

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### 11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA2990IDR | PREVIEW | SOIC | D | 8 | 2500 | TBD | Call TI | Call TI | -40 to 125 | | |
| OPA2990IPWR | PREVIEW | TSSOP | PW | 8 | 2000 | TBD | Call TI | Call TI | -40 to 125 | | |
| POPA2990IDR | ACTIVE | SOIC | D | 8 | 2500 | TBD | Call TI | Call TI | -40 to 125 | | Samples |
| POPA2990IPWR | ACTIVE | TSSOP | PW | 8 | 2000 | TBD | Call TI | Call TI | -40 to 125 | | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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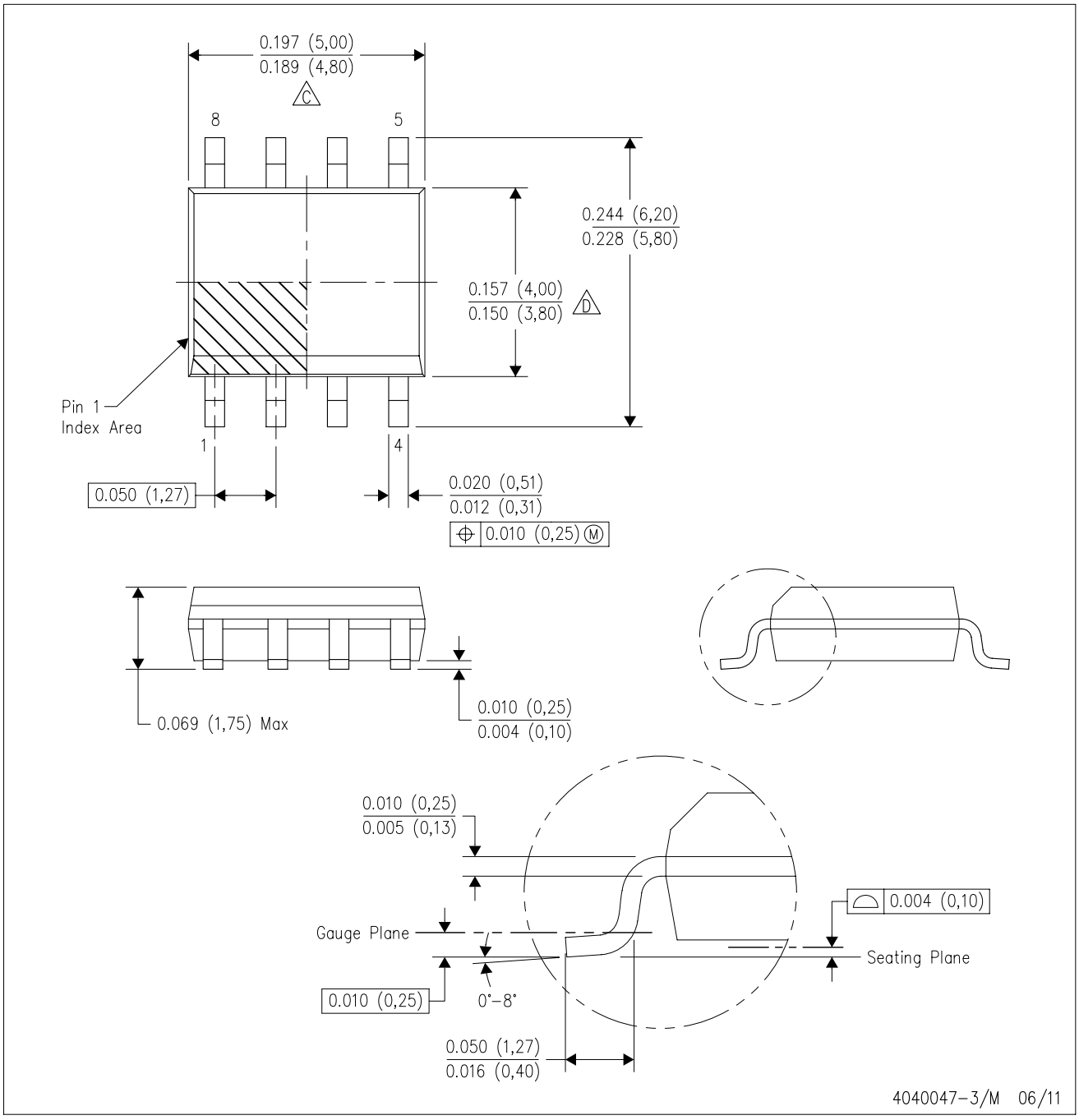
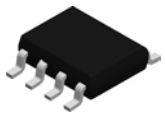
D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

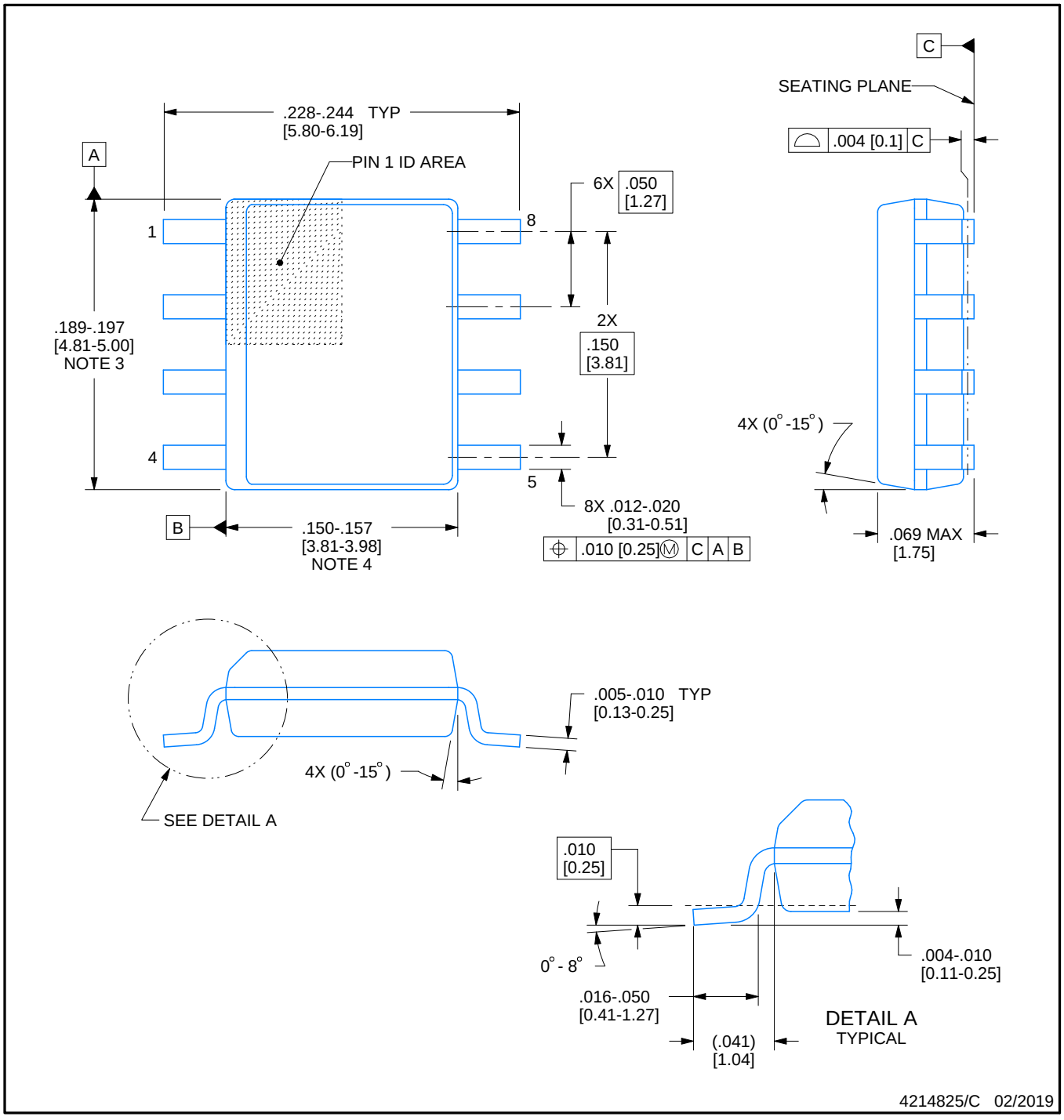


# PACKAGE OUTLINE

## D0008A

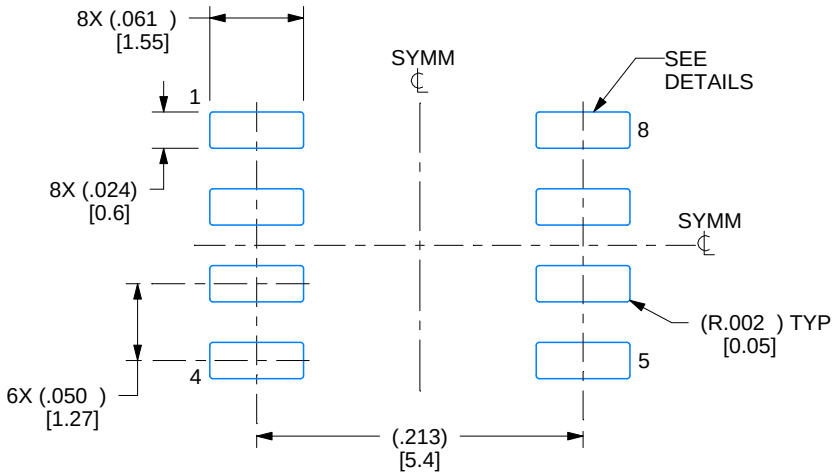
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

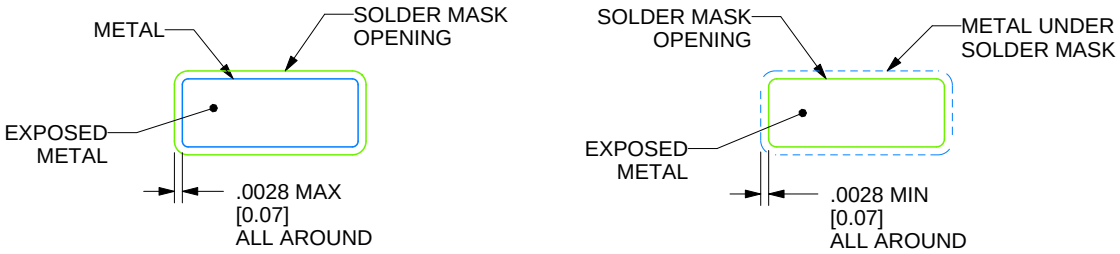



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

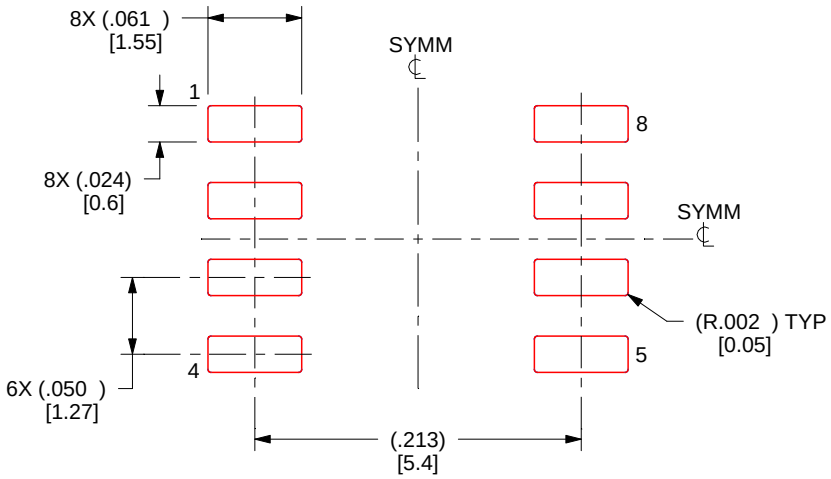
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

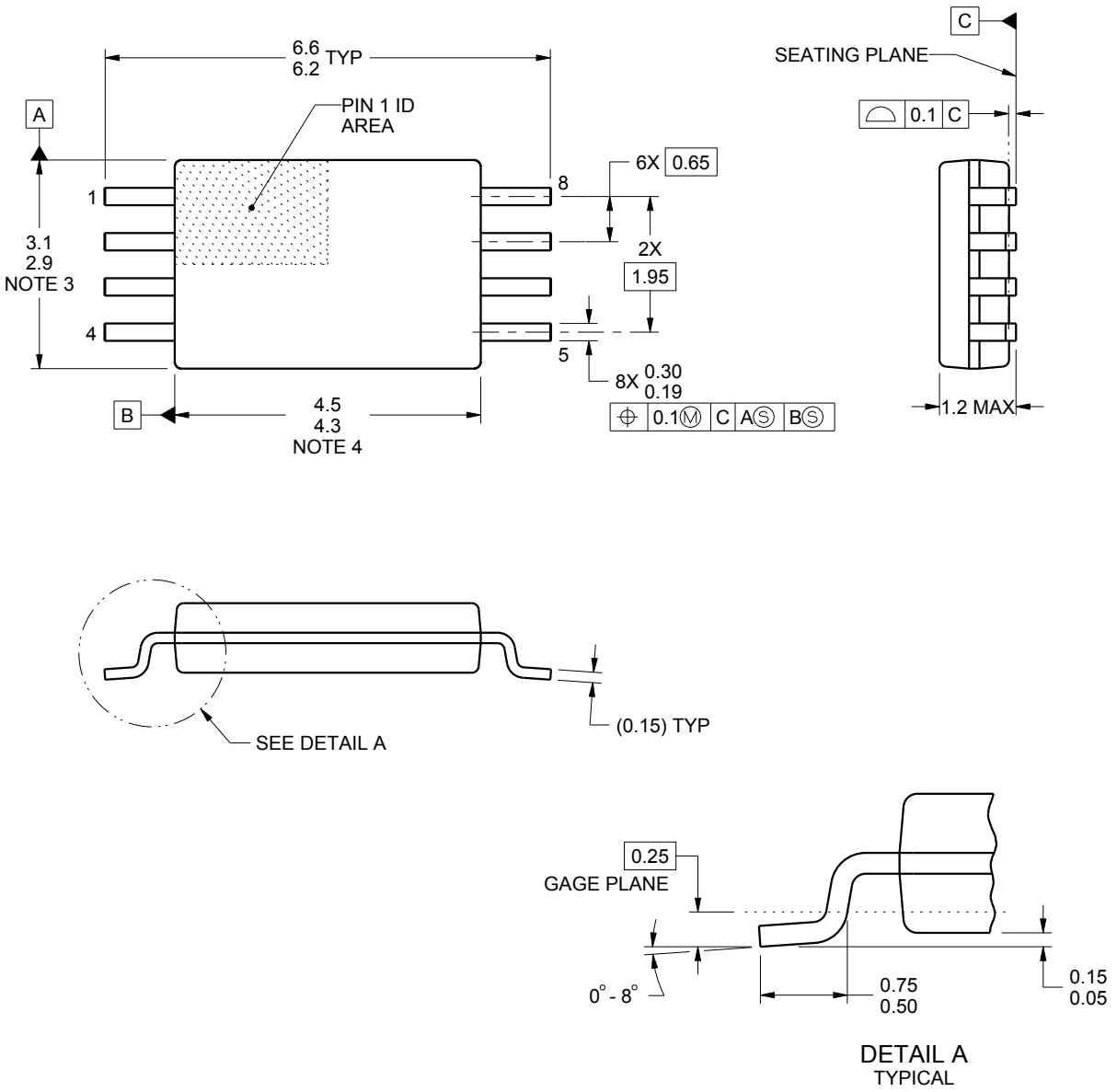
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## PW0008A

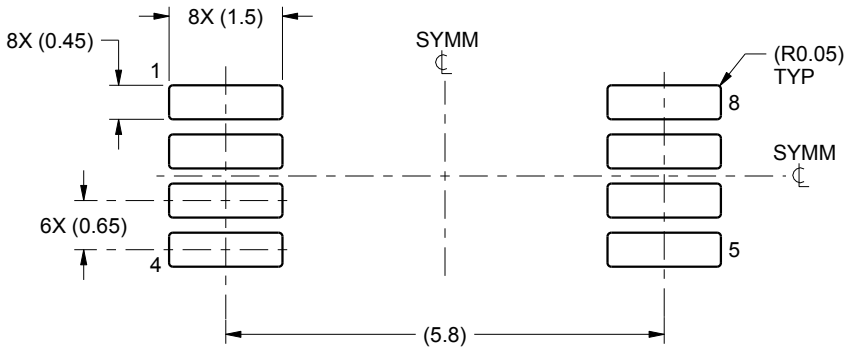
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

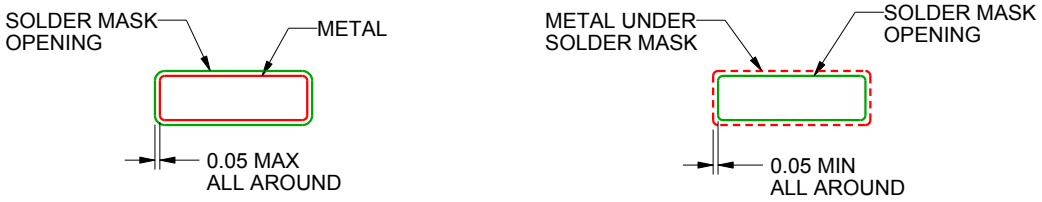



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.




LAND PATTERN EXAMPLE
SCALE:10X

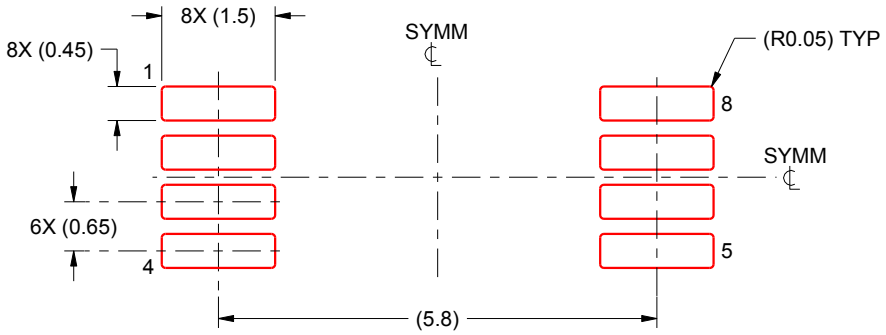



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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