Wide Bandwidth OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA) and BUFFER

OTA FEATURES

- **Wide Bandwidth (80MHz, Open-Loop, G = +5)**
- **High Slew Rate (900V/µs)**
- **High Transconductance (95mA/V)**
- **External I_Q-Control**

BUFFER FEATURES

- **Closed-Loop Buffer**
- **Wide Bandwidth (1600MHz, V_O = 1V_{PP})**
- **High Slew Rate (4000V/µs)**
- **60mA Output Current**

OPA860 FEATURES

- **Low Quiescent Current (11.2mA)**
- **Versatile Circuit Function**

APPLICATIONS

- **Baseline Restore Circuits**
- **Video/Broadcast Equipment**
- **Communications Equipment**
- **High-Speed Data Acquisition**
- **Wideband LED Driver**
- **AGC-Multiplier**
- **ns-Pulse Integrator**
- **Control Loop Amplifier**
- **OPA660 Upgrade**

DESCRIPTION

The OPA860 is a versatile monolithic component designed for wide-bandwidth systems, including high performance video, RF and IF circuitry. It includes a wideband, bipolar operational transconductance amplifier (OTA), and voltage buffer amplifier.

The OTA or voltage-controlled current source can be viewed as an *ideal transistor*. Like a transistor, it has three terminals—a high impedance input (base), a low-impedance input/output (emitter), and the current output (collector). The OTA, however, is self-biased and bipolar. The output collector current is zero for a zero base-emitter voltage. AC inputs centered about zero produce an output current, which is bipolar and centered about zero. The transconductance of the OTA can be adjusted with an external resistor, allowing bandwidth, quiescent current, and gain trade-offs to be optimized.

Also included in the OPA860 is an uncommited closed-loop, unity-gain buffer. This provides 1600MHz bandwidth and 4000V/µs slew rate.

Used as a basic building block, the OPA860 simplifies the design of AGC amplifiers, LED driver circuits for fiber optic transmission, integrators for fast pulses, fast control loop amplifiers and control amplifiers for capacitive sensors and active filters. The OPA860 is available in an SO-8 surface-mount package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA860	SO-8	D	–45°C to +85°C	OPA860	OPA860ID	Rails, 75
					OPA860IDR	Tape and Reel, 2500

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

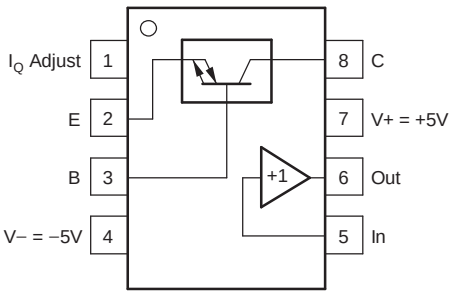
ABSOLUTE MAXIMUM RATINGS(1)

Power Supply	±6.5V_{DC}
Internal Power Dissipation	See Thermal Information
Differential Input Voltage	±1.2V
Input Common-Mode Voltage Range	±V_S
Storage Temperature Range: D	–65°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature (T_J)	+150°C
ESD Rating:	
Human Body Model (HBM)(2)	1500V
Charge Device Model (CDM)	1000V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress Ratings only, and functional operations of the device at these and any other conditions beyond those specified is not supported.
(2) Pin 2 > 500V HBM.

PIN CONFIGURATION

Top View **SO**



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ELECTRICAL CHARACTERISTICS: V_S = ±5V

R_L = 500Ω and R_{ADJ} = 250Ω, unless otherwise noted.

PARAMETER	CONDITIONS	OPA860ID				UNITS	MIN/ MAX	TEST LEVEL(1)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(2)	0°C to 70°C(3)	–40°C to +85°C(3)			
Closed Loop OTA + BUFFER (see Figure 53)								
AC PERFORMANCE	G = +2, See Figure 53							
Bandwidth	V_O = 200mV$_{PP}$	470	380	375	370	MHz	min	B
	V_O = 1V$_{PP}$	470				MHz	typ	C
	V_O = 5V$_{PP}$	350				MHz	typ	C
Bandwidth for 0.1dB Gain Flatness	V_O = 200mV$_{PP}$	42				MHz	typ	C
Slew Rate	V_O = 5V Step	3500	3000	2800	2700	V/µs	typ	C
Rise Time and Fall Time	V_O = 1V Step	0.7				ns	typ	C
Harmonic Distortion	G = +2, V_O = 2V$_{PP}$, 5MHz							
2nd-Harmonic	R_L = 100Ω	–54				dBc	typ	C
	R_L = 500Ω	–77				dBc	typ	C
3rd-Harmonic	R_L = 100Ω	–66				dBc	typ	C
	R_L = 500Ω	–79				dBc	typ	C
OTA - Open-Loop (see Figure 48)								
AC PERFORMANCE								
Bandwidth	G = +5, V_O = 200mV$_{PP}$, R_L = 500Ω	80	77	75	74	MHz	min	B
	G = +5, V_O = 1V$_{PP}$	80				MHz	typ	C
	G = +5, V_O = 5V$_{PP}$	80				MHz	typ	C
Slew Rate	G = +5, V_O = 5V Step	900	860	850	840	V/µs	min	B
Rise Time and Fall Time	V_O = 1V Step	4.4				ns	typ	C
Harmonic Distortion	G = +5, V_O = 2V$_{PP}$, 5MHz							
2nd-Harmonic	R_L = 500Ω	–68	–55	–54	–53	dB	max	B
3rd-Harmonic	R_L = 500Ω	–57	–52	–51	–49	dB	max	B
Base Input Voltage Noise	f > 100kHz	2.4	3.0	3.3	3.4	nV/√Hz	max	B
Base Input Current Noise	f > 100kHz	1.65	2.4	2.45	2.5	pA/√Hz	max	B
Emitter Input Current Noise	f > 100kHz	5.2	15.3	16.6	17.5	pA/√Hz	max	B
OTA DC PERFORMANCE(4) (see Figure 48)								
Min OTA Transconductance	V_O = ±10mV, R_C = 0Ω, R_E = 0Ω	95	**80**	77	75	mA/V	min	A
Max OTA Transconductance	V_O = ±10mV, R_C = 0Ω, R_E = 0Ω	95	**150**	155	160	mA/V	min	A
B-Input Offset Voltage	V_B = 0V, R_C = 0Ω, R_E = 100Ω	±3	**±12**	±15	±20	mV	max	A
Average B-Input Offset Voltage Drift	V_B = 0V, R_C = 0Ω, R_E = 100Ω	±3		±67	±120	µV/°C	max	B
B-Input Bias Current	V_B = 0V, R_C = 0Ω, R_E = 100Ω	±1	**±5**	±6	±6.6	µA	max	A
Average B-Input Bias Current Drift	V_B = 0V, R_C = 0Ω, R_E = 100Ω			±20	±25	nA/°C	max	B
E-Input Bias Current	V_B = 0V, V_C = 0V	±30	**±100**	±125	±140	µA	max	A
Average E-Input Bias Current Drift	V_B = 0V, V_C = 0V			±500	±600	nA/°C	max	B
C-Output Bias Current	V_B = 0V, V_C = 0V	±5	**±18**	±30	±38	µA	max	A
Average C-Output Bias Current Drift	V_B = 0V, V_C = 0V			±250	±300	nA/°C	max	B
OTA INPUT (see Figure 48)								
B-Input Voltage Range		±4.2	±3.7	±3.6	±3.6	V	min	B
B-Input Impedance		455 || 2.1				kΩ || pF	typ	C
Min E-Input Input Resistance		10.5	12.5	13.0	13.3	Ω	min	B
Max E-Input Input Resistance		10.5	6.7	6.5	6.3	Ω	max	B

(1) Test levels: (A) 100% tested at +25°C. Over temperature limits set by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(2) Junction temperature = ambient for +25°C specifications.
(3) Junction temperature = ambient at low temperature limit; junction temperature = ambient + 8°C at high temperature limit for over temperature specifications.
(4) Current is considered positive out of node. V_{CM} is the input common-mode voltage.

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ELECTRICAL CHARACTERISTICS: V_S = ±5V (continued)

R_L = 500Ω and R_{ADJ} = 250Ω, unless otherwise noted.

PARAMETER	CONDITIONS	OPA860ID TYP +25°C	OPA860ID MIN/MAX OVER TEMPERATURE +25°C[2]	0°C to 70°C[3]	–40°C to +85°C[3]	UNITS	MIN/ MAX	TEST LEVEL[1]
OTA OUTPUT								
E-Output Voltage Compliance	I_E = ±1mA	±4.2	**±3.7**	±3.6	±3.6	V	min	A
E-Output Current, Sinking/Sourcing	V_E = 0	±15	**±10**	±9	±9	mA	min	A
C-Output Voltage Compliance	I_C = ±1mA	±4.7	**±4.0**	±3.9	±3.9	V	min	A
C-Output Current, Sinking/Sourcing	V_C = 0	±15	**±10**	±9	±9	mA	min	A
C-Output Impedance		54 || 2				kΩ || pF	typ	C
BUFFER (see Figure 45)								
AC PERFORMANCE								
Bandwidth	V_O = 200mV$_{PP}$	1200	750	720	700	MHz	min	B
	V_O = 1V$_{PP}$	1600				MHz	typ	C
	V_O = 5V$_{PP}$	1000				MHz	typ	C
Slew Rate	V_O = 5V Step	4000	3500	3200	3000	V/µs	min	B
Rise Time and Fall Time	V_O = 1V Step	0.4				ns	typ	C
Settling Time to 0.05%	V_O = 1V Step	6				ns	typ	C
Harmonic Distortion	V_O = 2V$_{PP}$, 5MHz							
2nd-Harmonic	R_L = 100Ω	–52	–47	–46	–44	dBc	max	B
	R_L ≥ 500Ω	–72	–65	–63	–61	dBc	max	B
3rd-Harmonic	R_L = 100Ω	–67	–63	–63	–62	dBc	max	B
	R_L ≥ 500Ω	–96	–86	–85	–83	dBc	max	B
Input Voltage Noise	f > 100kHz	4.8	5.1	5.6	6.0	nV/√Hz	max	B
Input Current Noise	f > 100kHz	2.1	2.6	2.7	2.8	pA/√Hz	max	B
Differential Gain	NTSC, PAL	0.06				%	typ	C
Differential Phase	NTSC, PAL	0.02				Degrees	typ	C
BUFFER DC PERFORMANCE								
Gain	R_L = 500Ω	1	**0.98**	0.98	0.98	V/V	min	A
	R_L = 500Ω	1	**1**	1	1	V/V	max	A
Input Offset Voltage		±16	**±30**	±36	±38	mV	max	A
Average Input Offset Voltage Drift				±125	±125	µV/°C	max	B
Input Bias Current		±3	**±7**	±8	±8.5	µA	max	A
Average Input Bias Current Drift				±20	±20	nA/°C	max	B
BUFFER INPUT								
Input Impedance		1.0 || 2.1				MΩ || pF	typ	C
BUFFER OUTPUT								
Output Voltage Swing	R_L = 500Ω	±4.0	**±3.8**	±3.8	±3.8	V	min	A
Output Current	V_O = 0	±60	**±50**	±49	±48	mA	min	A
Closed-Loop Output Impedance	f ≤ 100kHz	1.4				Ω	typ	C
POWER SUPPLY (OTA + BUFFER)								
Specified Operating Voltage		±5				V	typ	C
Maximum Operating Voltage			**±6.5**	±6.5	±6.5	V	max	A
Minimum Operating Voltage			**±2.5**	±2.5	±2.5	V	min	B
Maximum Quiescent Current	R_{ADJ} = 250Ω	11.2	**12**	13.5	14.5	mA	max	A
Minimum Quiescent Current	R_{ADJ} = 250Ω	11.2	**10.5**	9.5	7.9	mA	min	A
OTA Power-Supply Rejection Ratio (+PSRR)	$\Delta I_C/\Delta V_S$	±20	**±50**	±60	±65	µA/V	max	A
Buffer Power-Supply Rejection Ratio (–PSRR)	$\Delta V_O/\Delta V_S$	54	**48**	46	45	dB	min	A
THERMAL CHARACTERISTICS								
Specification: ID		–40 to +85				°C	typ	C
Thermal Resistance θ_{JA}								
D SO-8	Junction-to-Ambient	125				°C/W	typ	C

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TYPICAL CHARACTERISTICS: V_S = ±5V

At T_A = +25°C, I_Q = 11.2mA, and R_L = 500Ω, unless otherwise noted. (See Figure 53.)

OTA + BUF Performance

SMALL-SIGNAL FREQUENCY RESPONSE

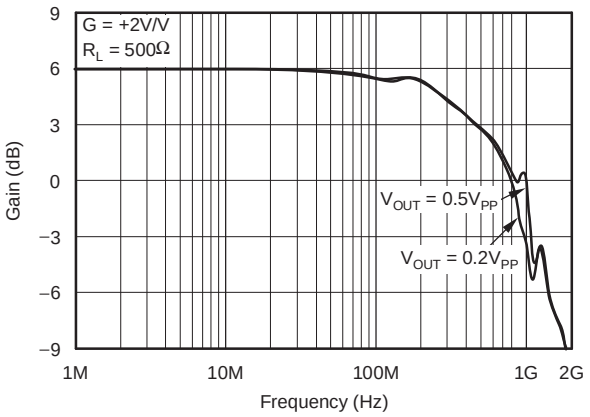


Figure 1.

LARGE-SIGNAL FREQUENCY RESPONSE

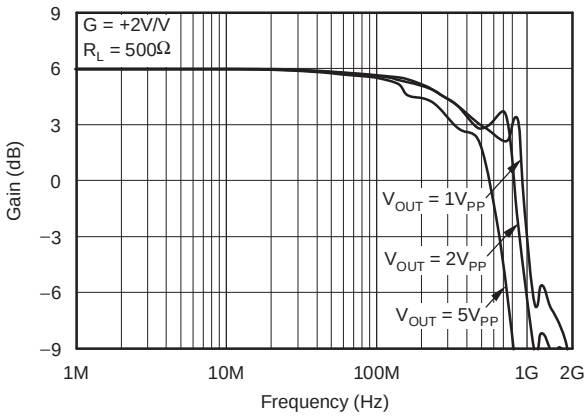


Figure 2.

SMALL-SIGNAL FREQUENCY RESPONSE vs QUIESCENT CURRENT

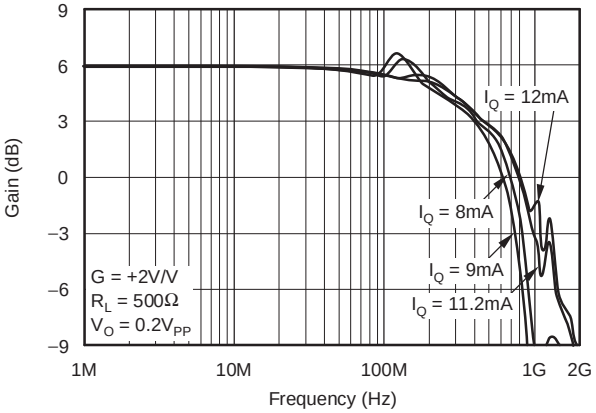


Figure 3.

GAIN FLATNESS vs QUIESCENT CURRENT

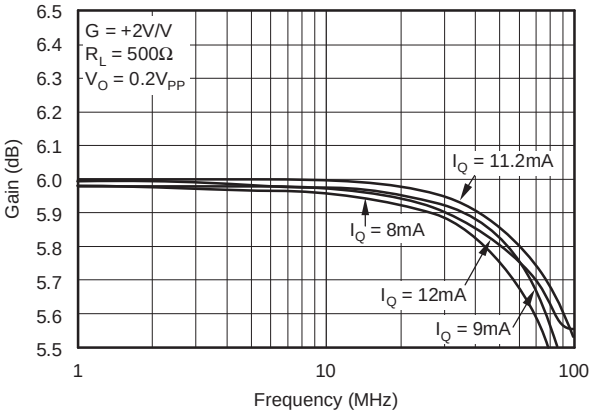


Figure 4.

SMALL-SIGNAL PULSE RESPONSE

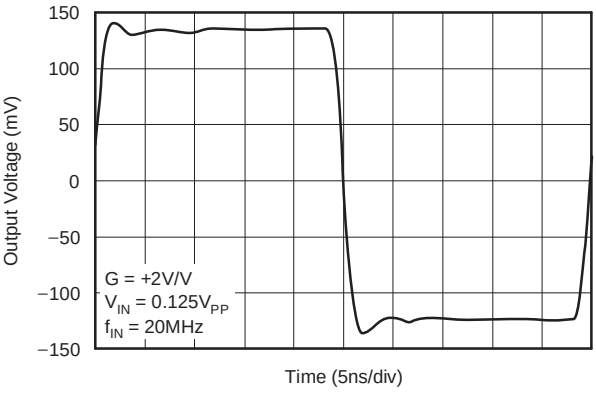


Figure 5.

LARGE-SIGNAL PULSE RESPONSE

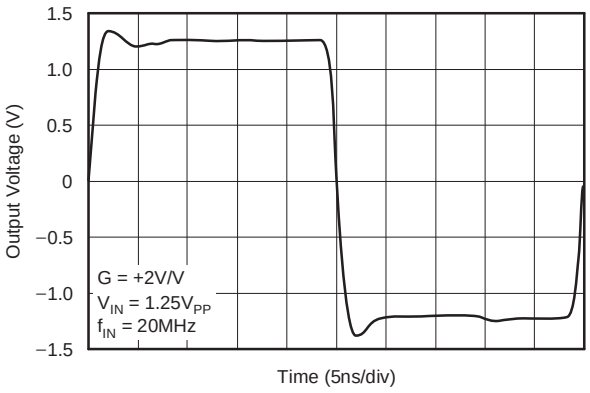


Figure 6.

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TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, I_Q = 11.2mA, and R_L = 500Ω, unless otherwise noted. (See Figure 53.)

HARMONIC DISTORTION vs FREQUENCY

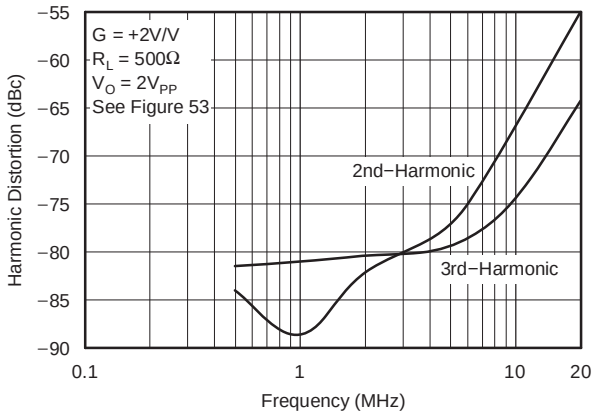


Figure 7.

HARMONIC DISTORTION vs OUTPUT RESISTANCE

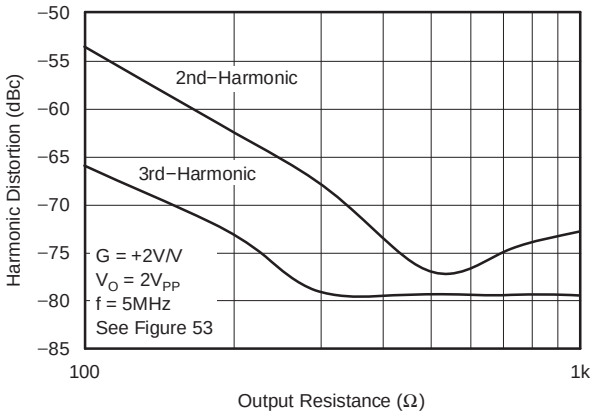


Figure 8.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

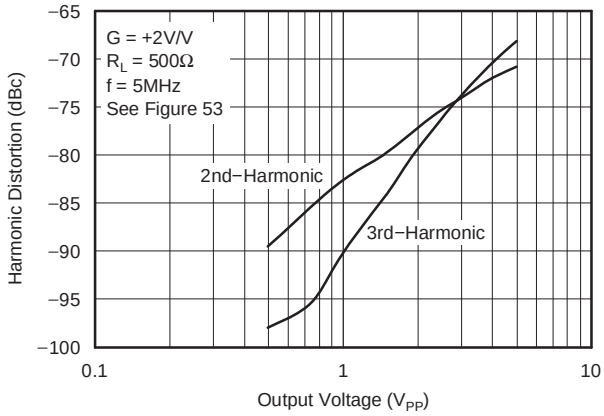


Figure 9.

HARMONIC DISTORTION vs SUPPLY VOLTAGE

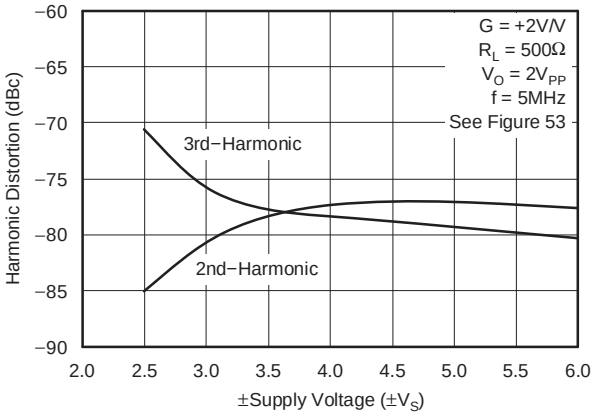


Figure 10.

HARMONIC DISTORTION vs QUIESCENT CURRENT

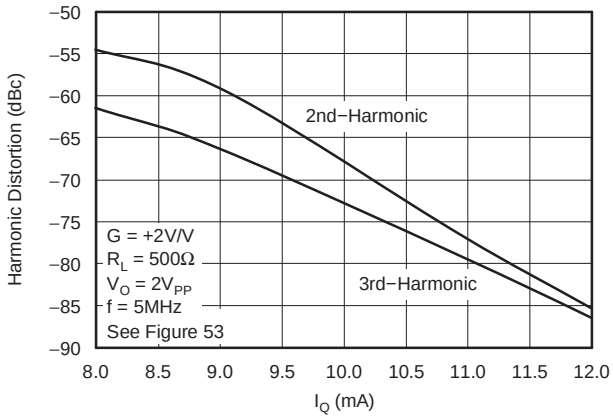


Figure 11.

QUIESCENT CURRENT vs R_{ADJ}

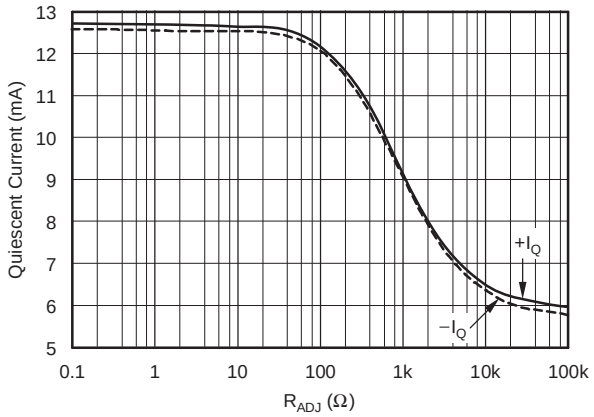


Figure 12.

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TYPICAL CHARACTERISTICS: V_S = ±5V

At T_A = +25°C, I_Q = 11.2mA, and R_L = 500Ω, unless otherwise noted.

OTA Performance

OTA TRANSCONDUCTANCE vs FREQUENCY

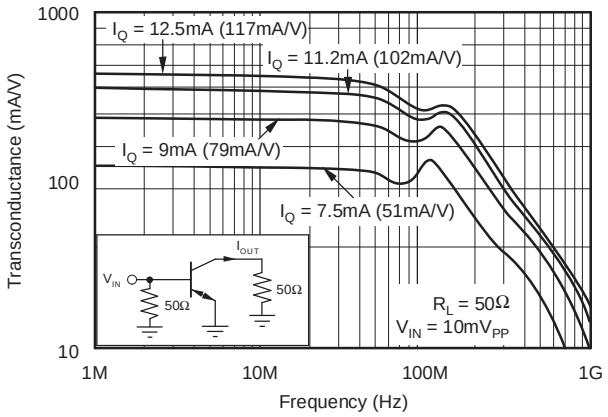


Figure 13.

OTA TRANSCONDUCTANCE vs QUIESCENT CURRENT

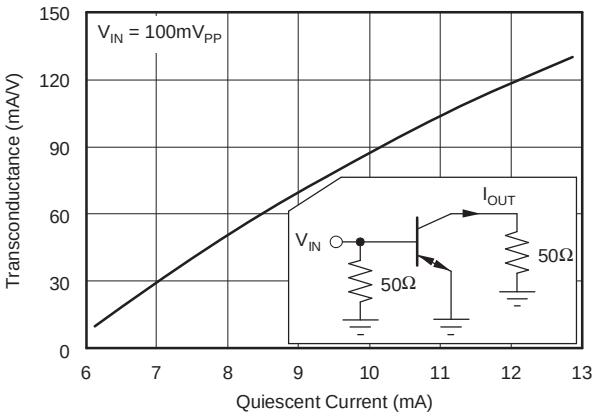


Figure 14.

OTA TRANSCONDUCTANCE vs INPUT VOLTAGE

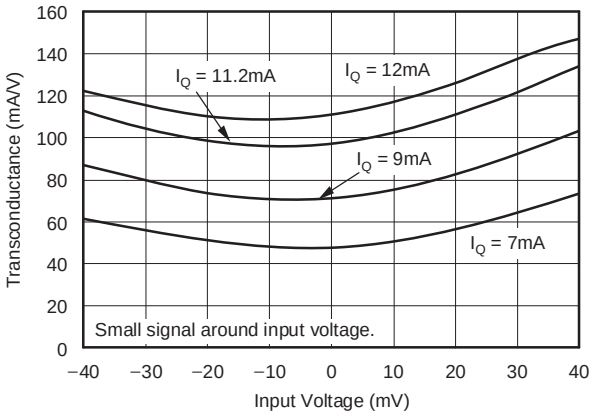


Figure 15.

OTA TRANSFER CHARACTERISTICS

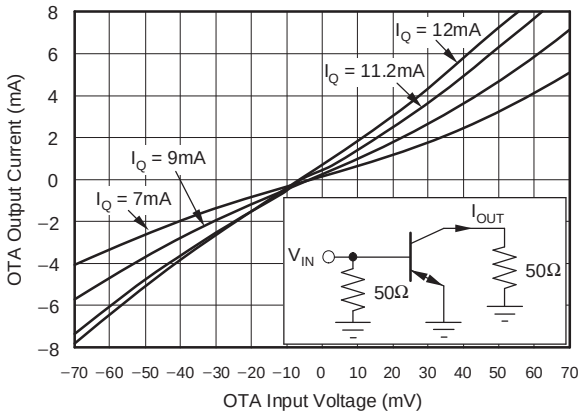


Figure 16.

OTA SMALL-SIGNAL PULSE RESPONSE

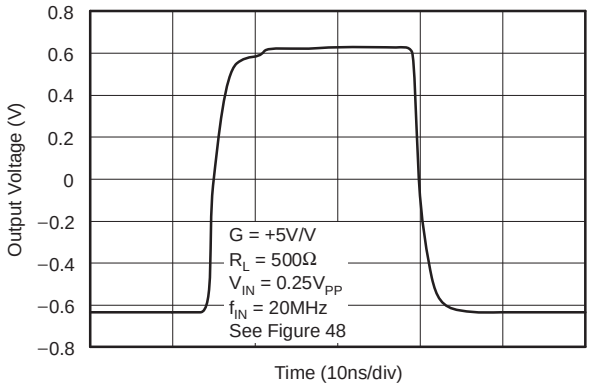


Figure 17.

OTA LARGE-SIGNAL PULSE RESPONSE

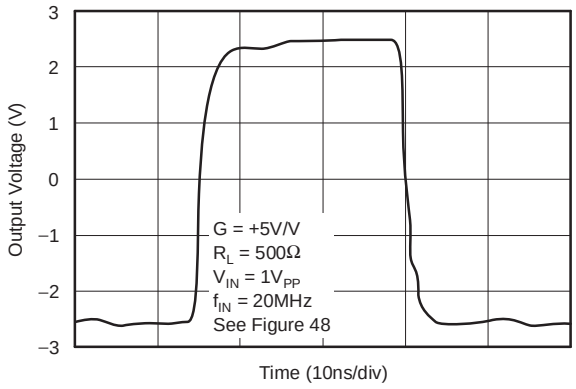


Figure 18.

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TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, I_Q = 11.2mA, and R_L = 500Ω, unless otherwise noted.

B-INPUT RESISTANCE vs QUIESCENT CURRENT

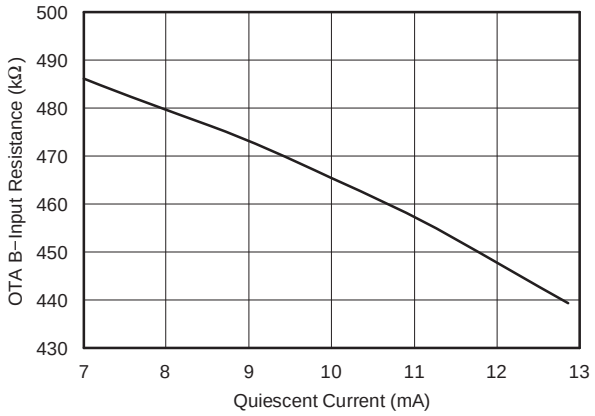


Figure 19.

C-OUTPUT RESISTANCE vs QUIESCENT CURRENT

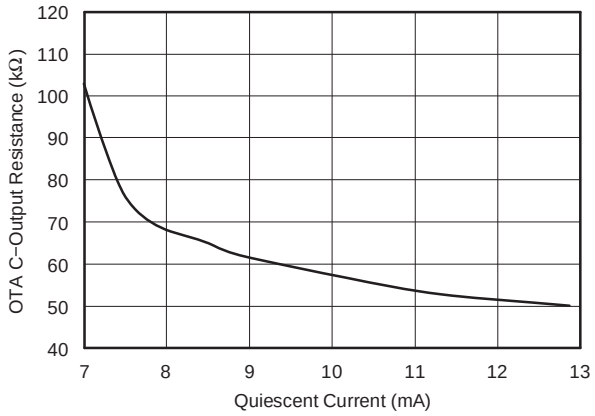


Figure 20.

E-OUTPUT RESISTANCE vs QUIESCENT CURRENT

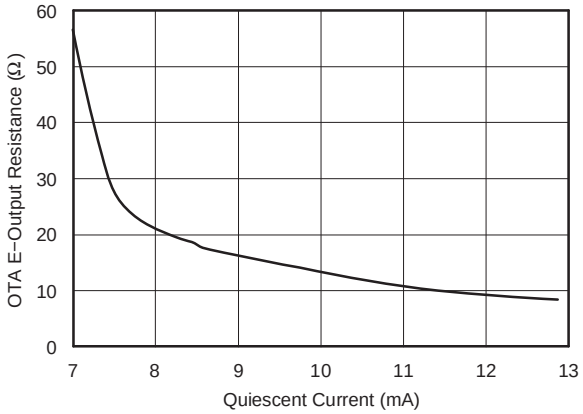


Figure 21.

INPUT VOLTAGE AND CURRENT NOISE DENSITY

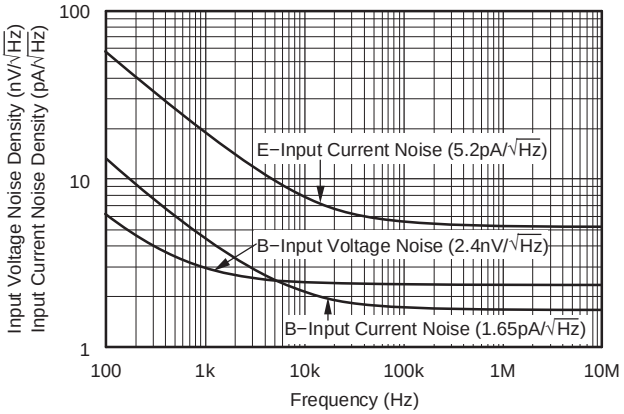


Figure 22.

1MHz OTA VOLTAGE AND CURRENT NOISE DENSITY vs QUIESCENT CURRENT ADJUST RESISTOR

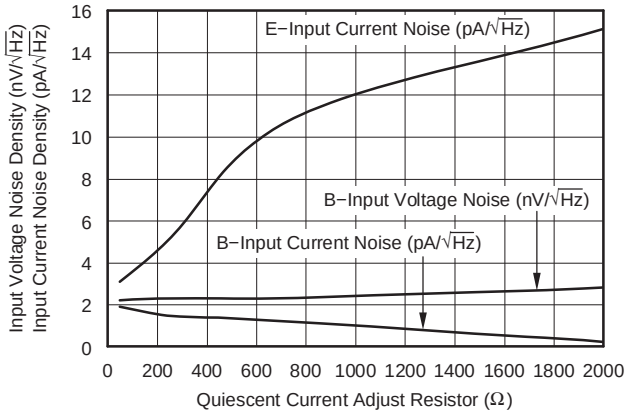


Figure 23.

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TYPICAL CHARACTERISTICS: V_S = ±5V

At T_A = +25°C, I_Q = 11.2mA, and R_L = 500Ω, unless otherwise noted.

BUF Performance

BUFFER BANDWIDTH vs OUTPUT VOLTAGE

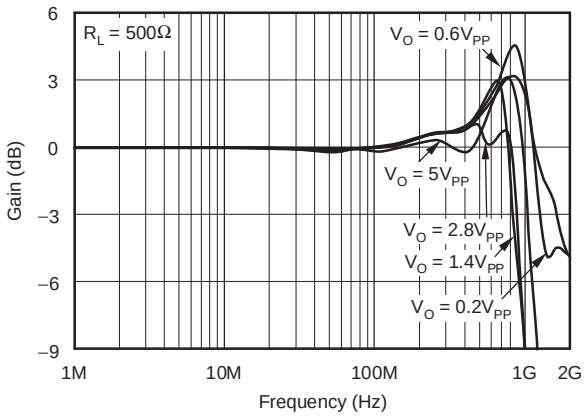


Figure 24.

BUFFER BANDWIDTH vs LOAD RESISTANCE

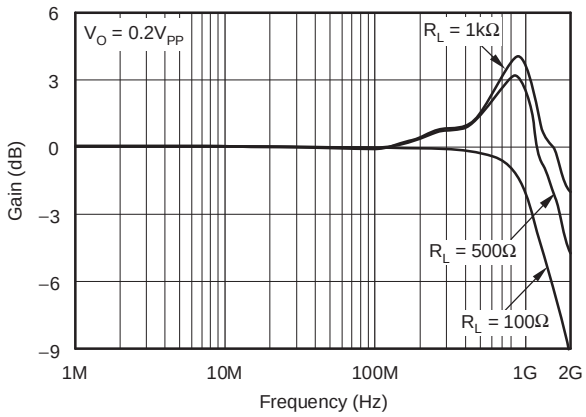


Figure 25.

BUFFER GAIN FLATNESS

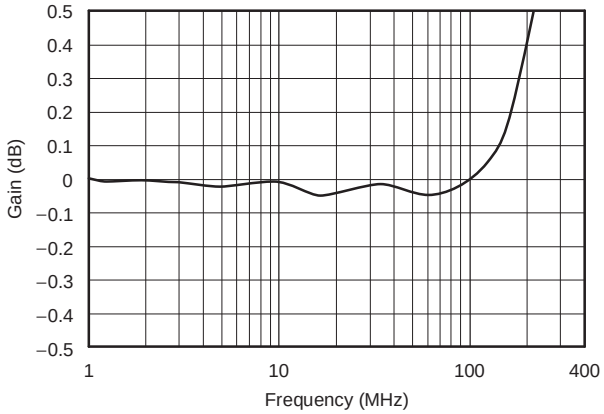


Figure 26.

BUFFER SMALL-SIGNAL PULSE RESPONSE

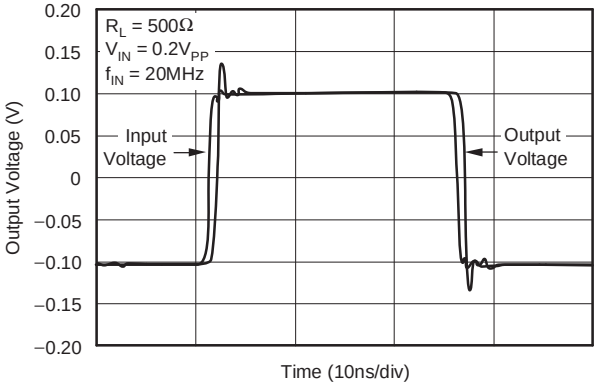


Figure 27.

BUFFER LARGE-SIGNAL PULSE RESPONSE

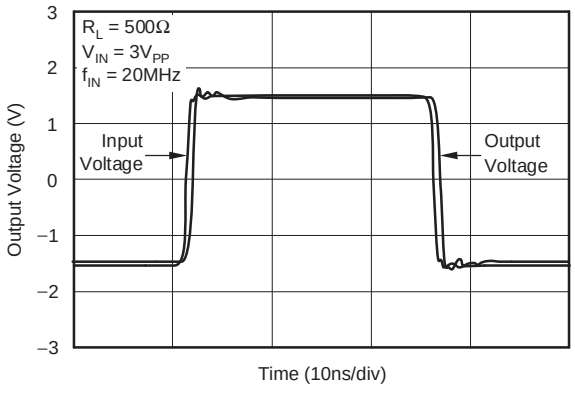


Figure 28.

HARMONIC DISTORTION vs FREQUENCY

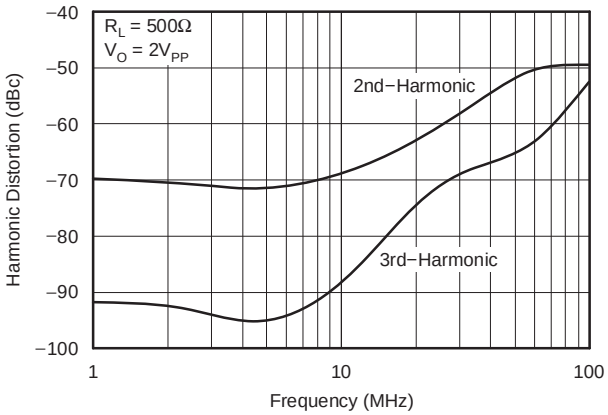


Figure 29.

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TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, I_Q = 11.2mA, and R_L = 500Ω, unless otherwise noted.

5MHz HARMONIC DISTORTION vs LOAD RESISTANCE

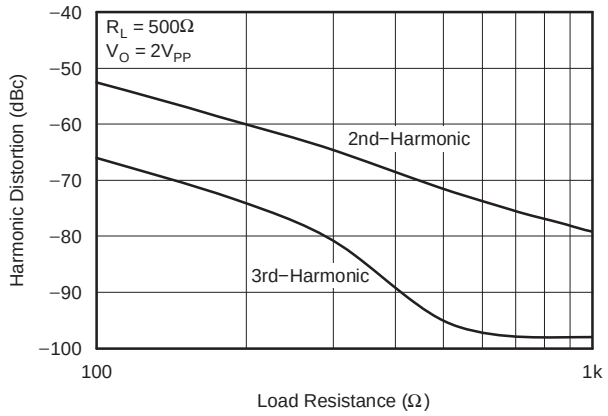


Figure 30.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

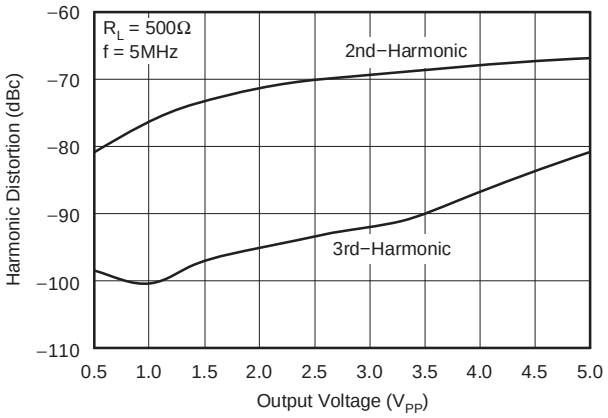


Figure 31.

5MHz HARMONIC DISTORTION vs SUPPLY VOLTAGE

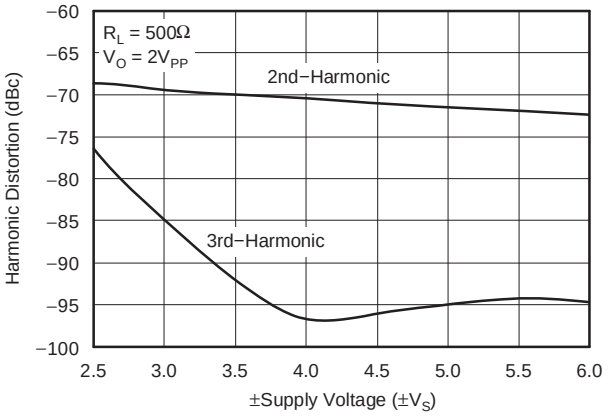


Figure 32.

BUFFER TRANSFER FUNCTION

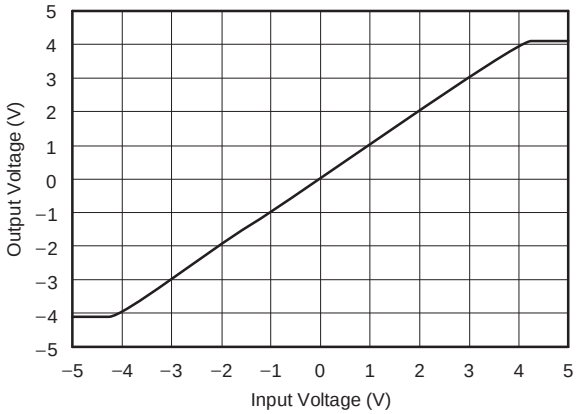


Figure 33.

INPUT VOLTAGE AND CURRENT NOISE DENSITY

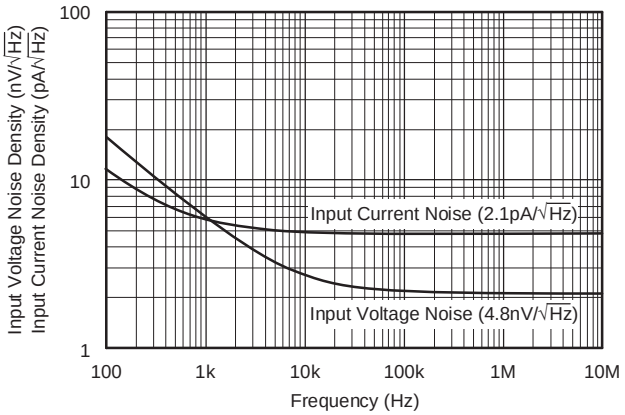


Figure 34.

BUFFER OUTPUT IMPEDANCE

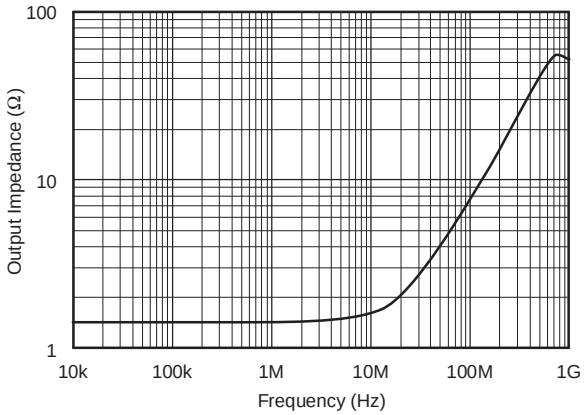


Figure 35.

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TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, I_Q = 11.2mA, and R_L = 500Ω, unless otherwise noted.

BUFFER GROUP DELAY TIME vs FREQUENCY

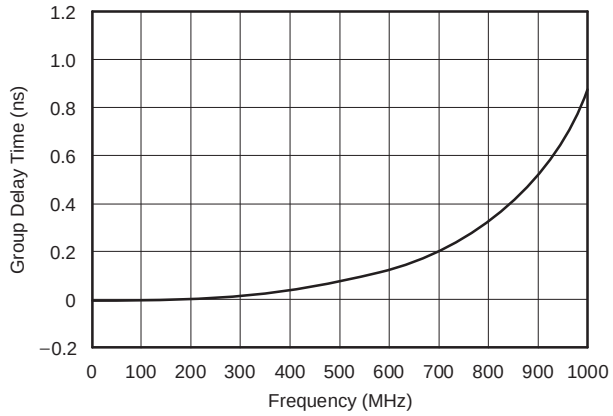


Figure 36.

BUFFER OUTPUT VOLTAGE AND CURRENT LIMITATIONS

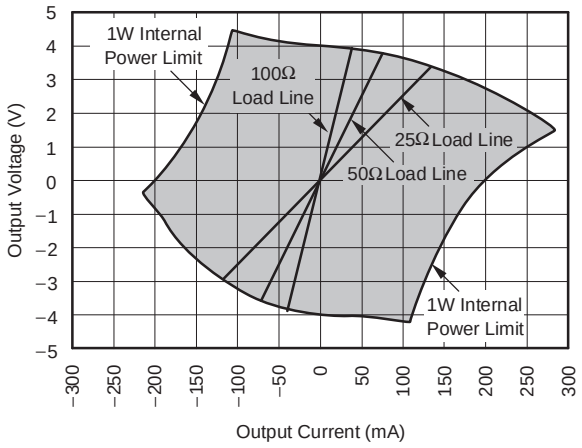


Figure 37.

QUIESCENT CURRENT vs TEMPERATURE

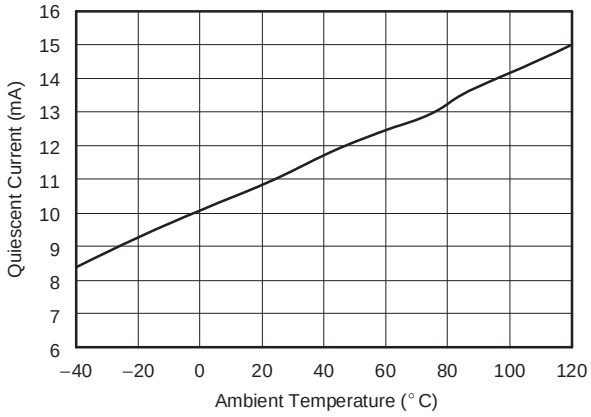


Figure 38.

POWER-SUPPLY REJECTION RATIO vs FREQUENCY

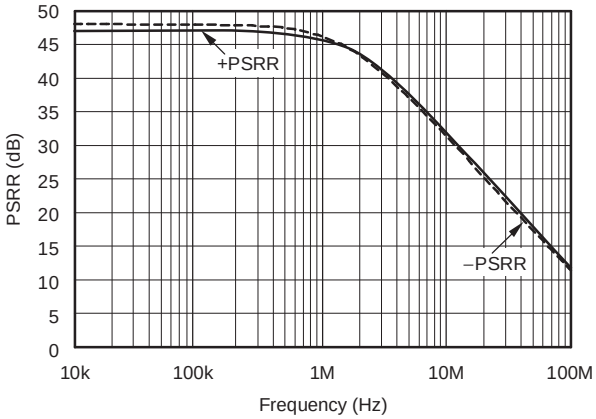


Figure 39.

VOLTAGE RANGE vs TEMPERATURE

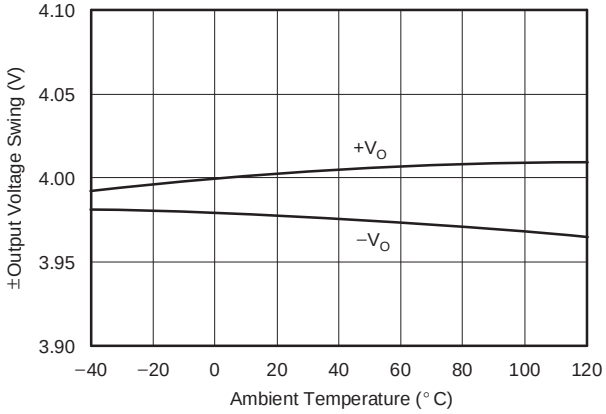


Figure 40.

OUTPUT CURRENT vs TEMPERATURE

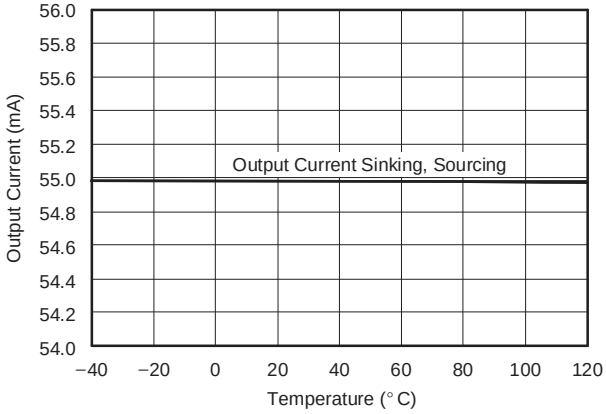


Figure 41.

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TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, I_Q = 11.2mA, and R_L = 500Ω, unless otherwise noted.

DC DRIFT vs TEMPERATURE

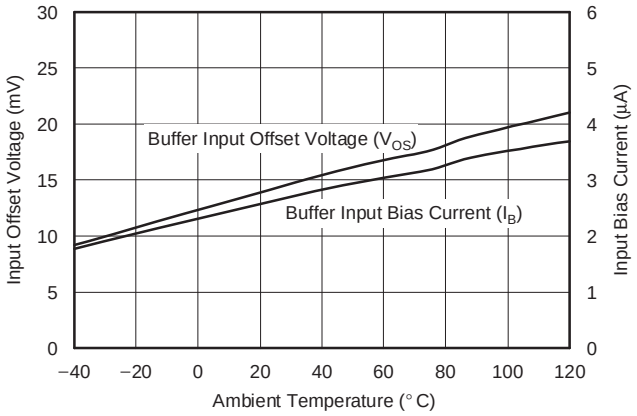


Figure 42.

C-OUTPUT BIAS CURRENT vs TEMPERATURE

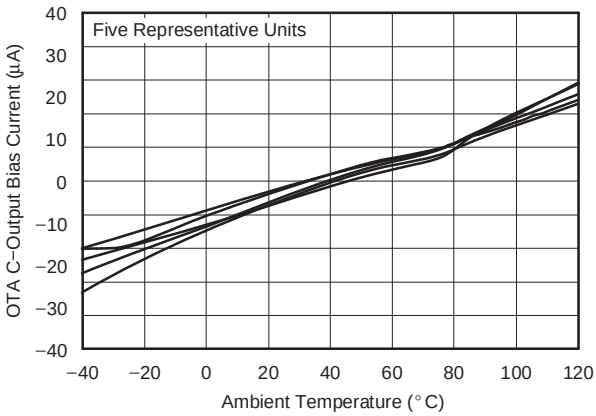


Figure 43.

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APPLICATION INFORMATION

The OPA860 combines a high-performance buffer with a transconductance section. This transconductance section is discussed in the *OTA (Operational Transconductance Amplifier)* section of this data sheet. Over the years and depending on the writer, the OTA section of an op amp has been referred to as a Diamond Transistor, Voltage-Controlled Current source, Transconductor, Macro Transistor, or positive second-generation current conveyor (CCII+). Corresponding symbols for these terms are shown in Figure 44.

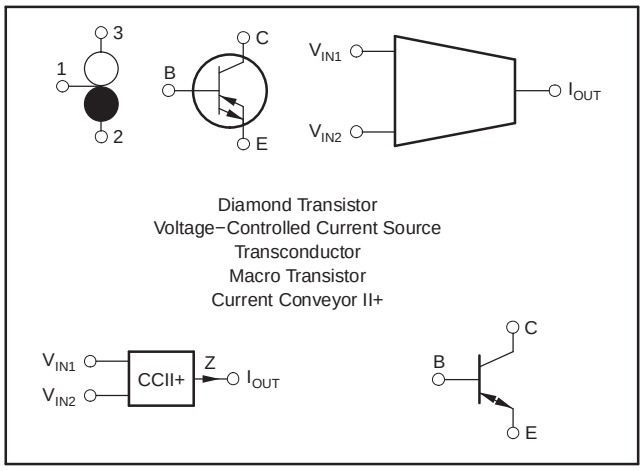


Figure 44. Symbols and Terms

Regardless of its depiction, the OTA section has a high-input impedance (B input), a low-input/output impedance (E input), and a high impedance current source output (C output).

BUFFER SECTION—AN OVERVIEW

The buffer section of the OPA860 is an 1600MHz, 4000V/µs closed-loop buffer that can be used as a building block for AGC amplifiers, LED driver circuit, integrator for fast pulse, fast control loop amplifiers, and control amplifiers for capacitive sensors and active filters. The Buffer section does not share the bias circuit of the OTA section; thus, it is not affected by changes in the I_Q adjust resistor (R_{ADJ}).

TRANSCONDUCTANCE (OTA) SECTION—AN OVERVIEW

The symbol for the OTA section is similar to a transistor (see Figure 44). Applications circuits for the OTA look and operate much like transistor circuits—the transistor is also a voltage-controlled current source. Not only does this characteristic simplify the understanding of application circuits, it aids the circuit optimization process as well. Many of the same intuitive techniques used with transistor designs apply to OTA circuits. The three terminals of the OTA are labeled B, E, and C. This labeling calls attention to its similarity to a transistor, yet draws distinction for clarity. While the OTA is similar to a transistor, one essential difference is the sense of the C-output current: it flows out the C terminal for positive B-to-E input voltage and in the C terminal for negative B-to-E input voltage. The OTA offers many advantages over a discrete transistor. The OTA is self-biased, simplifying the design process and reducing component count. In addition, the OTA is far more linear than a transistor. Transconductance of the OTA is constant over a wide range of collector currents—this feature implies a fundamental improvement of linearity.

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BASIC CONNECTIONS

Figure 46 shows basic connections required for operation. These connections are not shown in subsequent circuit diagrams. Power-supply bypass capacitors should be located as close as possible to the device pins. Solid tantalum capacitors are generally best.

QUIESCENT CURRENT CONTROL PIN

The quiescent current of the transconductance portion of the OPA860 is set with a resistor, R_{ADJ}, connected from pin 1 to $-V_S$. It affects only the operating currents of OTA sections. The bias circuitry of the Buffer section is independent of the bias circuitry for the OTA section; therefore, the quiescent current cannot go below 5.8mA. The maximum quiescent current is 12.7mA. R_{ADJ} should be set between 50Ω and 1kΩ for optimal performance of the OTA section. This range corresponds to the 12.5mA quiescent current for R_{ADJ} = 50Ω, and 9mA for R_{ADJ} = 1kΩ. If the I_Q adjust pin is connected to the negative supply, the quiescent current will be set by the 250Ω internal resistor.

Reducing or increasing the quiescent current for the OTA section controls the bandwidth and AC behavior as well as the transconductance. With R_{ADJ} = 250Ω, this sets approximately 11.2mA total quiescent current at 25°C. It may be appropriate in some applications to trim this resistor to achieve the desired quiescent current or AC performance.

Applications circuits generally do not show the resistor R_Q, but it is required for proper operation.

With a fixed R_{ADJ} resistor, quiescent current increases with temperature (see Figure 43 in the *Typical Characteristics* section). This variation of current with temperature holds the transconductance, g_m, of the OTA relatively constant with temperature (another advantage over a transistor).

It is also possible to vary the quiescent current with a control signal. The control loop in Figure 45 shows 1/2 of a REF200 current source used to develop 100mV on R_1. The loop forces 125mV to appear on R_2. Total quiescent current of the OPA860 is approximately 37 × I_1, where I_1 is the current made to flow out of pin 1.

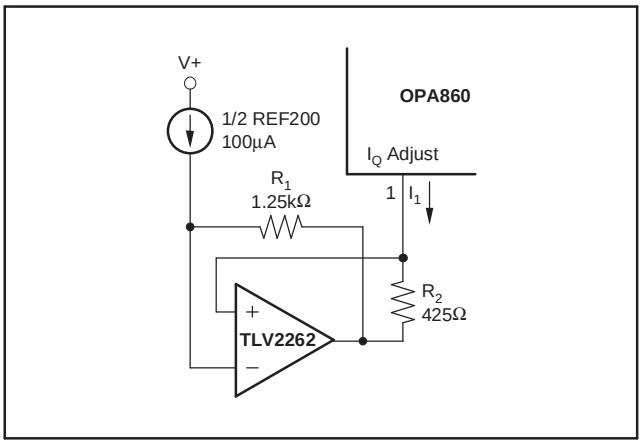


Figure 45. Optional Control Loop for Setting Quiescent Current

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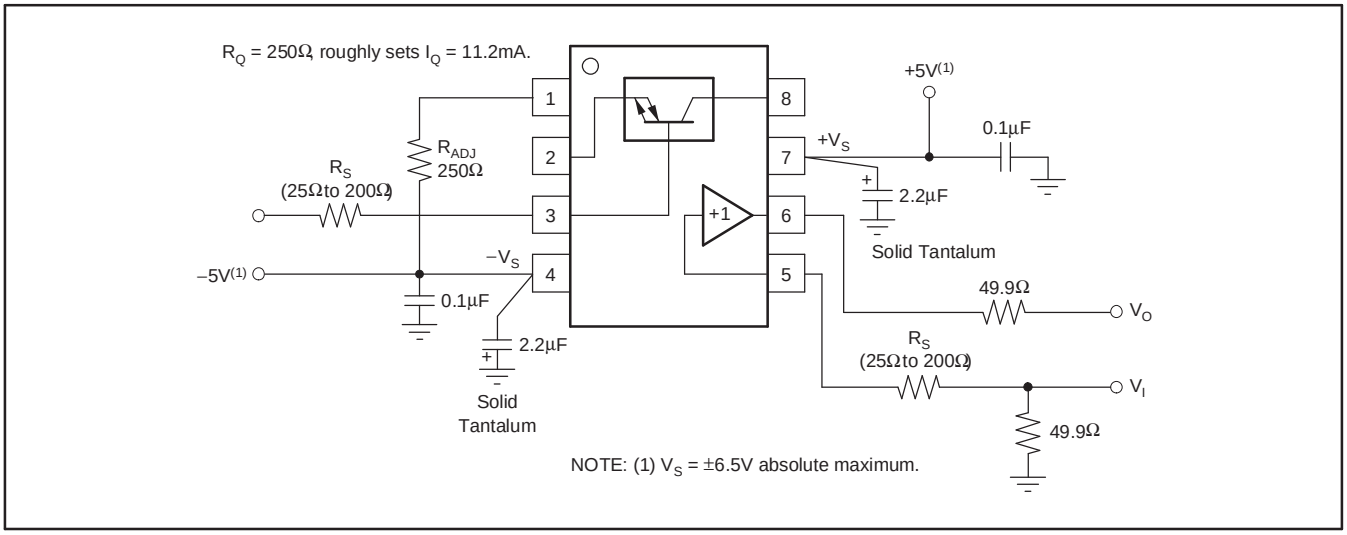


Figure 46. Basic Connections

With this control loop, quiescent current will be nearly constant with temperature. Since this differs from the temperature-dependent behavior of the internal current source, other temperature-dependent behavior may differ from that shown in the Typical Characteristics. The circuit of Figure 45 will control the I_Q of the OTA section of the OPA860 somewhat more accurately than with a fixed external resistor, R_Q. Otherwise, there is no fundamental advantage to using this more complex biasing circuitry. It does, however, demonstrate the possibility of signal-controlled quiescent current. This capability may suggest other possibilities such as AGC, dynamic control of AC behavior, or VCO.

BASIC APPLICATIONS CIRCUITS

Most applications circuits for the OTA section consist of a few basic types, which are best understood by analogy to a transistor. Used in voltage-mode, the OTA section can operate in three basic operating states—common emitter, common base, and common collector. In the current-mode, the OTA can be useful for analog computation such as current amplifier, current differentiator, current integrator, and current summer.

Common-E Amplifier or Forward Amplifier

Figure 47 compares the common-emitter configuration for a BJT with the common-E amplifier for the OTA section. There are several advantages in using the OTA section in place of a BJT in this configuration. Notably, the OTA does not require any biasing, and the transconductance gain remains constant over temperature. The output offset voltage is close to 0, compared with several volts for the common-emitter amplifier.

The gain is set in a similar manner as for the BJT equivalent with Equation 1:

$$G = \frac{R_L}{\frac{1}{g_m} + R_E} \quad (1)$$

Just as transistor circuits often use emitter degeneration, OTA circuits may also use degeneration. This option can be used to reduce the effects that offset voltage and offset current might otherwise have on the DC operating point of the OTA. The E-degeneration resistor may be bypassed with a large capacitor to maintain high AC gain. Other circumstances may suggest a smaller value capacitor used to extend or optimize high-frequency performance.

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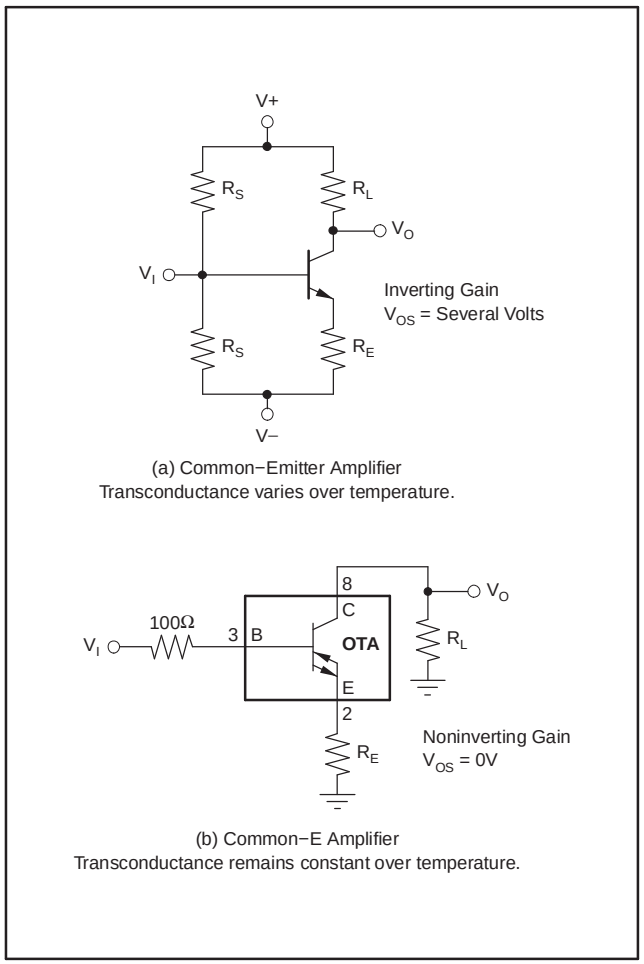


Figure 47. Common-Emitter vs Common-E Amplifier

The transconductance of the OTA with degeneration can be calculated by Equation 2:

$$g_{m_deg} = \frac{1}{\frac{1}{g_m} + R_E} \quad (2)$$

A positive voltage at the B-input, pin 3, causes a positive current to flow out of the C-input, pin 8. Figure 47b shows an amplifier connection of the OTA, the equivalent of a common-emitter transistor amplifier. Input and output can be ground-referenced without any biasing. The amplifier is noninverting because of the sense of the output current.

The forward amplifier shown in Figure 48 and Figure 49 corresponds to one of the basic circuits used to characterize the OPA860. Extended characterization of this topology appears in the *Typical Characteristics* section of this data sheet.

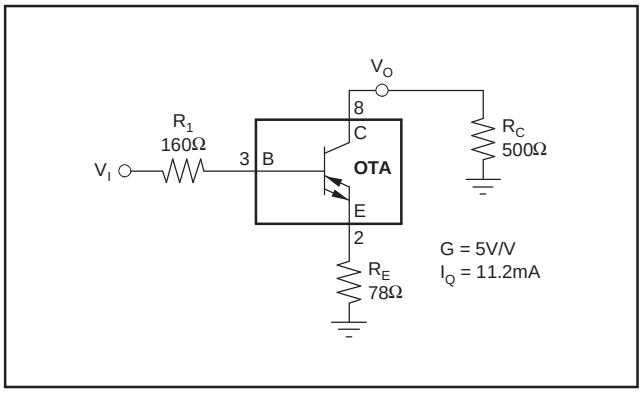


Figure 48. Forward Amplifier Configuration and Test Circuit

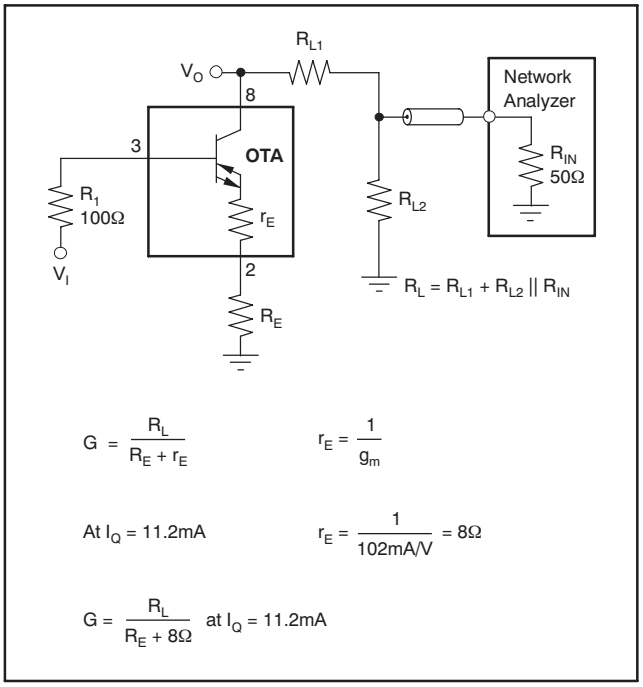


Figure 49. Forward Amplifier Design Equations

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Common-C Amplifier

Figure 50b shows the OTA connected as an E-follower—a voltage buffer. It is interesting to notice that the larger the R_E resistor, the closer to unity gain the buffer will be. If the OTA section is to be used as a buffer, use $R_E \geq 500\Omega$ for best results. For the OTA section used as a buffer, the gain is given by Equation 3:

$$G = \frac{1}{1 + \frac{1}{g_m \times R_E}} \approx 1 \quad (3)$$

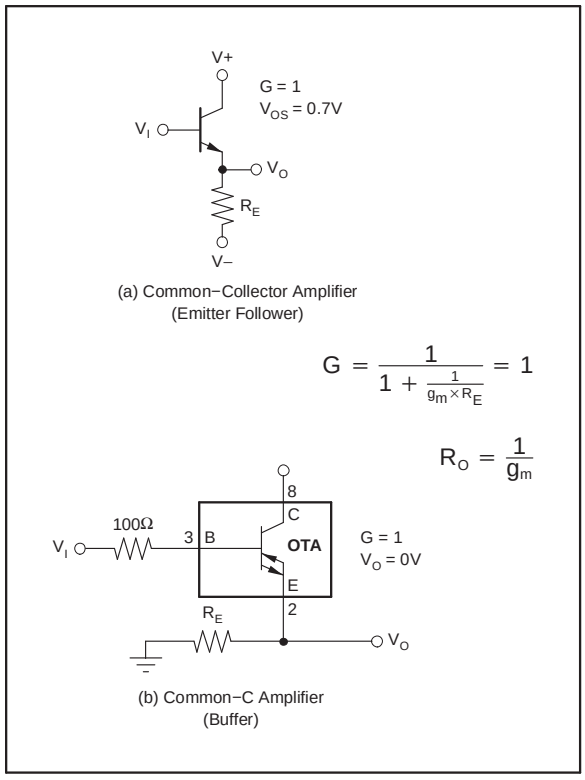


Figure 50. Common-Collector vs Common-C Amplifier

A low value resistor in series with the B OTA and buffer inputs is recommended. This resistor helps isolate trace parasitic from the inputs, reduces any tendency to oscillate, and controls frequency response peaking. Typical resistor values are from 25Ω to 200Ω.

Common-B Amplifier

Figure 51 shows the Common-B amplifier. This configuration produces an inverting gain and a low impedance input. Equation 4 shows the gain for this configuration.

$$G = \frac{R_L}{R_E + \frac{1}{g_m}} \approx -\frac{R_L}{R_E} \quad (4)$$

This low impedance can be converted to a high impedance by inserting the buffer amplifier in series.

Current-Mode Analog Computations

As mentioned earlier, the OTA section of the OPA860 can be used advantageously for analog computation. Among the application possibilities are functionality as a current amplifier, current differentiator, current integrator, current summer, and weighted current summer. Table 1 lists these different uses with the associated transfer functions.

These functions can easily be combined to form active filters. Some examples using these current-mode functions are shown later in this document.

OPA860 APPLICATIONS

The OPA860 is comprised of both the OTA section and the Buffer section. This applications information focuses more on using both sections together to form various useful amplifiers. A more thorough description of the OTA section in filter applications can be found in the OPA861 data sheet, available for download at www.ti.com.

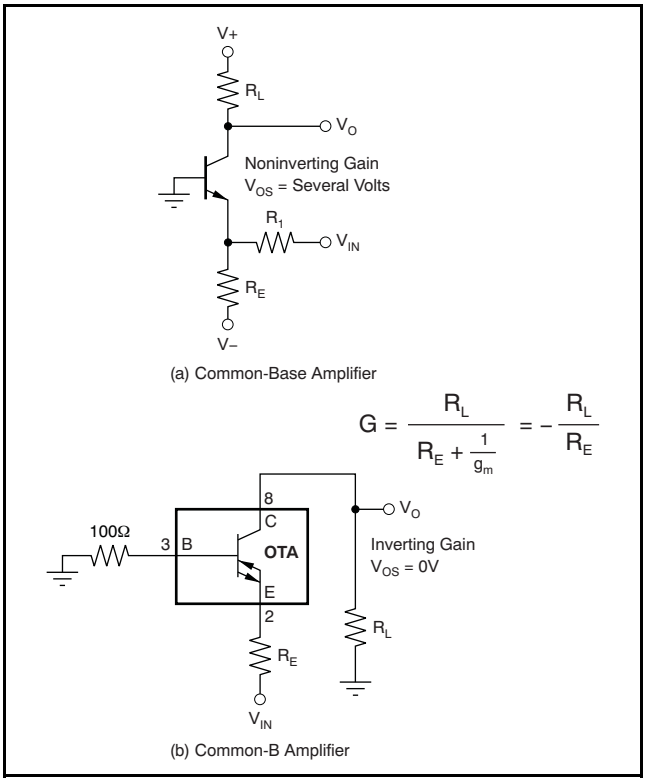


Figure 51. Common-Base Transistor vs Common-B OTA

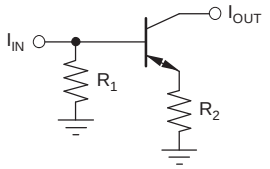
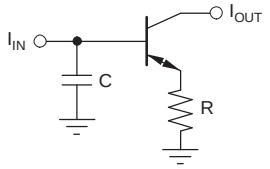
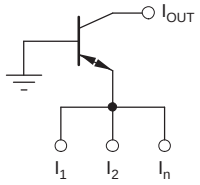
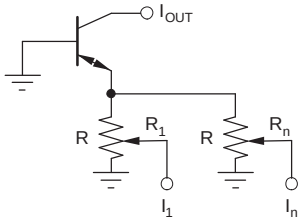
Direct Feedback Amplifier

The direct feedback amplifier (shown in Figure 53) topology has been used to characterize the OPA860. Extended characterization of this topology appears in the *Typical Characteristics* section of this data sheet. This topology is obtained by closing the loop between the C-output and the E-input of the common-E topology, and then buffered.

The gain for this topology is given by Equation 5:

$$G = \frac{\frac{R_3}{2} + R_5}{R_5 + \frac{1}{2 \times g_m}} \approx 1 + \frac{R_3}{2R_5} \quad (5)$$

Table 1. Current-Mode Analog Computation Using the OTA Section

FUNCTIONAL ELEMENT	TRANSFER FUNCTION	IMPLEMENTATION WITH THE OTA SECTION
Current Amplifier	$I_{OUT} = \frac{R_1}{R_2} \times I_{IN}$	
Current Integrator	$I_{OUT} = \frac{1}{C \times R \times \int I_{IN} dt}$	
Current Summer	$I_{OUT} = -\sum_{j=1}^{n} I_j$	
Weighted Current Summer	$I_{OUT} = -\sum_{j=1}^{n} I_j \times \frac{R_j}{R}$	

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Current-Feedback Amplifier

Building a current-feedback amplifier with the OPA860 is extremely simple. One advantage of building a current-feedback amplifier with the OPA860 instead of getting an off-the-shelf current-feedback amplifier is the control gained on the bandwidth though the use of external capacitors. Figure 54 shows a typical circuit for the OPA860 in a noninverting current-feedback amplifier configuration. Input and output parasitic capacitances are shown. R_1 is the output impedance of the C-output of the OTA section. C_1 is the output parasitic capacitance on the C-output pin of the OTA-section. C_2 is the input parasitic capacitance for the input of the Buffer section. As shown in Equation 6, the poles formed by R_1, C_1, R_2, and C_2 control the frequency response. The frequency response in this configuration is shown in Figure 52. Setting an external capacitor on the C-output to ground allows adjusting the bandwidth.

$$\frac{V_{OUT}}{V_{IN}} = \frac{\alpha\left(1 + \frac{R_F}{R_G}\right)}{1 + \left(1 + \frac{R_F}{R_G}\right) \times \frac{1}{g_m \times R_1} \times [1 + s(R_1C_1 + R_1C_2 + R_2C_2) + s^2R_1C_1C_2]} \quad (6)$$

Note that both peaking and bandwidth can be adjusted by changing the feedback resistance, R_F.

Control-Loop Amplifier

A new type of control loop amplifier for fast and precise control circuits can be designed with the OPA860. The circuit of Figure 55 shows a series connection of two voltage control current sources that have an integral (and at higher frequencies, a proportional) behavior versus frequency. The control loop amplifiers show an integrator behavior from DC to the frequency, represented by the RC time constant of the network from the C-output to GND. Above this frequency, they operate as an amp with constant gain. The series connection increases the overall gain to about 110dB and thus minimizes the control loop deviation. The differential configuration at the inputs enables one to apply the measured output signal and the reference voltage to two identical high-impedance inputs. The output buffer decouples the C-output of the second OTA in order to insure the AC performance and to drive subsequent output stages.

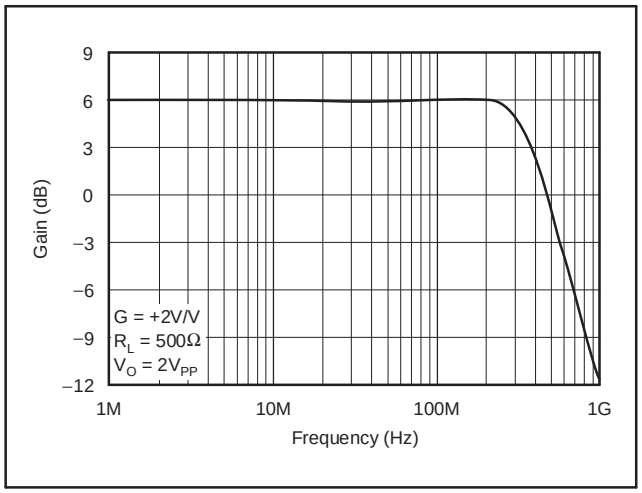


Figure 52. Current-Feedback Architecture Frequency Response

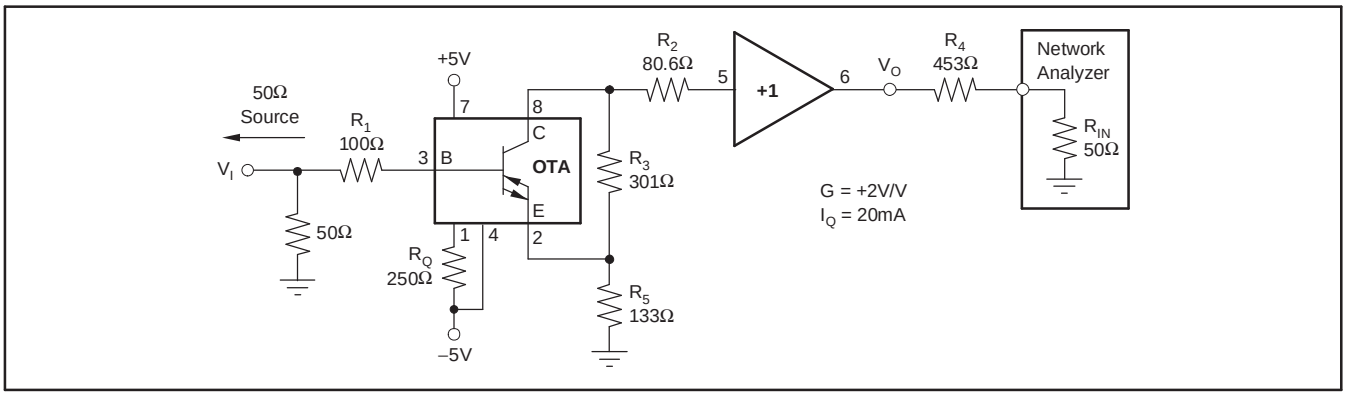


Figure 53. Direct Feedback Amplifier Specification and Test Circuit

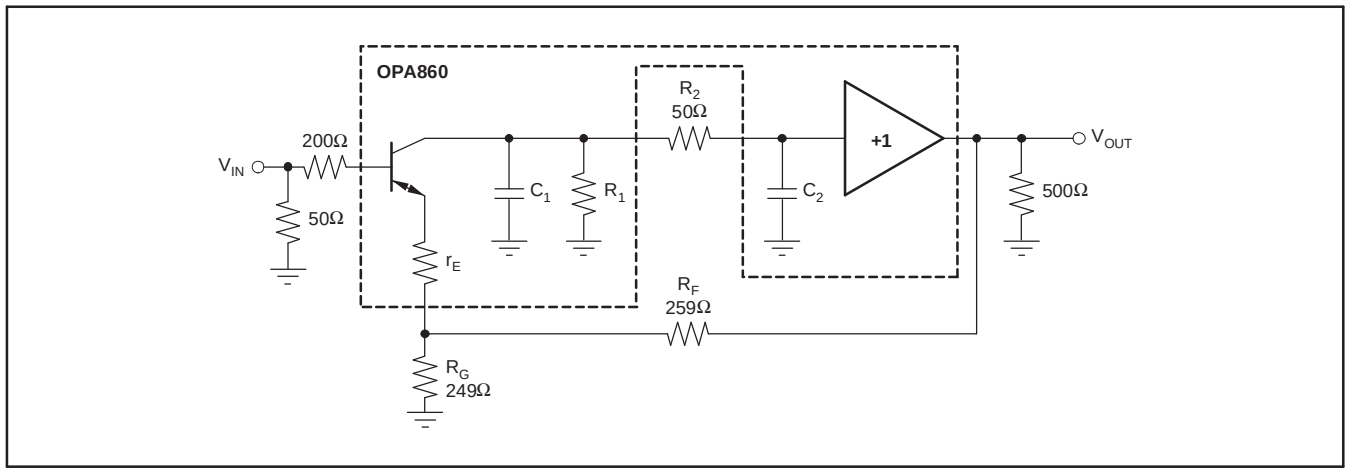


Figure 54. OPA860 Used in a Noninverting Current-Feedback Architecture

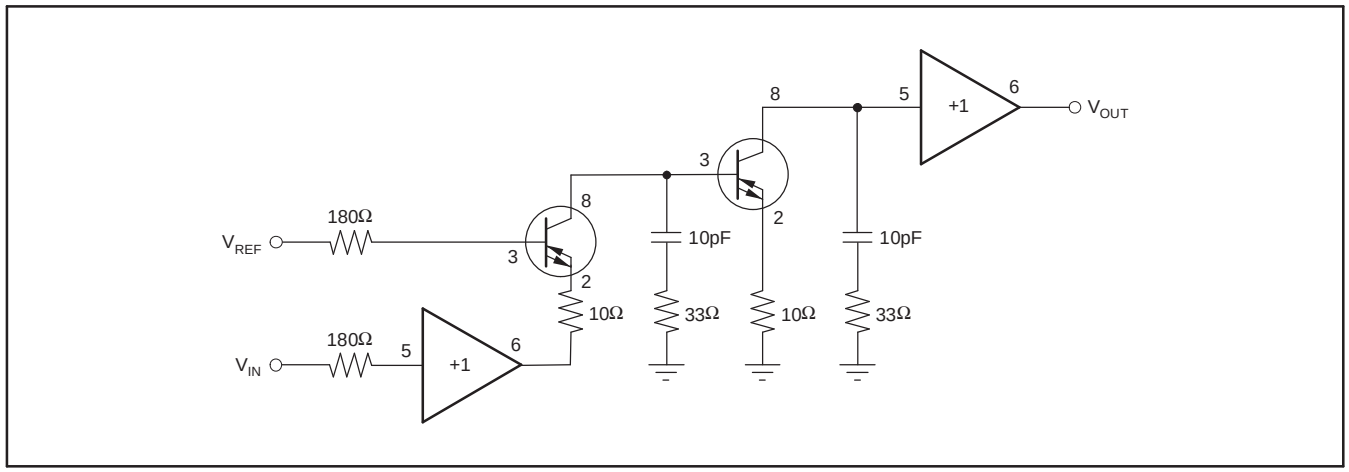


Figure 55. Control-Loop Amplifier Using Two OPA860s

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DC-Restore Circuit

The OPA860 can be used advantageously with an operational amplifier, here the OPA820, as a DC-restore circuit. Figure 56 illustrates this design. Depending on the collector current of the transconductance amplifier (OTA) of the OPA860, a switching function is realized with the diodes D_1 and D_2.

When the C-output is sourcing current, the capacitor C_1 is being charged. When the C-output is sinking current, D_1 is turned off and D_2 is turned on, letting the voltage across C_1 be discharged through R_2.

The condition to charge C_1 is set by the voltage difference between V_{REF} and V_{OUT}. For the OTA C-output to source current, V_{REF} has to be greater than V_{OUT}. The rate of charge of C_1 is set by both R_1 and C_1. The discharge rate is given by R_2 and C_1.

Comparator

An interesting and also cost-effective circuit solution using the OPA860 as a low-jitter comparator is shown in Figure 57. At the same time, this circuit uses a positive and negative feedback. The input is connected to the inverting E-input. The output signal is applied in a direct feedback over the two antiparallel, connected gallium-arsenide diodes back to the emitter. A second feedback path over the RC combination to the base, which is a positive feedback, accelerates the output voltage change when the input voltage crosses the threshold voltage. The output voltage is limited to the threshold voltage of the back-to-back diodes.

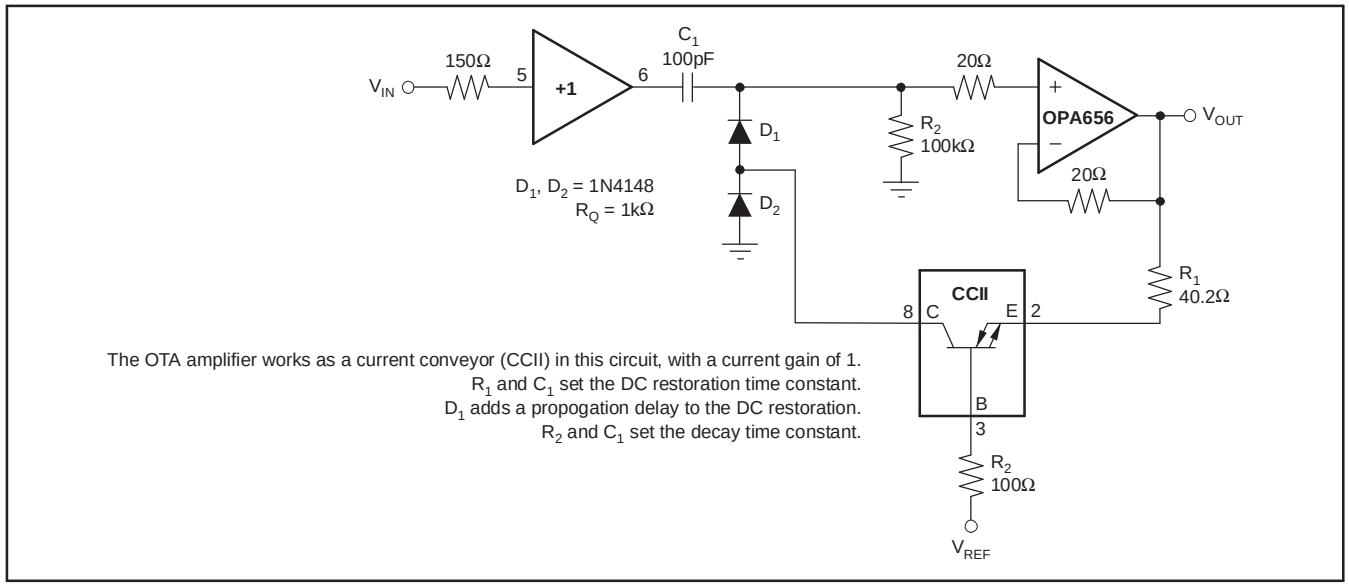


Figure 56. DC Restorer Circuit

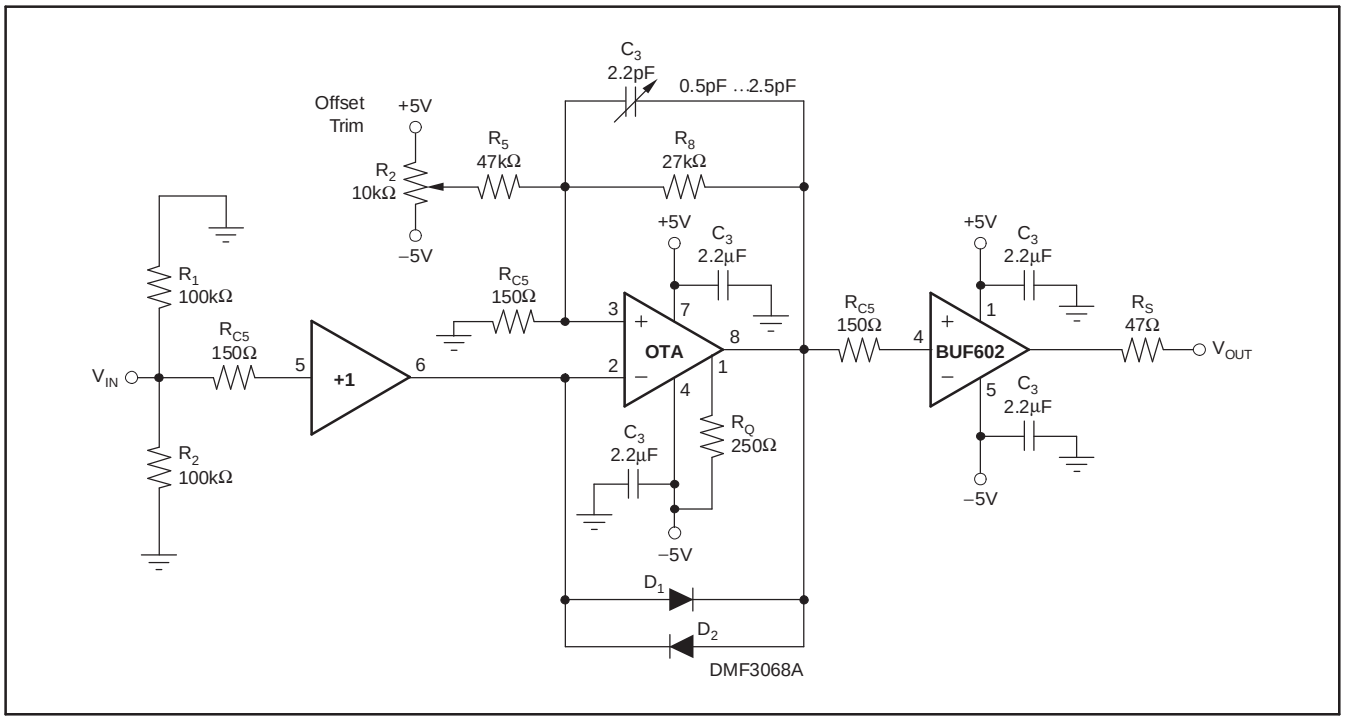


Figure 57. Comparator (Low Jitter)

Integrator for ns-Pulse

One very interesting application using the OPA860 in physical measurement technology is an open-loop ns-integrator (shown in Figure 58) which can process pulses with an amplitude of ±2.5V, have a rise/fall time of as little as 2ns, and also have a pulse width of more than 8ns. The voltage-controlled current source charges the integration capacitor linearly according to Equation 7:

$$V_C = V_{BE} \times g_m \times \frac{t}{C} \quad (7)$$

Where:

- V_C = Voltage At Pin 8
- V_{BE} = Base-Emitter Voltage
- g_m = Transconductance
- t = Time
- C = Integration Capacitance

The output voltage is the time integral of the input voltage. It can be calculated from Equation 8:

$$V_O = \frac{g_m}{C} \int_O^T V_{BE}\ dt \quad (8)$$

Where:

- V_O = Output Voltage
- T = Integration Time
- C = Integration Capacitance

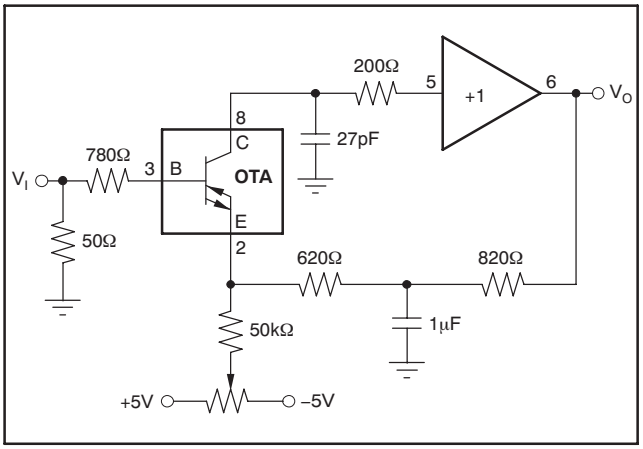


Figure 58. Integrator for ns-Pulses

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Video Luminance Matrix

The inverting amplifier in Figure 59 amplifies the three input voltages that correspond to the luminance section of the RGB color signal. Different feedback resistances weight the voltages differently, resulting in an output voltage consisting of 30% of the red, 59% of the green, and 11% of the blue section of the input voltage. The way in which the signal is weighted corresponds to the transformation equation for converting RGB pictures into B/W pictures. The output signal is the black/white replay. It might drive a monochrome control monitor or an analog printer (hardcopy output).

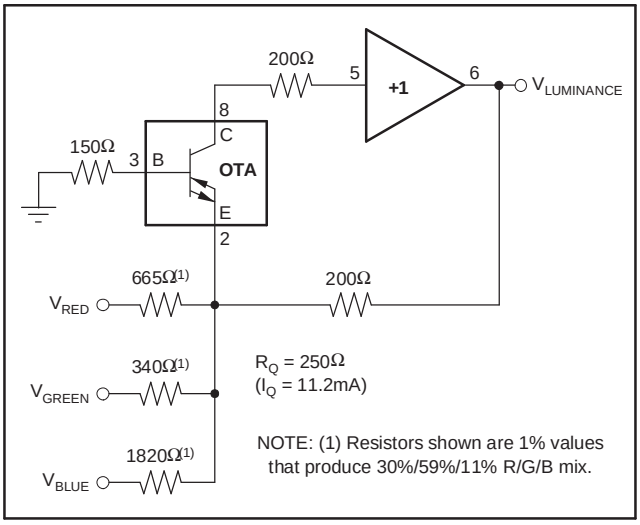


Figure 59. Video Luminance Matrix

State-Variable Filters

The ability of the OPA860 to easily drive a capacitor can be put to good use in implementing state-variable filters. A state-variable filter, or KHN filter, can be represented with integrators and coefficients. For example, the filter represented in the block diagram of Figure 60 can easily be implemented with two OPA860s, as shown in Figure 61.

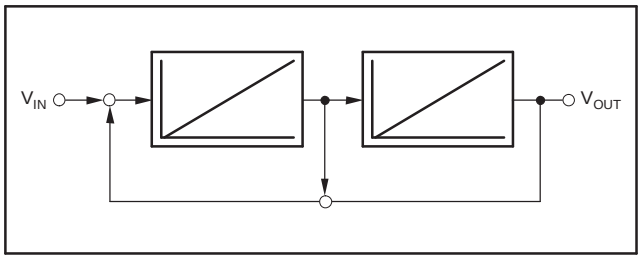


Figure 60. State Variable Filter Block Diagram

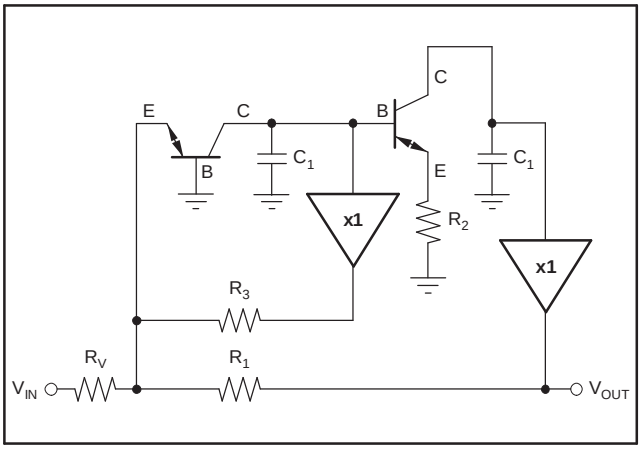


Figure 61. State Variable Filter Using the OPA860

The transfer function is then:

$$H(s) = \frac{a_0}{s^2 + C_1 s + C_0} = -\frac{R_1}{R_V} \times \frac{1}{1 + sC_2\frac{R_1 \times R_2}{R_3} + s^2 C_1 C_2 R_1 R_2} \quad (9)$$

$$\omega_0 = \frac{1}{\sqrt{C_1 C_2 R_1 R_2}} \quad (10)$$

$$Q = \sqrt{\frac{C_1}{C_2}} \times \frac{R_3}{\sqrt{R_1 R_2}} \quad (11)$$

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DESIGN-IN TOOLS

DEMONSTRATION BOARDS

A printed circuit board (PCB) is available to assist in the initial evaluation of circuit performance using the OPA860. This module is available free, as an unpopulated PCB delivered with descriptive documentation. The summary information for the board is shown below:

PRODUCT	PACKAGE	BOARD PART NUMBER	LITERATURE REQUEST NUMBER
OPA860ID	SO-8	DEM-OTA-SO-1A	SBOU035A

The board can be requested on Texas Instruments web site (www.ti.com).

MACROMODELS AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This principle is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the OPA860 is available through the Texas Instruments web page (www.ti.com). These models do a good job of predicting small-signal AC and transient performance under a wide variety of operating conditions. They do not do as well in predicting the harmonic distortion. These models do not attempt to distinguish between the package types in their small-signal AC performance.

NOISE PERFORMANCE

The OTA noise model consists of three elements: a voltage noise on the B-input; a current noise on the B-input; and a current noise on the E-input. Figure 62 shows the OTA noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

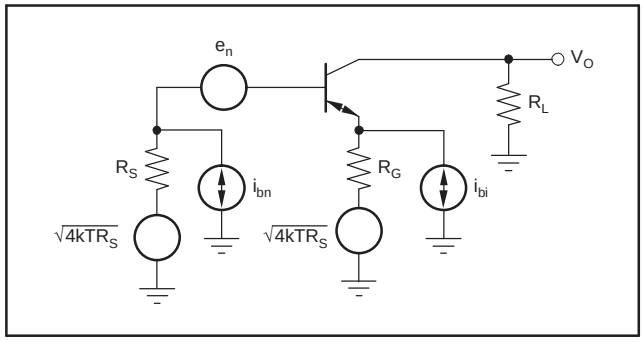


Figure 62. OTA Noise Analysis Model

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 12 shows the general form for the output noise voltage using the terms shown in Figure 62.

$$e_O = \sqrt{\left[e_n^2 + (R_S i_{bn})^2 + 4kTR_S\right]\left[\frac{R_L}{R_G + \frac{1}{g_m}}\right]^2 + \left[(R_G i_{bi})^2 + 4kTR_G\right]\frac{R_L}{\frac{1}{g_m}}} \quad (12)$$

For the buffer, the noise model is shown in Figure 63. Equation 13 shows the general form for the output noise voltage using the terms shown in Figure 63.

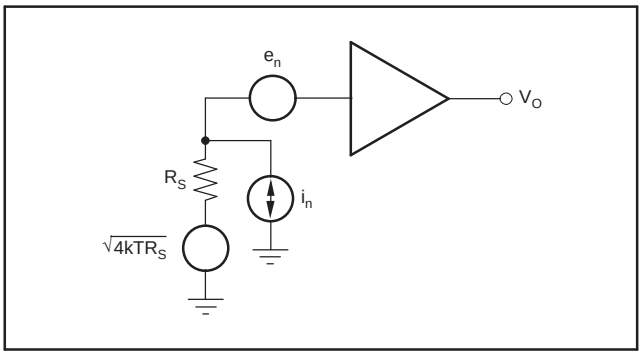


Figure 63. Buffer Noise Analysis Model

$$e_O = \sqrt{e_n^2 + (i_n R_S)^2 + 4kTR_S} \quad (13)$$

THERMAL ANALYSIS

Due to the high output power capability of the OPA860, heatsinking or forced airflow may be required under extreme operating conditions. Maximum desired junction temperature will set the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed +150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \times \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for equal bipolar supplies). Under this condition, $P_{DL} = V_S^2/(4 \times R_L)$ where R_L includes feedback network loading.

Note that it is the power in the output stage and not into the load that determines internal power dissipation.

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As a worst-case example, compute the maximum T_J using an OPA860ID in the circuit of Figure 53 operating at the maximum specified ambient temperature of +85°C and driving a grounded 20Ω load.

$P_D = 10V \times 11.2mA + 5^2/(4 \times 20\Omega) = 424mW$

Maximum $T_J = +85°C + (0.43W \times 125°C/W) = 139°C$.

Although this is still well below the specified maximum junction temperature, system reliability considerations may require lower tested junction temperatures. The highest possible internal dissipation will occur if the load requires current to be forced into the output for positive output voltages or sourced from the output for negative output voltages. This puts a high current through a large internal voltage drop in the output transistors. The output V-I plot shown in the Typical Characteristics includes a boundary for 1W maximum internal power dissipation under these conditions.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier like the OPA860 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability: on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the power-supply pins to high-frequency 0.1µF decoupling capacitors. At the device pins, the ground and power-plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. An optional supply decoupling capacitor (0.1µF) across the two power supplies (for bipolar operation) will improve 2nd-harmonic distortion performance. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c) Careful selection and placement of external components will preserve the high-frequency performance of the OPA860. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film or carbon composition, axially-leaded resistors can also provide good high-frequency performance. Again, keep their leads and PC board traces as short as possible. Never use wirewound type resistors in a high-frequency application.

d) Connections to other wideband devices on the board may be made with short, direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. If a long trace is required at the buffer output, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary on board, and in fact, a higher impedance environment will improve distortion as shown in the distortion versus load plots.

e) Socketing a high-speed part like the OPA860 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network that makes it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA860 onto the board.

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INPUT AND ESD PROTECTION

The OPA860 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the *Absolute Maximum Ratings* table. All device pins are protected with internal ESD protection diodes to the power supplies as shown in Figure 64.

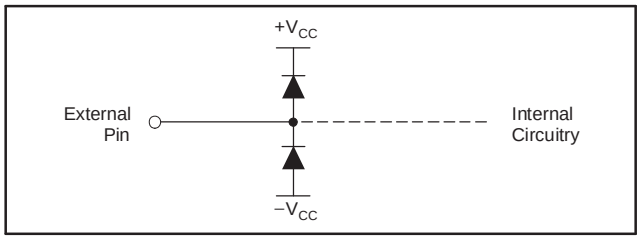


Figure 64. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±15V supply parts driving into the OPA860), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response.

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (June 2006) to Revision C **Page**

- Changed storage temperature range rating in Absolute Maximum Ratings table from –40°C to +125°C to –65°C to +125°C 2

Changes from Revision A (January 2006) to Revision B **Page**

- Changed Figure 49—corrected equations 16
- Changed Figure 58—corrected resistor value 22

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA860ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 860	Samples
OPA860IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 860	Samples
OPA860IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 860	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

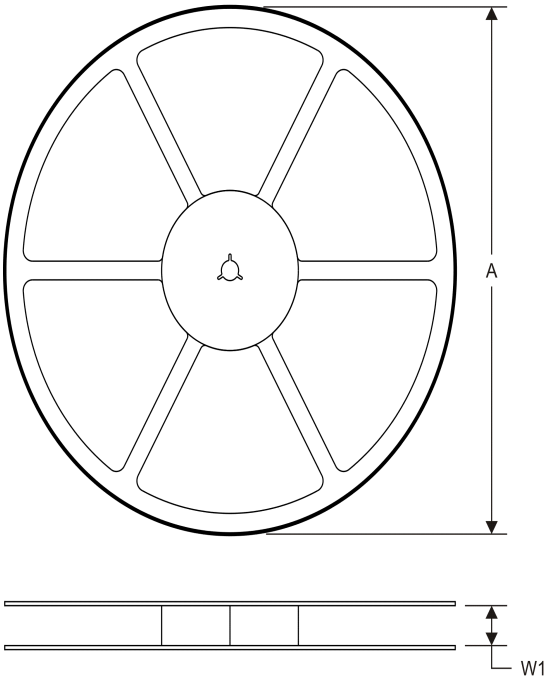
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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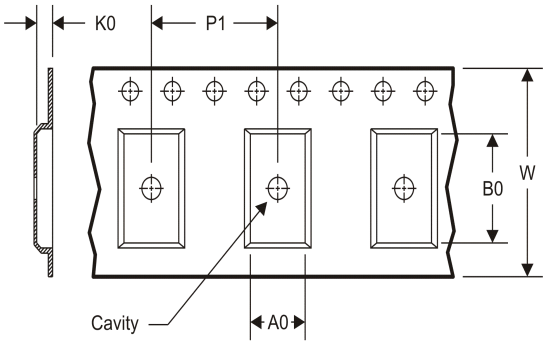
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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



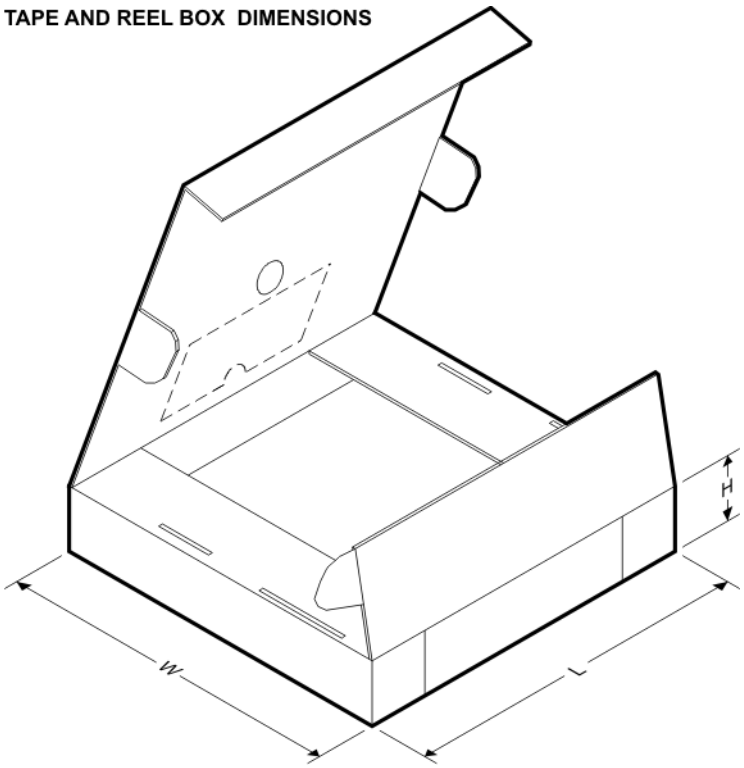
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

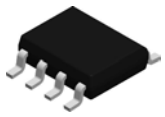
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA860IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA860IDR	SOIC	D	8	2500	367.0	367.0	35.0

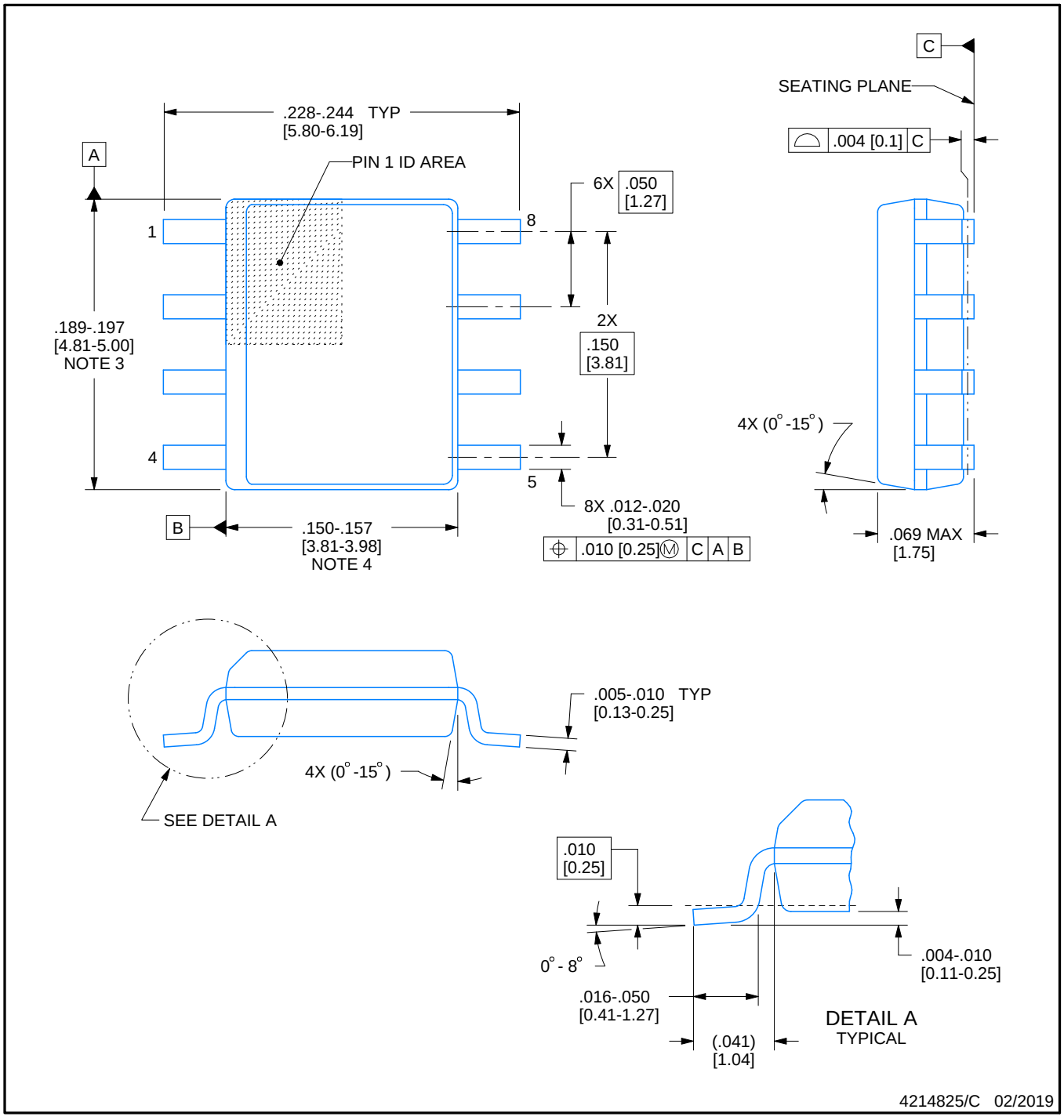


PACKAGE OUTLINE

D0008A

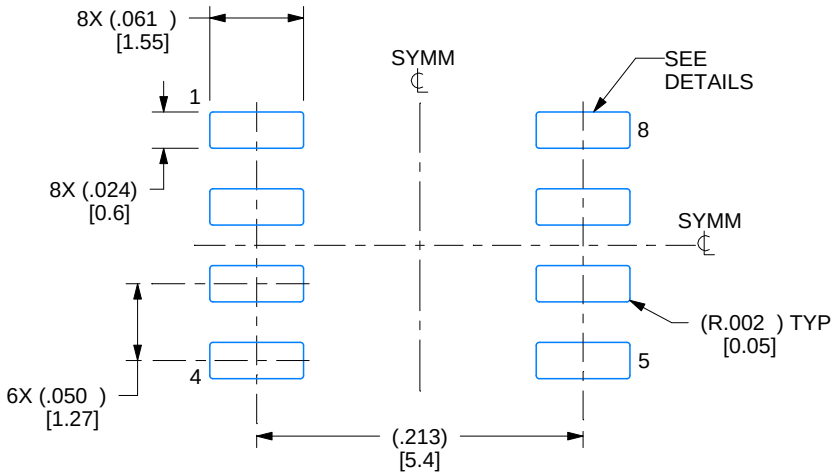
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

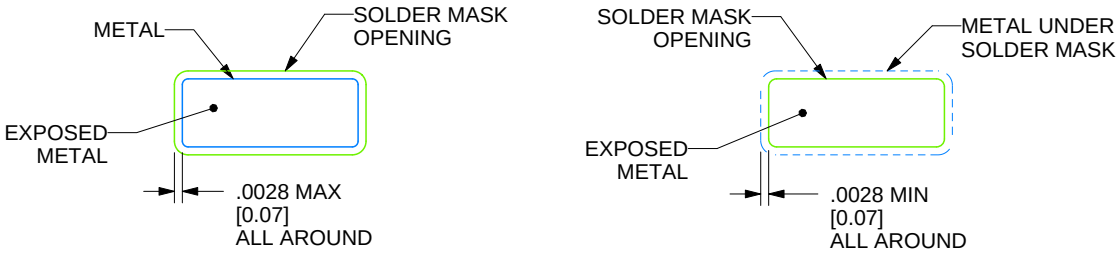


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

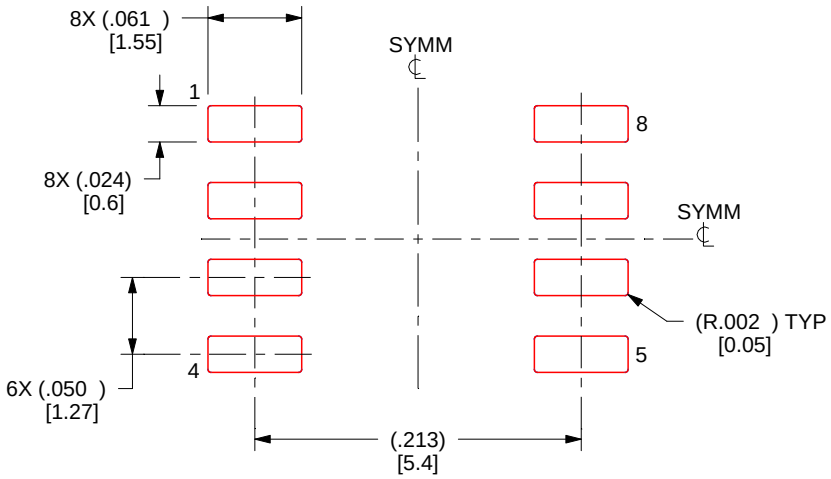
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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