OPAx607 50-MHz, Low-Power, Gain of 6-V/V Stable, Rail-to-Rail Output CMOS Operational Amplifier

1 Features

- Gain Bandwidth Product: 50 MHz
- Quiescent Current: 900 µA (Typical)
- Broadband Noise: 3.8 nV/√Hz
- Input Offset Drift: 1.5 µV/°C (Maximum)
- Offset Voltage: 120 µV (Typical)
- Input Bias Current: 10 pA (Maximum)
- Rail-to-Rail Output (RRO)
- Decompensated, Gain ≥ 6 V/V (Stable)
- Shutdown Current: 1 µA (Maximum)
- Supply Range: 2.2 V to 5.5 V

2 Applications

- Current-Sensing
- Fish Finders and Sonar
- Ultrasonic Flow Meters
- Garden and Power Tools
- Printers
- Light Curtains and Safety Guards
- Optical Modules
- Handheld Test Equipment
- PM2.5 and PM10 Particle Sensors

3 Description

The OPA607 and OPA2607 devices are decompensated minimum gain of 6 V/V stable, general-purpose CMOS operational amplifier with low noise of 3.8 nV/√Hz and a wide gain bandwidth of 50 MHz. The low noise and wide bandwidth of the OPAx607 devices make them attractive for general-purpose applications which require a good balance between cost and performance. The high-impedance CMOS inputs make the OPAx607 devices an ideal amplifier to interface with sensors with high output impedance (for example, piezoelectric transducers).

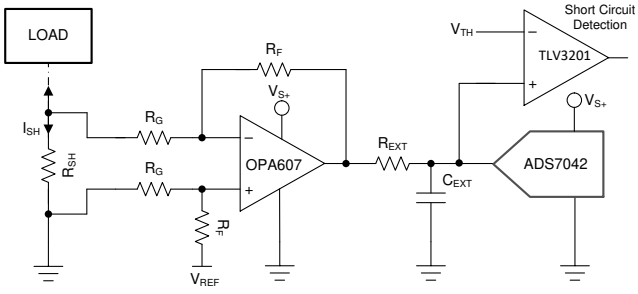
The OPAx607 devices feature a Power-down mode with a maximum quiescent current of less than 1 µA, making the device suitable for use in portable battery-powered applications. The rail-to-rail output (RRO) of the OPAx607 devices can swing up to 8 mV from the supply rails, maximizing dynamic range.

The OPAx607 is optimized for low supply voltage operation as low as 2.2 V (±1.1 V) and up to 5.5 V (±2.75 V), and is specified over the temperature range of –40°C to +125°C.

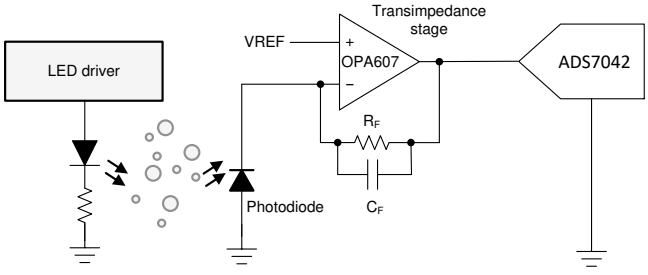
Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA607	SC70 (6)	2.00 mm × 1.25 mm
	SOT23 (5)	2.90 mm × 1.60 mm
	X2QFN (8) (2)	1.50 mm × 1.50 mm
OPA2607	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8) (2)	3.00 mm × 3.00 mm
	X2QFN (10) (2)	1.50 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) Preview package.



OPAx607 for Current-Sensing Application



OPAx607 for Transimpedance Application

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Revision History....2
5 Device Comparison....3
6 Pin Configuration and Functions....4
Pin Functions - Single Channel....4
Pin Functions - Dual Channel....5
7 Specifications....6
7.1 Absolute Maximum Ratings....6
7.2 ESD Ratings....6
7.3 Recommended Operating Conditions....6
7.4 Thermal Information....6
7.5 Electrical Characteristics....7
7.6 Typical Characteristics....9
8 Detailed Description....15
8.1 Overview....15
8.2 Functional Block Diagram....15
8.3 Feature Description....16
8.4 Device Functional Modes....19
9 Application and Implementation....20
9.1 Application Information....20
9.2 Typical Applications....20
10 Power Supply Recommendations....27
11 Layout....28
11.1 Layout Guidelines....28
11.2 Layout Examples....28
12 Device and Documentation Support....29
12.1 Device Support....29
12.2 Documentation Support....29
12.3 Related Links....29
12.4 Receiving Notification of Documentation Updates....29
12.5 Support Resources....29
12.6 Trademarks....29
12.7 Electrostatic Discharge Caution....29
12.8 Glossary....29
13 Mechanical, Packaging, and Orderable Information....30

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (August 2020) to Revision F (September 2020)	Page
• Deleted blank CMRR specifications from Electrical Characteristics table	7

Changes from Revision D (May 2020) to Revision E (August 2020)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed status of OPA2607 SOIC (8) package From: *Preview* To: *Active*	1

Changes from Revision C (April 2020) to Revision D (May 2020)	Page
• Changed status From: *Advanced Information* To: *Production Data*	1

Copyright © 2020 Texas Instruments Incorporated

5 Device Comparison

DEVICE	NO. OF CHANNELS	PACKAGE LEADS					
		SOIC (D)	X2QFN(1) (RUG)(2)	VSSOP(1) (DGK)	SC-70 (DCK)(2)	SOT-23 (DBV)	X2QFN(1) (RUG)(2)
OPA607	1	—	—	—	6(2)	5	8(2)
OPA2607	2	8	10(2)	8	—	—	—

(1) Preview Package.
(2) Package with Power-down mode.

DEVICE	INPUT	OFFSET DRIFT (µV/°C, TYP)	MINIMUM STABLE GAIN (V/V)	I_Q / CHANNEL (mA, TYP)	GBW (MHz)	SLEW RATE (V/µs)	VOLTAGE NOISE (nV/√Hz)
OPAx365	CMOS	1	1	4.6	50	25	4.5
OPAx607	CMOS	0.3	6	0.9	50	24	3.8
OPAx837	Bipolar	0.4	1	0.6	50	105	4.7

Copyright © 2020 Texas Instruments Incorporated

6 Pin Configuration and Functions

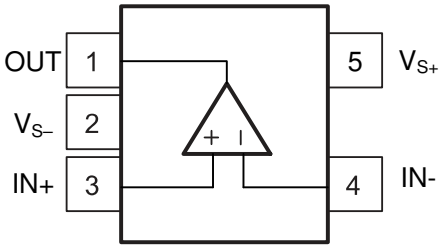


Figure 6-1. DBV Package 5-Pin SOT-23 Top View

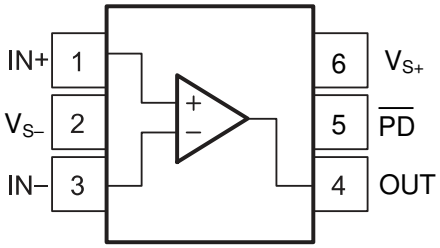


Figure 6-2. DCK Package 6-Pin SC70 Top View

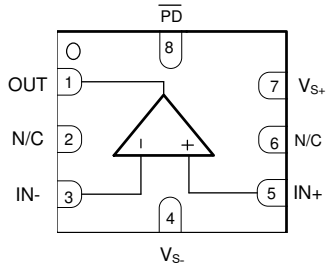


Figure 6-3. RUG Package (Preview) 8-Pin X2QFN Top View

Pin Functions - Single Channel

PIN				I/O(1)	DESCRIPTION
NAME	DBV	DCK	RUG		
IN–	4	3	3	I	Inverting input
IN+	3	1	5	I	Noninverting input
OUT	1	4	1	O	Output
$\overline{PD}$	—	5	8	I	Low = amplifier disabled, high = amplifier enabled; see the *Power-Down Mode* section for more information.
$V_{S–}$	2	2	4	P	Negative supply or ground (for single-supply operation)
V_{S+}	5	6	7	P	Positive supply
N/C	—	—	2,6	N/C	No connection (can be left floating)

(1) I = input, O = output, and P = power.

Copyright © 2020 Texas Instruments Incorporated

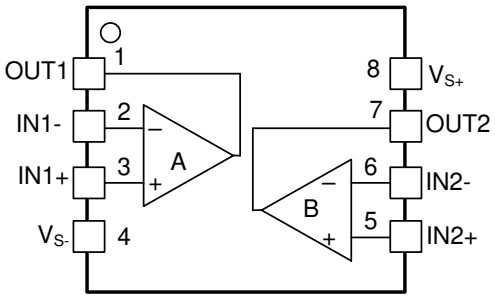


Figure 6-4. OPA2607 D, DGK (Preview) 8-Pin SOIC, VSSOP Top View

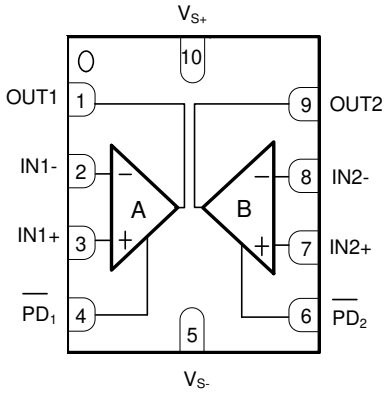


Figure 6-5. OPA2607 RUG Package (Preview) 10-Pin X2QFN Top View

Pin Functions - Dual Channel

PIN			I/O	DESCRIPTION
NAME	D, DGK	RUG		
IN1–	2	2	I	Inverting input, channel 1
IN1+	3	3	I	Noninverting input, channel 1
IN2–	6	8	I	Inverting input, channel 2
IN2+	5	7	I	Noninverting input, channel 2
OUT1	1	1	O	Output, channel 1
OUT2	7	9	O	Output, channel 2
$V_{S–}$	4	5	—	Negative (lowest) supply or ground (for single-supply operation)
V_{S+}	8	10	—	Positive (highest) supply
$\overline{PD1}$	—	4	I	Low = amplifier 1 disabled, high = amplifier 1 enabled; see the *Power-Down Mode* section for more information.
$\overline{PD2}$	—	6	I	Low = amplifier 2 disabled, high = amplifier 2 enabled; see the *Power-Down Mode* section for more information.

Copyright © 2020 Texas Instruments Incorporated

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
$(V_{S+}) – (V_{S–})$	Supply voltage, V_s		6	V
V_{IN+}, $V_{IN–}$	Input voltage	$(V_{S–}) – 0.5$	$(V_{S+}) + 0.5$	V
$V_{\overline{PD}}$	$\overline{PD}$ voltage	$(V_{S–}) – 0.5$	6	V
V_{ID}	Differential input voltage(4)		±5	V
I_I	Continuous input current(2)		±10	mA
I_O	Continuous output current(3)		±20	mA
	Continuous power dissipation	See Thermal Information		
T_J	Maximum junction temperature		150	°C
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.
(4) Long term drift of offset voltage (> 1mV) if a differential input in excess of ≈ 2V is applied continuously between the IN+ and IN- pins at elevated temperatures.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage $(V_{S+}) – (V_{S–})$	2.2		5.5	V
		±1.1		±2.75	
T_A	Ambient operating temperature	–40	25	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		OPAx607			UNIT
		D (SOIC)	DBV (SOT23)	DCK (SC70)	
		8 PINS	5 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	131.1	196.5	219.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.2	118.7	182.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	74.5	64.5	105.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	24.5	41.1	87	°C/W
ψ_{JB}	Junction-to-board characterization parameter	73.3	64.2	105.4	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

Copyright © 2020 Texas Instruments Incorporated

7.5 Electrical Characteristics

At T_A = 25°C, V_S = 2.2 V to 5.5 V, G = 6 V/V[4], R_F = 5 kΩ, C_F = 2.5 pF, V_{CM} = (V_S / 2) – 0.5 V, C_L = 10 pF, R_L = 10 kΩ connected to (V_S / 2) – 0.5 V and PD connected to (V_{S+}) (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage		–0.6	0.12	0.6	mV
	Input offset voltage[2]	T_A = –40°C to +125°C	–0.7	0.12	0.7	
dV_{OS}/dT	Input offset voltage drift[2]	T_A = –40°C to +125°C		±0.3	±1.5	µV/°C
PSRR	Power-supply rejection ratio	V_S = 2.2 V to 5.5 V	95	120		dB
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		($V_{S–}$)		(V_{S+})–1.1	V
CMRR	Common-mode rejection ratio	($V_{S–}$) < V_{CM} < (V_{S+}) – 1.1 V	90	100		dB
INPUT BIAS CURRENT						
I_B	Input bias current[2]			±3	±10	pA
		T_A = –40°C to 125°C		See Fig. 29		
I_{OS}	Input offset current[2]			±3	±10	
NOISE						
	Input voltage noise (peak-to-peak)	f = 0.1 Hz to 10 Hz		1.6		$µV_{PP}$
e_N	Input voltage noise density	f = 10 kHz, 1/f corner at 1 kHz		3.8		$nV/\sqrt{Hz}$
i_N	Input current noise density	f = 1 kHz		46		$fA/\sqrt{Hz}$
INPUT IMPEDANCE						
C_{IN}	Differential			11.5		pF
	Common-mode			5.5		
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	($V_{S–}$) + 400 mV < V_{OUT} < (V_{S+}) – 400 mV	110	130		dB
	Phase margin			65		°
AC Characteristics (V_S = 5 V)						
SSBW	Small-signal bandwidth	V_{OUT} = 20 mVpp		9		MHz
GBW	Gain-bandwidth product	G = 20 V/V		50		
SR	Slew rate	3-V output step (10-90%), V_{OCM} = mid-supply		24		V/µs
t_S	Settling time	To 0.1%, 3-V step, G = 40, V_{OCM} = mid-supply		1		µs
		To 0.01%, 3-V step, G = 40, V_{OCM} = mid-supply		1.8		
	Overdrive recovery time	V_{IN+} × Gain > V_S		0.25		µs
THD + N	Total Harmonic Distortion + Noise[5]	V_{OUT} = 2 V_{PP}, f = 1 kHz , R_L = 10 kΩ		-103		dB
		V_{OUT} = 2 V_{PP}, f = 20 kHz , R_L = 10 kΩ		-91.5		
		V_{OUT} = 2 V_{PP}, f = 1 kHz , R_L = 1 kΩ		-96		
		V_{OUT} = 2 V_{PP}, f = 20 kHz , R_L = 1 kΩ		-72.8		
HD2	Second-order harmonic distortion	V_{OUT} = 2 V_{PP} f = 20 kHz		-105		dBc
HD3	Third-order harmonic distortion	V_{OUT} = 2 V_{PP} f = 20 kHz		-95		
	Channel-to-channel crosstalk	V_{OUT} = 2 V_{PP}, f = 100 kHz		TBD		dBc
OUTPUT						
	Output voltage swing from supply rails			8	12	mV
		T_A = – 40°C to +125°C		8	12	
I_{SC}	Output Short-circuit current			60		mA

Copyright © 2020 Texas Instruments Incorporated

7.5 Electrical Characteristics (continued)

At T_A = 25°C, V_S = 2.2 V to 5.5 V, G = 6 V/V(4), R_F = 5 kΩ, C_F = 2.5 pF, V_{CM} = (V_S / 2) – 0.5 V, C_L = 10 pF, R_L = 10 kΩ connected to (V_S / 2) – 0.5 V and PD connected to (V_{S+}) (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Z_O	Open-loop output impedance	f = 1 MHz		500		Ω
POWER SUPPLY						
I_Q	Quiescent current per amplifier	I_O = 0 mA		900	1100	µA
		I_O = 0 mA, T_A = –40°C to +125°C			1200	
POWER DOWN (Device Enabled When Floating)						
	Power-down quiescent current per amplifier(3)	$\overline{PD}$= $V_{S–}$		750	1000	nA
	Power-down pin bias current per amplifier(6)	$\overline{PD}$= $V_{S–}$		–750	–1000	
	Enable voltage threshold	Logic-high threshold			0.7 x V_S	V
	Disable voltage threshold	Logic-low threshold	0.2 x V_S			
t_{ON}	Turn-on time delay(2)			10	15	µs
t_{OFF}	Turn-off time delay			0.5		

(1) Parameters with minimum or maximum specification limits are 100% production tested at 25ºC, unless otherwise noted. Over temperature limits are based on characterization and statistical analysis.
(2) Specified by design or/and characterization; not production tested.
(3) In Power-Down Mode current drawn by the opamp is equal to the bias current sourced on the $\overline{PD}$ pin
(4) All Gains (G) mentioned are in V/V unless otherwise noted.
(5) Lowpass-filter bandwidth is 92kHz for f = 20 kHz and 20 kHz for f = 1 kHz.
(6) Negative value of the powed-down bias current indicates current being sourced from the opamp's $\overline{PD}$ pin towards external circuit.

Copyright © 2020 Texas Instruments Incorporated

7.6 Typical Characteristics

At T_A = +25°C, V_S = 5.5 V, R_L = 10 kΩ, R_F= 5 kΩ, C_F= 2.5 pF, V_{CM} = midsupply – 0.5 V, G = 6 V/V (unless otherwise noted).

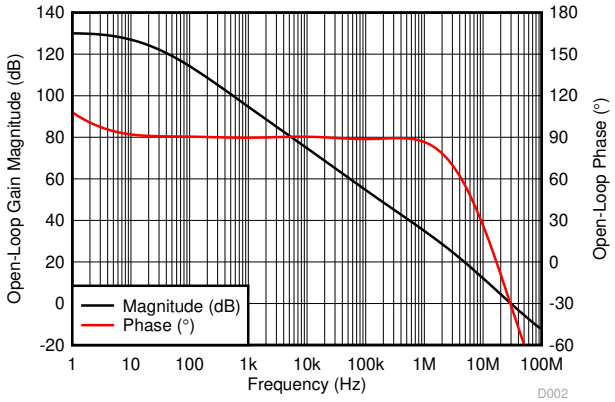


Figure 7-1. Open Loop Gain and Phase vs Frequency

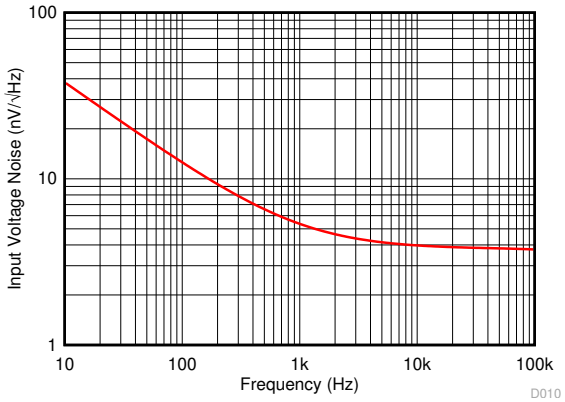


Figure 7-2. Input Voltage Noise Density vs Frequency

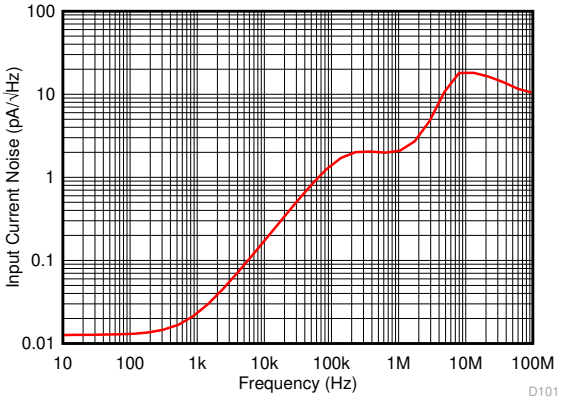
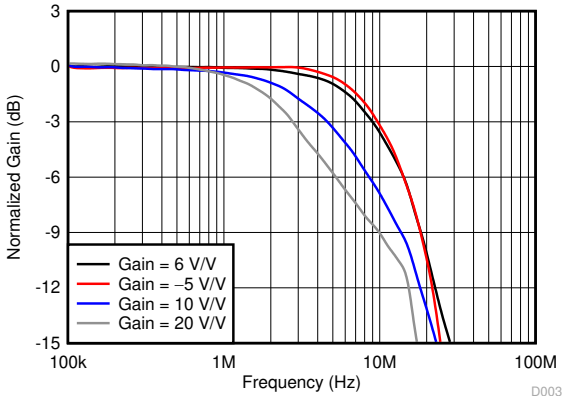
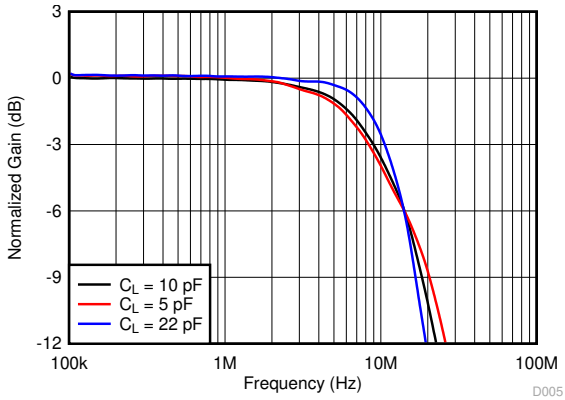


Figure 7-3. Input Current Noise Density vs Frequency



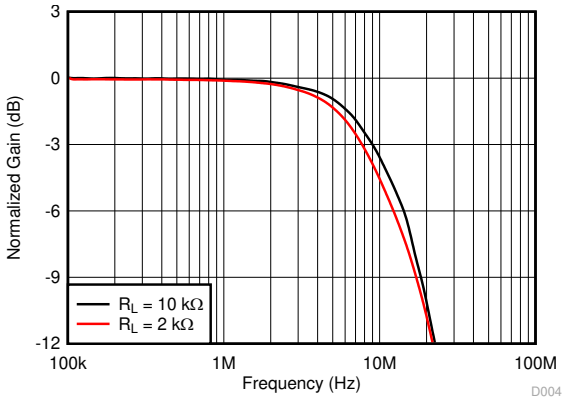
V_{OUT} = 20 mV_{PP}

Figure 7-4. Small-Signal Frequency Response vs Gain



V_{OUT} = 20 mV_{PP}

Figure 7-5. Small-Signal Frequency Response vs Capacitive Load



V_{OUT} = 20 mV_{PP}

Figure 7-6. Small-Signal Frequency Response vs Output Load

Copyright © 2020 Texas Instruments Incorporated

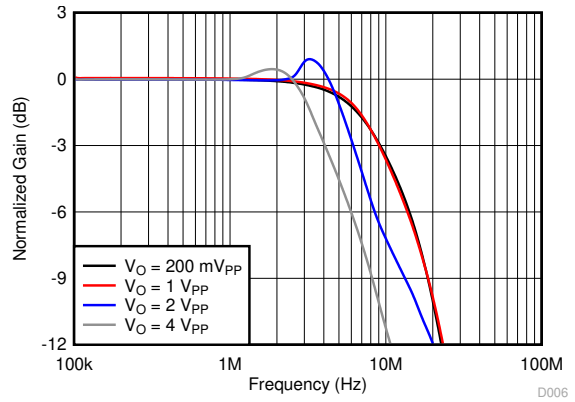


Figure 7-7. Large-Signal Frequency Response vs Output Voltage

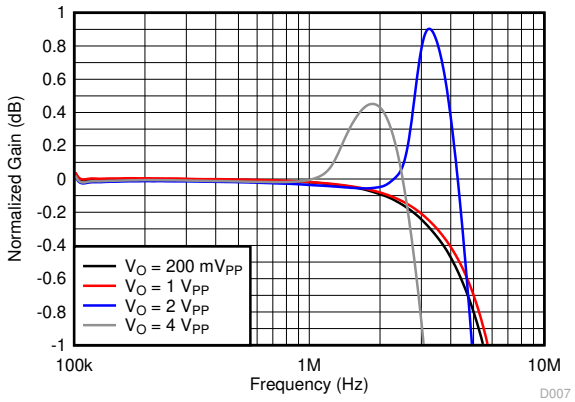
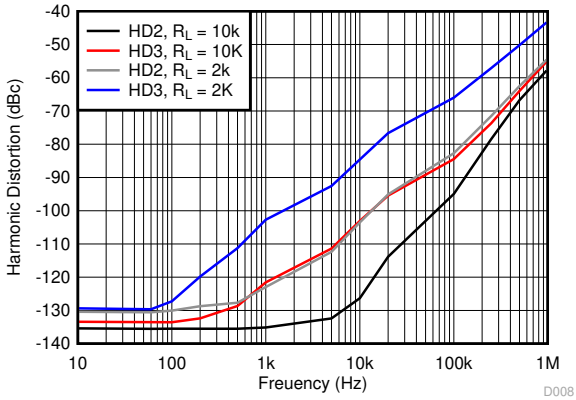
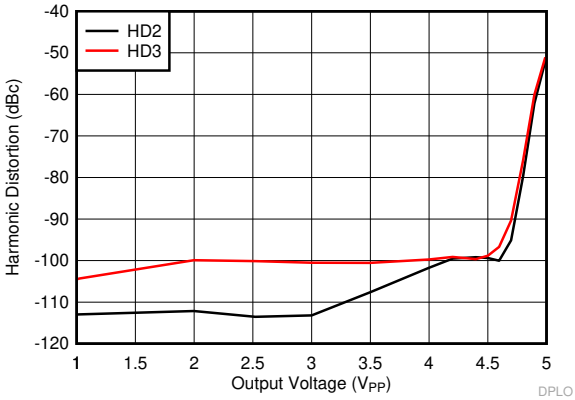


Figure 7-8. Figure 8. Large-Signal Response Flatness vs Frequency



V_{OUT} = 2 V_{PP}

Figure 7-9. Harmonic Distortion vs Frequency



Frequency = 20 kHz

Figure 7-10. Harmonic Distortion vs Output Voltage

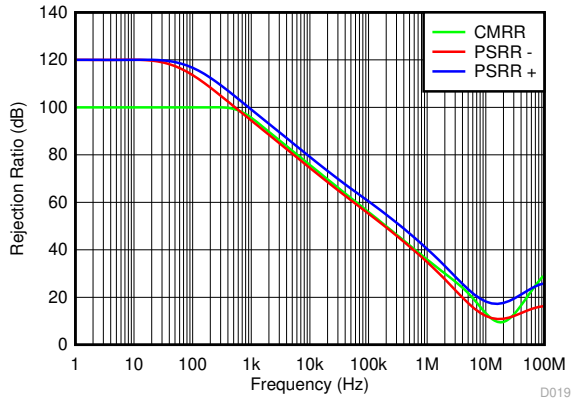


Figure 7-11. Rejection Ratio vs frequency

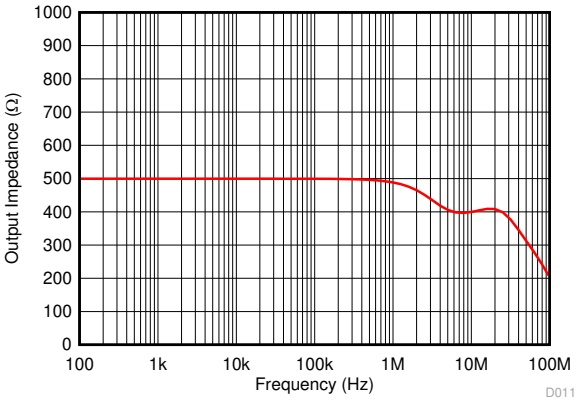


Figure 7-12. Open Loop Output Impedance vs Frequency

Copyright © 2020 Texas Instruments Incorporated

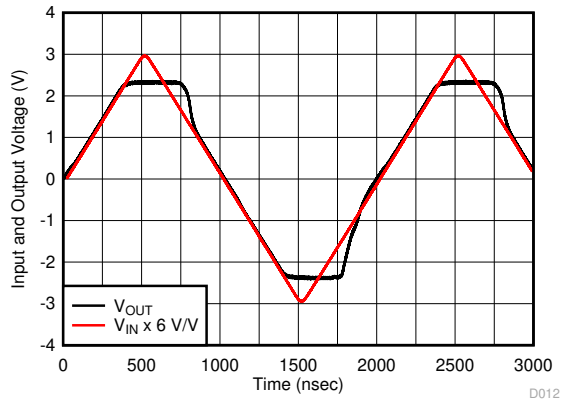
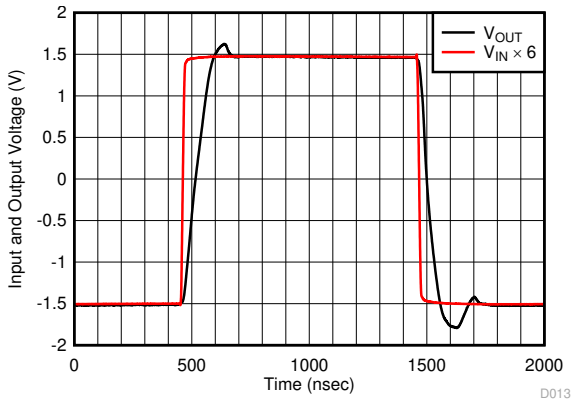
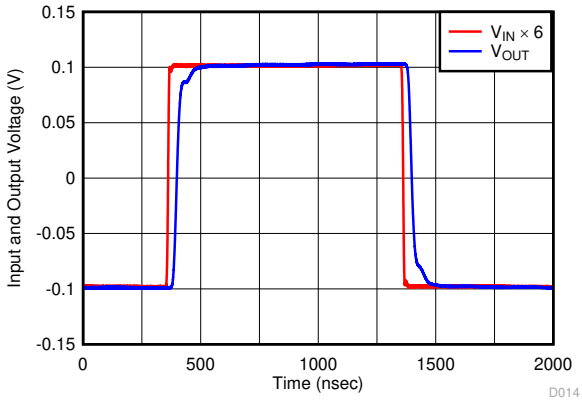


Figure 7-13. Output Overdrive Recovery



T_{RISE} = 1 µsec , T_{FALL} = 0.7 µsec

Figure 7-14. Large-Signal Transient Response



T_{RISE} = T_{FALL} = 40 nsec

Figure 7-15. Small-Signal Transient Response

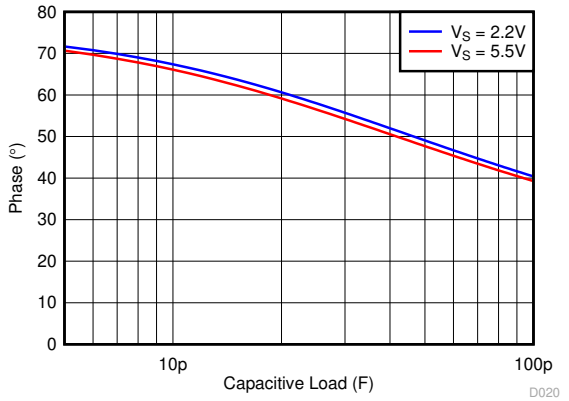
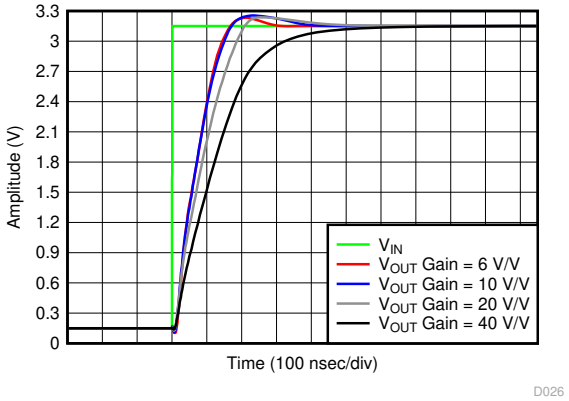


Figure 7-16. Phase Margin vs Capacitive Load



Simulated

Figure 7-17. Step Settling Time

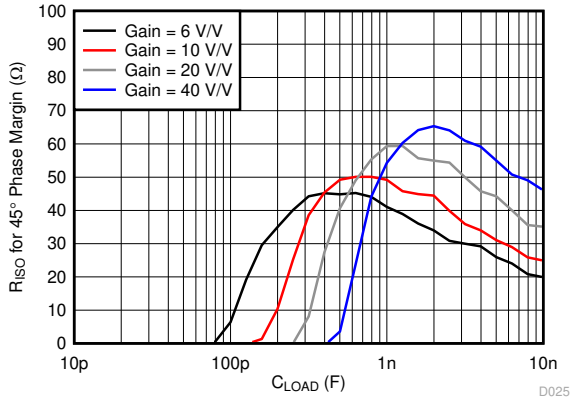
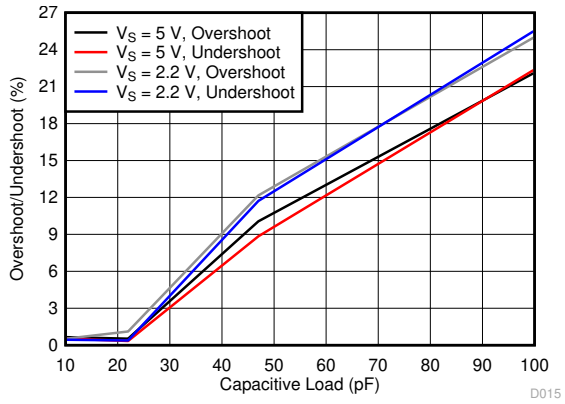


Figure 7-18. Suggested Isolation Resistor vs Capacitive Load

Copyright © 2020 Texas Instruments Incorporated



V_{OUT} = 200 mV_{PP}

Figure 7-19. Overshoot vs Capacitive Load

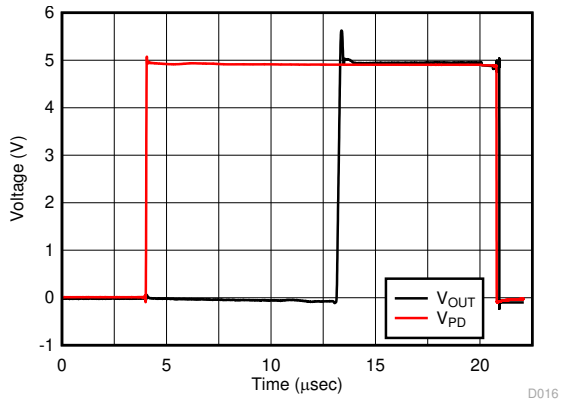


Figure 7-20. Turn-On and Turn-Off Time

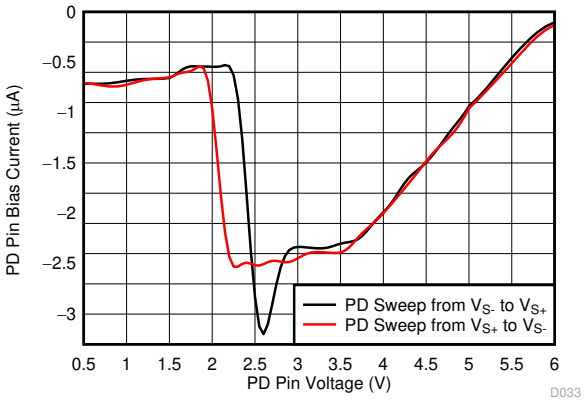
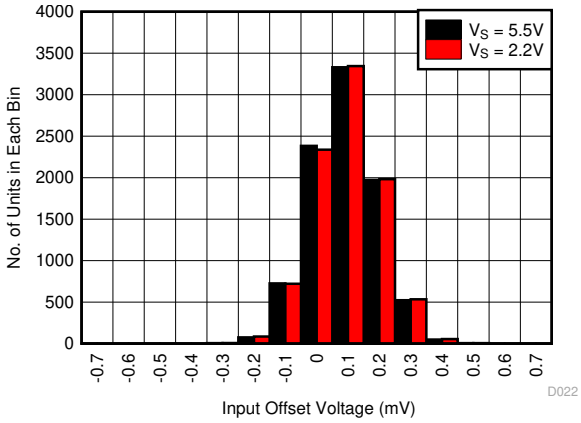
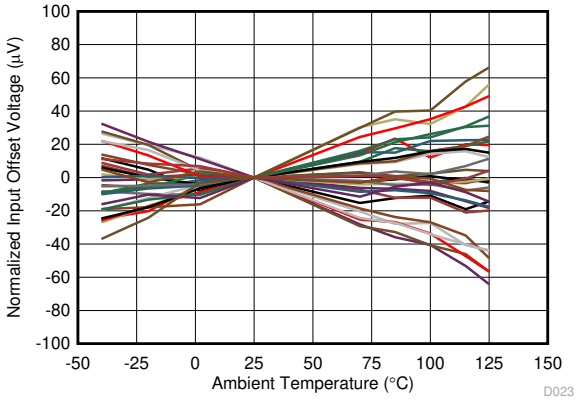


Figure 7-21. Power Down Pin Bias Current vs Power Down Pin Voltage



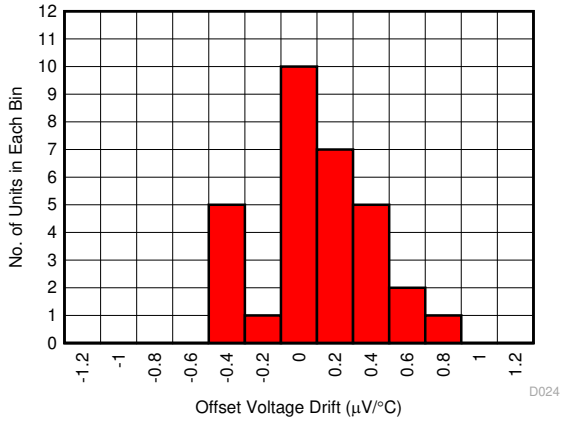
9000 units

Figure 7-22. Input Offset Voltage Distribution



32 Units, Normalized to Zero at 25°C

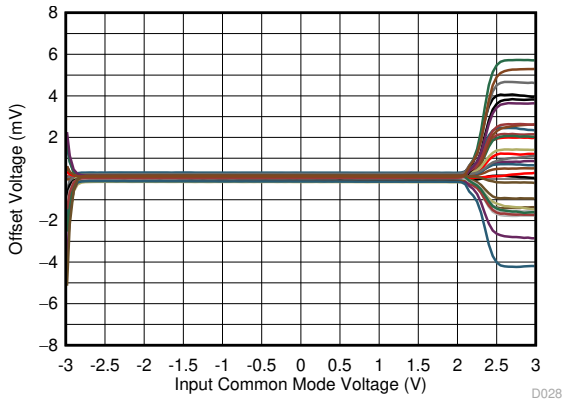
Figure 7-23. Input Offset Voltage vs Temperature



32 Units, –40°C to +125°C

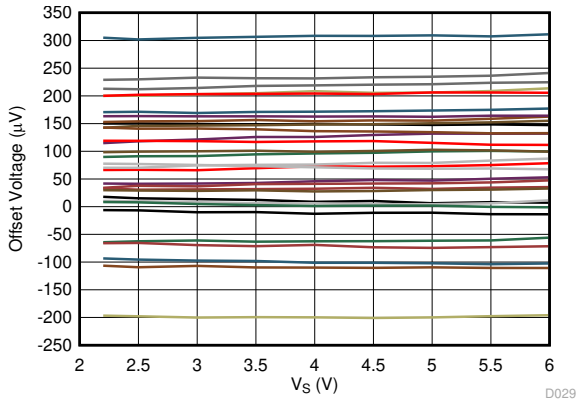
Figure 7-24. Input Offset Drift Distribution

Copyright © 2020 Texas Instruments Incorporated



V_S = ±2.75 V

Figure 7-25. Input Offset vs Common Mode Voltage



32 Units

Figure 7-26. Input Offset vs Supply

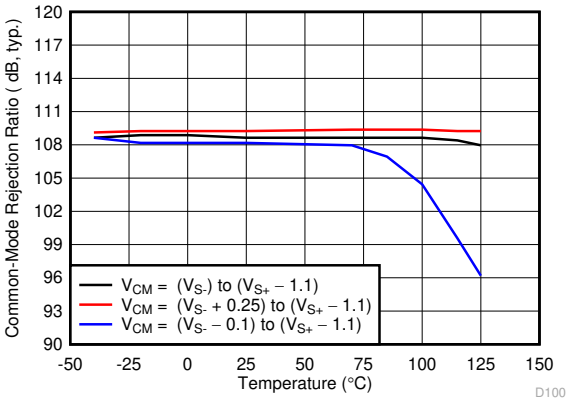


Figure 7-27. Common Mode Rejection Ratio vs Temperature

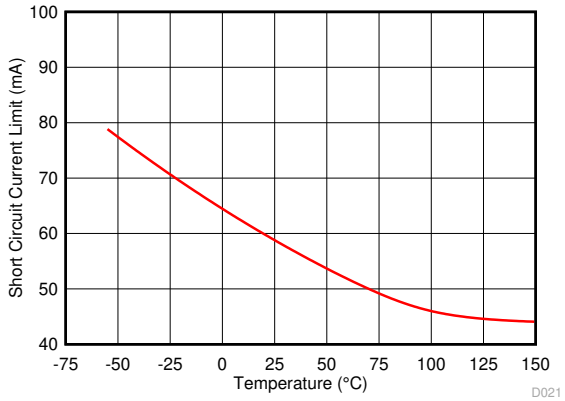


Figure 7-28. Short-Circuit Current vs Temperature

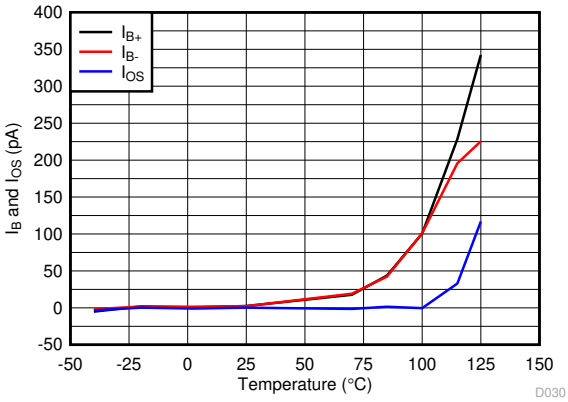


Figure 7-29. Input Bias and Offset Current vs Temperature

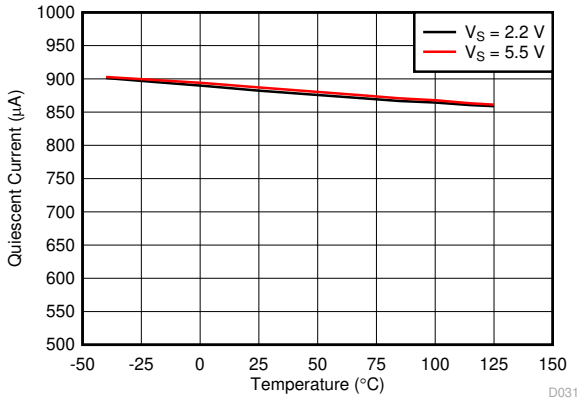


Figure 7-30. Quiescent Current vs Temperature

Copyright © 2020 Texas Instruments Incorporated

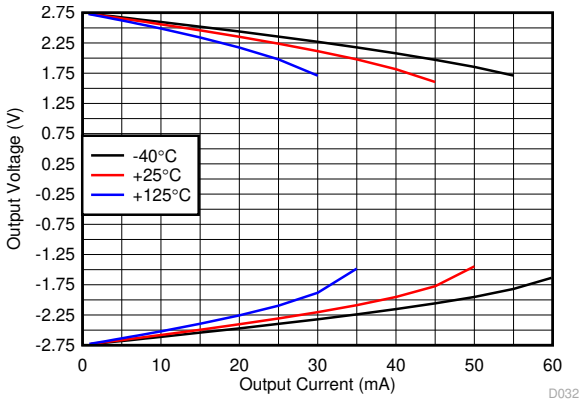


Figure 7-31. Output Voltage vs Output Current Sourcing and Sinking

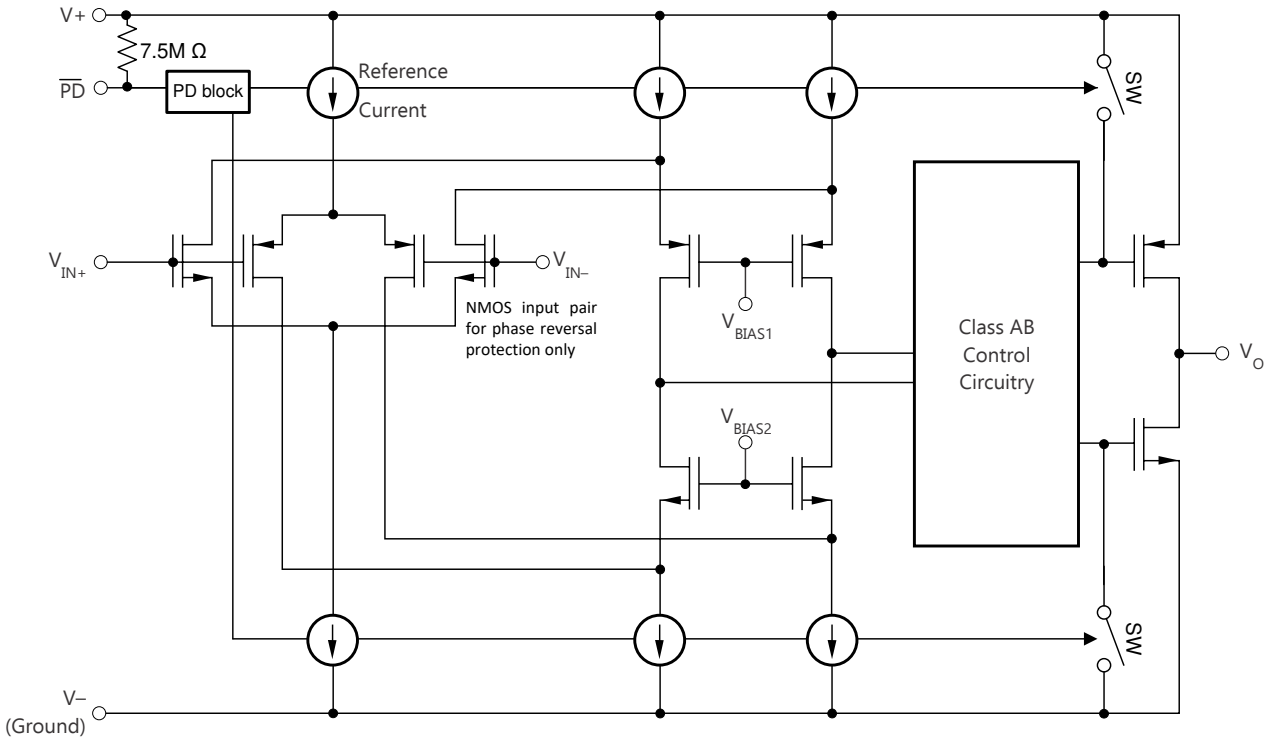
Copyright © 2020 Texas Instruments Incorporated

8 Detailed Description

8.1 Overview

The OPAx607 devices are low-noise, rail-to-rail output (RRO) operational amplifiers (op amp). The devices operate from a supply voltage of 2.2 V to 5.5 V. The input common-mode voltage range also extends down to the negative rail allowing the OPAx607 to be used in most single-supply applications. Rail-to-rail output swing significantly increases dynamic range, especially in low-supply, voltage-range applications, which results in complete usage of the full-scale range of the consecutive analog-to-digital converters (ADCs). The decompensated architecture allows for a favorable tradeoff of low-quiescent current for a very-high gain-bandwidth product (GBW) and low-distortion performance in high-gain applications.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Voltage

The OPAx607 operational amplifiers are fully specified and assured for operation from 2.2 V to 5.5 V, applicable from –40°C to +125°C. The OPAx607 devices are completely operational with asymmetric, symmetric and single supply voltages applied across the supply pins. The total voltage (that is, $(V_{S+}) – (V_{S–})$) must be less than the supply voltage mentioned in Section 7.1.

8.3.2 Rail-to-Rail Output and Driving Capacitive Loads

Designed as a low-power, low-voltage operational amplifier, the OPAx607 devices are capable of delivering a robust output drive. For resistive loads of 10 kΩ, the output swings to within a few millivolts of either supply rail, regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails. The OPAx607 devices drive up to a nominal capacitive load of 47 pF on the output with no special consideration and without the need of a series isolation resistor R_{ISO} while still being able to achieve 45° of phase margin. When driving capacitive loads greater than 47 pF, TI recommends using R_{ISO} as shown in Figure 8-1 in series with the output as close to the device as possible. Refer to Figure 7-18 for looking up different values of R_{ISO} required for C_L to achieve 45° phase margin. Without R_{ISO}, the external capacitance (C_L) interacts with the output impedance (Z_O) of the amplifier, resulting in stability issues. Inserting R_{ISO} isolates C_L from Z_O and restores the phase margin. Figure 8-1 shows the test circuit.

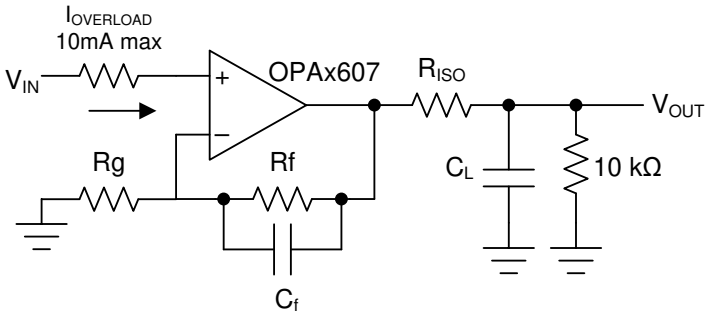
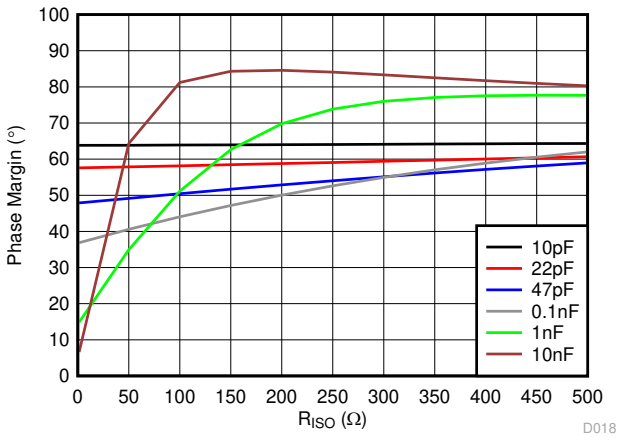


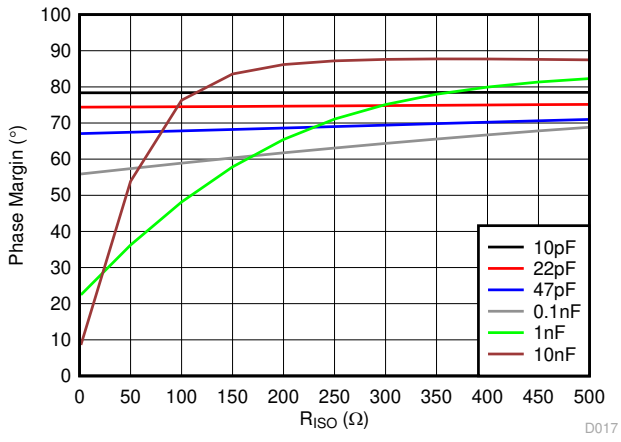
Figure 8-1. Input Current Protection and Driving Capacitive Loads

Figure 8-2 and Figure 8-3 show the phase margin achieved with varying R_{ISO} with different values of C_L.



Gain = 10 V/V, C_f = 2.5 pF, R_L = 10 kΩ

Figure 8-2. Phase Margin vs. Series Isolation Resistor



Gain = 20 V/V, C_f = 2.5 pF, R_L = 10 kΩ

Figure 8-3. Phase Margin vs. Series Isolation Resistor

Copyright © 2020 Texas Instruments Incorporated

8.3.3 Input and ESD Protection

When the primary design goal is a linear amplifier with high CMRR, do not exceed the op amp input common-mode voltage range (V_{CM}). This CMRR is used to set the common-mode input range specifications in Section 7.5. The typical V_{CM} specifications for the OPAx607 devices are from the negative rail to 1.1 V below the positive rail. Assuming the op amp is in linear operation, the voltage difference between the input pins is small (ideally 0 V) and the input common-mode voltage can be analyzed at either input pin; the other input pin is assumed to be at the same potential. The voltage at V_{IN+} is easy to evaluate. In a noninverting configuration (Figure 8-1) the input signal, V_{IN+}, must not exceed the V_{CM} rating. However, in an inverting amplifier configuration, V_{IN+} must be connected to the voltage within V_{CM}. The input signal applied at V_{IN-} can be any voltage, such that the output voltage swings with a headroom of 10 mV from either of the supply rails.

The input voltage limits have fixed headroom to the power rails and track the power-supply voltages. For single 5-V supply, the linear input voltage range is 0 V to 3.9 V and with a 2.2-V supply this range is 0 V to 1.1 V. The headroom to each power-supply rail is the same in either case: 0 V and 1.1 V. A weak NMOS input pair from V_{IN+} to V_{IN+} – 1.1 V ensures that an output phase reversal issue does not occur when the V_{CM} is violated.

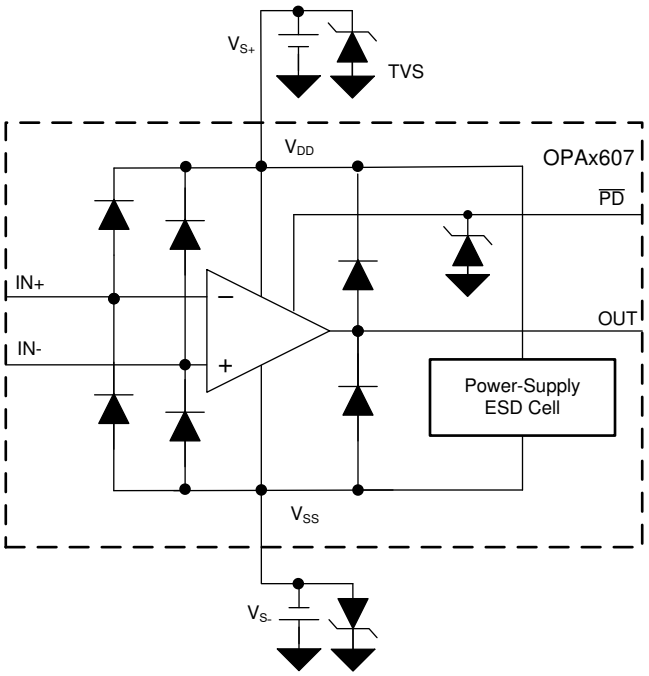


Figure 8-4. Internal ESD Structure

The OPAx607 devices also incorporate internal electrostatic discharge (ESD) protection circuits on all pins. For the input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provides input overdrive protection, as long as the current is limited with a series resistor to 10 mA, as stated in the Section 7.1. Figure 8-1 shows a series input resistor can be added to the driven input to limit the input current.

Copyright © 2020 Texas Instruments Incorporated

8.3.4 Decompensated Architecture with Wide Gain-Bandwidth Product

Amplifiers such as the OPAx607 devices are not unity-gain stable are referred to as *decompensated amplifiers*. The decompensated architecture typically allows for higher GBW, higher slew rate, and lower noise compared to a unity-gain stable amplifier with similar quiescent currents. The increased available bandwidth reduces the rise time and the settling time of the op amp, allowing for sampling at faster rates in an ADC-based signal chain.

As shown in Figure 8-5, the dominant pole f_d is moved to the frequency f_1 in the case of a decompensated op amp. The solid A_{OL} plot is the open-loop gain plot of a traditional unity-gain stable op amp. The change in internal compensation in a decompensated amp such as the OPAx607, increase the bandwidth for the same amount of power. That is, the decompensated op amp has an increased bandwidth to power ratio when compared to a unity-gain stable op amp of equivalent architecture. Besides the advantages in the above mentioned parameters, an increased slew rate and a better distortion (HD2 and HD3) value is achieved because of the higher available loop-gain, compared to its unity-gain counterpart. The most important factor to consider is ensuring that the op amp is in a noise gain (NG) greater than G_{min}. A value of NG lower than G_{min} results in instability, as shown in Figure 8-5, because the 1/ß curve intersects the A_{OL} curve at 40 dB/decade. This method of analyzing stability is called the *rate of closure method*. See the precision lab training videos from TI for a better understanding on device stability and for different techniques of ensuring stability.

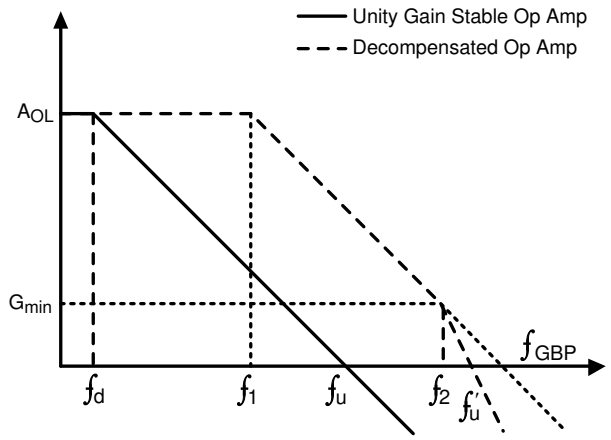


Figure 8-5. Gain vs Frequency Characteristics for a Unity-Gain Stable Op Amp and a Decompensated Op Amp

The OPAx607 devices are stable in a noise gain of 6 V/V (15.56 dB) or higher in conventional gain circuits; see Figure 8-6. The device has 9 MHz of small-signal bandwidth (SSBW) in this gain configuration with approximately 65° of phase margin. The high GBW and low voltage noise of the OPAx607 devices make them suitable for general-purpose, high-gain applications.

Copyright © 2020 Texas Instruments Incorporated

8.4 Device Functional Modes

The OPAx607 devices have two functional modes: normal operating mode and Power-down ($\overline{PD}$) mode.

8.4.1 Normal Operating Mode

The OPAx607 devices are operational when the power-supply voltage is between 2.2 V (±1.1 V) and 5.5 V (±2.75 V). Most newer systems use a single power supply to improve efficiency and simplify the power tree design. The OPAx607 devices can be used with a single-supply power ($V_{S–}$ connected to GND) with no change in performance from split supply, as long as the input and output pins are biased within the linear operating region of the device. The valid input and output voltage ranges are given in Section 7.5. The outputs nominally swing rail-to-rail with approximately 10-mV headroom required for linear operation. The inputs can typically swing up to the negative rail (typically ground) and to within 1.1 V from the positive supply. Figure 8-6 shows changing from a ±2.5-V split supply to a 5-V single-supply.

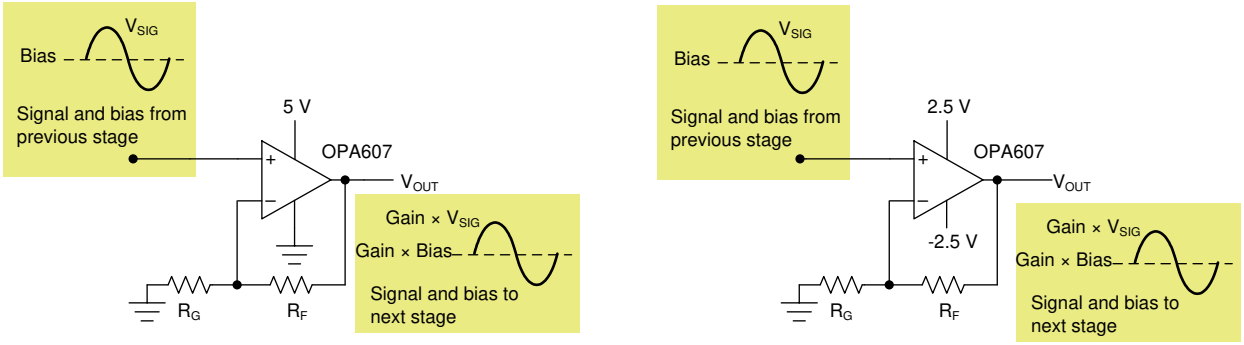


Figure 8-6. Single-Supply and Dual-Supply Operation

8.4.2 Power-Down Mode

The OPAx607 devices feature a Power-down mode for power critical applications. Under logic control, the amplifier can be switched from normal operation (consuming ≤ 1 mA) to a Power-down current of less than 1 µA. When the $\overline{PD}$ pin is connected high, the amplifier is active. Connecting the $\overline{PD}$ pin to logic low disables the amplifier and places the output in a high-impedance state. The output of an op amp is high impedance similar to a tri-state high-impedance gate under a Power-down condition; however, the feedback network behaves as a parallel load.

If the Power-down mode is not used, connect $\overline{PD}$ to the positive supply pin or leave floating. See the *Power Down (Device Enabled When Floating)* section in Section 7.5 table for the enable and disable threshold voltages. The $\overline{PD}$ pin can be left floating to keep the op amp always enabled, which is primarily possible because of the presence of an internal pullup resistor within the op amp that, by default, always keeps the $\overline{PD}$ pin weakly tied to V_{S+}. However it is also acceptable to strengthen the pull up from the $\overline{PD}$ pin by connecting a low value resistance from the $\overline{PD}$ pin to V_{S+}. This helps make the part less susceptible to noise and transient pick up on the $\overline{PD}$ pin. Looking at the $\overline{PD}$ pin bias current in Figure 7-21 can help us get an accurate understanding of the voltage required to be applied on the $\overline{PD}$ pin for enabling and powering down. Note: the hysteresis present in Figure 7-21 help with single shot power up and power down of OPAx607 devices.

The $\overline{PD}$ pin exhibits a special type of ESD protection which allows users to apply any voltage between $V_{S–}$ to 6 V irrespective of the voltage at the V_{S+}. Special ESD structure at the $\overline{PD}$ pin helps in relaxing the requirements on power sequencing during power up and power down condition. Refer to Figure 8-4 for details of the internal ESD structure. The absolute voltage limits applicable on $\overline{PD}$ pin can be found in Section 7.1 table. Another key care about in PD condition is to ensure the IN+ and IN– are not exposed to a high differential voltage continuously. In a power up condition the op-amp's loop gain ensure the IN+ pin and the IN– track each other closely. However in PD condition the op-amp is inactive and IN– will be usually weakly tied to GND via the R_G resistor. Exposing the IN+ pin continuously to a high voltage in such a condition will result in irreversible offset voltage (V_{OS}) shift.

Copyright © 2020 Texas Instruments Incorporated

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The OPAx607 devices feature a 50-MHz gain bandwidth with 900 µA of supply current, providing good AC performance at low-power consumption. The low input noise voltage of 3.8 nV/√Hz, the approximate pA of bias current, and a typical input offset voltage of 0.1 mV make the device very suitable for both AC and DC applications.

9.2 Typical Applications

9.2.1 100-kΩ Gain Transimpedance Design

The high GBW and low input voltage and current noise for the OPAx607 devices make it an excellent wideband transimpedance amplifier for moderate to high transimpedance gains.

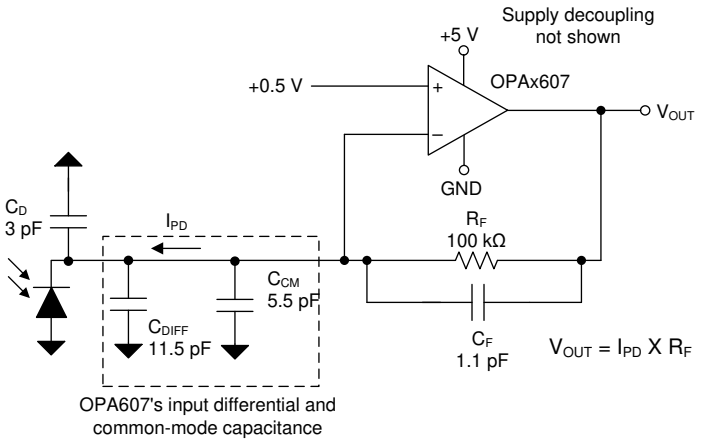


Figure 9-1. Wideband, High-Sensitivity, Transimpedance Amplifier

9.2.1.1 Design Requirements

Design a high-bandwidth, high-transimpedance-gain amplifier with the design requirements shown in Table 9-1.

Table 9-1. Design Requirements

TARGET BANDWIDTH (MHz)	TRANSIMPEDANCE-GAIN (kΩ)	PHOTODIODE CAPACITANCE (pF)
2	100	3

Copyright © 2020 Texas Instruments Incorporated

9.2.1.2 Detailed Design Procedure

Designs that require high bandwidth from a large area detector with relatively high transimpedance-gain benefit from the low input voltage noise of the OPAx607 devices. Use the Excel™ calculator available at *What You Need To Know About Transimpedance Amplifiers – Part 1* to help with the component selection based on total input capacitance and C_{TOT}. C_{TOT} is referred as C_{IN} in the calculator. C_{TOT} is the sum of C_D, C_{DIFF}, and C_{CM} which is 20 pF. Using this value of C_{TOT}, and the targeted closed-loop bandwidth (f_{-3dB}) of 2 MHz and transimpedance gain of 100 kΩ results in amplifier GBW of approximately 50 MHz and a feedback capacitance (C_F) of 1.1 pF as shown in Figure 9-2. These results are for a Butterworth response with a Q = 0.707 and a phase margin of approximately 65° which corresponds to 4.3% overshoot.

Calculator II		
Closed-loop TIA Bandwidth (f_{-3dB})	2.00	***MHz***
Feedback Resistance (R_F)	100.00	***kOhm***
Input Capacitance (C_{IN})	20.00	***pF***
Opamp Gain Bandwidth Product (GBP)	50.27	***MHz***
Feedback Capacitance (C_F)	1.110	***pF***

Figure 9-2. Results of Inputting Design Parameters in the TIA Calculator

The OPA607's 50 MHz GBW, is suitable for the above design requirements. If the required feedback capacitance C_F comes out to be a very low value capacitor to be practically achievable, please refer to Section 9.2.1.2 for guidelines in designing a T-Network capacitor circuit. A very low capacitor value (C_{EQ}) can be achieved between $Port_1$ and $Port_2$ using standard value capacitors in a T-Network circuit as shown in Figure 9-3.

$$C_{EQ} = \frac{C_1 \times C_2}{C_1 + C_2 + C_T} \quad (1)$$

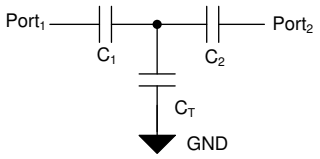


Figure 9-3. T-Network

9.2.1.3 Application Curves

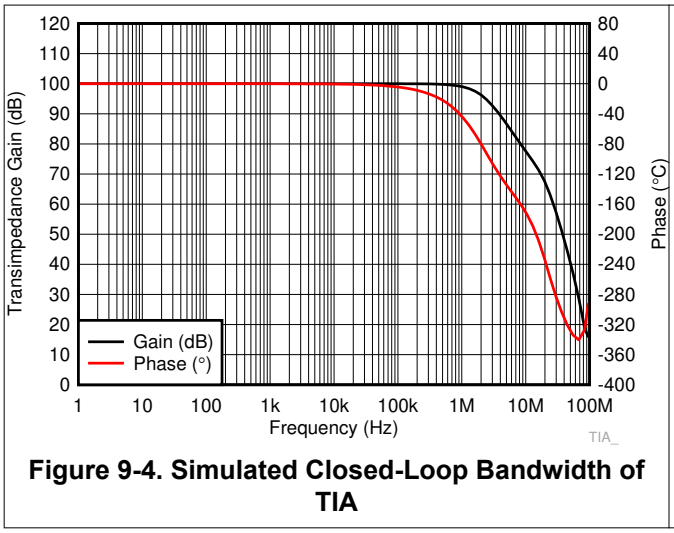


Figure 9-4. Simulated Closed-Loop Bandwidth of TIA

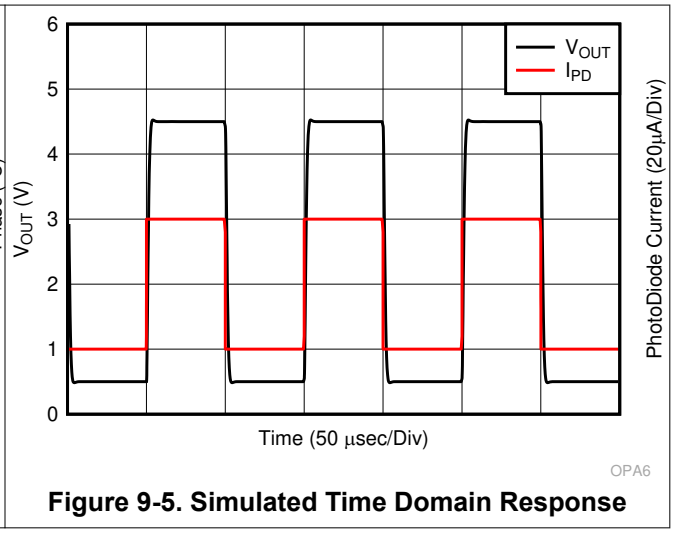


Figure 9-5. Simulated Time Domain Response

9.2.2 Noninverting Gain of 3 V/V

The OPAx607 devices are normally stable in noise gain configurations (see SBOA066) of greater than 6 V/V when conventional feedback networks are used, which is discussed in Section 8.3.4. The OPAx607 devices can be configured in noise gains of less than 6 V/V by using capacitors in the feedback path and between the inputs to maintain the desired gain at lower frequencies and increase the gain greater that 6 V/V at higher frequencies such that the amplifier is stable. Configuration (a) in Figure 9-6 shows OPAx607 devices configured in a gain of 3 V/V by using capacitors and resistors to shape the noise gain and achieve a phase margin of approximately 56° that is very close to the phase margin achieved for the conventional 6 V/V configuration (b) in Figure 9-6.

The key benefit of using a decompensated amplifier (such as the OPAx607) below the minimum stable gain, is that it takes advantage of the low noise and low distortion performance at quiescent powers smaller than comparable unity-gain stable architectures. By reducing the 100-pF input capacitor, higher closed-loop bandwidth can be achieved at the expense of increased peaking and reduced phase margin. Ensure that low parasitic capacitance layout techniques on the IN– pin are as small as 1 pF to 2 pF of parasitic capacitance on the inverting input, which will require tweaking the noise-shaping component values to get a flat frequency response and the desired phase margin. Configurations in Figure 9-6 does not take into account this parasitic capacitance but it must be considered for practical purposes. Details on the benefits of decompensated architectures are discussed in *Using a decompensated op amp for improved performance*. The *one-capacitor, externally compensated type* method is used for noise gain shaping in the below circuit.

In a difference amplifier circuit, typically used for low side current sensing applications, the (noise gain) = (signal gain + 1).

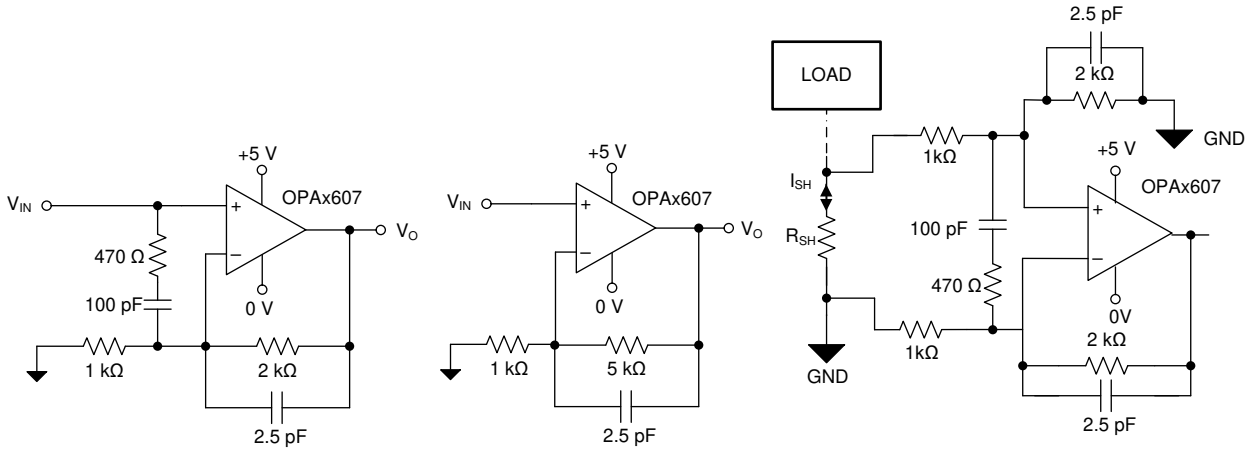


Figure 9-6. Noninverting Gain of 3 V/V, 6 V/V Configurations and Difference Amplifier in Signal Gain of 2 V/V.

Copyright © 2020 Texas Instruments Incorporated

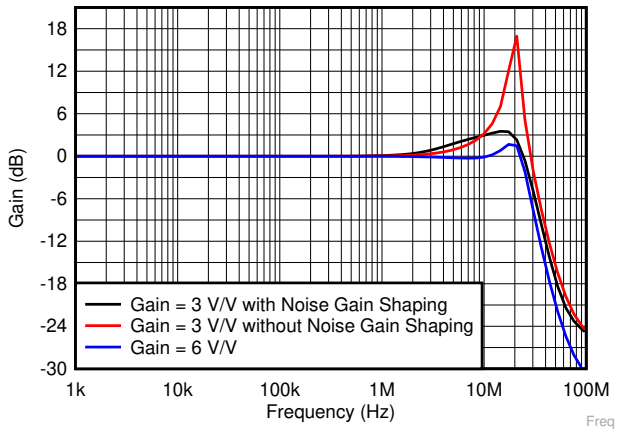


Figure 9-7. Small-Signal Frequency Response in Gains of 3V/V (a) and 6V/V (b)

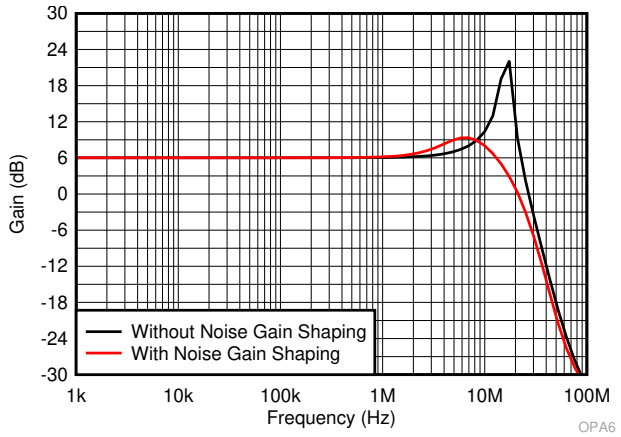


Figure 9-8. Small-Signal Frequency Response of Difference Amplifier (c) With and Without Noise Gain Shaping

9.2.3 High-Input Impedance (Hi-Z), High-Gain Signal Front-End

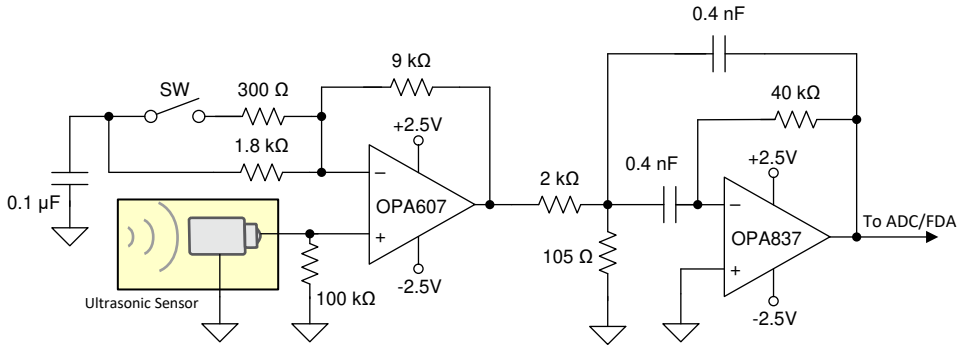


Figure 9-9. Hi-Z, High-Gain Front-End Circuit

9.2.3.1 Design Requirements

The objective is to design a high-input impedance, high-dynamic range, signal-conditioning front-end. An example application for such a front-end circuit is the receive signal chain in an ultrasonic-based end equipment (EE) such as fish finders, printers and flow meters. Table 9-2 lists the design requirements for this application.

Table 9-2. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Amplifier supply	±2.5 V
Input signal frequency	200 kHz
Minimum voltage	300 µVrms
Minimum SNR at 300 µVrms	40 dB

Copyright © 2020 Texas Instruments Incorporated

9.2.3.2 Detailed Design Procedure

To achieve a SNR of greater than 40 dB for signals from 300 uVrms to 30 mV the front-end stage has two gain settings: 6 V/V and 31 V/V. The SW (switch, relay, or analog mux) can be dynamically toggled to ensure maximum sensitively to the receiving signal. The OPAx607 devices prove to be an attractive solution for this front-end signal chain because of the right balance of low noise and high input impedance. The ultrasonic sensors (Ex. piezo crystal) have high output impedance. The OPAx607 devices have an input bias current of 20 pA (maximum). This small bias current results in reduced distortion and signal loss across the source impedance when compared with a bipolar amplifier with input bias currents in the range of a few hundreds of nano-amperes. The OPAx607's high-gain front-end is followed by a narrowband band-pass filter that is tuned to a 200-kHz center frequency. The narrowband filter is designed using the OPA837. OPA837 can be used as a variable gain mux / PGA as shown in TIDA-01565. In this application section the OPA837-based band-pass filter was designed using the techniques mentioned in the *Filter Design in Thirty Seconds* application report.

Figure 9-11 shows the frequency response of circuit in Figure 9-9. As shown in Figure 9-11, the frequency response is a high-Q factor band-pass filter centered around 200 kHz. Designing such a high-Q band-pass filter helps eliminate white band noise along with other interferences present in the circuitry, resulting in a high SNR signal chain. The OPAx607's front-end combined with the OPA837-based band-pass filter help to achieve a total gain of 33 dB (44 V/V) or 50 dB (316 V/V) based on the SW (switch) position.

9.2.3.3 Application Curves

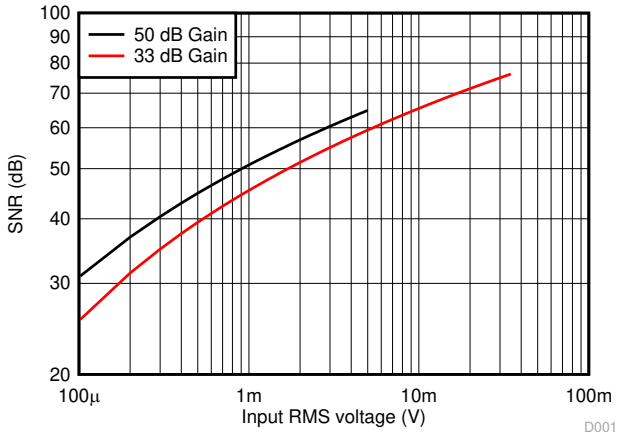


Figure 9-10. Hi-Z, High-Gain Front-End Circuit SNR vs Input

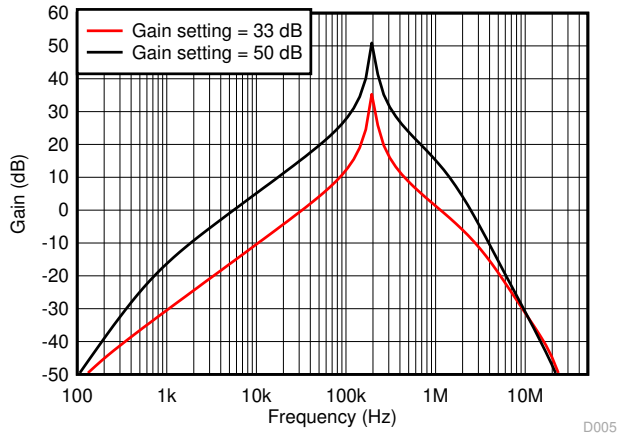


Figure 9-11. Hi-Z, High-Gain Front-End Circuit Gain vs Frequency

Copyright © 2020 Texas Instruments Incorporated

9.2.4 Low-Cost, Low Side, High-Speed Current Sensing

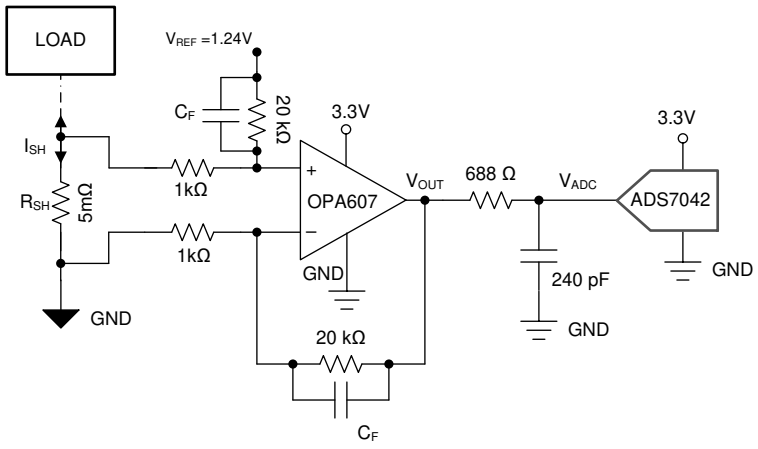


Figure 9-12. Low Side Current Sensing

9.2.4.1 Design Requirements

The objective is to design a high-speed, high-gain bidirectional current-sensing circuit for power systems and motor drive systems. Section 9.2.4.2 lists the design requirements of this application.

Table 9-3. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Amplifier and ADC supply	3.3 V
Peak current to be measured from load to ground	20 A
Peak current to be measured from ground to load	12 A
Required Accuracy of current measurement	0.1%
Signal-Setting time at ADC input	< 1 µs
Current sensing direction	Bidirectional

9.2.4.2 Detailed Design Procedure

The aim of this application section is to measure bidirectional current with relatively high accuracy in a low-side-sensing-based, high-frequency switching system.

As shown in Figure 9-12, a single op amp of high bandwidth is capable of sensing current in a high gain configuration as well as have the required effective bandwidth to drive the consecutive SAR ADC input. The SAR ADC can be a standalone ADC or integrated inside a Micro-controller.

$$V_{OUT} = (20\ k\Omega / 1\ k\Omega \times V_{DIFF}) + V_{REF}, \text{ where } V_{DIFF} = I_{SH} \text{ X } R_{SH} \quad (2)$$

The reference voltage is 1.24 V. When the I_{SH} flowing across R_{SH} equals zero, the V_{OUT} of the difference amplifier sits ideal at 1.24 V.

When the current (I_{SH}) flows from LOAD to GND, the output of the OPAx607 increase above 1.24 V with a value equal to 20 × V_{SH} and when the current flows from GND to LOAD (in the opposite direction) the output of the OPAx607 decrease below 1.24 V with a value proportional to 20 × V_{SH}.

One of the main challenges in a high speed current sensing design is to choose an op amp of with sufficient GBW that can drive a SAR ADC, while still being able to gain the signal by the required amount. The 0.1% and 0.01% settling of OPAx607 can found in Section 7.5. Another key care about is to ensure the op amp output rises in less than 1 µs so as to feed the output to a comparator for short-circuit protection. This comparator based short circuit protection loop is extremely fast and enables to turn off the switching devices very quickly. This requirement makes a low cost high speed part like the OPAx607 very desirable in a current-sensing circuit. Equation of the rise time as a function of bandwidth is shown below.

Copyright © 2020 Texas Instruments Incorporated

$$t_R \text{ (10\% to 90\%)} = 0.35 \text{ Hz / BW} \quad (3)$$

For an ADC like ADS7042 running at a sampling rate of 500 kSPS of a clock of 12.5 MHz, the effective bandwidth of the op amp required to drive such an ADC is approximately 2.7 MHz. See the TI precision lab videos on driving SAR ADCs to understand the underlying calculation. The OPAx607 has a GBW of 50 MHz. With a gain of 20 V/V, the closed loop bandwidth turns out to approximately 2.5 MHz, making this device the most suitable, cost-optimized amplifier for this application. The RC charge bucket (240 Ω and 688 pF in Figure 9-12) designed at the input of the SAR ADC is derived from the calculations provided in the SAR ADC precision lab videos. The fundamental concept behind the design of this charge bucket filter is to ensure that the sample and hold capacitor is charged to the required final voltage within the acquisition window of the ADC.

As shown in Figure 9-14, a DC accuracy of higher than 0.05% is achieved with the OPAx607. The simulations are captured with and without voltage offset calibration. Frequency response shown in Figure 9-13 indicate different signal bandwidth at V_{OUT}, V_{ADC} and with and without C_F of 220 pF.

9.2.4.3 Application Curves

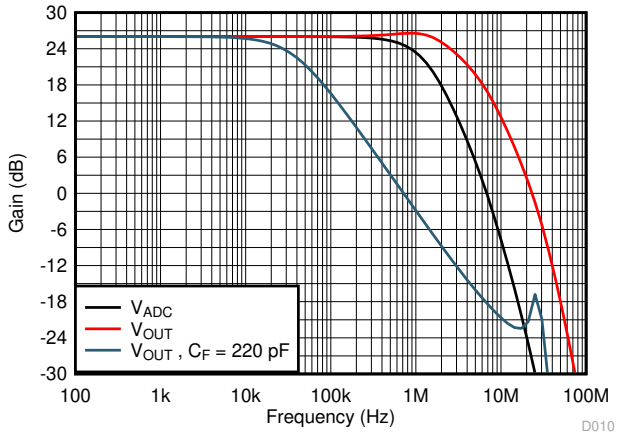


Figure 9-13. Frequency Response of Low Side Current Sensing

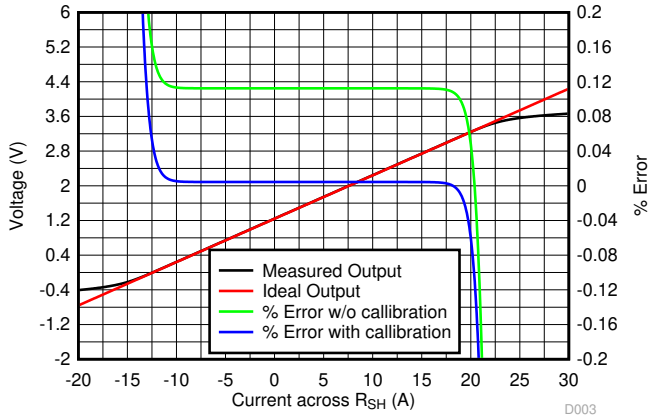


Figure 9-14. DC Current-Sense Transfer Function

Copyright © 2020 Texas Instruments Incorporated

9.2.5 Ultrasonic Flow Meters

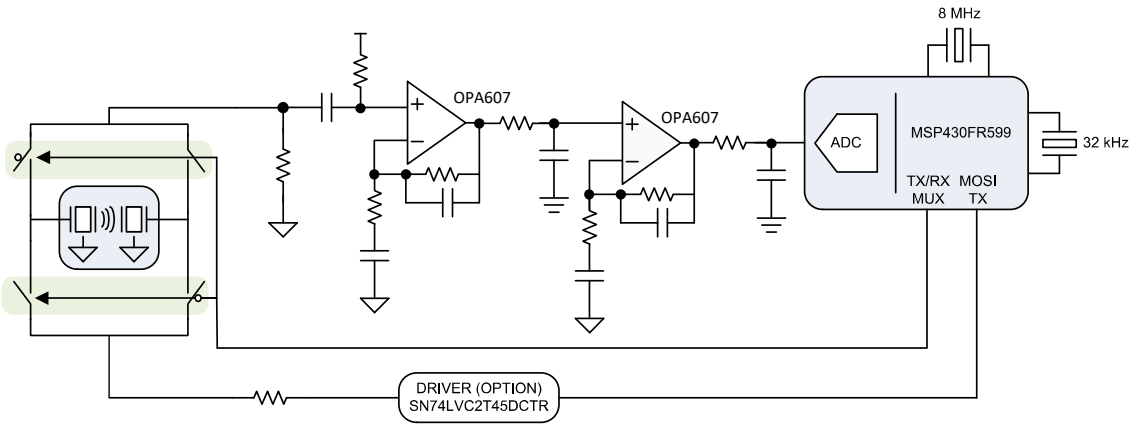


Figure 9-15. High-Gain Ultrasonic Front-End

9.2.5.1 Design Requirements

The OPAx607 devices have a wide operating voltage range of 2.2 V to 5.5 V with a maximum quiescent current of 1 mA. The availability of the inbuilt shutdown function enables designers to power cycle the front-end signal chain, reducing the net quiescent current even further. The minimum operating voltage range of 2.2 V proves to be very suitable for battery-powered and power sensitive applications such as the ultrasonic-based flow meters. The high-gain bandwidth of the OPAx607 devices enable the gain stages and the ADC drive stages to be designed and combined, thereby reducing component count. A schematic similar to that of Figure 9-12 can be used in ultrasonic flow meters for the front-end signal chain.

The *Ultrasonic sensing subsystem reference design for gas flow measurement* design guide has a detailed design procedure for ultrasonic-based sensing for gas flow measurement. The OPAx607 devices are very suitable op amps for the discrete front-end design described in this design guide.

10 Power Supply Recommendations

The OPAx607 devices are specified for operation from 2.2 V to 5.5 V (±1.1 V to ±2.75 V), applicable from –40°C to +125°C. Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies.

CAUTION

Supply voltages larger than 6 V can permanently damage the device (see Section 7.1).

For more detailed information on bypass capacitor placement, see *Section 11.1*.

Copyright © 2020 Texas Instruments Incorporated

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power-supply pins of the circuit as a whole and of the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-equivalent series resistance (ESR), 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping R_F and R_G close to the inverting input minimizes parasitic capacitance; see Figure 11-1 and Figure 11-2.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Examples

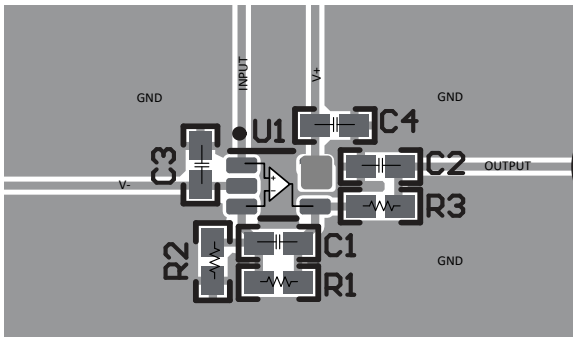


Figure 11-1. Operational Amplifier Board Layout for a Noninverting Configuration

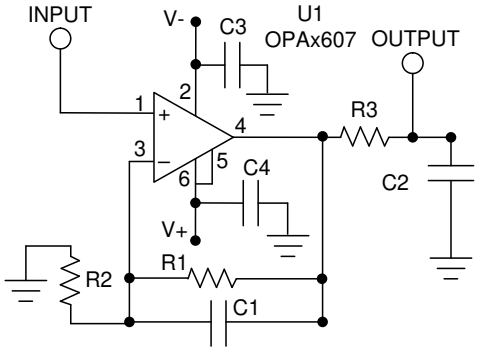


Figure 11-2. Layout Example Schematic

Copyright © 2020 Texas Instruments Incorporated

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

Texas Instruments, precision lab videos

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *OPA2834 50-MHz, 170-µA, Negative-Rail In, Rail-to-Rail Out, Voltage-Feedback Amplifier* data sheet
- Texas Instruments, *ADS7042 Ultra-Low Power, Ultra-Small Size, 12-Bit, 1-MSPS, SAR ADC* data sheet
- Texas Instruments, *Ultrasonic Sensing Subsystem Reference Design For Gas Flow Measurement* design guide
- Texas Instruments, *OPAx836 Very-Low-Power, Rail-to-Rail Out, Negative Rail In, Voltage-Feedback Operational Amplifiers* data sheet
- Texas Instruments, *Filter Design in Thirty Seconds* application report

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

12.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4.1 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.6 Trademarks

Excel™ is a trademark of Microsoft Coproration.
TI E2E™ is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.8 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

Copyright © 2020 Texas Instruments Incorporated

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2020 Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2607IDR	PREVIEW	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125		
OPA607IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O6BV	Samples
OPA607IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O6BV	Samples
OPA607IDCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1G4	Samples
OPA607IDCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1G4	Samples
XOPA2607IDR	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

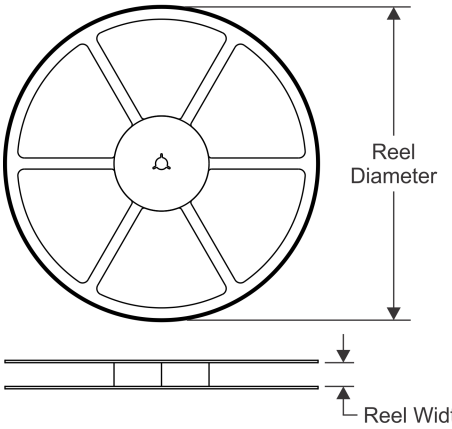
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

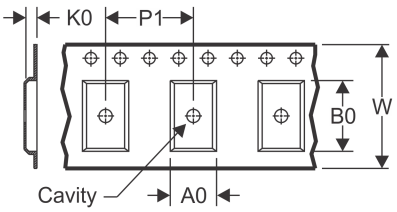
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

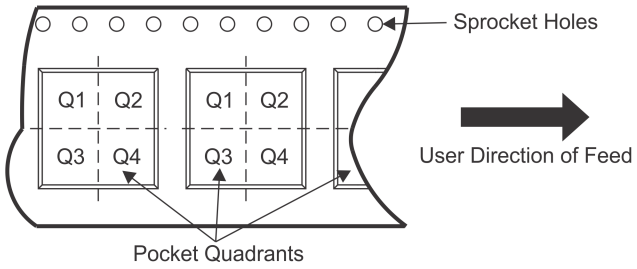


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

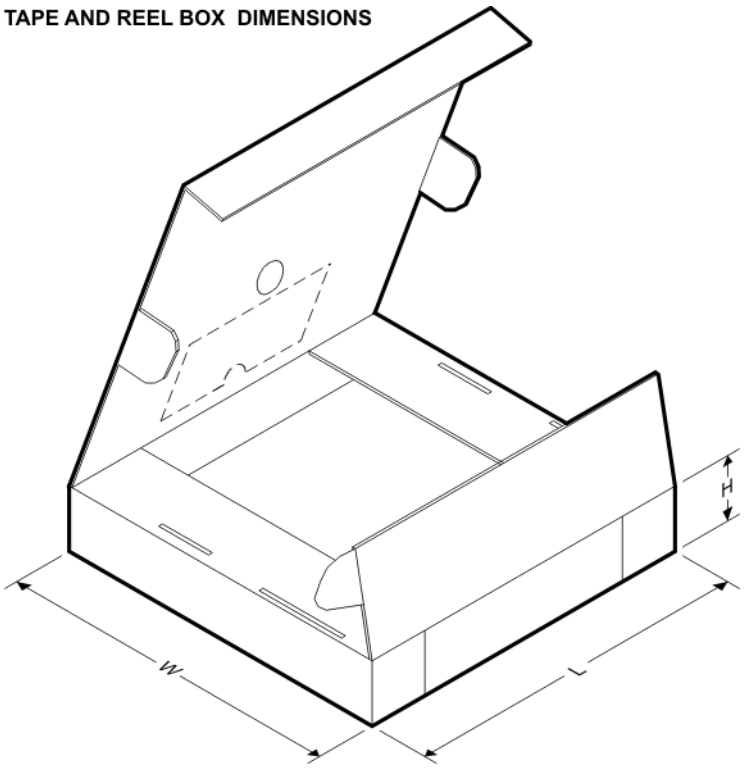
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA607IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA607IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA607IDCKR	SC70	DCK	6	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
OPA607IDCKT	SC70	DCK	6	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

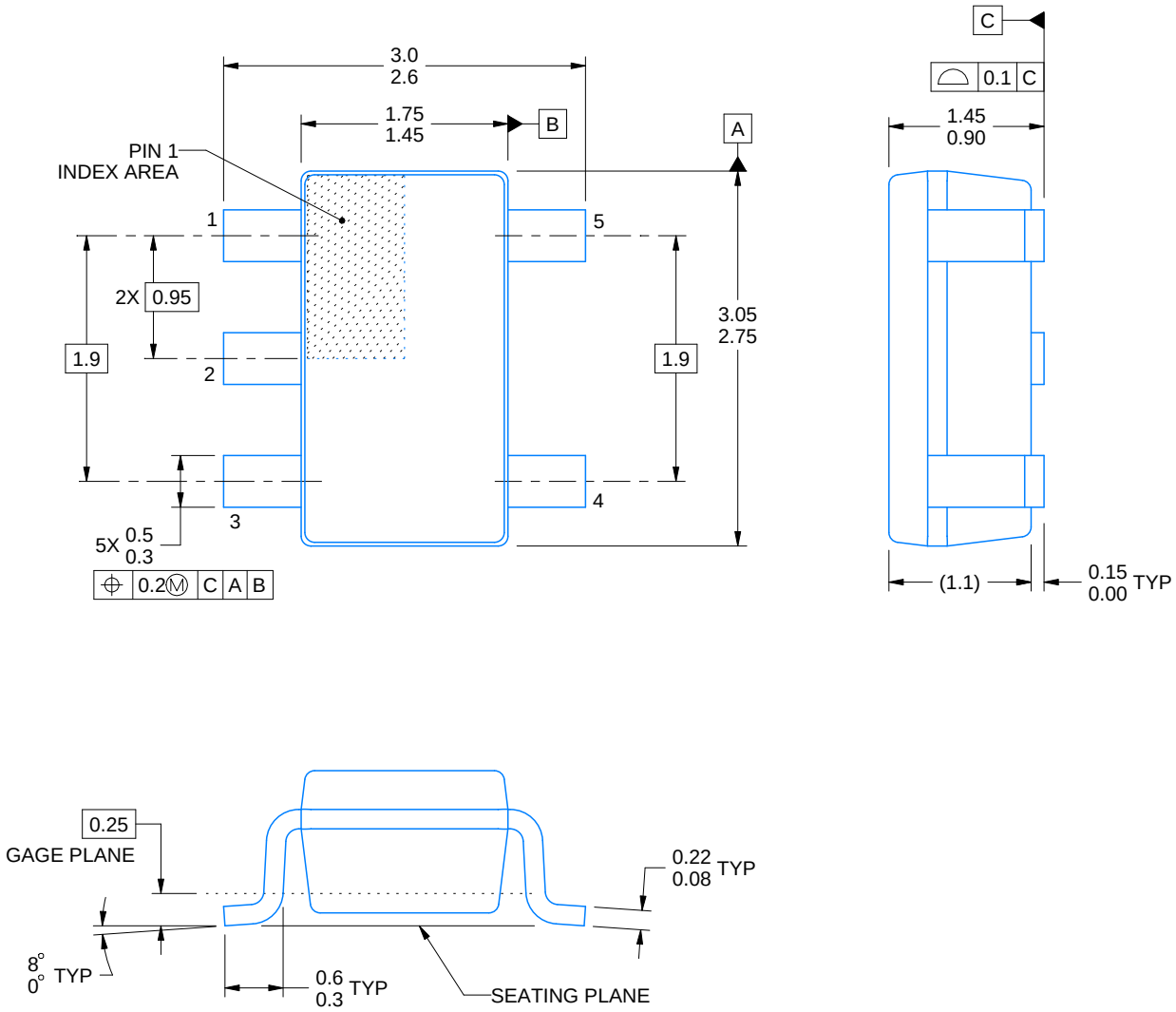
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA607IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
OPA607IDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
OPA607IDCKR	SC70	DCK	6	3000	213.0	191.0	35.0
OPA607IDCKT	SC70	DCK	6	250	213.0	191.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

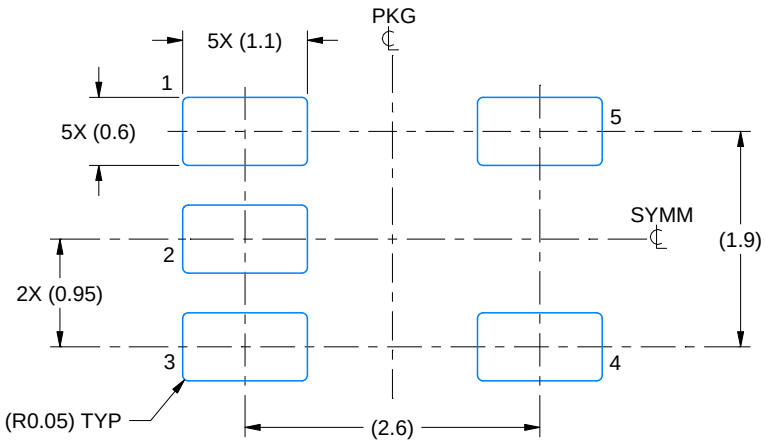
SMALL OUTLINE TRANSISTOR



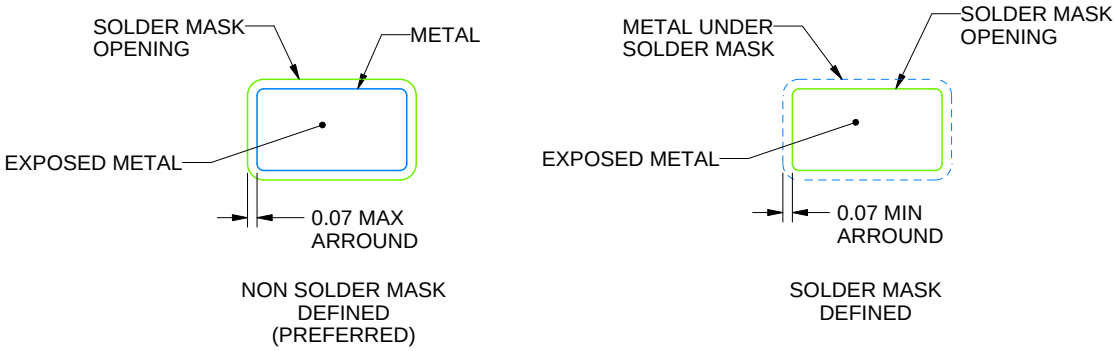
4214839/E 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

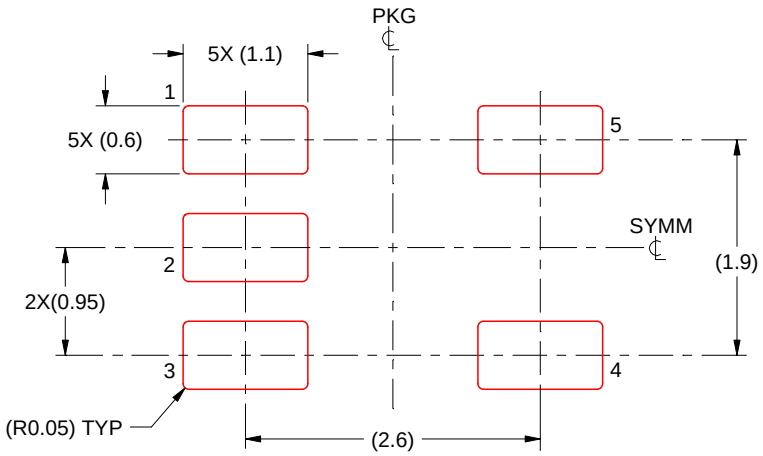


SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



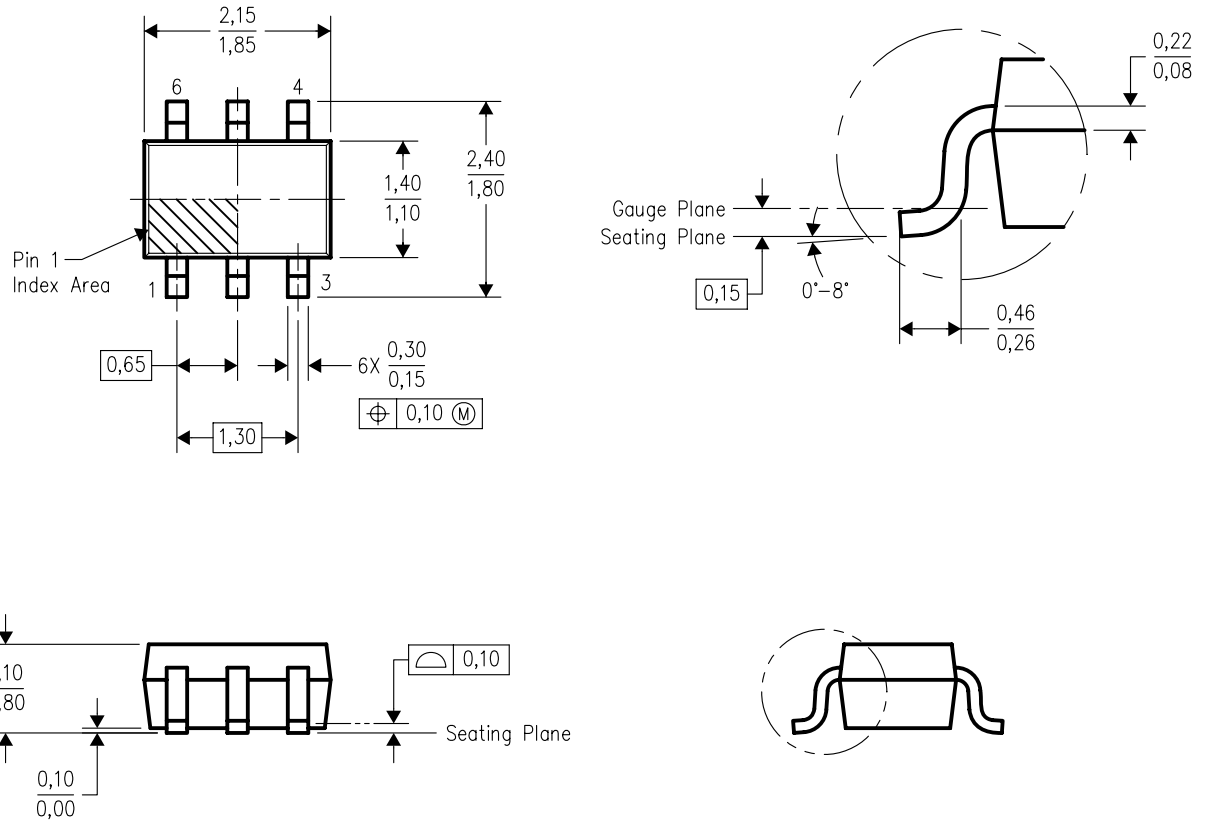
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

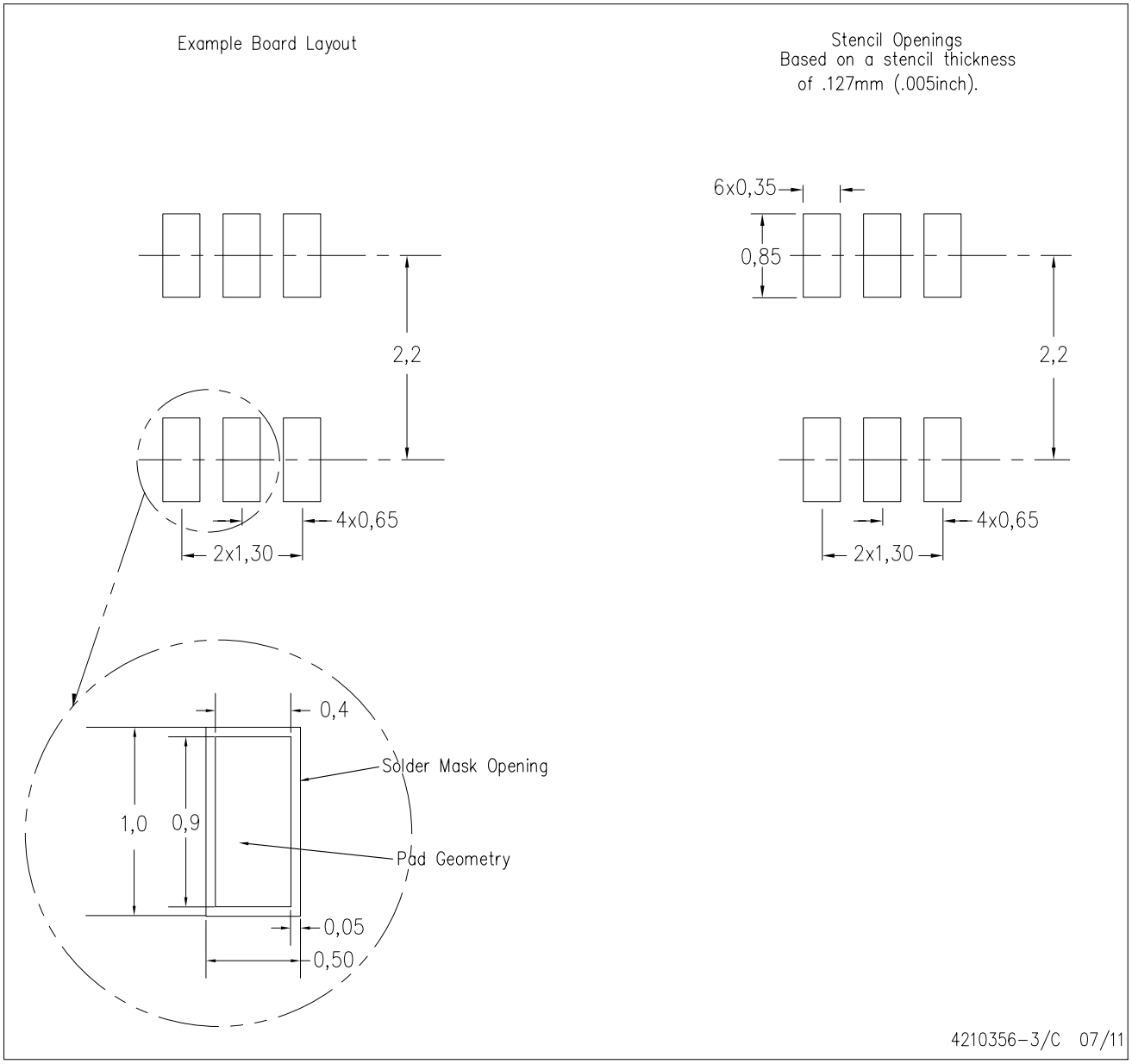
DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



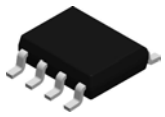
4093553–4/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

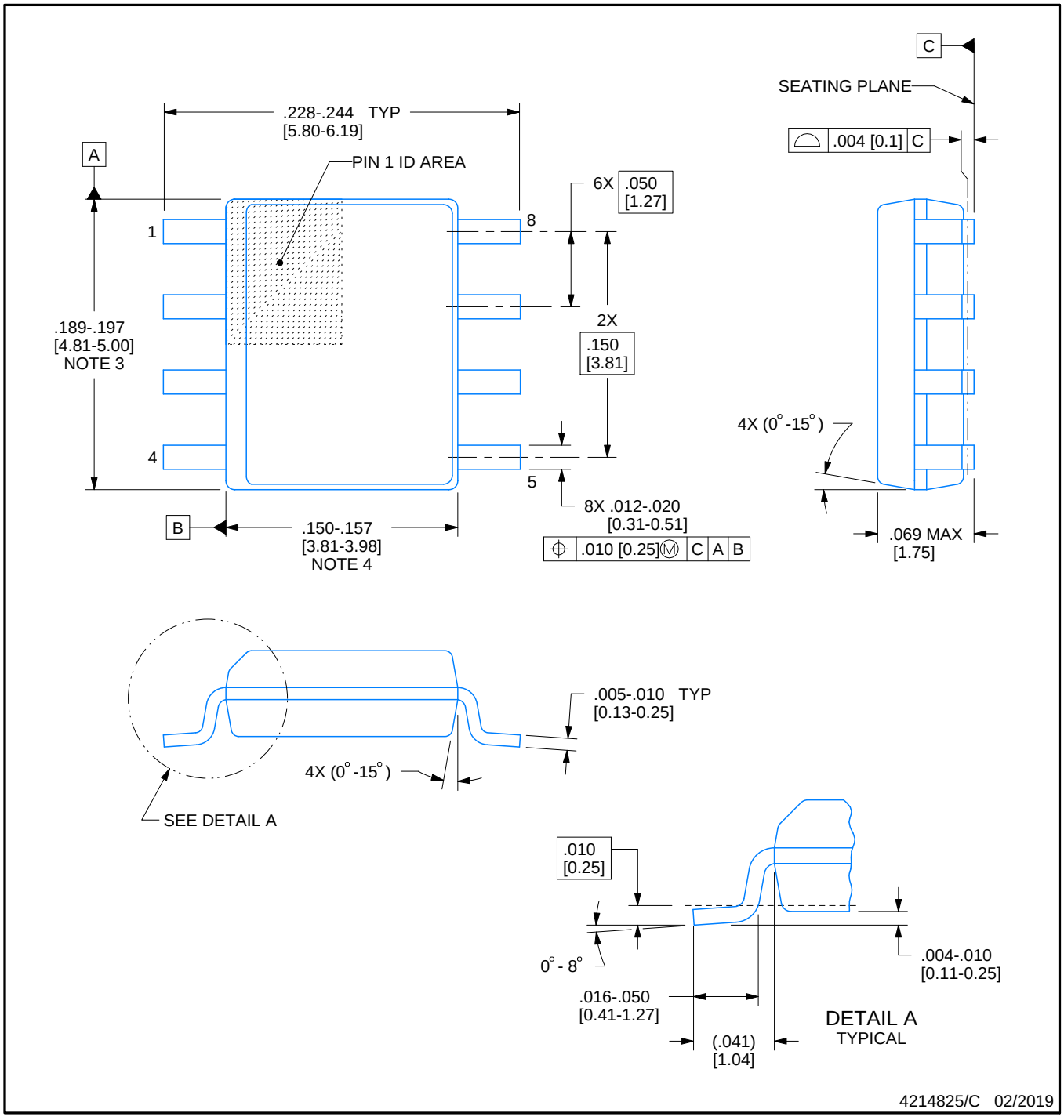


PACKAGE OUTLINE

D0008A

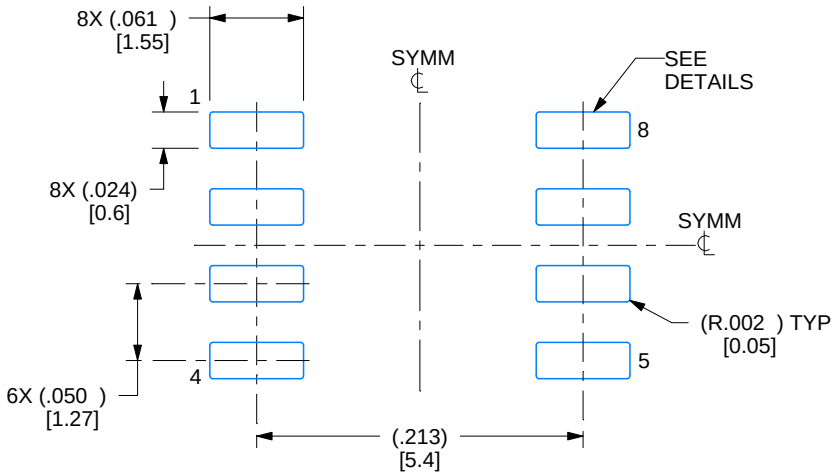
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

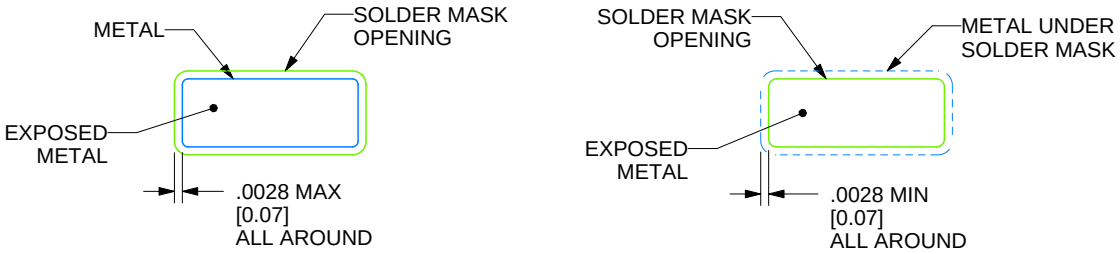


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

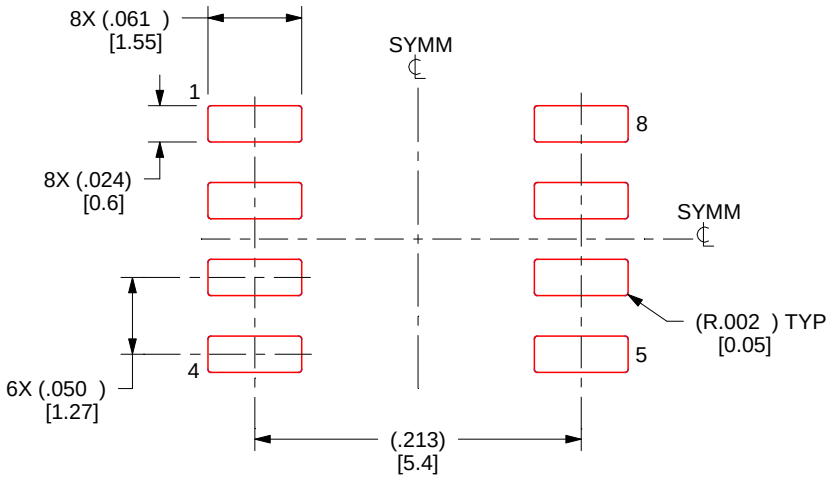
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated