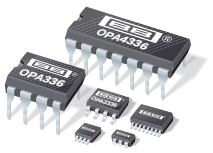
Burr-Brown Products
from Texas Instruments



OPA336
OPA2336
OPA4336

SBOS068C – JANUARY 1997 – REVISED JANUARY 2005

SINGLE-SUPPLY, *micro*Power CMOS OPERATIONAL AMPLIFIERS
*micro*Amplifier™ Series

FEATURES

- SINGLE-SUPPLY OPERATION
- RAIL-TO-RAIL OUTPUT (within 3mV)
- *micro*POWER: I_Q = 20μA/Amplifier
- *micro*SIZE PACKAGES
- LOW OFFSET VOLTAGE: 125μV max
- SPECIFIED FROM V_S = 2.3V to 5.5V
- SINGLE, DUAL, AND QUAD VERSIONS

APPLICATIONS

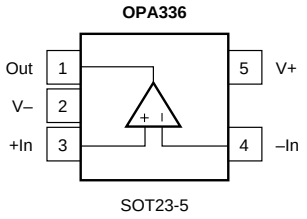
- BATTERY-POWERED INSTRUMENTS
- PORTABLE DEVICES
- HIGH-IMPEDANCE APPLICATIONS
- PHOTODIODE PRE-AMPS
- PRECISION INTEGRATORS
- MEDICAL INSTRUMENTS
- TEST EQUIPMENT

DESCRIPTION

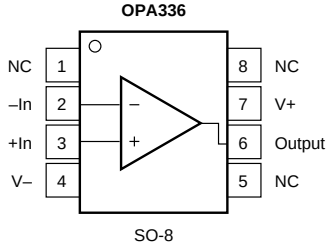
OPA336 series *micro*Power CMOS operational amplifiers are designed for battery-powered applications. They operate on a single supply with operation as low as 2.1V. The output is rail-to-rail and swings to within 3mV of the supplies with a 100kΩ load. The common-mode range extends to the negative supply—ideal for single-supply applications. Single, dual, and quad versions have identical specifications for maximum design flexibility.

In addition to small size and low quiescent current (20μA/amplifier), they feature low offset voltage (125μV max), low input bias current (1pA), and high open-loop gain (115dB). Dual and quad designs feature completely independent circuitry for lowest crosstalk and freedom from interaction.

OPA336 packages are the tiny SOT23-5 surface mount and SO-8 surface-mount. OPA2336 come in the miniature MSOP-8 surface-mount, SO-8 surface-mount, and DIP-8 packages. The OPA4336 package is the space-saving SSOP-16 surface-mount. All are specified from –40°C to +85°C and operate from –55°C to +125°C. A macromodel is available for download (at www.ti.com) for design analysis.

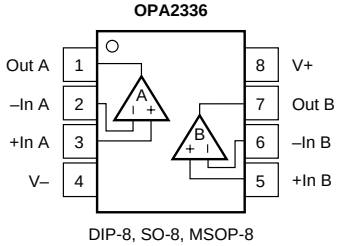


SOT23-5

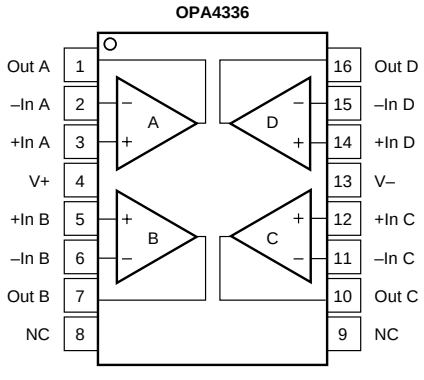


SO-8

NC = No Connection



DIP-8, SO-8, MSOP-8



SSOP-16

NC = No Connection

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1997-2005, Texas Instruments Incorporated

PACKAGE/ORDERING INFORMATION[1]

PRODUCT	PACKAGE-LEAD	PACKAGE DRAWING DESIGNATOR	PACKAGE MARKING
Single			
OPA336N	SOT23-5	DBV	A36[2]
OPA336NA	SOT23-5	DBV	A36[2]
OPA336NJ	SOT23-5	DBV	J36
OPA336U	SO-8 Surface-Mount	D	OPA336U
OPA336UA	SO-8 Surface-Mount	D	OPA336UA
OPA336UJ	SO-8 Surface-Mount	D	OPA336UJ
Dual			
OPA2336E	MSOP-8 Surface-Mount	DGK	B36[2]
OPA2336EA	MSOP-8 Surface-Mount	DGK	B36[2]
OPA2336P	DIP-8	P	OPA2336P
OPA2336PA	DIP-8	P	OPA2336PA
OPA2336U	SO-8 Surface-Mount	D	OPA2336U
OPA2336UA	SO-8 Surface-Mount	D	OPA2336UA
Quad			
OPA4336EA	SSOP-16 Surface-Mount	DBQ	OPA4336EA

NOTES: (1) For the most current package and ordering information, see the package option addendum at the end of this data sheet. (2) Grade will be marked on the Reel.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	7.5V
Signal Input Terminals, Voltage[2]	(V–) –0.3V to (V+) +0.3V
Current[2]	10mA
Output Short-Circuit[3]	Continuous
Operating Temperature	–55°C to +125°C
Storage Temperature	–55°C to +125°C
Junction Temperature	150°C
Lead Temperature (soldering, 10s)	300°C
ESD Rating:	
Charged Device Model, OPA336 NJ and UJ only (CDM)[4]	1000V
Human Body Model (HBM)[4]	500V
Machine Model (MM)[4]	100V

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only. Functional operation of the device at these conditions, or beyond the specified operating conditions, is not implied. (2) Input terminals are diode-clamped to the power supply rails. Input signals that can swing more than 0.3V beyond the supply rails should be current-limited to 10mA or less. (3) Short-circuit to ground, one amplifier per package. (4) OPA336 NJ and UJ have been tested to CDM of 1000V. All other previous package versions have been tested using HBM and MM. Results are shown.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ELECTRICAL CHARACTERISTICS: V_S = 2.3V to 5.5V

Boldface limits apply over the specified temperature range, T_A = –40°C to +85°C.

At T_A = +25°C, V_S = +5V, and R_L = 25kΩ connected to V_S/2, unless otherwise noted.

PARAMETER		CONDITION	OPA336N, U OPA2336E, P, U			OPA336NA, UA OPA2336EA, PA, UA OPA4336EA			OPA336NJ, UJ			UNITS
			MIN	TYP[1]	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE												
Input Offset Voltage	V_{OS}			±60	±125		*	±500		±500	±2500	µV
vs Temperature	dV_{OS}/dT			**±1.5**			*			*		**µV/°C**
vs Power Supply	PSRR	V_S = 2.3V to 5.5V		25	100		*	*	*	*	*	µV/V
Over Temperature		V_S = 2.3V to 5.5V			**130**			*	*		*	**µV/V**
Channel Separation, dc				0.1			*			*		µV/V
INPUT BIAS CURRENT												
Input Bias Current	I_B			±1	±10		*	*		*	*	pA
Over Temperature					**±60**			*			*	**pA**
Input Offset Current	I_{OS}			±1	±10		*	*		*	*	pA
NOISE												
Input Voltage Noise, f = 0.1 to 10Hz				3			*			*		µVp-p
Input Voltage Noise Density, f = 1kHz	e_n			40			*			*		$nV/\sqrt{Hz}$
Current Noise Density, f = 1kHz	i_n			30			*			*		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE												
Common-Mode Voltage Range	V_{CM}		–0.2		(V+) –1	*		*	*		*	V
Common-Mode Rejection Ratio	CMRR	–0.2V < V_{CM} < (V+) –1V	80	90		76	86		76	86		dB
Over Temperature		–0.2V < V_{CM} < (V+) –1V	**76**			**74**			**74**			**dB**
INPUT IMPEDANCE												
Differential				10^{13} || 2			*			*		Ω || pF
Common-Mode				10^{13} || 4			*			*		Ω || pF
OPEN-LOOP GAIN												
Open-Loop Voltage Gain	A_{OL}	R_L = 25kΩ, 100mV < V_O < (V+) – 100mV	100	115		90	*		90	*		dB
Over Temperature		R_L = 25kΩ, 100mV < V_O < (V+) – 100mV	**100**			**90**			**90**			**dB**
		R_L = 5kΩ, 500mV < V_O < (V+) – 500mV	90	106		*	*		*	*		dB
Over Temperature		R_L = 5kΩ, 500mV < V_O < (V+) – 500mV	**90**			*			*			**dB**
FREQUENCY RESPONSE												
Gain-Bandwidth Product	GBW	V_S = 5V, G = 1		100			*			*		kHz
Slew Rate	SR	V_S = 5V, G = 1		0.03			*			*		V/µs
Overload Recovery Time		V_{IN} • G = V_S		100			*			*		µs
OUTPUT												
Voltage Output Swing from Rail[2]		R_L = 100kΩ, A_{OL} ≥ 70dB		3			*			*		mV
		R_L = 25kΩ, A_{OL} ≥ 90dB		20	100		*	*		*	*	mV
Over Temperature		R_L = 25kΩ, A_{OL} ≥ 90dB			**100**			*			*	**mV**
		R_L = 5kΩ, A_{OL} ≥ 90dB		70	500		*	*		*	*	mV
Over Temperature		R_L = 5kΩ, A_{OL} ≥ 90dB			**500**			*			*	**mV**
Short-Circuit Current	I_{SC}			±5			*			*		mA
Capacitive Load Drive	C_{LOAD}			See Text			*			*		pF
POWER SUPPLY												
Specified Voltage Range	V_S		2.3		5.5	*		*	*		*	V
Minimum Operating Voltage				2.1			*			*		V
Quiescent Current (per amplifier)	I_Q	I_O = 0		20	32		*	*		23	38	µA
Over Temperature		I_O = 0			**36**			*			**42**	**µA**
TEMPERATURE RANGE												
Specified Range			–40		+85	*		*	*		*	°C
Operating Range			–55		+125	*		*	*		*	°C
Storage Range			–55		+125	*		*	*		*	°C
Thermal Resistance	θ_{JA}											
SOT-23-5 Surface-Mount				200			*			*		°C/W
MSOP-8 Surface-Mount				150			*					°C/W
SO-8 Surface-Mount				150			*			*		°C/W
DIP-8				100			*					°C/W
SSOP-16 Surface-Mount				100			*					°C/W
DIP-14				80			*					°C/W

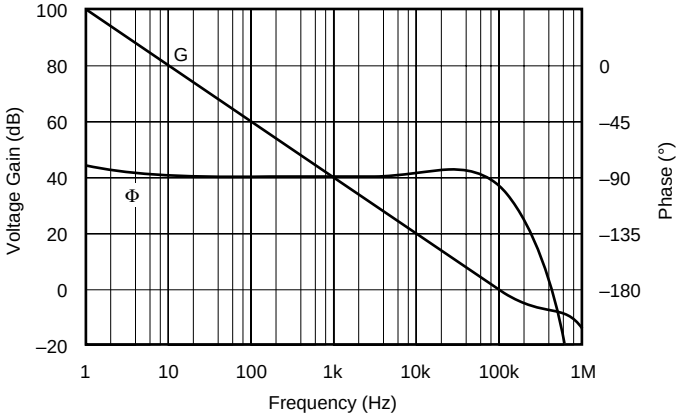
*Specifications same as OPA2336E, P, U.

NOTES: (1) V_S = +5V. (2) Output voltage swings are measured between the output and positive and negative power-supply rails.

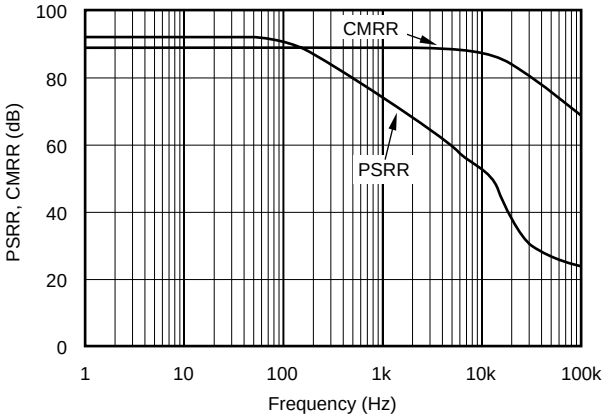
TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = +5V, and R_L = 25kΩ connected to V_S/2, unless otherwise noted.

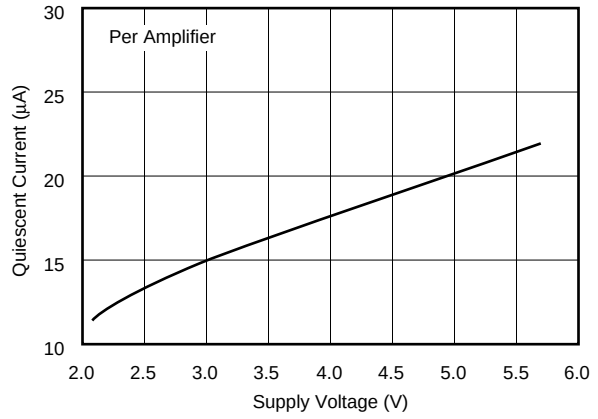
OPEN-LOOP GAIN/PHASE vs FREQUENCY



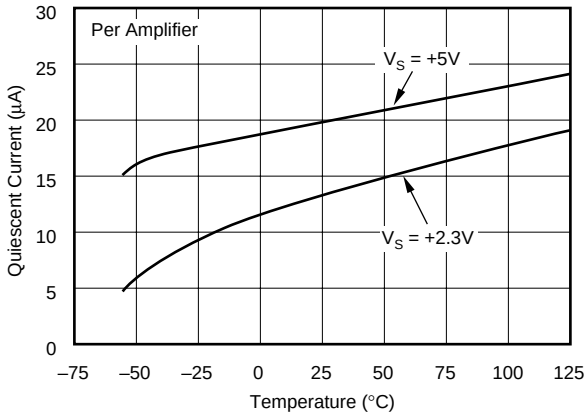
POWER-SUPPLY and COMMON-MODE REJECTION RATIO vs FREQUENCY



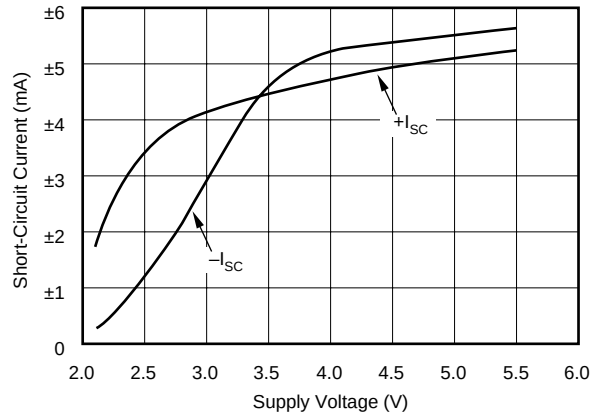
QUIESCENT CURRENT vs SUPPLY VOLTAGE



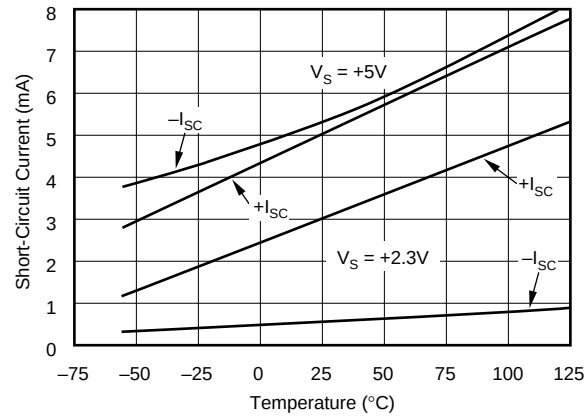
QUIESCENT CURRENT vs TEMPERATURE



SHORT-CIRCUIT CURRENT vs SUPPLY VOLTAGE



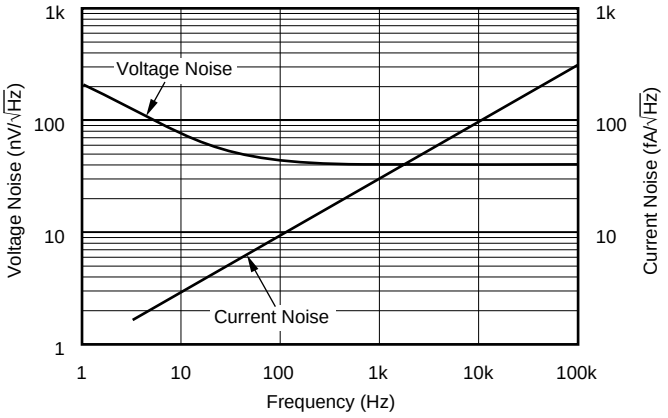
SHORT-CIRCUIT CURRENT vs TEMPERATURE



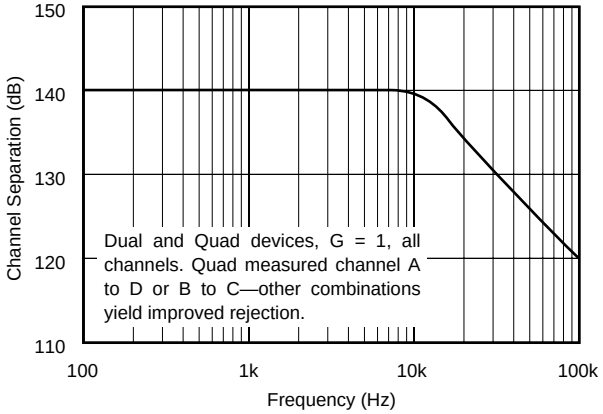
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = +5V, and R_L = 25kΩ connected to V_S/2, unless otherwise noted.

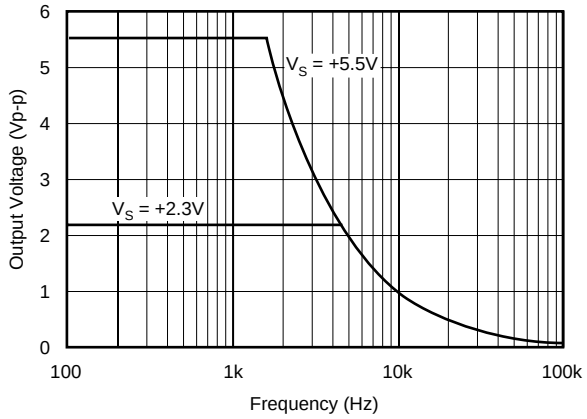
INPUT VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY



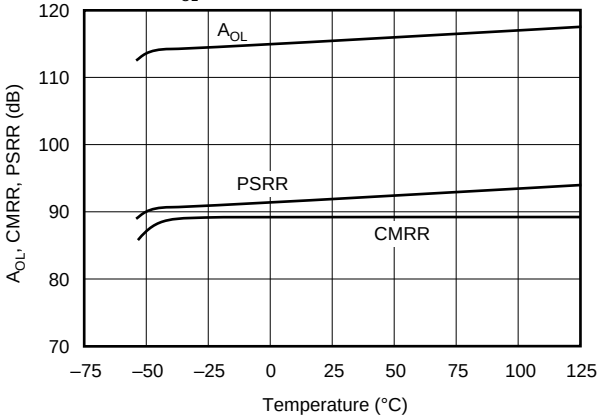
CHANNEL SEPARATION vs FREQUENCY



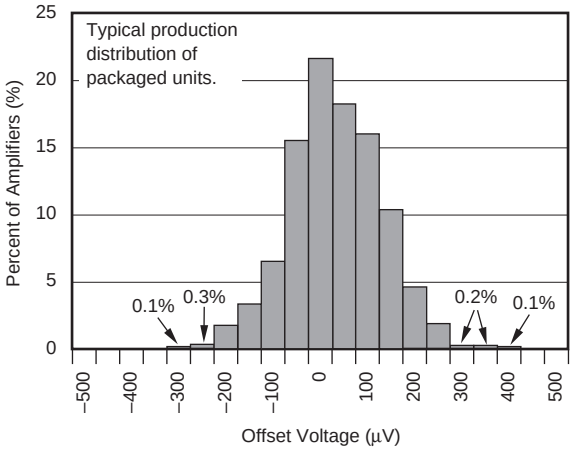
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



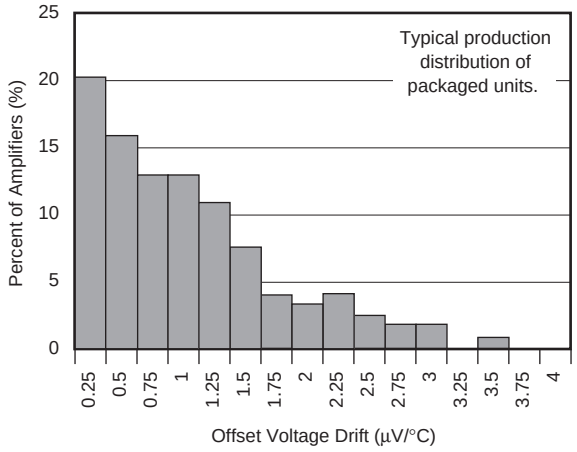
A_{OL}, CMRR, PSRR vs TEMPERATURE



OFFSET VOLTAGE PRODUCTION DISTRIBUTION



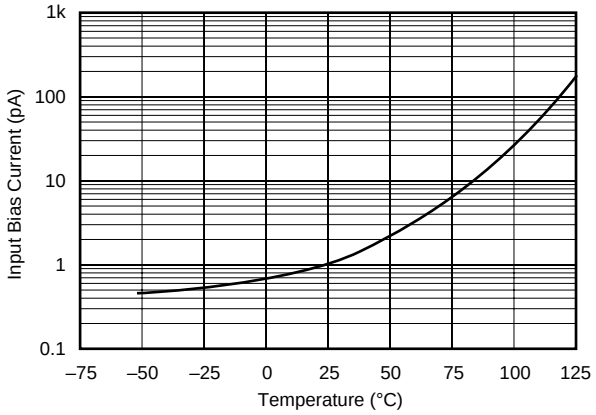
OFFSET VOLTAGE DRIFT MAGNITUDE PRODUCTION DISTRIBUTION



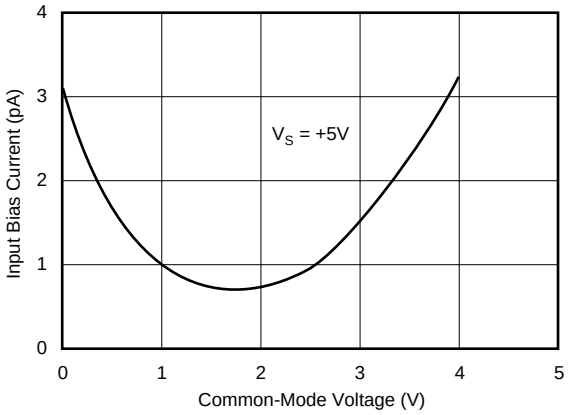
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = +5V, and R_L = 25kΩ connected to V_S/2, unless otherwise noted.

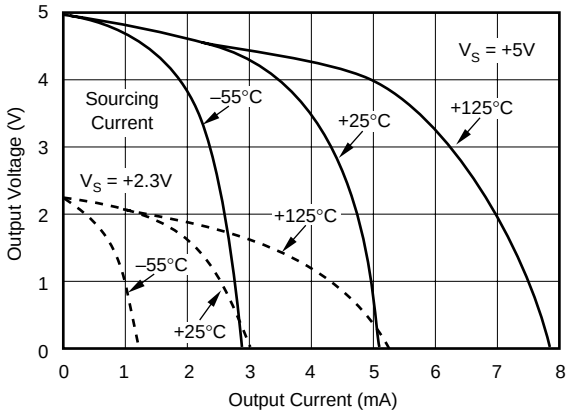
INPUT BIAS CURRENT vs TEMPERATURE



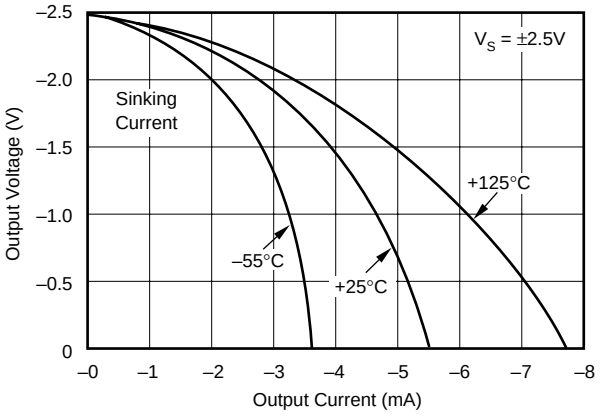
INPUT BIAS CURRENT
vs INPUT COMMON-MODE VOLTAGE



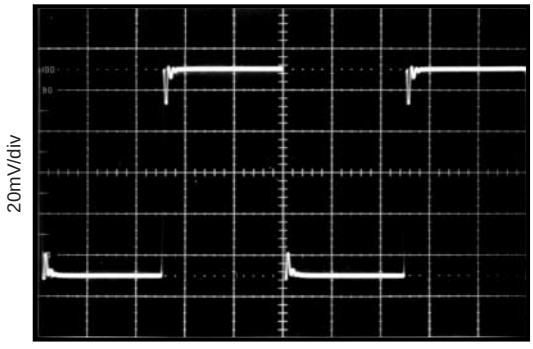
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



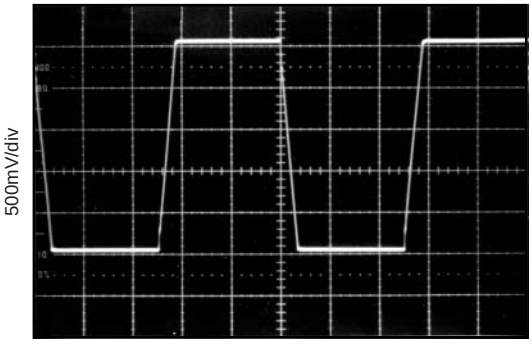
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



SMALL-SIGNAL STEP RESPONSE
G = 1, C_L = 200pF, V_S = +5V



LARGE-SIGNAL STEP RESPONSE
G = 1, C_L = 620pF, V_S = +5V



APPLICATIONS INFORMATION

OPA336 series op amps are fabricated on a state-of-the-art 0.6 micron CMOS process. They are unity-gain stable and suitable for a wide range of general-purpose applications. Power-supply pins should be bypassed with 0.01µF ceramic capacitors. OPA336 series op amps are protected against reverse battery voltages.

OPERATING VOLTAGE

OPA336 series op amps can operate from a +2.1V to +5.5V single supply with excellent performance. Most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in the typical characteristics. OPA336 series op amps are fully specified for operation from +2.3V to +5.5V; a single limit applies over the supply range. In addition, many parameters are ensured over the specified temperature range, –40°C to +85°C.

INPUT VOLTAGE

The input common-mode range of OPA336 series op amps extends from (V–) – 0.2V to (V+) – 1V. For normal operation, inputs should be limited to this range. The absolute maximum input voltage is 300mV beyond the supplies. Thus, inputs greater than the input common-mode range but less than maximum input voltage, while not valid, will not cause any damage to the op amp. Furthermore, the inputs may go beyond the power supplies without phase inversion, as shown in Figure 1, unlike some other op amps.

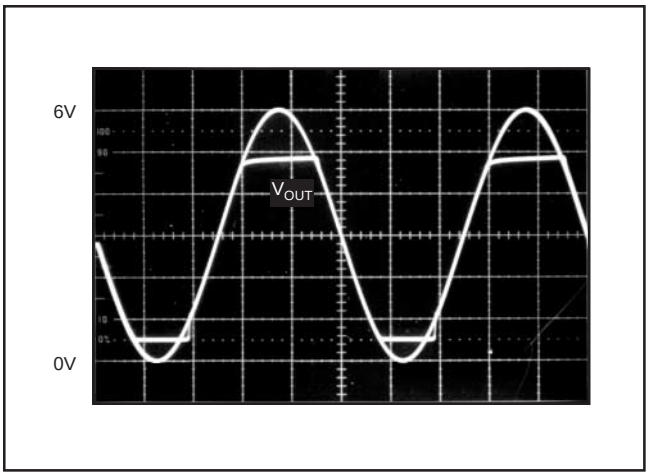


FIGURE 1. No Phase Inversion with Inputs Greater than the Power-Supply Voltage.

Normally, input bias current is approximately 1pA. However, input voltages exceeding the power supplies can cause excessive current to flow in or out of the input pins. Momentary voltages greater than the power supply can be tolerated as long as the current on the input pins is limited to 10mA. This is easily accomplished with an input resistor, as shown in Figure 2.

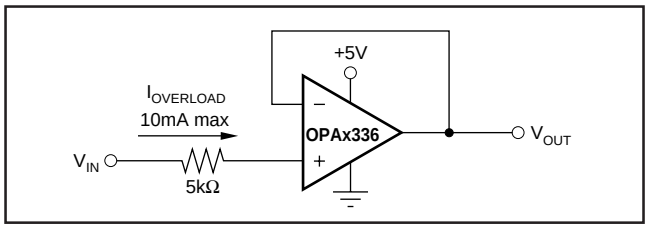


FIGURE 2. Input Current Protection for Voltages Exceeding the Supply Voltage.

CAPACITIVE LOAD AND STABILITY

OPA336 series op amps can drive a wide range of capacitive loads. However, all op amps under certain conditions may become unstable. Op-amp configuration, gain, and load value are just a few of the factors to consider when determining stability.

When properly configured, OPA336 series op amps can drive approximately 10,000pF. An op amp in unity-gain configuration is the most vulnerable to capacitive load. The capacitive load reacts with the op amp's output resistance, along with any additional load resistance, to create a pole in the response which degrades the phase margin. In unity gain, OPA336 series op amps perform well with a pure capacitive load up to about 300pF. Increasing gain enhances the amplifier's ability to drive loads beyond this level.

One method of improving capacitive load drive in the unity-gain configuration is to insert a 50Ω to 100Ω resistor inside the feedback loop, as shown in Figure 3. This reduces ringing with large capacitive loads while maintaining DC

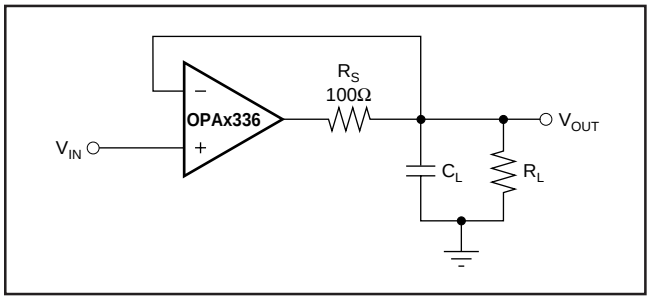


FIGURE 3. Series Resistor in Unity-Gain Configuration Improves Capacitive Load Drive.

accuracy. For example, with R_L = 25kΩ, OPA336 series op amps perform well with capacitive loads in excess of 1000pF, as shown in Figure 4. Without R_S, capacitive load drive is typically 350pF for these conditions, as shown in Figure 5.

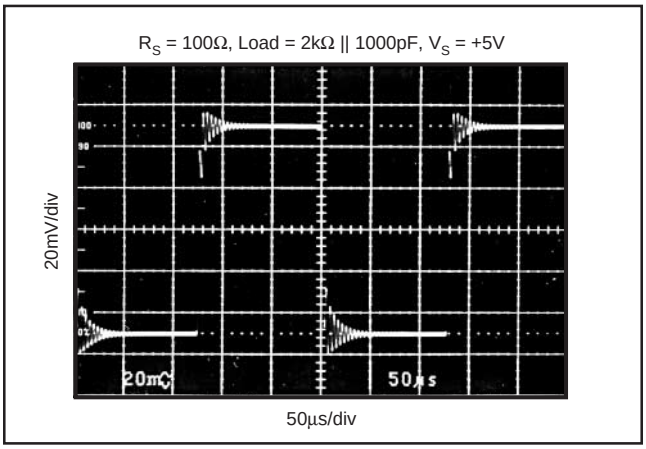


FIGURE 4. Small-Signal Step Response Using Series Resistor to Improve Capacitive Load Drive.

Alternatively, the resistor may be connected in series with the output outside of the feedback loop. However, if there is a resistive load parallel to the capacitive load, it and the series resistor create a voltage divider. This introduces a Direct Current (DC) error at the output; however, this error may be insignificant. For instance, with R_L = 100kΩ and R_S = 100Ω, there is only about a 0.1% error at the output.

Figure 5 shows the recommended operating regions for the OPA336. Decreasing the load resistance generally improves capacitive load drive. Figure 5 also illustrates how stability differs depending on where the resistive load is connected. With G = +1 and R_L = 10kΩ connected to V_S/2, the OPA336 can typically drive 500pF. Connecting the same load to ground improves capacitive load drive to 1000pF.

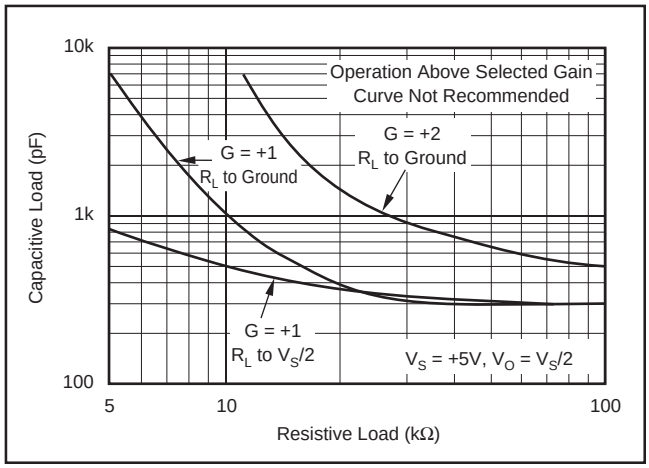


FIGURE 5. Stability—Capacitive Load vs Resistive Load.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HPA00779NA/3K	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		A36	Samples
OPA2336E/250	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	B36	Samples
OPA2336E/250G4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	B36	Samples
OPA2336E/2K5	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	B36	Samples
OPA2336E/2K5G4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	B36	Samples
OPA2336EA/250	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	B36	Samples
OPA2336EA/250G4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	B36	Samples
OPA2336EA/2K5	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	B36	Samples
OPA2336EA/2K5G4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	B36	Samples
OPA2336P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	OPA2336P	Samples
OPA2336PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	OPA2336P A	Samples
OPA2336PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	OPA2336P A	Samples
OPA2336PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	OPA2336P	Samples
OPA2336U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2336U	Samples
OPA2336U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2336U	Samples
OPA2336U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2336U	Samples
OPA2336UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2336U	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										A	
OPA2336UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2336U A	Samples
OPA2336UA/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2336U A	Samples
OPA2336UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2336U A	Samples
OPA2336UG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2336U	Samples
OPA336N/250	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		A36	Samples
OPA336N/250G4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		A36	Samples
OPA336N/3K	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		A36	Samples
OPA336N/3KG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		A36	Samples
OPA336NA/250	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		A36	Samples
OPA336NA/250G4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		A36	Samples
OPA336NA/3K	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		A36	Samples
OPA336NA/3KG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		A36	Samples
OPA336NJ/250	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	J36	Samples
OPA336NJ/250G4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	J36	Samples
OPA336NJ/3K	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	J36	Samples
OPA336NJ/3KG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	J36	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA336U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		OPA 336U	Samples
OPA336U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		OPA 336U	Samples
OPA336U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		OPA 336U	Samples
OPA336UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		OPA 336U A	Samples
OPA336UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		OPA 336U A	Samples
OPA336UA/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		OPA 336U A	Samples
OPA336UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		OPA 336U A	Samples
OPA336UG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		OPA 336U	Samples
OPA4336EA/250	ACTIVE	SSOP	DBQ	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4336EA	Samples
OPA4336EA/250G4	ACTIVE	SSOP	DBQ	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4336EA	Samples
OPA4336EA/2K5	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4336EA	Samples
OPA4336EA/2K5G4	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4336EA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA336 :

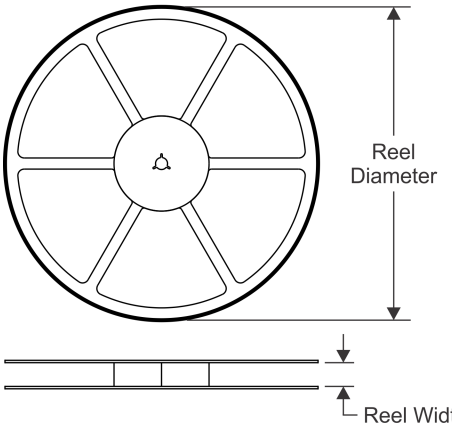
- Enhanced Product: OPA336-EP

NOTE: Qualified Version Definitions:

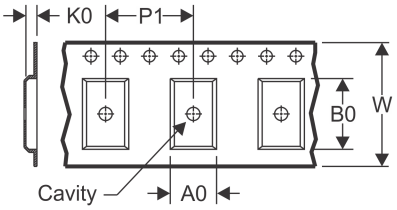
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

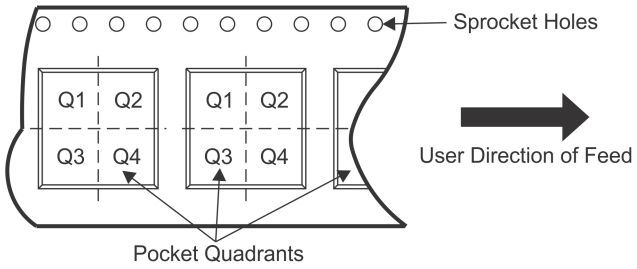


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

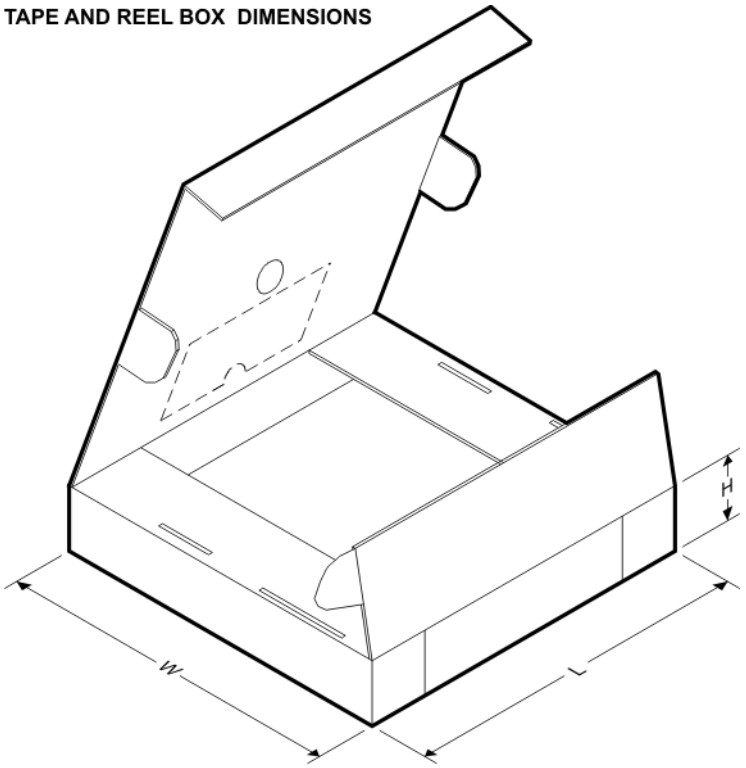


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2336E/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2336E/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2336EA/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2336EA/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2336U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2336UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA336N/250	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA336N/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA336N/3K	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA336NA/250	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA336NA/3K	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA336NA/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA336NJ/250	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA336NJ/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA336NJ/3K	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA336U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA336UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4336EA/250	SSOP	DBQ	16	250	180.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA4336EA/2K5	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

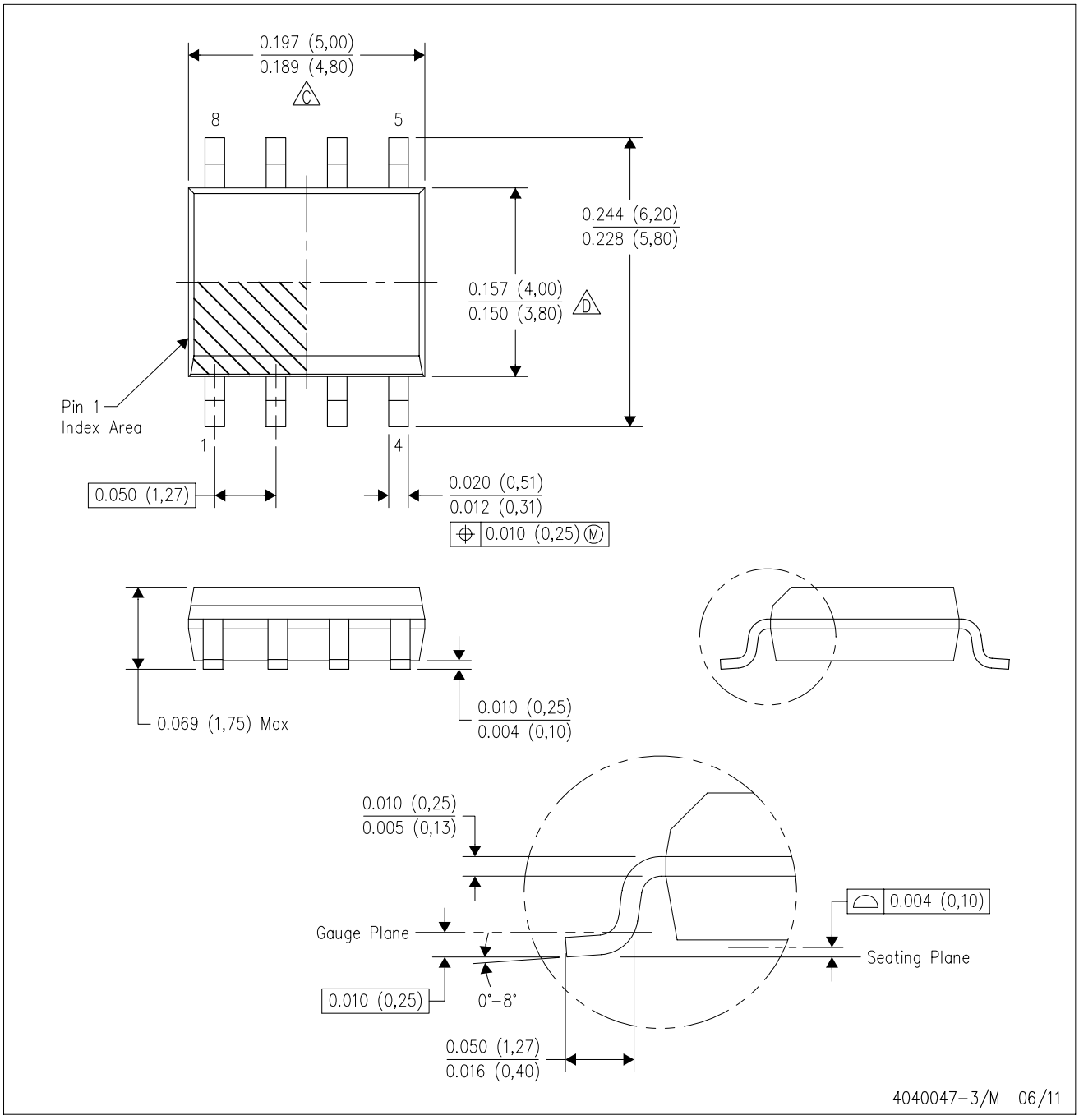


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2336E/250	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA2336E/2K5	VSSOP	DGK	8	2500	367.0	367.0	35.0
OPA2336EA/250	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA2336EA/2K5	VSSOP	DGK	8	2500	367.0	367.0	35.0
OPA2336U/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA2336UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA336N/250	SOT-23	DBV	5	250	180.0	180.0	18.0
OPA336N/3K	SOT-23	DBV	5	3000	203.0	203.0	35.0
OPA336N/3K	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA336NA/250	SOT-23	DBV	5	250	180.0	180.0	18.0
OPA336NA/3K	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA336NA/3K	SOT-23	DBV	5	3000	203.0	203.0	35.0
OPA336NJ/250	SOT-23	DBV	5	250	180.0	180.0	18.0
OPA336NJ/3K	SOT-23	DBV	5	3000	203.0	203.0	35.0
OPA336NJ/3K	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA336U/2K5	SOIC	D	8	2500	367.0	367.0	35.0

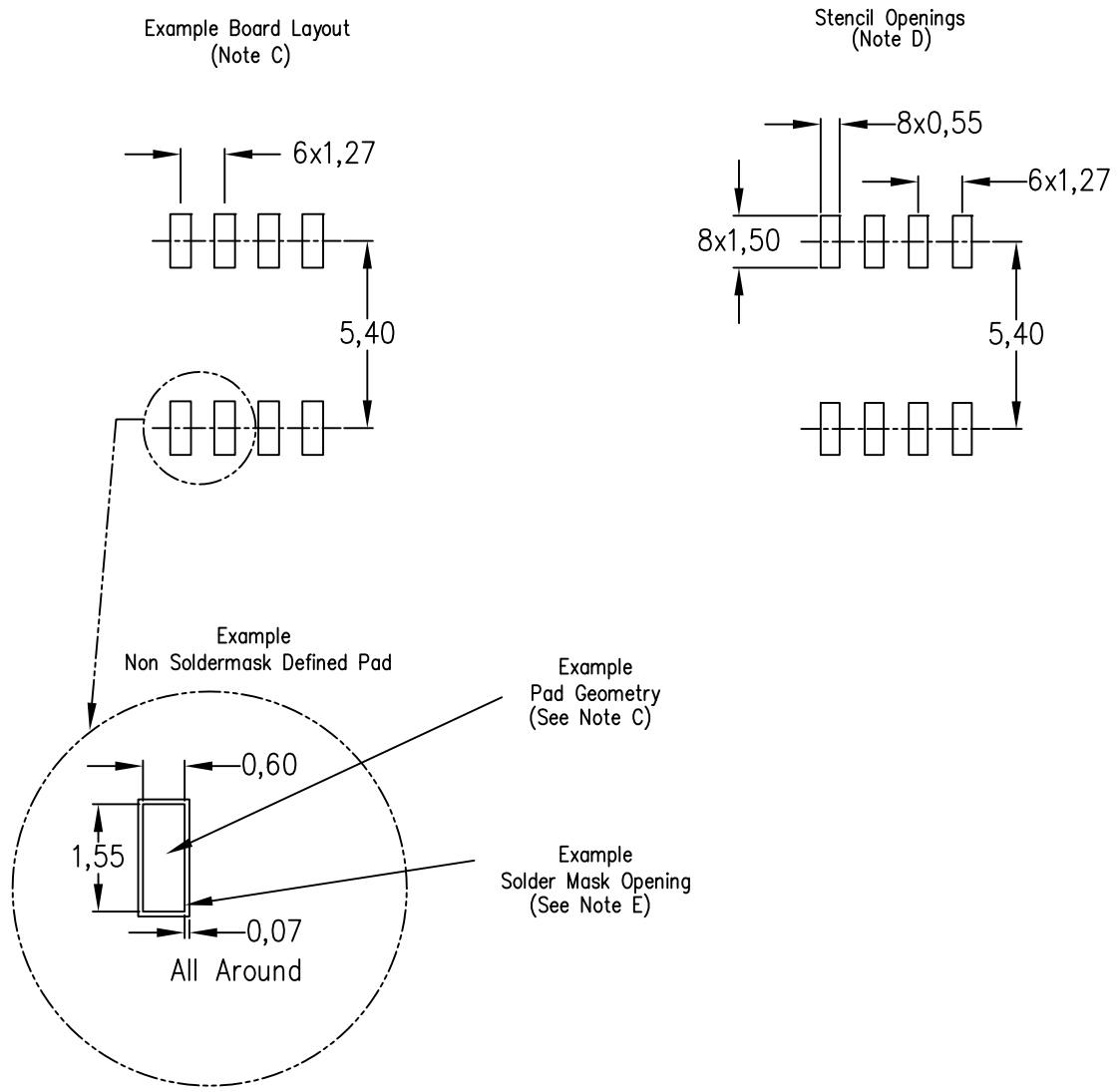
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA336UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA4336EA/250	SSOP	DBQ	16	250	210.0	185.0	35.0
OPA4336EA/2K5	SSOP	DBQ	16	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE

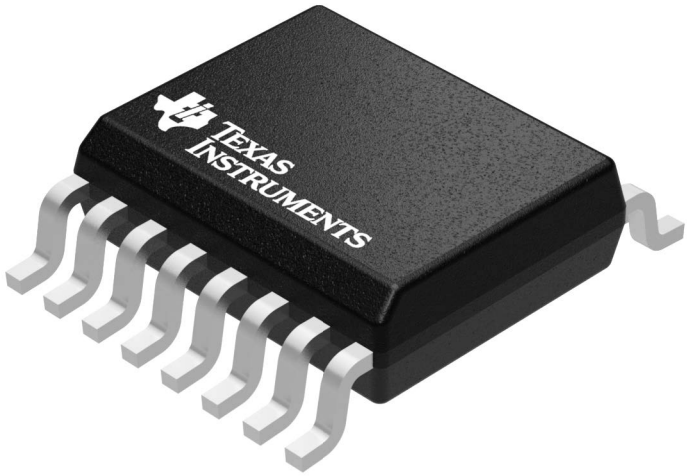


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

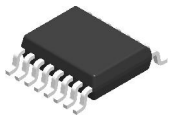
GENERIC PACKAGE VIEW

DBQ 16 SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

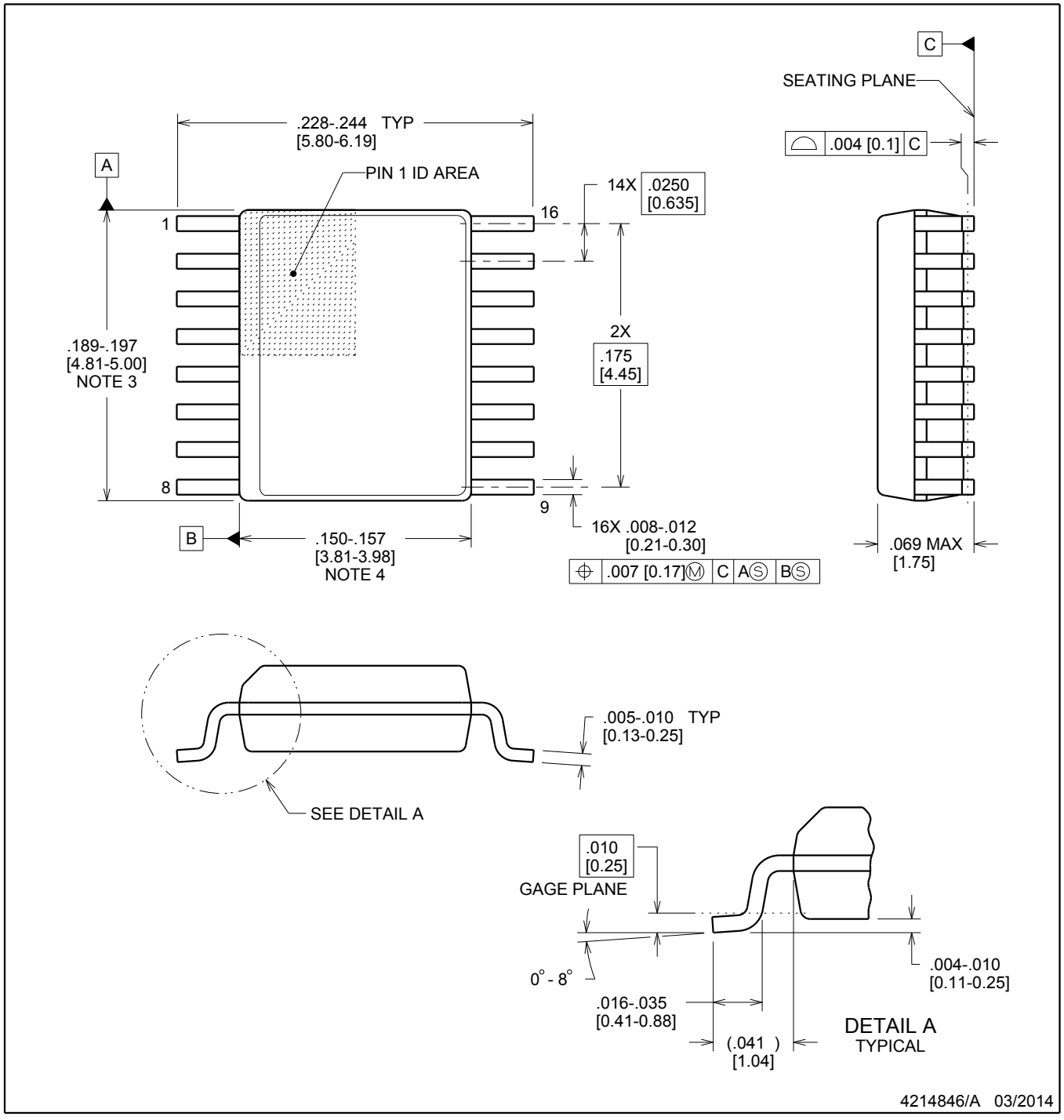


PACKAGE OUTLINE

DBQ0016A

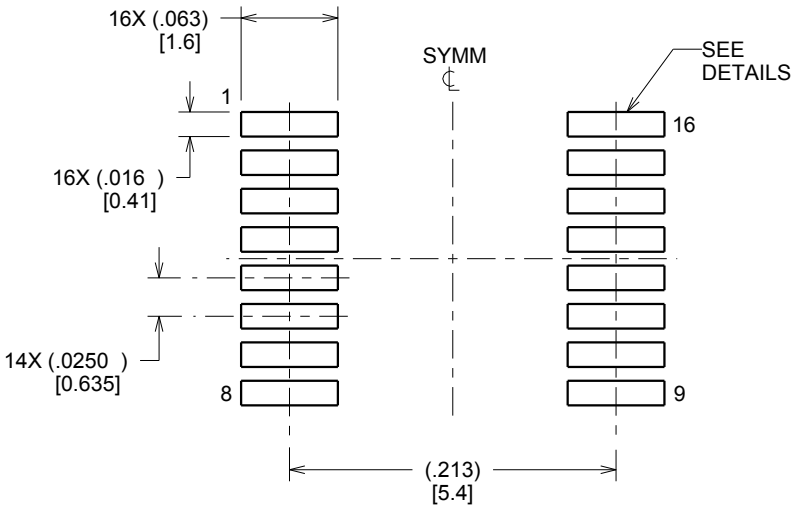
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

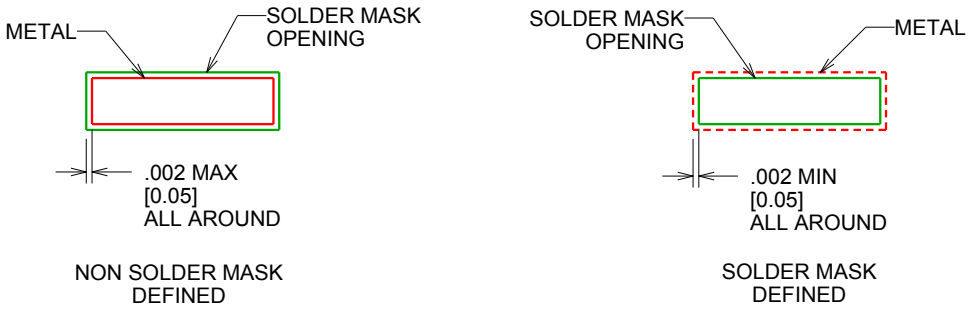


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

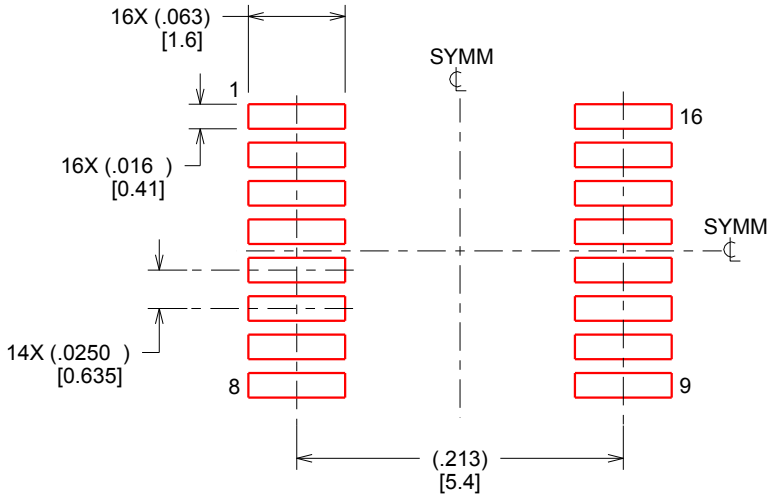
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



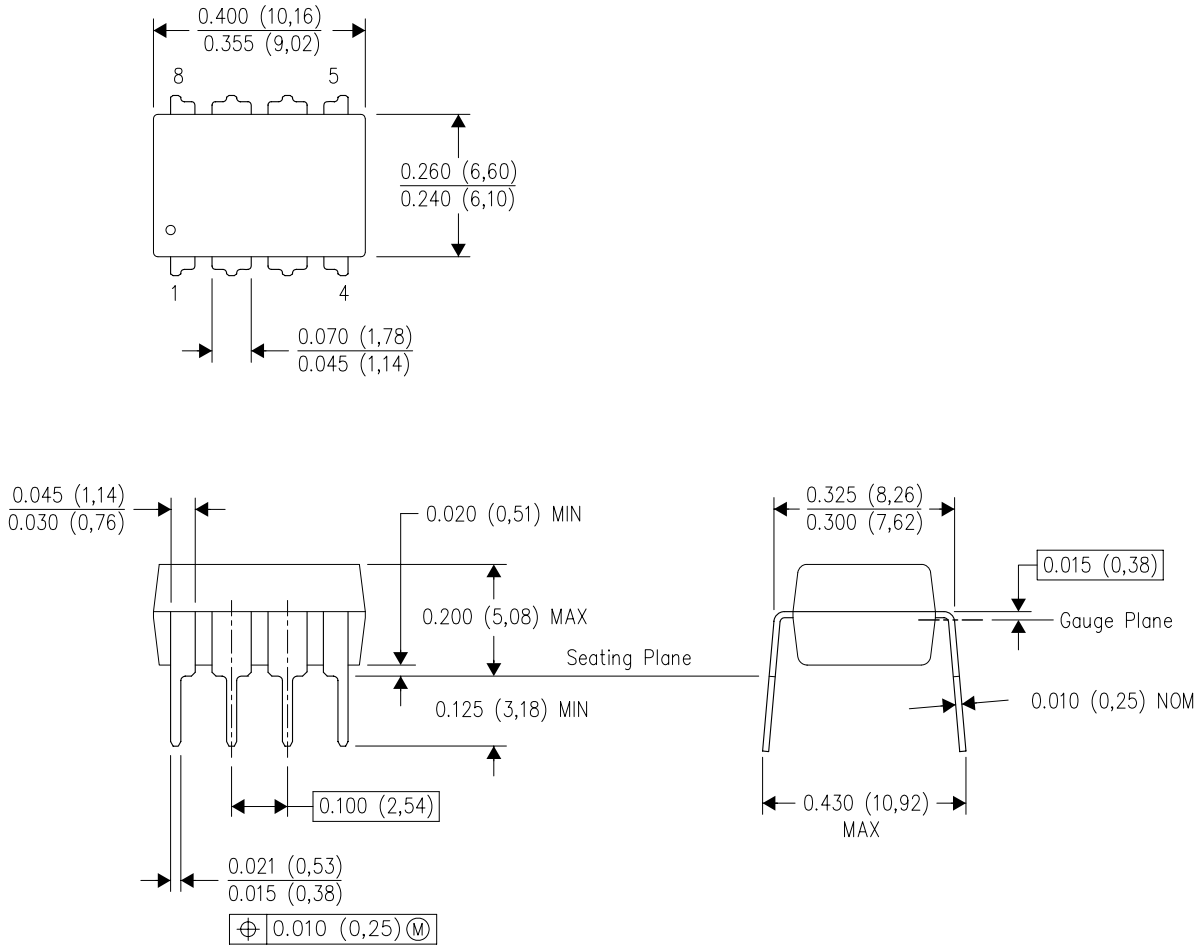
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

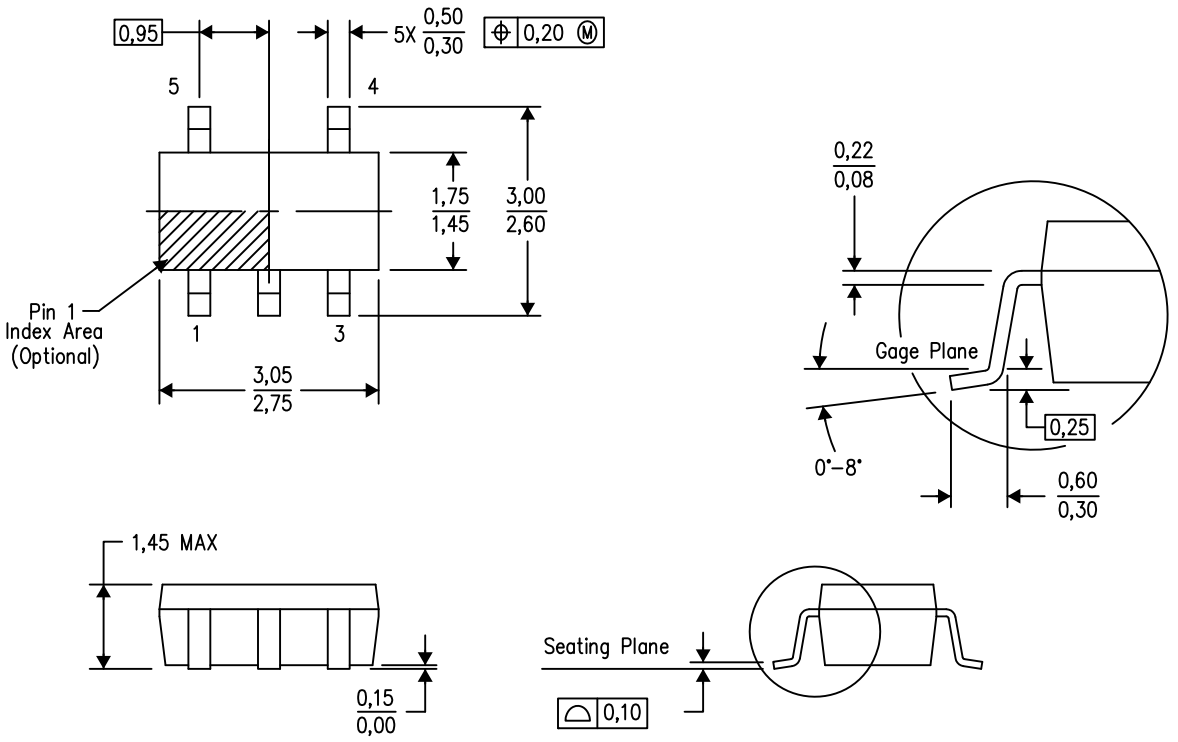
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

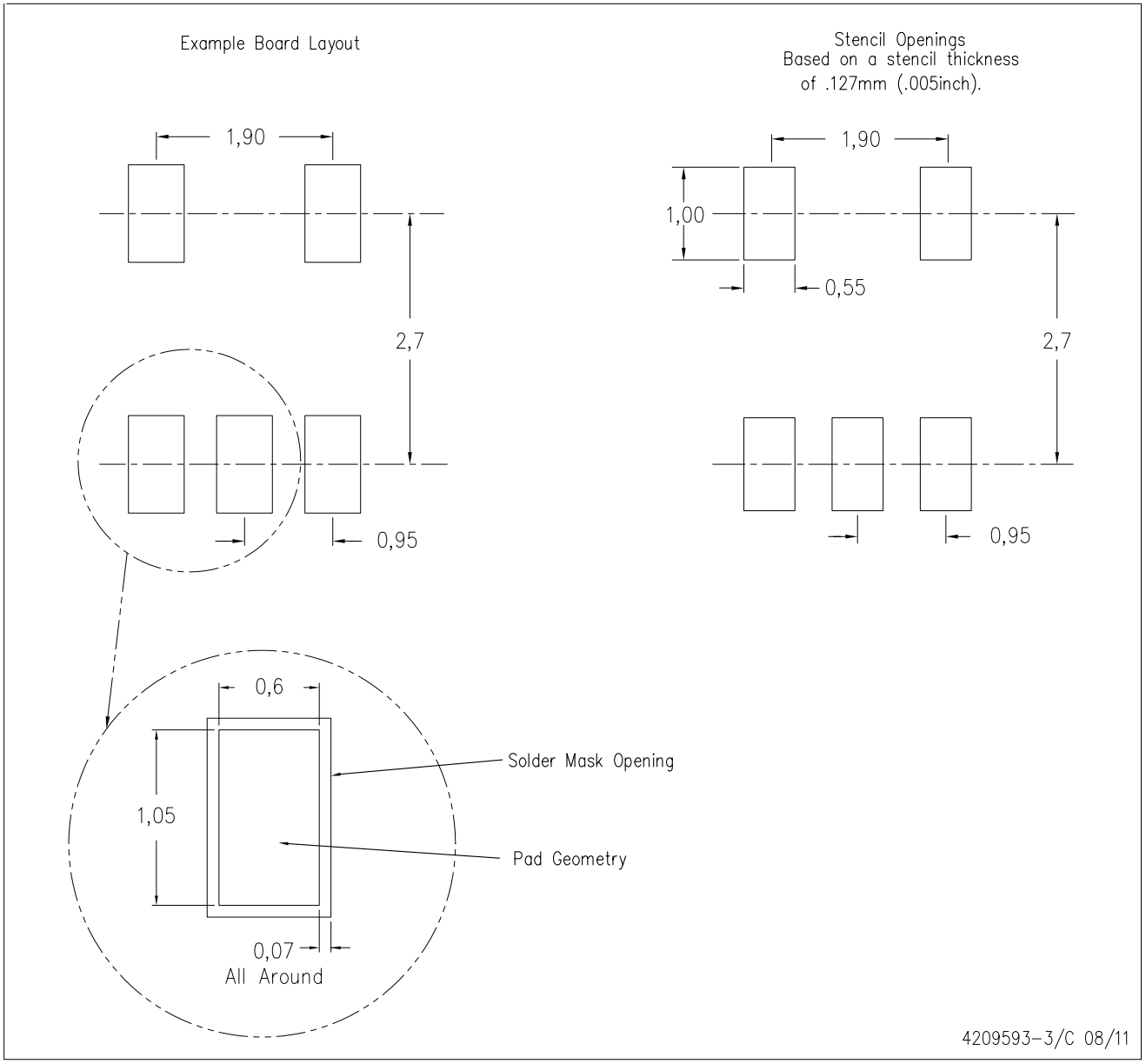
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/N 12/14

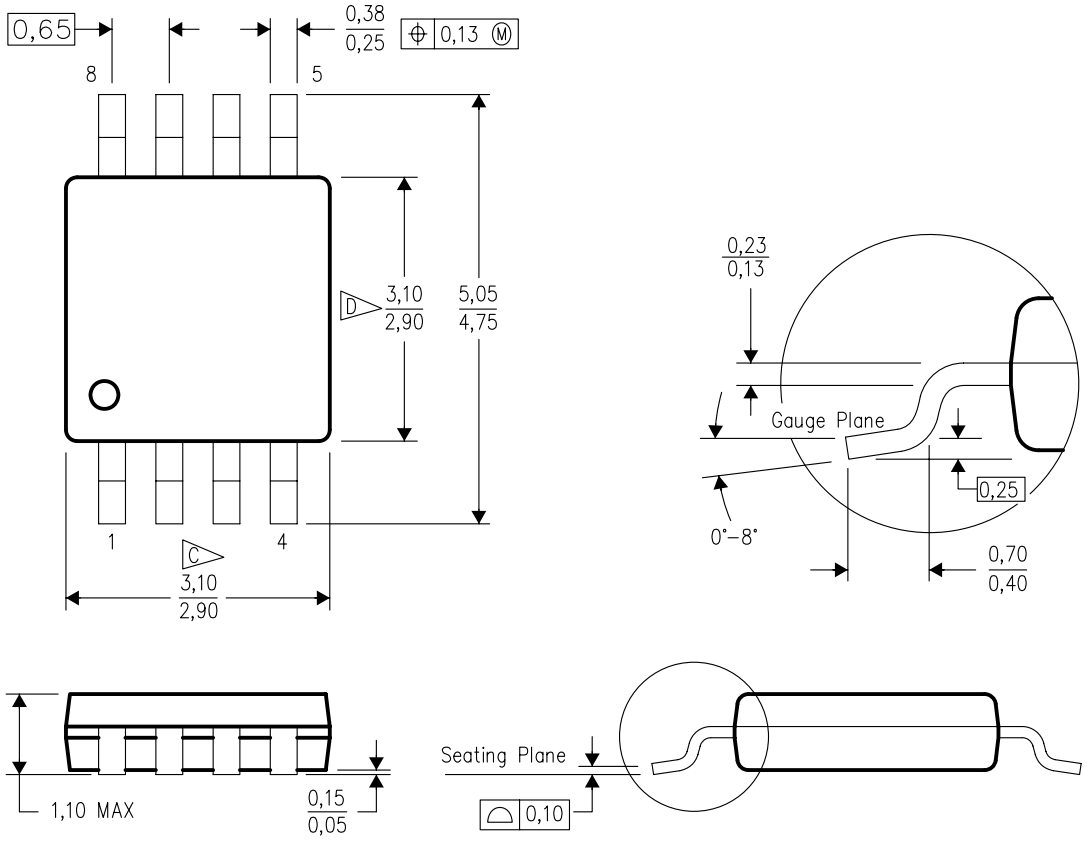
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

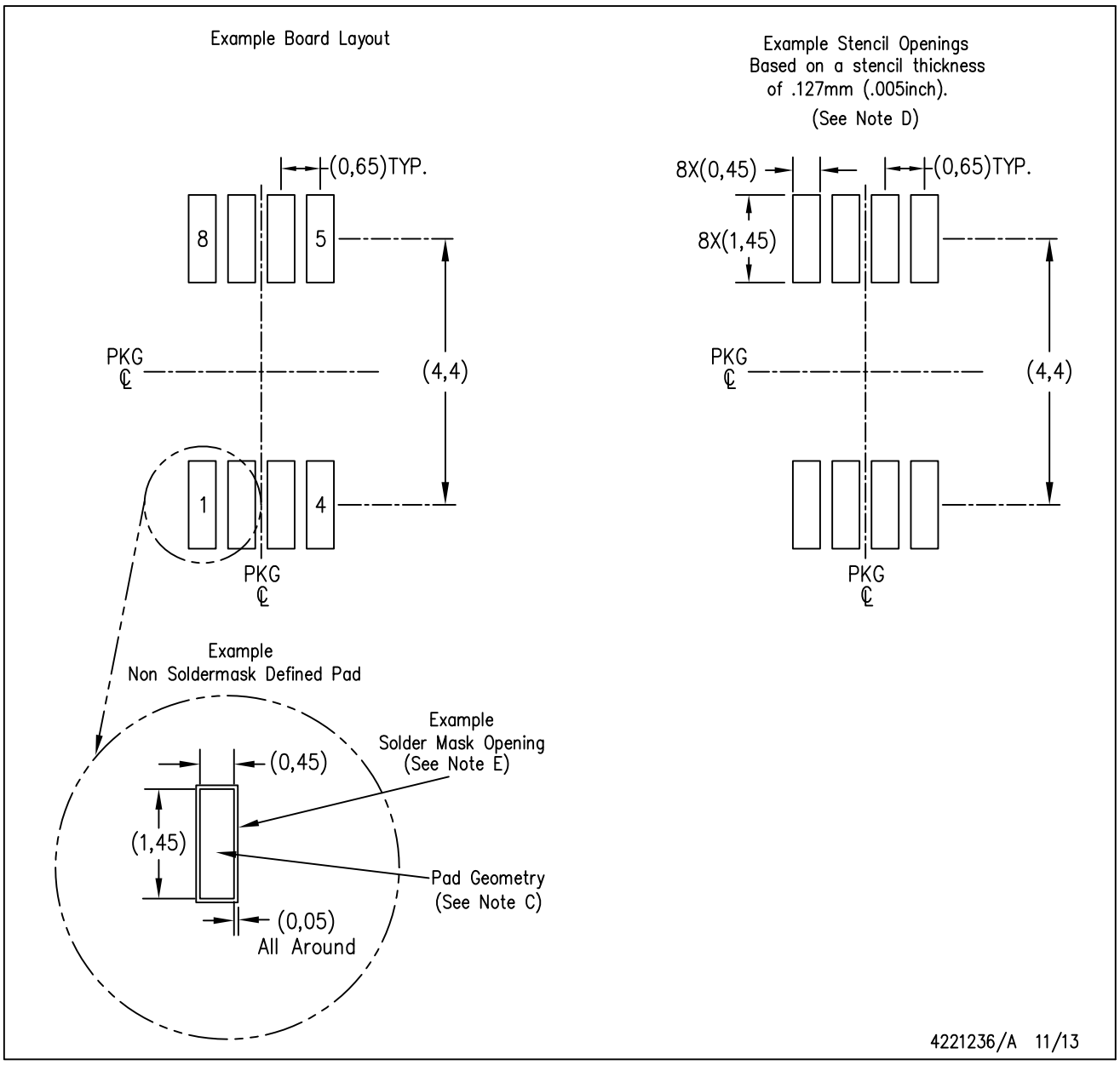
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2017, Texas Instruments Incorporated