Low-Power, Wideband, Voltage-Feedback OPERATIONAL AMPLIFIER with Disable

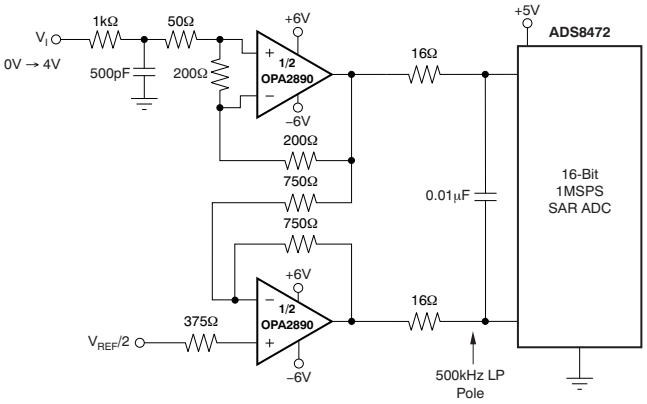
Check for Samples: OPA2890

FEATURES

- **FLEXIBLE SUPPLY RANGE:**
  +3V to +12V Single Supply
  ±1.5V to ±6V Dual Supplies
- **UNITY-GAIN STABLE**
- **WIDEBAND +5V OPERATION: 90MHz (G = 2V/V)**
- **OUTPUT VOLTAGE SWING: ±4.1V**
- **HIGH SLEW RATE: 400V/µs**
- **LOW QUIESCENT CURRENT: 1.1mA/ch**
- **LOW DISABLE CURRENT: 30µA/ch**

APPLICATIONS

- **VIDEO LINE DRIVING**
- **xDSL LINE DRIVERS/RECEIVERS**
- **HIGH-SPEED IMAGING CHANNELS**
- **ADC BUFFERS**
- **PORTABLE INSTRUMENTS**
- **TRANSIMPEDANCE AMPLIFIERS**
- **ACTIVE FILTERS**



Low Power, DC-Coupled, Single-to-Differential Driver for ≤100kHz Inputs

DESCRIPTION

The OPA2890 represents a major step forward in unity-gain stable, voltage-feedback op amps. A new internal architecture provides slew rate and full-power bandwidth previously found only in wideband, current-feedback op amps. These capabilities give exceptional single-supply operation. Using a single +5V supply, the OPA2890 can deliver a 0.9V to 4.1V output swing with over 30mA drive current and 210MHz bandwidth. This combination of features makes the OPA2890 an ideal RGB line driver or single-supply analog-to-digital converter (ADC) input driver.

The low 1.1mA/ch supply current of the OPA2890 is precisely trimmed at +25°C. This trim, along with low temperature drift, ensures lower maximum supply current than competing products. System power may be reduced further using the optional disable control pin (MSOP-10 package only). Leaving this disable pin open, or holding it high, operates the OPA2890 normally. If pulled low, the OPA2890 supply current drops to less than 30µA/ch while the output goes into a high-impedance state.

RELATED OPERATIONAL AMPLIFIER PRODUCTS

	SINGLES	DUALS	TRIPLES
Low-power voltage-feedback with disable	OPA890		
Very low-power voltage-feedback with disable		OPA2889	
Voltage-feedback amplifier with disable (1800V/µs)	OPA690	OPA2690	OPA3690

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA2890	SO-8	D	–40°C to +85°C	OPA2890	OPA2890ID	Rail, 75
					OPA2890IDR	Tape and Reel, 2500
OPA2890	MSOP-10	DGS	–40°C to +85°C	BPQ	OPA2890IDGST	Tape and Reel, 250
					OPA2890IDGSR	Tape and Reel, 2500

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

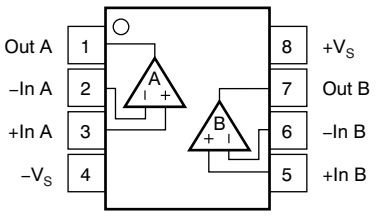
Over operating free-air temperature range, unless otherwise noted.

	OPA2890	UNIT
Power supply	±6.5	V
Internal power dissipation	See Thermal Characteristics	
Input voltage range	$\pm V_S$	V
Storage temperature range	–65 to +125	°C
Maximum junction temperature (T_J)	+150	°C
Minimum junction temperature: continuous operation, long-term reliability	+140	°C
ESD Rating:		
Human body model (HBM)	2000	V
Charge device model (CDM)	1500	V
Machine model (MM)	200	V

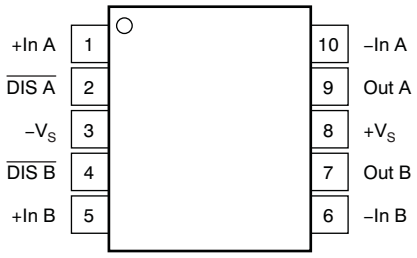
(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

PIN CONFIGURATIONS

SO-8
Top View



MSOP-10
Top View



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ELECTRICAL CHARACTERISTICS: V_S = ±5V

At T_A = +25°C, R_F = 0Ω, G = +1V/V, and R_L = 200Ω, unless otherwise noted.

PARAMETER	CONDITIONS	OPA2890ID, IDGS				UNITS	MIN/ MAX	TEST LEVEL[1]
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C[2]	0°C to +70°C[3]	–40°C to +85°C[3]			
AC PERFORMANCE								
Small-signal bandwidth	G = +1V/V, V_O = 100mV$_{PP}$, R_F = 0Ω	250				MHz	typ	C
	G = +2V/V, V_O = 100mV$_{PP}$	100	60	50	45	MHz	min	B
	G = +10V/V, V_O = 100mV$_{PP}$	12	8	7	6.5	MHz	min	B
Gain bandwidth product	G > +20V/V	120	90	80	78	MHz	min	B
Bandwidth for 0.1dB flatness	G = +2V/V, V_O = 100mV$_{PP}$	15				MHz	typ	C
Peaking at a gain of +1V/V	V_O < 100mV$_{PP}$	0.2				dB	typ	C
Large-signal bandwidth	G = +2V/V, V_O = 2V$_{PP}$	110				MHz	typ	C
Slew rate	G = +2V/V, V_O = 2V step	400	300	275	270	V/µs	min	B
Rise-and-fall time	0.2V step	3.5				ns	typ	C
Settling time to 0.02%	G = +1V/V, V_O = 2V step	16				ns	typ	C
Settling time to 0.1%		10				ns	typ	C
Harmonic distortion	G = +2V/V, f = 1MHz, V_O = 2V$_{PP}$							
2nd harmonic	R_L = 200Ω	84	73	69	68	dBc	max	B
	R_L ≥ 500Ω	100	83	81	80	dBc	max	B
3rd harmonic	R_L = 200Ω	89	84	81	80	dBc	max	B
	R_L ≥ 500Ω	94	90	87	86	dBc	max	B
Input voltage noise	f > 100kHz	8	9	10	11	nV/√Hz	max	B
Input current noise	f > 100kHz	1	1.3	1.7	1.9	pA/√Hz	max	B
Differential gain	G = +2V/V, V_O = 1.4V$_{PP}$, R_L = 150Ω	0.05				%	typ	C
Differential phase	G = +2V/V, V_O = 1.4V$_{PP}$, R_L = 150Ω	0.03				°	typ	C
Channel-to-channel crosstalk	f = 5MHz, Input-referred	–68				dB	typ	C
DC PERFORMANCE[4]								
Open-loop voltage gain (A_{OL})	V_O = 0V, R_L = 100Ω	62	**57**	56	54	dB	min	A
Input offset voltage	V_{CM} = 0V	±2	**±5**	±6.6	±7.1	mV	max	A
Average offset voltage drift	V_{CM} = 0V			±35	±35	µV/°C	max	B
Input bias current	V_{CM} = 0V	±0.1	**±1.6**	±1.8	±2	µA	max	A
Average input bias current drift	V_{CM} = 0V			±5	±6	nA/°C	max	B
Input offset current	V_{CM} = 0V	±70	**±350**	±450	±500	nA	max	A
Average input offset current drift	V_{CM} = 0V			±2.5	±2.5	nA/°C	max	B
INPUT								
Common-mode input range (CMIR)[5]		±3.9	**±3.7**	±3.6	±3.5	V	min	A
Common-mode rejection ratio (CMRR)	V_{CM} = 0V, Input-referred	66	60	57	56	dB	min	A
Input impedance								
Differential	V_{CM} = 0V	190 || 0.6				kΩ || pF	typ	C
Common-mode	V_{CM} = 0V	3.2 || 0.9				MΩ || pF	typ	C
OUTPUT								
Output voltage swing	No load	±4.0	**±3.9**	±3.8	±3.7	V	min	A
	R_L = 100Ω	±3.6	**±3.1**	±3.05	±2.9	V	min	A
Output current, sourcing, sinking	V_O = 0V	±40	**±35**	±33	±30	mA	min	A
Peak output current	Output shorted to ground	±75				mA	typ	C
Closed-loop output impedance	G = +2V/V, f = 100kHz	0.04				Ω	typ	C

(1) Test levels: (A) 100% tested at +25°C. Over temperature limits set by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(2) Junction temperature = ambient for +25°C tested specifications.
(3) Junction temperature = ambient at low temperature limit; junction temperature = ambient +4°C at high temperature limit for over temperature specifications.
(4) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage.
(5) Tested < 3dB below minimum specified CMRR at ±CMIR limits

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ELECTRICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, R_F = 0Ω, G = +1V/V, and R_L = 200Ω, unless otherwise noted.

PARAMETER	CONDITIONS	OPA2890ID, IDGS				UNITS	MIN/ MAX	TEST LEVEL[1]
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C[2]	0°C to +70°C[3]	–40°C to +85°C[3]			
DISABLE (MSOP-10 ONLY)	Disablelow							
Power-down supply current (+V_S)	$V_{\overline{DIS}}$ = 0, Both channels	60	**110**	120	150	µA	max	A
Disable time	V_{IN} = 1V_{DC}	7				µs	typ	C
Enable time	V_{IN} = 1V_{DC}	200				ns	typ	C
Off isolation	G = +2V/V, f = 5MHz	70				dB	typ	C
Output capacitance in disable		4				pF	typ	C
Enable voltage		3.0	**3.2**	3.4	3.8	V	min	A
Disable voltage		1.4	**1.1**	1.0	0.8	V	max	A
Control pin input bias current ($V_{\overline{DIS}}$)	$V_{\overline{DIS}}$ = 0V, Each channel	15	**30**	35	40	µA	max	A
POWER SUPPLY								
Specified operating voltage		±5				V	typ	C
Minimum operating voltage		±1.5				V	typ	C
Maximum operating voltage			**±6.0**	±6.0	±6.0	V	max	A
Maximum quiescent current	V_S = ±5V, Both channels	2.25	**2.4**	2.45	2.5	mA	max	A
Minimum quiescent current	V_S = ±5V, Both channels	2.25	**2.1**	2.05	2.0	mA	min	A
Power-supply rejection ratio (+PSRR)	+V_S = 4.5V to 5.5V	68	**60**	58	56	dB	min	A
THERMAL CHARACTERISTICS								A
Specified operating range: D and DGS packages		–40 to +85				°C	typ	C
Thermal resistance, θ_{JA}		Junction-to-ambient						
D SO-8		100				°C/W	typ	C
DGS MSOP-10		135				°C/W	typ	C

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ELECTRICAL CHARACTERISTICS: V_S = +5V

At R_F = 0Ω, G = +1V/V, and R_L = 100Ω, unless otherwise noted.

PARAMETER	CONDITIONS	OPA2890ID, IDGS				UNITS	MIN/ MAX	TEST LEVEL[1]
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C[2]	0°C to +70°C[3]	–40°C to +85°C[3]			
AC PERFORMANCE								
Small-signal bandwidth	G = +1V/V, V_O = 100mV$_{PP}$, R_F = 0Ω	210				MHz	typ	C
	G = +2V/V, V_O = 100mV$_{PP}$	90	55	45	40	MHz	min	B
	G = +10V/V, V_O = 100mV$_{PP}$	12	8	6.8	6.3	MHz	min	B
Gain bandwidth product	G > +20V/V	120	85	70	68	MHz	min	B
Bandwidth for 0.1dB flatness	G = +2V/V, V_O = 100mV$_{PP}$	15				MHz	typ	C
Peaking at a gain of +1V/V	V_O < 100mV$_{PP}$	0.2				dB	typ	C
Large-signal bandwidth	G = +2V/V, V_O = 2V$_{PP}$	100				MHz	typ	C
Slew rate	G = +2V/V, V_O = 2V step	350	250	200	175	V/µs	min	B
Rise-and-fall time	0.2V step	3.8				ns	typ	C
Settling time to 0.02%	G = +1V/V, V_O = 2V step	18				ns	typ	C
Settling time to 0.1%		12				ns	typ	C
Harmonic distortion	G = +2V/V, f = 1MHz, V_O = 2V$_{PP}$							
2nd harmonic	R_L = 200Ω	80	71	68	67	dBc	max	B
	R_L ≥ 500Ω	87	75	71	70	dBc	max	B
3rd harmonic	R_L = 200Ω	83	79	77	76	dBc	max	B
	R_L ≥ 500Ω	86	83	81	80	dBc	max	B
Input voltage noise	f > 100kHz	8.1	9.1	10.1	11.1	nV/√Hz	max	B
Input current noise	f > 100kHz	1.1	1.4	1.7	2.0	pA/√Hz	max	B
Differential gain	G = +2V/V, V_O = 1.4V$_{PP}$, R_L = 150Ω	0.06				%	typ	C
Differential phase	G = +2V/V, V_O = 1.4V$_{PP}$, R_L = 150Ω	0.04				°	typ	C
Channel-to-channel crosstalk	f = 5MHz, Input-referred	–68				dB	typ	C
DC PERFORMANCE[4]								
Open-loop voltage gain (A_{OL})	V_O = V_S/2, R_L = 100Ω	60	**55**	54	52	dB	min	A
Input offset voltage	V_{CM} = V_S/2	±2	**±5**	±6.6	±7.1	mV	max	A
Average offset voltage drift	V_{CM} = V_S/2			±35	±35	µV/°C	max	B
Input bias current	V_{CM} = V_S/2	±0.1	**±1.7**	±1.9	±2.1	µA	max	A
Average input bias current drift	V_{CM} = V_S/2			±5	±6	nA/°C	max	B
Input offset current	V_{CM} = V_S/2	±70	**±400**	±500	±550	nA	max	A
Average input offset current drift	V_{CM} = V_S/2			±2.5	±2.5	nA/°C	max	B
INPUT								
Most positive input voltage[5]		+4	**+3.7**	+3.63	+3.6	V	min	A
Least positive input voltage[5]		+1	**+1.3**	+1.3	+1.4	V	max	A
Common-mode rejection ratio (CMRR)	V_{CM} = V_S/2, Input-referred	65	**59**	56	55	dB	min	A
Input impedance								
Differential	V_{CM} = V_S/2	190 || 0.6				kΩ || pF	typ	C
Common-mode	V_{CM} = V_S/2	3.2 || 0.9				MΩ || pF	typ	C
OUTPUT								
Most positive output voltage	No load	+4.1	**+3.9**	+3.85	+3.8	V	min	A
	R_L = 100Ω	+3.9	**+3.75**	+3.7	+3.65	V	min	A
Least positive output voltage	No load	+0.9	**+1.1**	+1.15	+1.2	V	max	A
	R_L = 100Ω	+1.1	**+1.35**	+1.4	+1.45	V	max	A
Output current: sourcing, sinking	V_O = V_S/2	±35	**±30**	±28	±25	mA	min	A
Short-circuit output current	Output shorted to ground	±65				mA	typ	C
Closed-loop output impedance	G = +2V/V, f = 100kHz	0.04				Ω	typ	C

(1) Test levels: (A) 100% tested at +25°C. Over temperature limits set by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(2) Junction temperature = ambient for +25°C tested specifications.
(3) Junction temperature = ambient at low temperature limit; junction temperature = ambient +2°C at high temperature limit for over temperature specifications.
(4) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage.
(5) Tested < 3dB below minimum specified CMRR at ±CMIR limits

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ELECTRICAL CHARACTERISTICS: V_S = +5V (continued)

At R_F = 0Ω, G = +1V/V, and R_L = 100Ω, unless otherwise noted.

PARAMETER	CONDITIONS	OPA2890ID, IDGS				UNITS	MIN/ MAX	TEST LEVEL[1]
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C[2]	0°C to +70°C[3]	–40°C to +85°C[3]			
DISABLE (MSOP-10 ONLY)	Disable low							
Power-down supply current (+V_S)	$V_{\overline{DIS}}$ = 0V, Both channels	35	**90**	100	130	µA	max	A
Disable time	V_{OUT} = 1V_{DC}					ns	typ	C
Enable time	V_{OUT} = 1V_{DC}					ns	typ	C
Off isolation	G = +2V/V, f = 5MHz					dB	typ	C
Output capacitance in disable						pF	typ	C
Enable voltage		3.0	**3.2**	3.4	3.8	V	min	A
Disable voltage		1.4	**1.1**	1.0	0.8	V	max	A
Control pin input bias current ($V_{\overline{DIS}}$)	$V_{\overline{DIS}}$ = 0V, Each channel	15	**30**	35	40	µA	max	A
POWER SUPPLY								
Specified operating voltage		+5				V	typ	C
Minimum operating voltage		+3				V	typ	C
Maximum operating voltage			**+12**	+12	+12	V	max	A
Maximum quiescent current	V_S = +5V, Both channels	2.1	**2.35**	2.4	2.45	mA	max	A
Minimum quiescent current	V_S = +5V, Both channels	2.1	**1.85**	1.8	1.75	mA	min	A
Power-supply rejection ratio (+PSRR)	+V_S = 4.5V to 5.5V	65				dB	typ	C
THERMAL CHARACTERISTICS								
Specified operating range: D and DGS packages		–40 to +85				°C	typ	C
Thermal resistance, θ_{JA}	Junction-to-ambient							
D SO-8		100				°C/W	typ	C
DGS MSOP-10		135				°C/W	typ	C

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TYPICAL CHARACTERISTICS: V_S = ±5V

At T_A = +25°C, G = +2V/V, R_F = 750Ω, and R_L = 200Ω, unless otherwise noted. See Figure 49.

SMALL-SIGNAL FREQUENCY RESPONSE

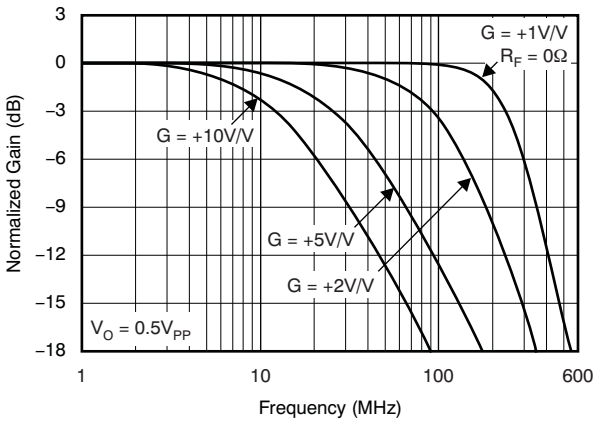

Figure 1.

LARGE-SIGNAL FREQUENCY RESPONSE

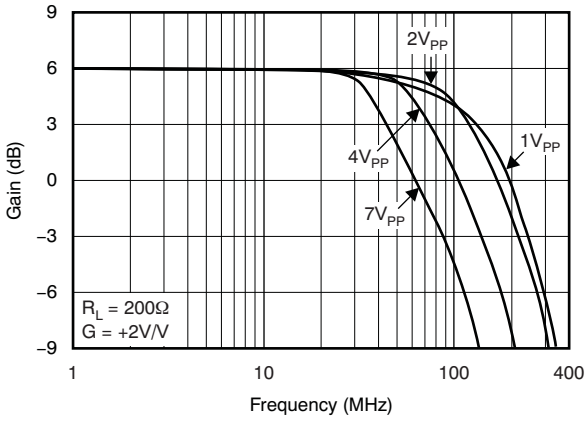

Figure 2.

SMALL-SIGNAL PULSE RESPONSE

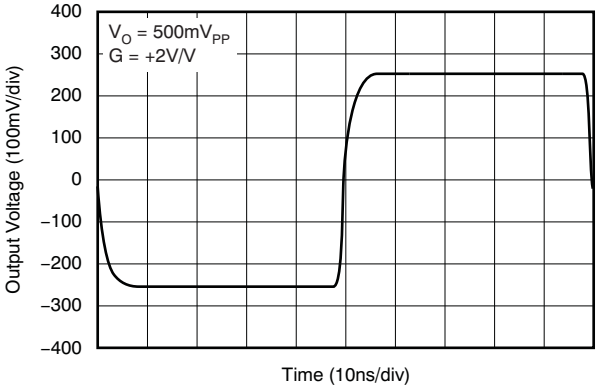

Figure 3.

LARGE-SIGNAL PULSE RESPONSE

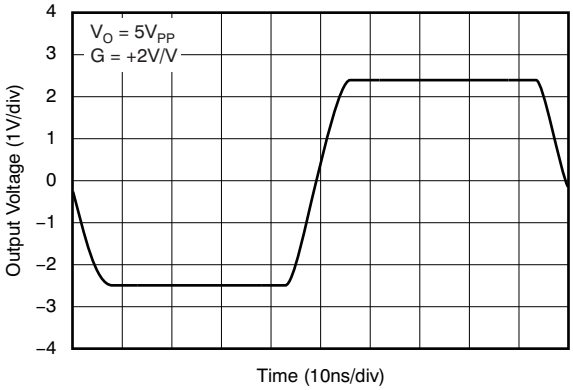

Figure 4.

VIDEO DIFFERENTIAL GAIN/DIFFERENTIAL PHASE

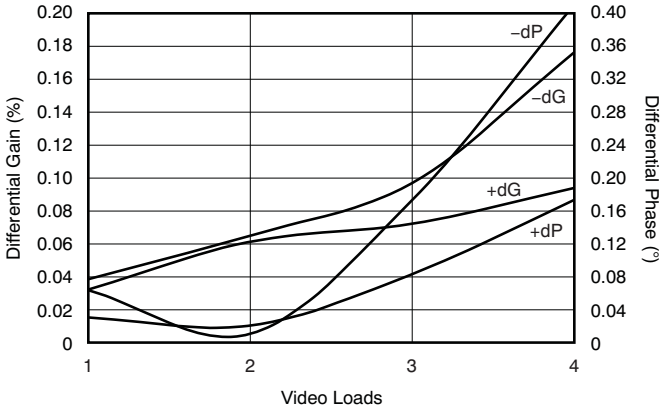

Figure 5.

CHANNEL-TO-CHANNEL CROSSTALK

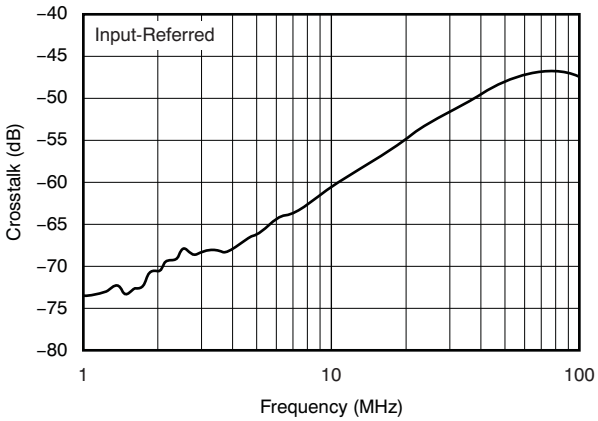

Figure 6.

TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, G = +2V/V, R_F = 750Ω, and R_L = 200Ω, unless otherwise noted. See Figure 49.

HARMONIC DISTORTION vs LOAD RESISTANCE

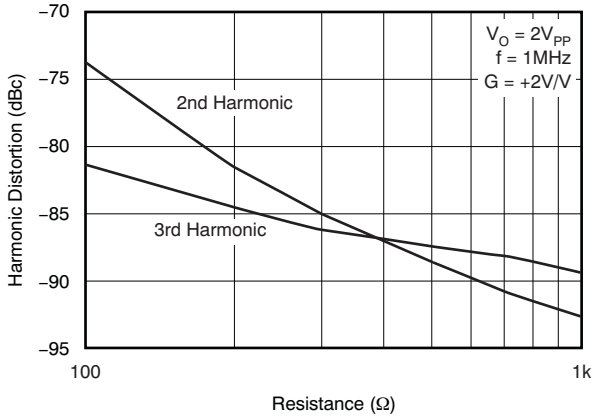

Figure 7.

1MHz HARMONIC DISTORTION vs SUPPLY VOLTAGE

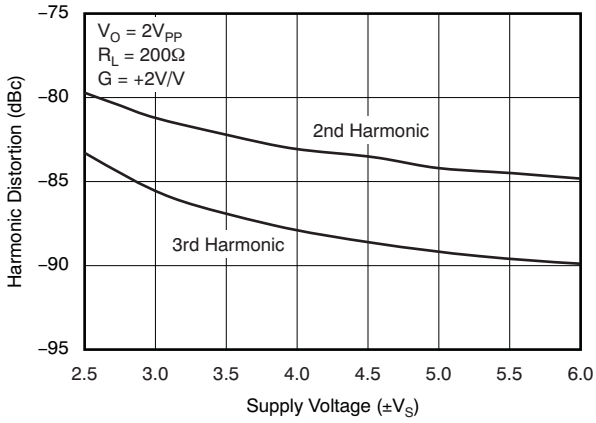

Figure 8.

HARMONIC DISTORTION vs FREQUENCY

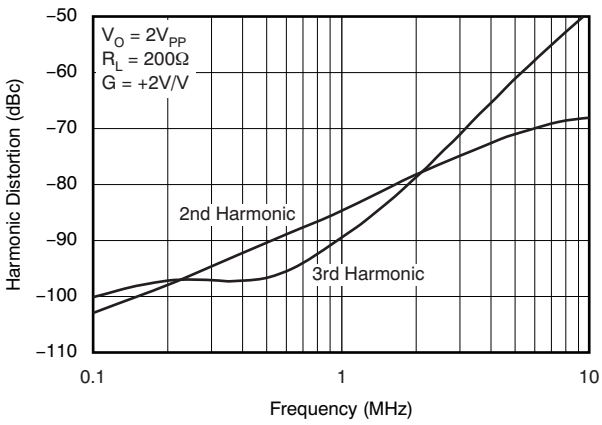

Figure 9.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

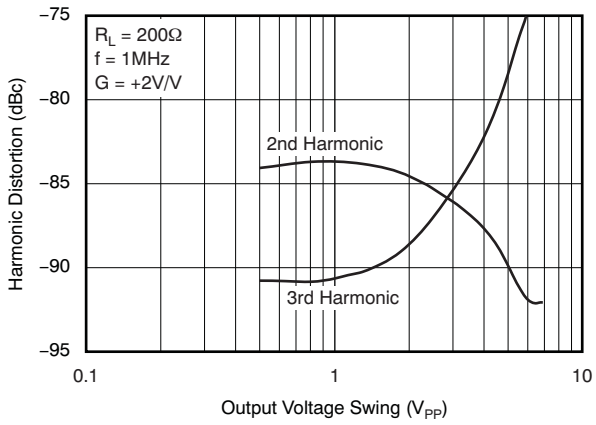

Figure 10.

HARMONIC DISTORTION vs NONINVERTING GAIN

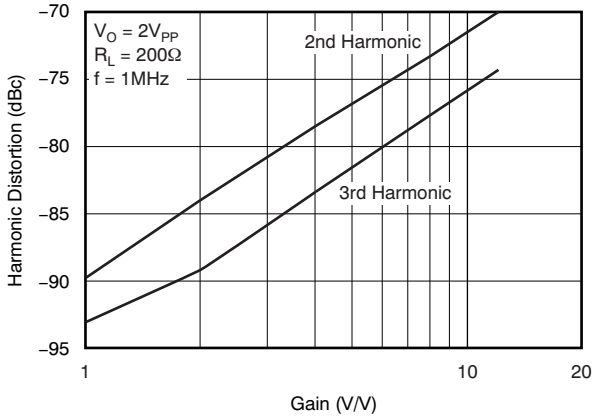

Figure 11.

HARMONIC DISTORTION vs INVERTING GAIN

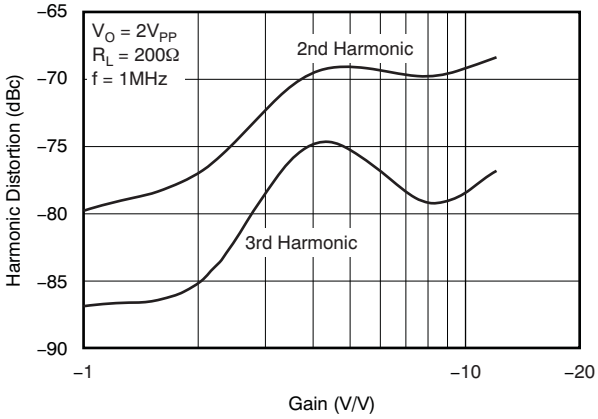

Figure 12.

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TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, G = +2V/V, R_F = 750Ω, and R_L = 200Ω, unless otherwise noted. See Figure 49.

LOW-FREQUENCY INVERTING HARMONIC DISTORTION

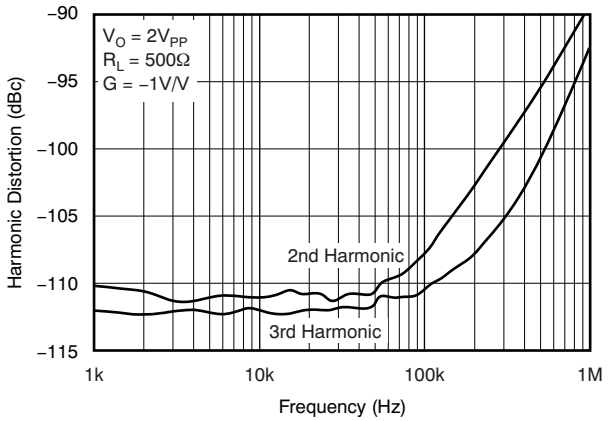

Figure 13.

TWO-TONE, 3RD-ORDER INTERMODULATION SPURIOUS

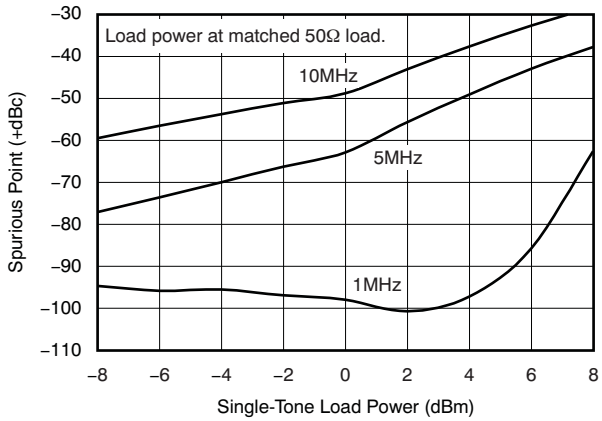

Figure 14.

RECOMMENDED R_S vs CAPACITIVE LOAD

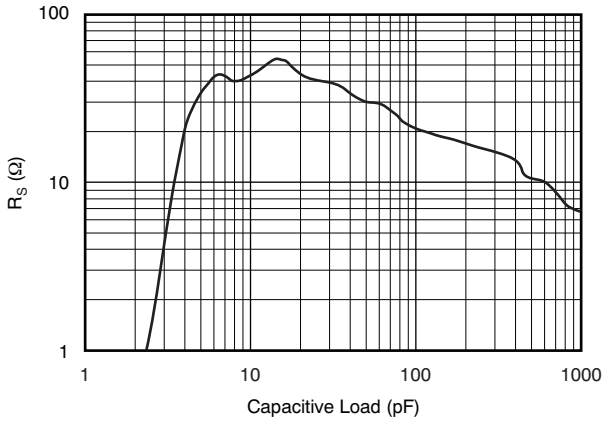

Figure 15.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

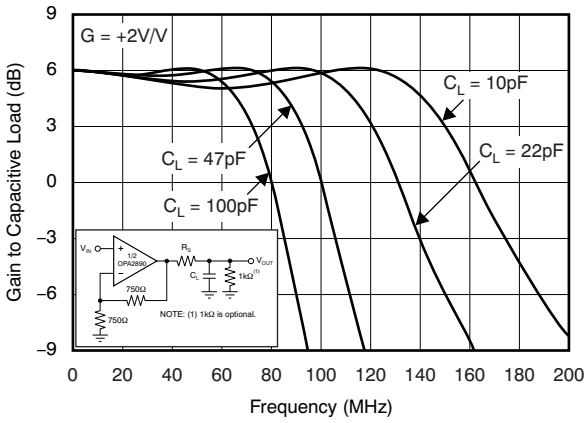

Figure 16.

COMMON-MODE REJECTION RATIO AND POWER-SUPPLY REJECTION RATIO vs FREQUENCY

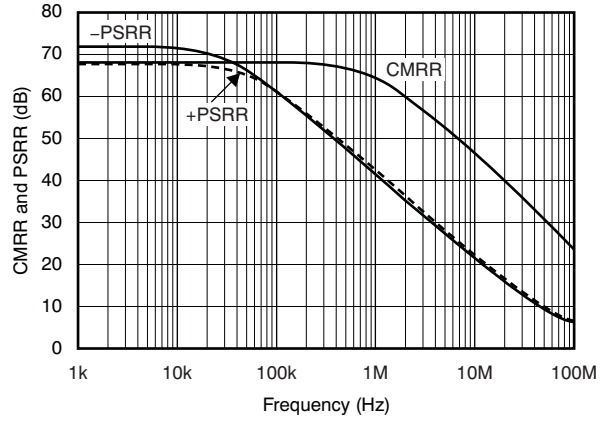

Figure 17.

INPUT VOLTAGE AND CURRENT NOISE

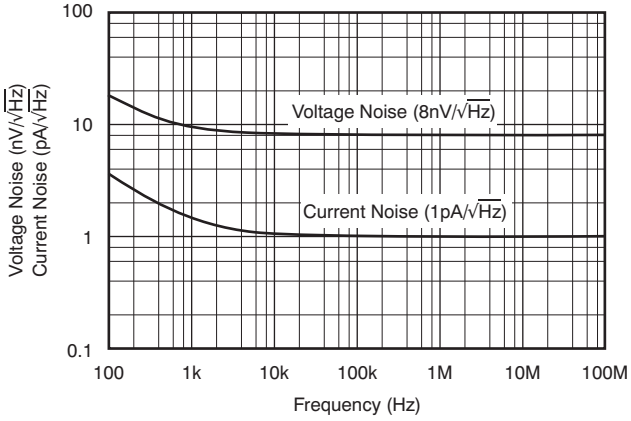

Figure 18.

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TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, G = +2V/V, R_F = 750Ω, and R_L = 200Ω, unless otherwise noted. See Figure 49.

SUPPLY AND OUTPUT CURRENT vs TEMPERATURE

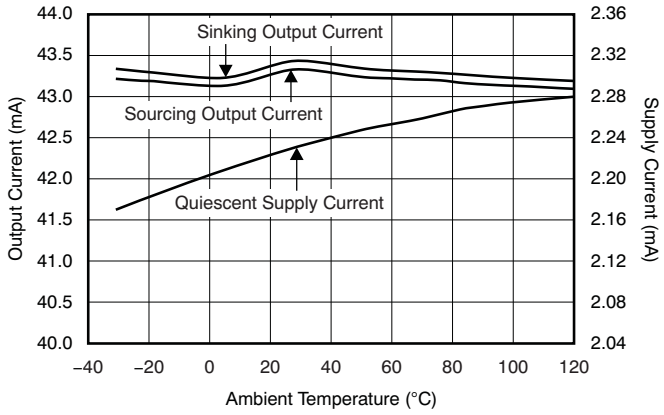

Figure 19.

TYPICAL DC DRIFT OVER TEMPERATURE

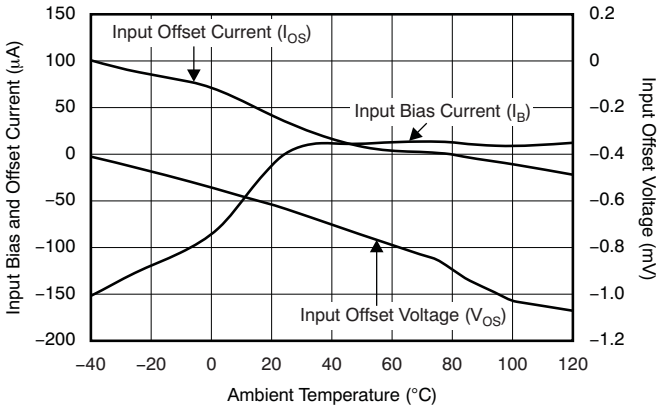

Figure 20.

LARGE-SIGNAL DISABLE/ENABLE RESPONSE

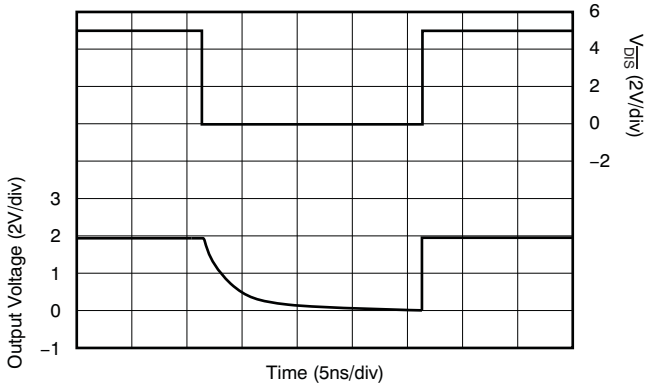

Figure 21.

NONINVERTING OVERDRIVE RECOVERY

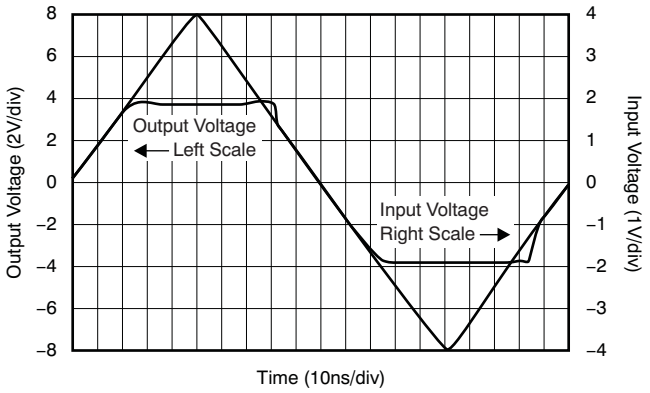

Figure 22.

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

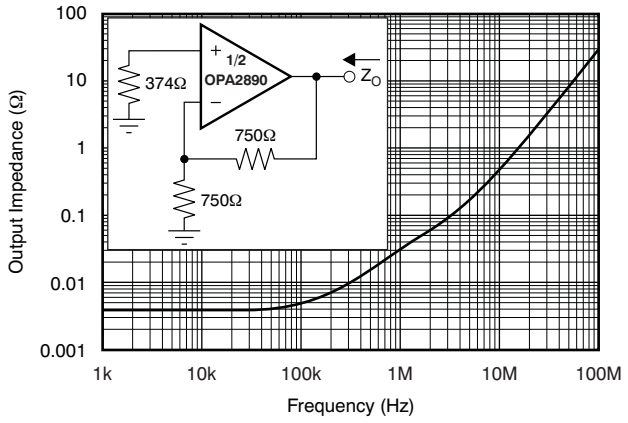

Figure 23.

OPEN-LOOP GAIN AND PHASE

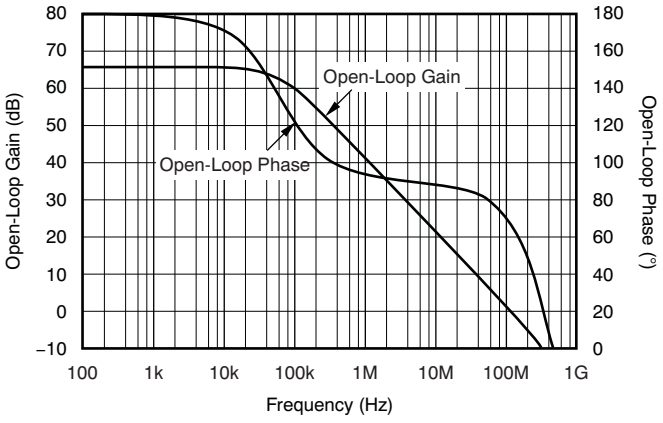

Figure 24.

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TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, G = +2V/V, R_F = 750Ω, and R_L = 200Ω, unless otherwise noted. See Figure 49.

DISABLE FEEDTHROUGH

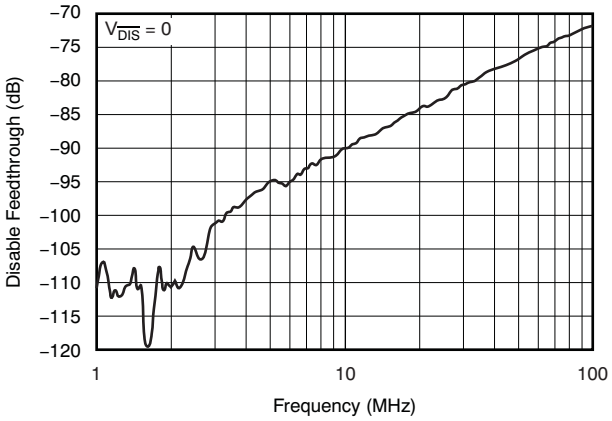

Figure 25.

TYPICAL CHARACTERISTICS: V_S = ±5V, Differential

At T_A = +25°C, Differential Gain = +2V/V, and R_L = 400Ω, unless otherwise noted. See Figure 52.

DIFFERENTIAL SMALL-SIGNAL FREQUENCY RESPONSE

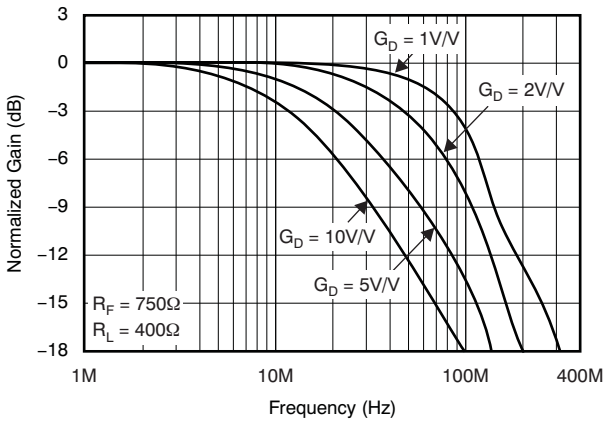

Figure 26.

DIFFERENTIAL LARGE-SIGNAL FREQUENCY RESPONSE

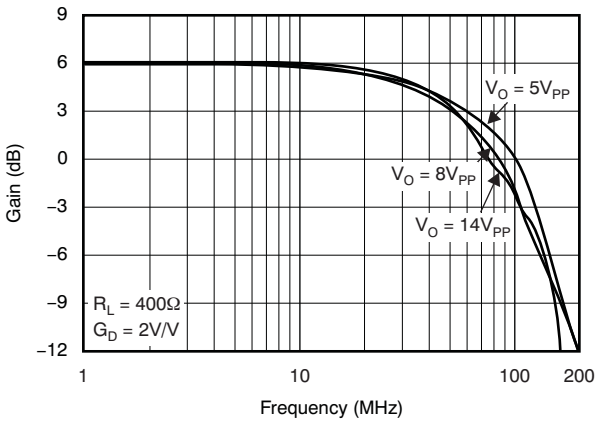

Figure 27.

DIFFERENTIAL DISTORTION vs LOAD RESISTANCE

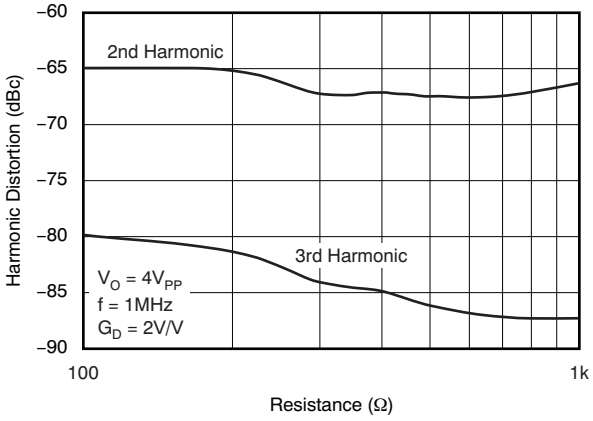

Figure 28.

DIFFERENTIAL DISTORTION vs FREQUENCY

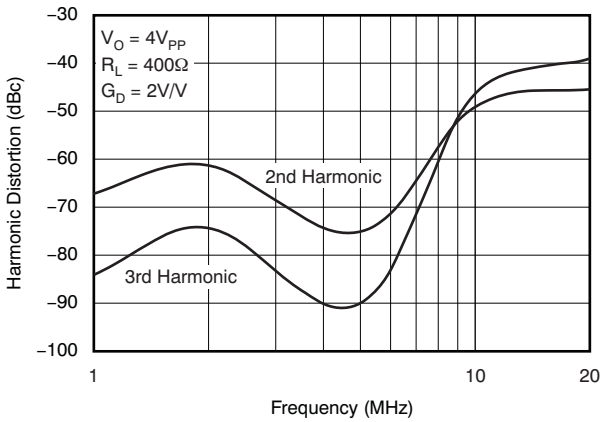

Figure 29.

DIFFERENTIAL DISTORTION vs OUTPUT VOLTAGE

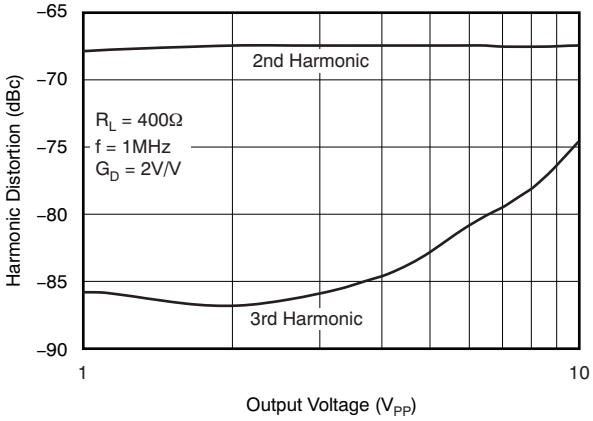

Figure 30.

DIFFERENTIAL DISTORTION vs FREQUENCY

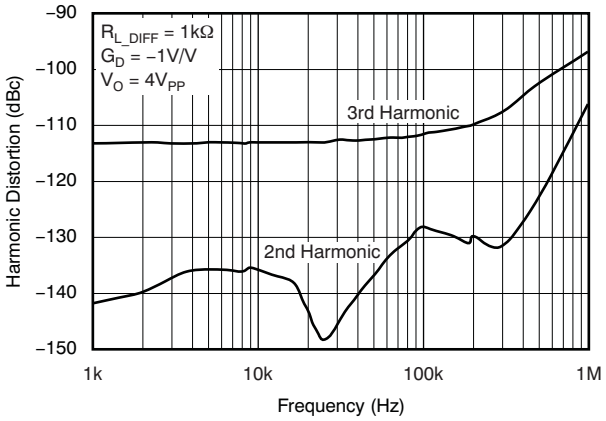

Figure 31.

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TYPICAL CHARACTERISTICS: V_S = +5V

At T_A = +25°C, G = +2V/V, R_F = 750Ω, and R_L = 200Ω, unless otherwise noted. See Figure 49.

NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE

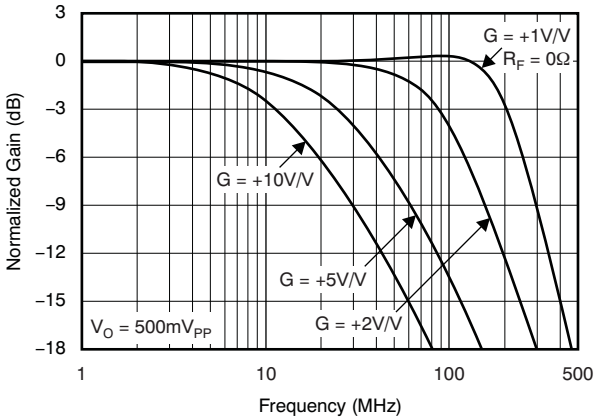

Figure 32.

NONINVERTING LARGE-SIGNAL FREQUENCY RESPONSE

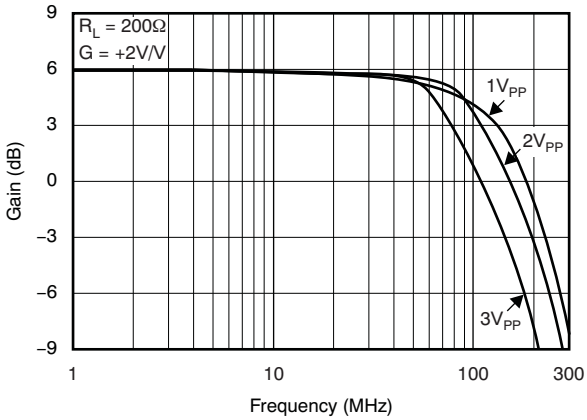

Figure 33.

SMALL-SIGNAL PULSE RESPONSE

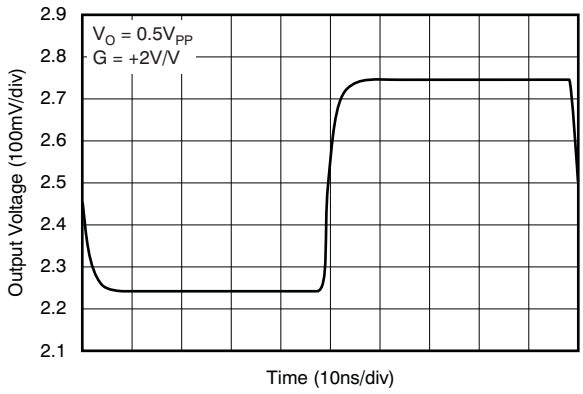

Figure 34.

LARGE-SIGNAL PULSE RESPONSE

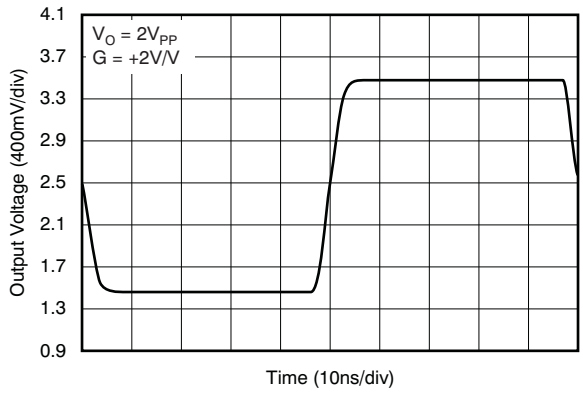

Figure 35.

RECOMMENDED R_S vs CAPACITIVE LOAD

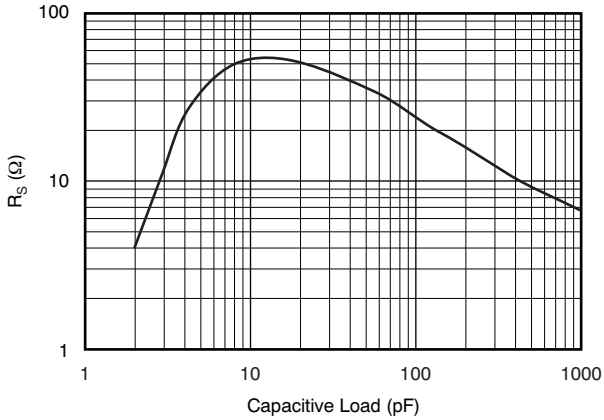

Figure 36.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

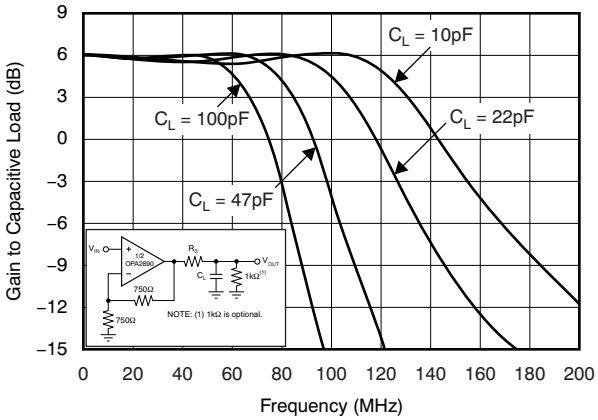

Figure 37.

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TYPICAL CHARACTERISTICS: V_S = +5V (continued)

At T_A = +25°C, G = +2V/V, R_F = 750Ω, and R_L = 200Ω, unless otherwise noted. See Figure 49.

NONINVERTING OVERDRIVE RECOVERY

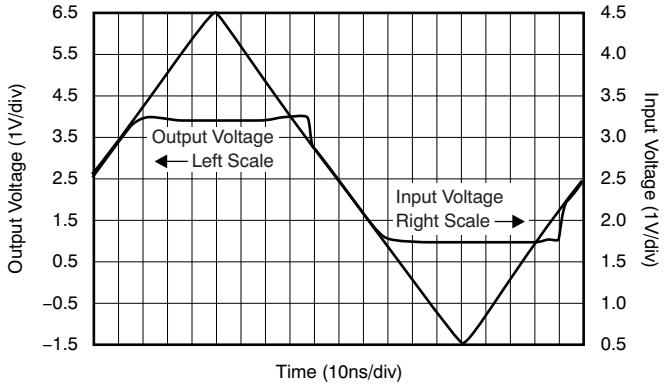

Figure 38.

HARMONIC DISTORTION vs LOAD RESISTANCE

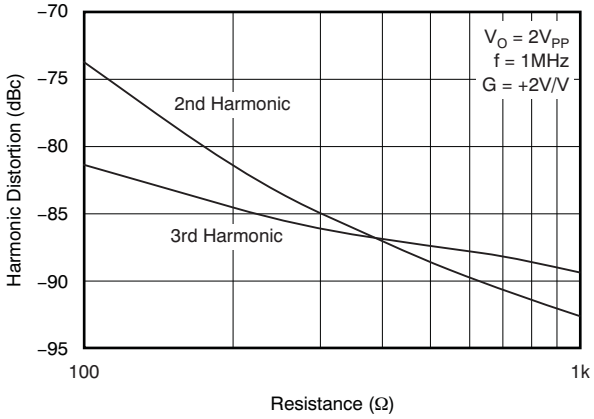

Figure 39.

HARMONIC DISTORTION vs FREQUENCY

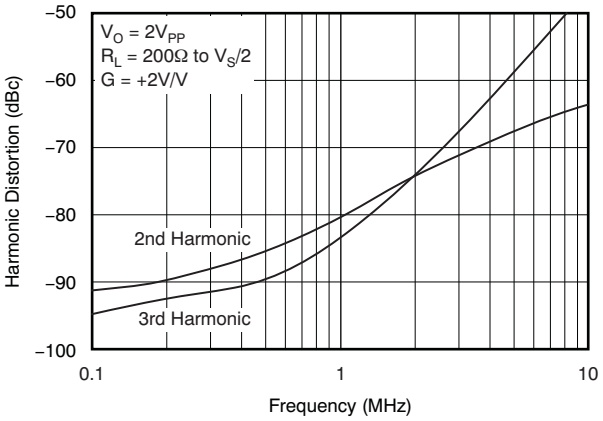

Figure 40.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

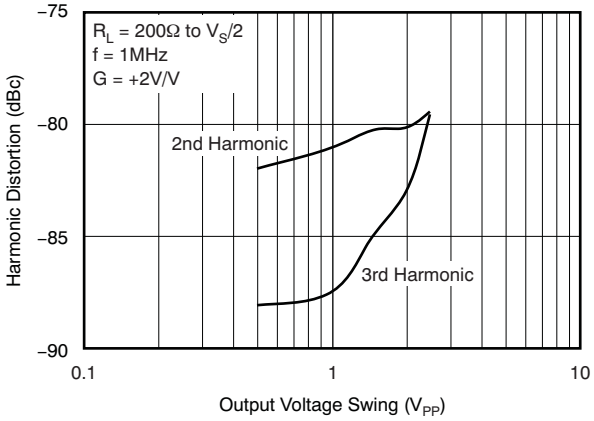

Figure 41.

TWO-TONE, 3RD-ORDER INTERMODULATION SPURIOUS

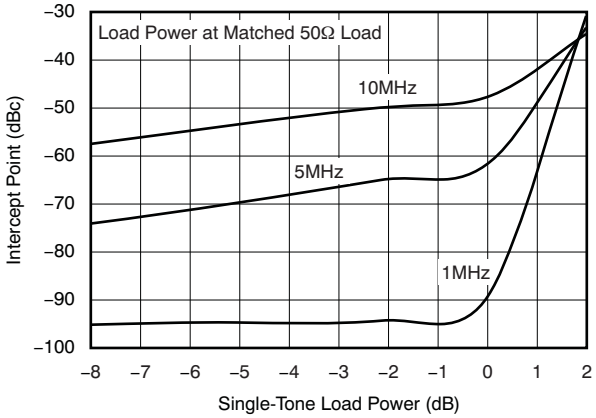

Figure 42.

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TYPICAL CHARACTERISTICS: V_S = +5V, Differential

At T_A = +25°C, Differential Gain = +2V/V, and R_L = 400Ω, unless otherwise noted. See Figure 58.

DIFFERENTIAL SMALL-SIGNAL FREQUENCY RESPONSE

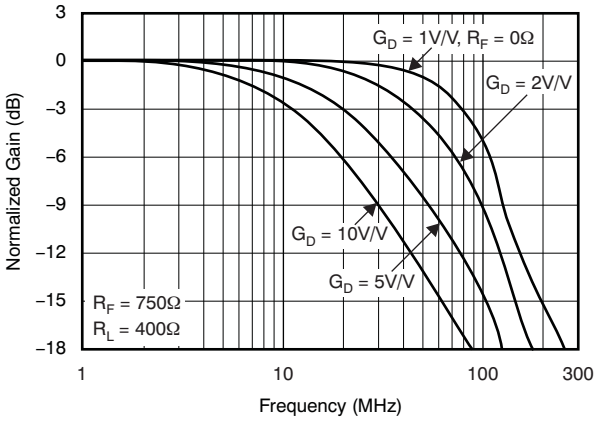

Figure 43.

DIFFERENTIAL LARGE-SIGNAL FREQUENCY RESPONSE

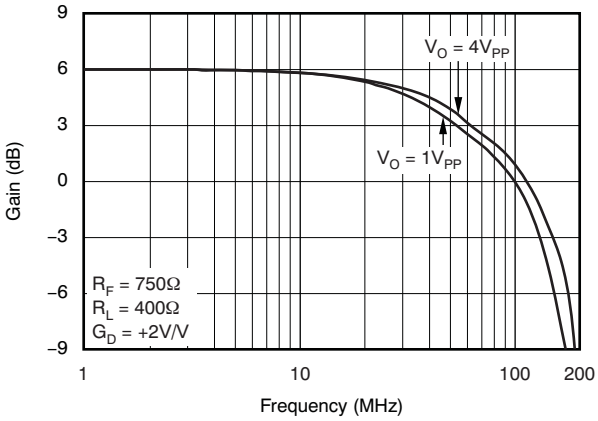

Figure 44.

DIFFERENTIAL DISTORTION vs LOAD RESISTANCE

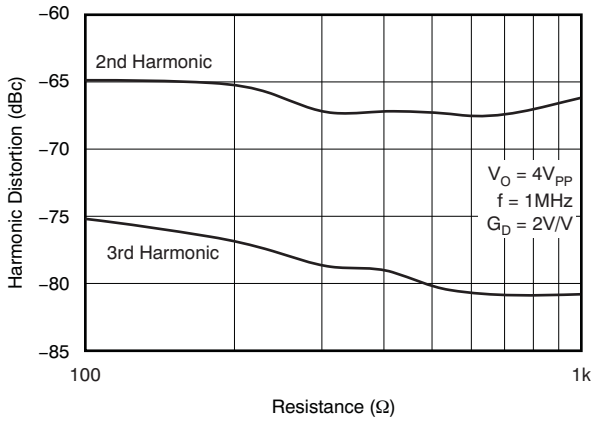

Figure 45.

DIFFERENTIAL DISTORTION vs FREQUENCY

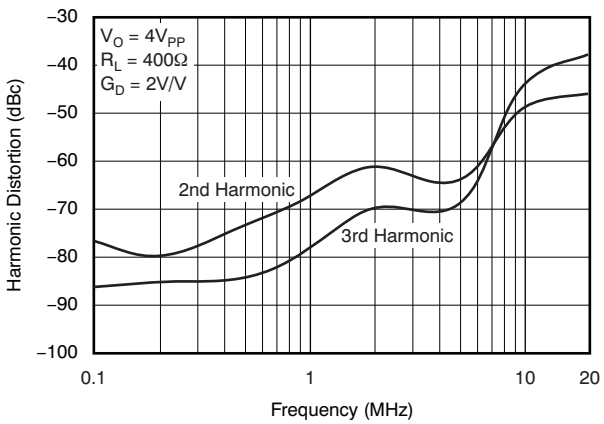

Figure 46.

DIFFERENTIAL DISTORTION vs OUTPUT VOLTAGE

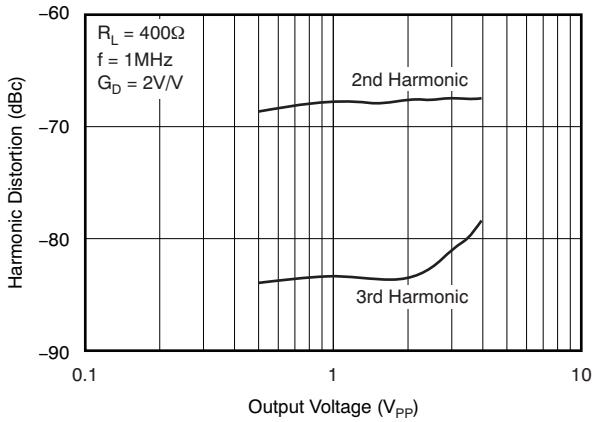

Figure 47.

DIFFERENTIAL DISTORTION vs FREQUENCY

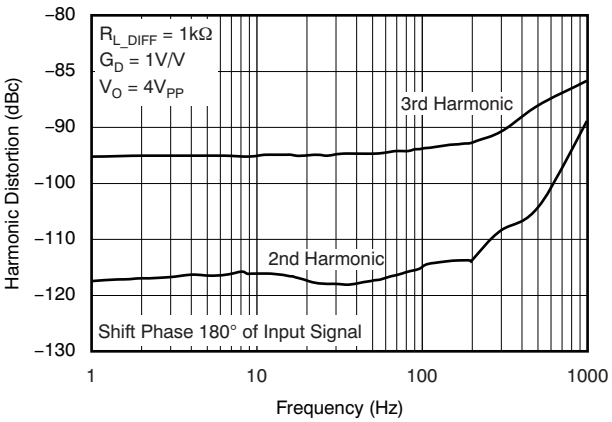

Figure 48.

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APPLICATIONS INFORMATION

WIDEBAND VOLTAGE-FEEDBACK OPERATION

The OPA2890 provides an exceptional combination of high output power capability in a dual, wideband, unity-gain stable, voltage-feedback op amp using a new high slew rate input stage. Typical differential input stages used for voltage-feedback op amps are designed to steer a fixed-bias current to the compensation capacitor, setting a limit to the achievable slew rate. The OPA2890 uses a new input stage that places the transconductance element between two input buffers, using the output currents as the forward signal. As the error voltage increases across the two inputs, an increasing current is delivered to the compensation capacitor. This configuration provides high slew rate (400V/μs) while consuming relatively low quiescent current (1.12mA/ch). This exceptional full-power performance comes at the price of a slightly higher input noise voltage than alternative architectures; however, the 8nV/√Hz input voltage noise for the OPA2890 is exceptionally low for this type of input stage.

Figure 49 shows the DC-coupled, gain of +2V/V, dual power-supply circuit configuration used as the basis of the ±5V Electrical Characteristics and Typical Characteristics. This illustration is for one channel; the other channel is connected similarly. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 200Ω. Voltage swings reported in the Electrical Characteristics are taken directly at the input and output pins, while output powers (dBm) are at the matched 50Ω load. For the circuit of Figure 49, the total effective load is 200Ω || 1.5kΩ. The disable control line (MSOP-10 package only) is typically left open for normal amplifier operation. Two optional components are included in Figure 49. First, an additional resistor (350Ω) is included in series with the noninverting input. Combined with the 25Ω dc source resistance looking back towards the signal generator, this resistor gives an input bias current cancelling resistance that matches the 750Ω source resistance seen at the inverting input (see the DC Accuracy and Offset Control section). In addition to the usual power-supply decoupling capacitors to ground, a 0.1μF capacitor is also included between the two power-supply pins. In practical printed circuit board (PCB) layouts, this optional capacitor typically improves the 2nd-harmonic distortion performance by 3dB to 6dB.

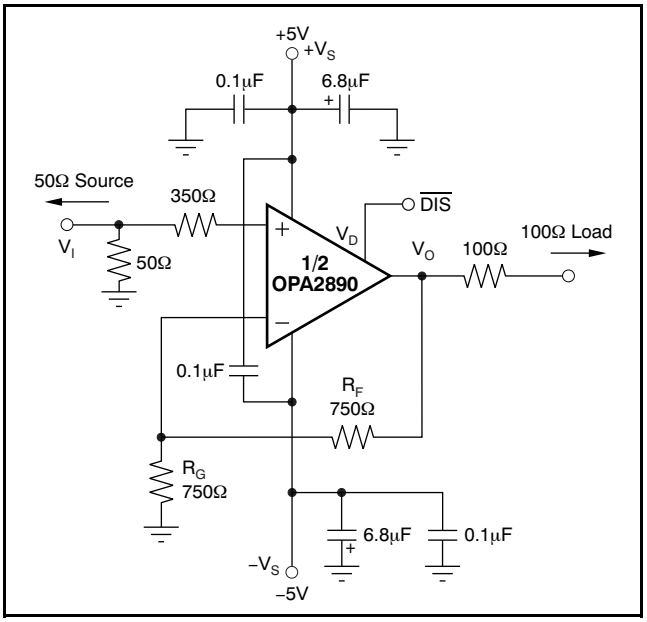

Figure 49. DC-Coupled, G = +2V/V, Bipolar Supply, Specification and Test Circuit

Figure 50 illustrates the ac-coupled, gain of +2V/V, single-supply circuit configuration used as the basis of the +5V Electrical Characteristics and Typical Characteristics. Though not a rail-to-rail design, the OPA2890 requires minimal input and output voltage headroom compared to other very wideband voltage-feedback op amps. It delivers a $3V_{PP}$ output swing on a single +5V supply with greater than 80MHz bandwidth. The key requirement of broadband single-supply operation is to maintain input and output signal swings within the usable voltage ranges at both the input and the output. The circuit of Figure 50 establishes an input midpoint bias using a simple resistive divider from the +5V supply (two 698Ω resistors). Separate bias networks would be required at each input. The input signal is then ac-coupled into the midpoint voltage bias. The input voltage can swing to within 1.5V of either supply pin, giving a $2V_{PP}$ input signal range centered between the supply pins. The input impedance matching resistor (59Ω) used for testing is adjusted to give a 50Ω input load when the parallel combination of the biasing divider network is included.

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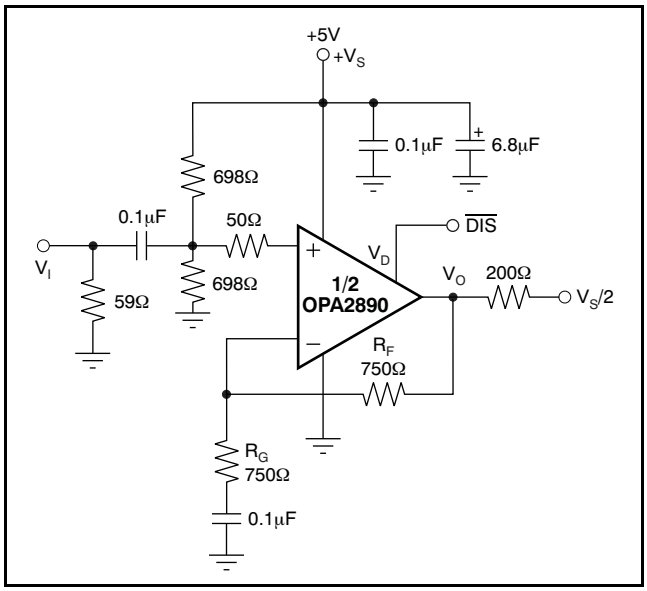

Figure 50. DC-Coupled, G = +2V/V, Single-Supply, Specification and Test Circuit

Again, an additional resistor (50Ω in this case) is included directly in series with the noninverting input. This minimum recommended value provides part of the dc source resistance matching for the noninverting input bias current. It is also used to form a simple parasitic pole to roll off the frequency response at very high frequencies (> 500MHz) using the input parasitic capacitance. The gain resistor (R_G) is AC-coupled, giving the circuit a dc gain of +1V/V, which puts the input dc bias voltage (2.5V) on the output as well. The output voltage can swing to within 1V of either supply pin while delivering greater than 40mA output current.

DIFFERENTIAL OPERATION

Figure 51 shows the inverting differential configuration used as the basis for the ±5V and +5V Typical Characteristics. This circuit offers a combination of excellent distortion with low quiescent current for frequencies below 100kHz.

The other possibility is to use the OPA2890 in a differential configuration as shown in Figure 52. This figure illustrates the differential noninverting configuration that has the advantage of showing a high input impedance to any prior stage.

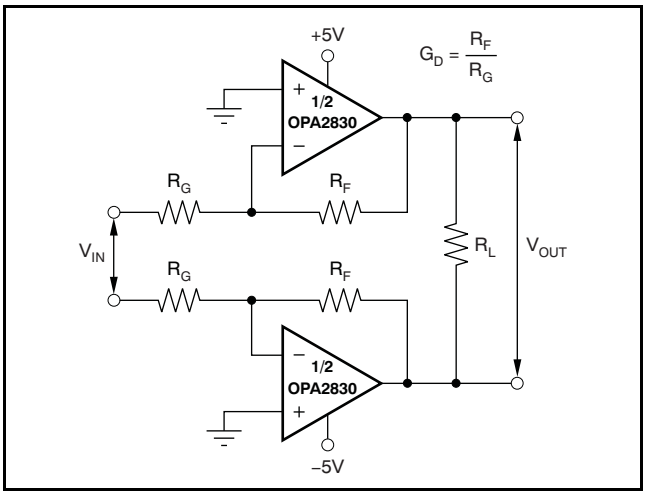

Figure 51. Differential Inverting Specification and Test Circuit

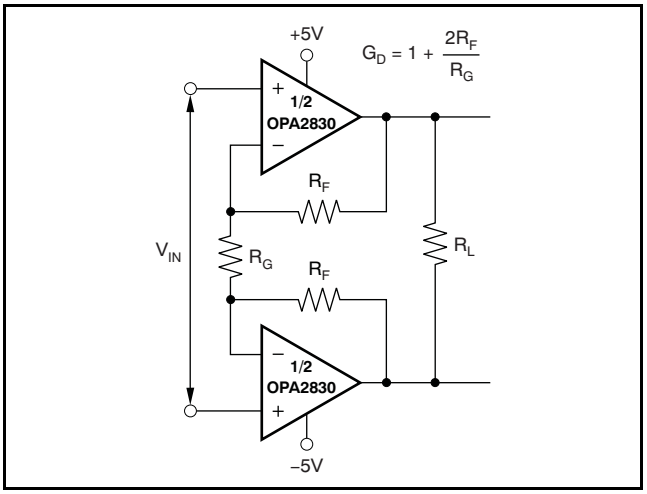

Figure 52. Differential Noninverting Specification and Test Circuit

HIGH-PERFORMANCE DAC TRANSIMPEDANCE AMPLIFIER

High-frequency DDS digital-to-analog converters (DACs) require a low distortion output amplifier to retain SFDR performance into real-world loads. Figure 53 shows a single-ended output drive implementation. The diagram shows the signal output current(s) connected into the virtual ground summing junction(s) of the OPA2890, which is set up as a transimpedance stage or I-V converter. If the DAC requires that its outputs terminate to a compliance voltage other than ground for operation, the appropriate voltage level may be applied to the noninverting input of the OPA2890. The dc gain for this circuit is equal to R_F. At high frequencies, the DAC output capacitance (C_D in Figure 53) produces a zero in the noise gain for the OPA2890 that may cause peaking in the closed-loop frequency response. C_F is added across R_F to compensate for this noise gain peaking. To achieve a flat transimpedance frequency response, the pole in each feedback network should be set to:

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBP}{4\pi R_F C_D}} \quad (1)$$

which gives a cutoff frequency f_{-3dB} of approximately:

$$f_{-3dB} = \sqrt{\frac{GBP}{2\pi R_F C_D}} \quad (2)$$

WIDEBAND VIDEO MULTIPLEXING

One common application for video speed amplifiers that include a disable pin is to wire multiple amplifier outputs together, then select one of several possible video inputs to source onto a single line. This simple wired-OR video multiplexer can be easily implemented using the OP2890IDGS (MSOP-10 package only), as shown in Figure 54.

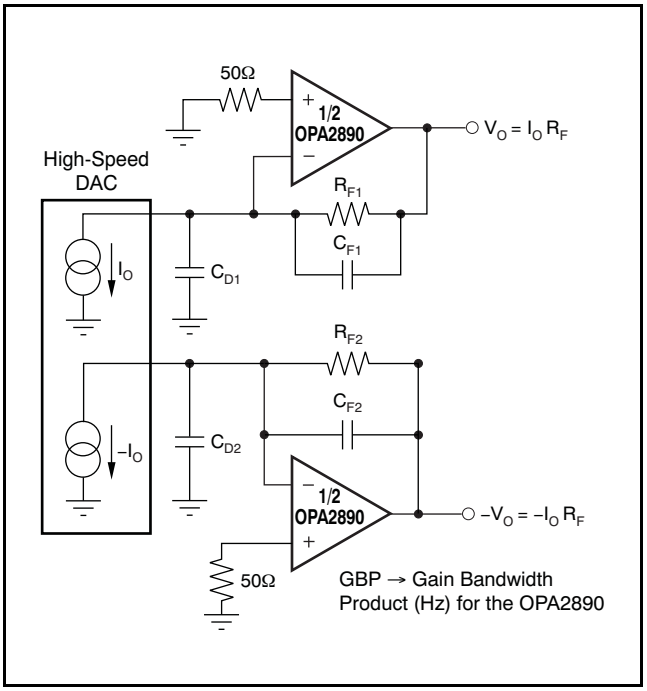

Figure 53. DAC Transimpedance Amplifier

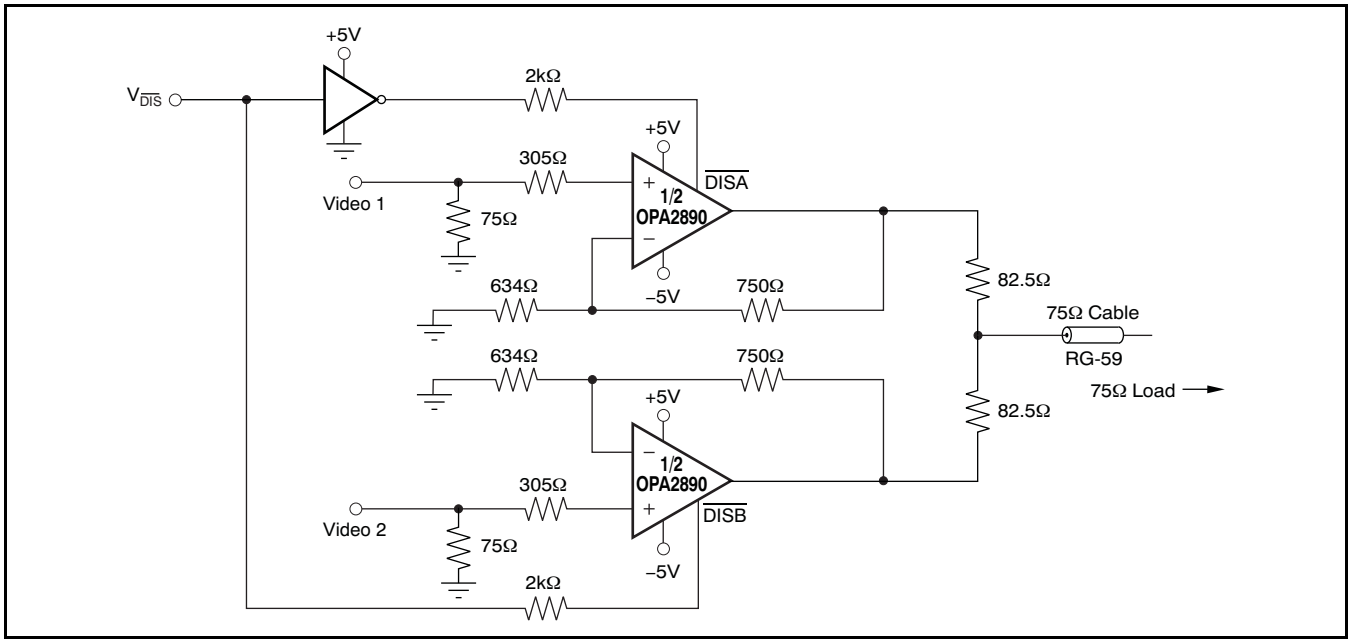

Figure 54. 2-Channel Video Multiplexer (MSOP-10 package only)

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Typically, channel switching is performed either on sync or retrace time in the video signal. The two inputs are approximately equal at this point. The make-before-break disable characteristic of the OPA2890 ensures that there is always one amplifier controlling the line when using a wired-OR circuit such as that shown in Figure 54. Because both inputs may be on for a short period during the transition between channels, the outputs are combined through the output impedance matching resistors (82.5Ω in this case). When one channel is disabled, its feedback network forms part of the output impedance and slightly attenuates the signal in getting out onto the cable. The gain and output matching resistor are slightly increased to get a signal gain of +1V/V at the matched load and provide a 75Ω output impedance to the cable. The video multiplexer connection (see Figure 54) also ensures that the maximum differential voltage across the inputs of the unselected channel does not exceed the rated ±1.2V maximum for standard video signal levels.

See the Disable Operation section for the turn-on and turn-off switching glitches using a 0V input for a single channel is typically less than ±50mV. Where two outputs are switched (see Figure 54), the output line is always under the control of one amplifier or the other as a result of the make-before-break disable timing. In this case, the switching glitches for two 0V inputs drops to less than 20mV.

HIGH-SPEED DELAY CIRCUIT

The OPA2890 makes an ideal amplifier for a variety of active filter designs. Figure 55 illustrates a circuit that uses the two amplifiers within the dual OPA2890 to design a two-stage analog delay circuit. For simplicity, the circuit uses a dual-supply (±5V) operation, but it can also be modified to operate on a signal supply. The input to the first filter stage is driven by the OPA890 as a gain of +2V/V to isolate the signal input from the filter network.

Each of the two filter stages is a 1st-order filter with a voltage gain of +1V/V. The delay time through one filter is given by Equation 3.

$$t_{GR0} = 2RC \quad (3)$$

For a more accurate analysis of the circuit, consider the group delay for the amplifiers. For example, in the case of the OPA2890, the group delay in the bandwidth from 1MHz to 100MHz is approximately 1.0ns. To account for this delay, modify the transfer function, which now comes out to be:

$$t_{GR} = 2\,(2RC + T_D) \quad (4)$$

with $T_D = (1/360) \times (d\varphi/df)$ = delay of the op amp itself. The values of resistors R_F and R_G should be equal and low to avoid parasitic effects. If the all-pass filter is designed for very low delay times, include parasitic board capacitances to calculate the correct delay time. Simulating this application using the PSpice model of the OPA2890 allows this design to be tuned to the desired performance.

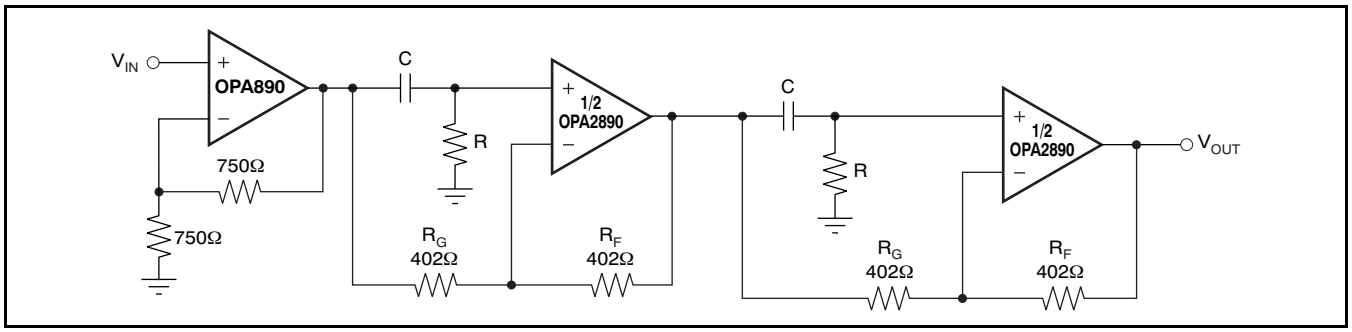

Figure 55. Two-Stage, All-Pass Network

DIFFERENTIAL RECEIVER/DRIVER

A very versatile application for a dual operational amplifier is the differential amplifier configuration shown in Figure 56. With both amplifiers of the OPA2890 connected for noninverting operation, the circuit provides a high input impedance, while the gain can easily be set by just one resistor, R_G. When operated in low gains, the output swing may be limited as a result of the common-mode input swing limits of the amplifier itself. An interesting modification of this circuit is to place a capacitor in series with R_G. Now the dc gain for each side is reduced to +1V/V; the ac gain follows the standard transfer function of G = 1 + $2R_F/R_G$. This configuration might be advantageous for applications processing only a frequency band that excludes dc or very low frequencies. An input dc voltage resulting from input bias currents is not amplified by the ac gain and can be kept low. This circuit can be used as a differential line receiver, driver, or as an interface to a differential input ADC.

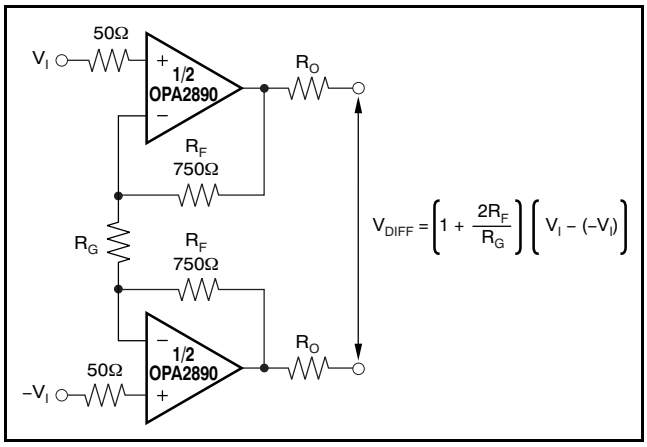

Figure 56. High-Speed Differential Receiver

SINGLE-SUPPLY MFB DIFFERENTIAL ACTIVE FILTER: 2MHz BUTTERWORTH CONFIGURATION

The active filter circuit illustrated in Figure 58 can be easily implemented using the OPA2890. In this configuration, each amplifier of the OPA2890 operates as an integrator. For this reason, this type of application is also called an *infinite gain filter* implementation. A Butterworth filter can be implemented using the following component ratios:

$$f_O = \frac{1}{2 \times \pi \times R \times C}$$

$R_1 = R_2 = 0.65 \times R$

$R_3 = 0.375 \times R$

$C_1 = C$

$C_2 = 2 \times C$

The frequency response for a 2MHz Butterworth filter is shown in Figure 57. One advantage for using this type of filter is the independent setting of ω_o and Q. Q can be easily adjusted by changing the $R_{3A,\ B}$ resistors without affecting ω_o.

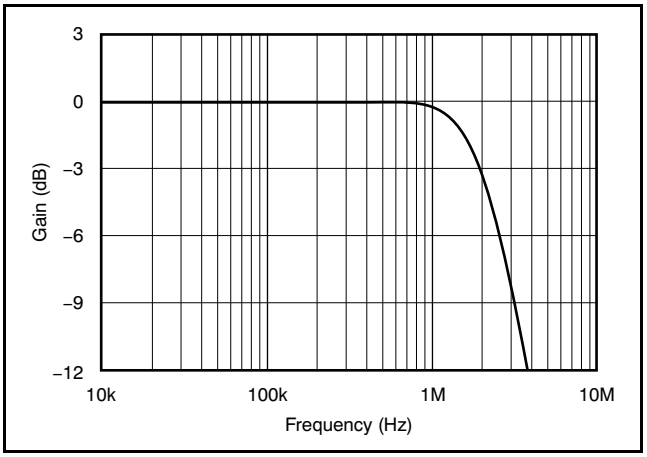

Figure 57. Multiple Feedback Filter Frequency Response

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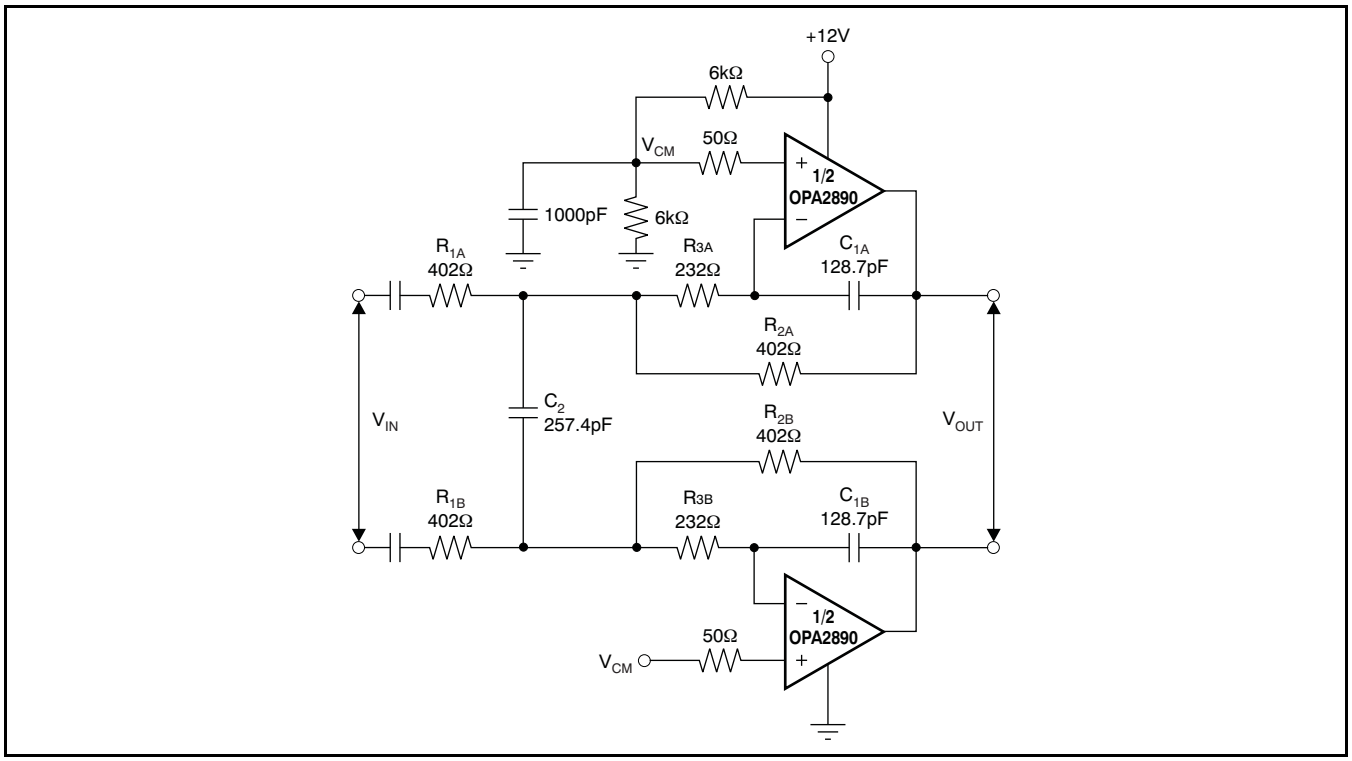

Figure 58. Single-Supply, MFB Active Filter, 2MHz LP Butterworth

DESIGN-IN TOOLS

DEMONSTRATION FIXTURES

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA2890 in its two package options. Both of these are offered free of charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown in Table 1.

Table 1. Demonstration Fixtures by Package

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA2890ID	SO-8	DEM-OPA-SO-2A	SBOU003
OPA2890IDGS	MSOP-10	DEM-OPA-MSOP-2B	SBOU040

The demonstration fixtures can be requested at the Texas Instruments web site (www.ti.com) through the OPA2890 product folder.

MACROMODELS

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This principle is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the OPA2890 (use two OPA890 SPICE models) is available through the Texas Instruments web page (www.ti.com). This model does a good job of predicting small-signal ac and transient performance under a wide variety of operating conditions. It does not do as well in predicting the harmonic distortion or dG/dP characteristics. This model does not attempt to distinguish between the package types in small-signal ac performance.

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OPERATING RECOMMENDATIONS

OPTIMIZING RESISTOR VALUES

Because the OPA2890 is a unity-gain stable, voltage-feedback op amp, a wide range of resistor values may be used for the feedback and gain setting resistors. The primary limits on these values are set by dynamic range (noise and distortion) and parasitic capacitance considerations. For a noninverting unity-gain follower application, the feedback connection should be made with a 25Ω resistor, not a direct short. This feedback resistor isolates the inverting input capacitance from the output pin and improve the frequency response flatness. Usually, the feedback resistor value should be between 200Ω and 1.5kΩ. Below 200Ω, the feedback network presents additional output loading that can degrade the harmonic distortion performance of the OPA2890. Above 1.5kΩ, the typical parasitic capacitance (approximately 0.2pF) across the feedback resistor can cause unintentional band-limiting in the amplifier response.

A good rule of thumb is to target the parallel combination of R_F and R_G (see Figure 49) to be less than approximately 400Ω. The combined impedance $R_F \parallel R_G$ interacts with the inverting input capacitance, placing an additional pole in the feedback network and thus, a zero in the forward response. Assuming a 2pF total parasitic on the inverting node, holding $R_F \parallel R_G < 400\Omega$ keeps this pole above 160MHz. By itself, this constraint implies that the feedback resistor R_F can increase to several kΩ at high gains. This increase in resistor size is acceptable as long as the pole formed by R_F and any parasitic capacitance appearing in parallel is kept out of the frequency range of interest.

BANDWIDTH vs GAIN: NONINVERTING OPERATION

Voltage-feedback op amps exhibit decreasing closed-loop bandwidth as the signal gain increases. In theory, this relationship is described by the Gain Bandwidth Product (GBP) shown in the Electrical Characteristics. Ideally, dividing GBP by the noninverting signal gain (also called the Noise Gain, or NG) predicts the closed-loop bandwidth. In practice, this principle only holds true when the phase margin approaches 90°, as it does in high gain configurations. At low gains (increased feedback factors), most amplifiers exhibit a more complex response with lower phase margin. The OPA2890 is compensated to give a slightly peaked response in a noninverting gain of 2V/V (see Figure 49). This compensation results in a typical gain of +2V/V bandwidth of 100MHz, far exceeding that predicted by dividing the 60MHz GBP by 2. Increasing the gain causes the phase margin to approach 90° and the bandwidth to more closely approach the predicted value of (GBP/NG). At a gain of +10V/V, the 12MHz bandwidth shown in the Electrical Characteristics agrees with that predicted using the simple formula and the typical GBP of 120MHz.

The frequency response in a gain of +2V/V may be modified to achieve exceptional flatness simply by increasing the noise gain to 2.5V/V. One way to modify the response without affecting the +2V/V signal gain, is to add an 1.5kΩ resistor across the two inputs, as illustrated in the circuit of Figure 49. A similar technique may be used to reduce peaking in unity-gain (voltage follower) applications. For example, by using a 750Ω feedback resistor along with a 750Ω resistor across the two op amp inputs, the voltage follower response is similar to the gain of +2V/V response of Figure 50. Reducing the value of the resistor across the op amp inputs further limits the frequency response due to increased noise gain.

The OPA2890 exhibits minimal bandwidth reduction going to single-supply (+5V) operation as compared with ±5V. This feature arises because the internal bias control circuitry retains nearly constant quiescent current as the total supply voltage between the supply pins changes.

INVERTING AMPLIFIER OPERATION

The OPA2890 is a general-purpose, wideband, voltage-feedback op amp; therefore, all of the familiar op amp application circuits are available to the designer. Inverting operation is one of the more common requirements and offers several performance benefits. See Figure 59 for a typical inverting configuration where the I/O impedances and signal gain from Figure 49 are retained in an inverting circuit configuration.

In the inverting configuration, three key design considerations must be noted. The first is that the gain resistor (R_G) becomes part of the signal channel input impedance. If input impedance matching is desired (which is beneficial whenever the signal is coupled through a cable, twisted-pair, long PCB trace, or other transmission line conductor), R_G may be set equal to the required termination value and R_F adjusted to give the desired gain. This consideration is the simplest approach and results in optimum bandwidth and noise performance. However, at low inverting gains, the resultant feedback resistor value can present a significant load to the amplifier output. For an inverting gain of –2V/V, setting R_G to 50Ω for input matching eliminates the need for R_M but requires a 100Ω feedback resistor. This consideration has the interesting advantage that the noise gain becomes equal to 2V/V for a 50Ω source impedance—the same as the noninverting circuits

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discussed in the previous section. The amplifier output, however, now sees the 100Ω feedback resistor in parallel with the external load. In general, the feedback resistor should be limited to the 200Ω to 1.5kΩ range. In this case, it is preferable to increase both the R_F and R_G values (see Figure 56), and then achieve the input matching impedance with a third resistor (R_M) to ground. The total input impedance becomes the parallel combination of R_G and R_M.

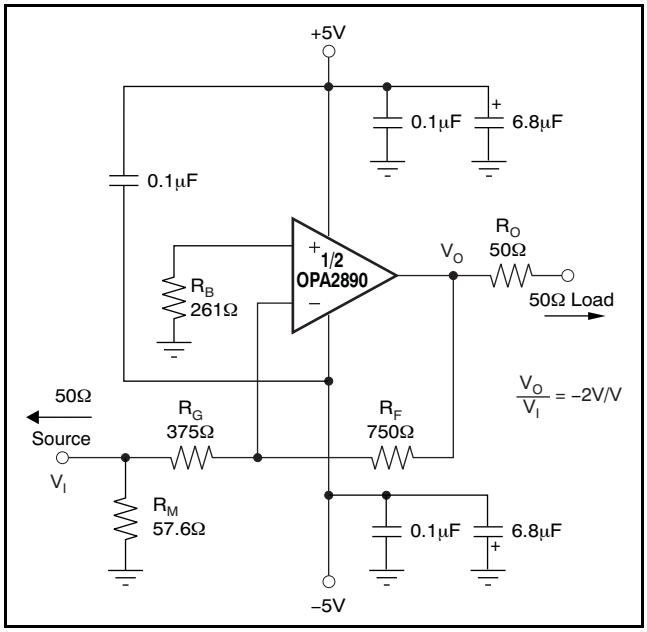

Figure 59. Gain of –2V/V Example Circuit

The second major consideration, touched on in the previous paragraph, is that the signal source impedance becomes part of the noise gain equation and influences the bandwidth. For the example in Figure 59, the R_M value combined in parallel with the external 50Ω source impedance yields an effective driving impedance of 50Ω || 57.6Ω = 26.7Ω. This impedance is added in series with R_G for calculating the noise gain (NG). The resultant NG is 2.86V/V for Figure 59, as opposed to only 2V/V if R_M could be eliminated as discussed above. Therefore, the bandwidth is slightly lower for the gain of –2V/V circuit of Figure 59 than for the gain of +2V/V circuit of Figure 49.

The third important consideration in inverting amplifier design is setting the bias current cancellation resistor on the noninverting input (R_B). If this resistor is set equal to the total dc resistance looking out of the inverting node, the output dc error (as a result of the input bias currents) is reduced to [(Input Offset Current) × R_F]. If the 50Ω source impedance is DC-coupled in Figure 57, the total resistance to ground on the inverting input is 402Ω.

Combining this resistance in parallel with the feedback resistor gives the R_B = 261Ω used in this example. To reduce the additional high-frequency noise introduced by this resistor, it is sometimes bypassed with a capacitor. As long as R_B < 350Ω, the capacitor is not required because the total noise contribution of all other terms is less than that of the op amp input noise voltage. As a minimum, the OPA2890 requires an R_B value of 50Ω to damp out parasitic-induced peaking—a direct short to ground on the noninverting input runs the risk of a very high-frequency instability in the input stage.

DRIVING CAPACITIVE LOADS

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an ADC—including additional external capacitance that may be recommended to improve ADC linearity. A high-speed, high open-loop gain amplifier such as the OPA2890 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the open-loop output resistance of the amplifier is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series-isolation resistor between the amplifier output and the capacitive load. This solution does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Characteristics show the recommended R_S versus capacitive load (see Figure 15 and Figure 36) and the resulting frequency response at the load. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA2890. Long PCB traces, unmatched cables, and connections to multiple devices can easily exceed this value. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA2890 output pin (see the Board Layout Guidelines section).

DISTORTION PERFORMANCE

The OPA2890 provides good distortion performance into a 100Ω load on ±5V supplies. Relative to alternative solutions, it provides exceptional performance into lighter loads and/or operating on a single +5V supply. Generally, until the fundamental

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signal reaches very high frequency or power levels, the 2nd harmonic dominates the distortion with a negligible 3rd harmonic component. Focusing then on the 2nd harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network; in the noninverting configuration (see Figure 49), this value is the sum of $R_F + R_G$, while in the inverting configuration it is only R_F. Also, providing an additional supply-decoupling capacitor (0.1µF) between the supply pins (for bipolar operation) improves the 2nd-order distortion slightly (3dB to 6dB). Operating differentially also lowers 2nd-harmonic distortion terms (see the plot on the front page).

In most op amps, increasing the output voltage swing increases harmonic distortion directly. The output stage used in the OPA2890 holds the difference between fundamental power and the 2nd- and 3rd-harmonic powers relatively constant with increasing output power until very large output swings are required (> $4V_{PP}$). This also shows up in the two-tone, 3rd-order intermodulation spurious (IM3) response curves. The 3rd-order spurious levels are extremely low at low output power levels. The output stage continues to hold them low even as the fundamental power reaches very high levels. As the Typical Characteristics show, the spurious intermodulation powers do not increase as predicted by a traditional intercept model. As the fundamental power level increases, the dynamic range does not decrease significantly. For two tones centered at 10MHz, with 4dBm/tone into a matched 50Ω load (that is, $1V_{PP}$ for each tone at the load, which requires $4V_{PP}$ for the overall two-tone envelope at the output pin), the Typical Characteristics show a 38dBc difference between the test tone powers and the 3rd-order intermodulation spurious powers. This exceptional performance for all 22.5mW internal power dissipation parts improves further when operating at lower frequencies or powers.

NOISE PERFORMANCE

High slew rate, unity-gain stable, voltage-feedback op amps usually achieve the slew rate at the expense of a higher input noise voltage. However, the 8nV/√Hz input voltage noise for the OPA2890 is much lower than that of comparable amplifiers. The input-referred voltage noise, and the two input-referred current noise terms, combine to give low output noise under a wide variety of operating conditions. Figure 60 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

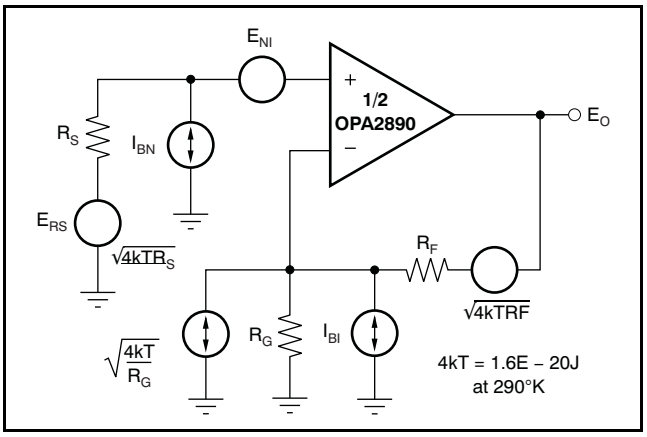

Figure 60. Op Amp Noise Analysis Model

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 5 shows the general form for the output noise voltage using the terms shown in Figure 60.

$$E_O = \sqrt{[E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S]NG^2 + (I_{BI}R_F)^2 + 4kTR_FNG} \quad (5)$$

Dividing this expression by the noise gain (NG = (1 + R_F/R_G)) gives the equivalent input-referred spot noise voltage at the noninverting input, as shown in Equation 6.

$$E_N = \sqrt{E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \quad (6)$$

Evaluating these two equations for the OPA2890 circuit and component values (see Figure 49) gives a total output spot noise voltage of 17.5nV/√Hz and a total equivalent input spot noise voltage of 8.7nV/√Hz. This result includes the noise added by the bias current cancellation resistor (350Ω) on the noninverting input. This total input-referred spot noise voltage is only slightly higher than the 8nV/√Hz specification for the op amp voltage noise alone. This result is the case as long as the impedances appearing at each op amp input are limited to the previously recommend maximum value of 400Ω. Keeping both (R_F || R_G) and the noninverting input source impedance less than 400Ω satisfies both noise and frequency response flatness considerations. Because the resistor-induced noise is relatively negligible, additional capacitive decoupling across the bias current cancellation resistor (R_B) for the inverting op amp configuration of Figure 59 is not required.

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DC ACCURACY AND OFFSET CONTROL

The balanced input stage of a wideband voltage-feedback op amp allows good output dc accuracy in a wide variety of applications. The power-supply current trim for the OPA2890 gives even tighter control than comparable amplifiers. Although the high-speed input stage does require relatively high input bias current (typically 5μA out of each input terminal), the close matching between them may be used to reduce the output dc error caused by this current. The total output offset voltage may be considerably reduced by matching the dc source resistances appearing at the two inputs. This matching reduces the output dc error resulting from the input bias currents to the offset current times the feedback resistor. Evaluating the configuration of Figure 49, and using worst-case +25°C input offset voltage and current specifications, gives a worst-case output offset voltage equal to:

$\pm(NG \times V_{OS(MAX)}) \pm (R_F \times I_{OS(MAX)})$

$= \pm(2 \times 5mV) \pm (750\Omega \times 1.6\mu A)$

$= \pm 11.2mV$ with $-(NG$ = noninverting signal gain)

A fine-scale output offset null, or dc operating point adjustment, is often required. Numerous techniques are available for introducing dc offset control into an op amp circuit. Most of these techniques eventually reduce to adding a dc current through the feedback resistor. In selecting an offset trim method, one key consideration is the impact on the desired signal path frequency response. If the signal path is intended to be noninverting, the offset control is best applied as an inverting summing signal to avoid interaction with the signal source. If the signal path is intended to be inverting, applying the offset control to the noninverting input may be considered. However, the dc offset voltage on the summing junction sets up a dc current back into the source that must be considered. Applying an offset adjustment to the inverting op amp input can change the noise gain and frequency response flatness. For a DC-coupled inverting amplifier, Figure 61 shows one example of an offset adjustment technique that has minimal impact on the signal frequency response. In this case, the dc offsetting current is brought into the inverting input node through resistor values that are much larger than the signal path resistors. This configuration ensures that the adjustment circuit has minimal effect on the loop gain and thus, the frequency response.

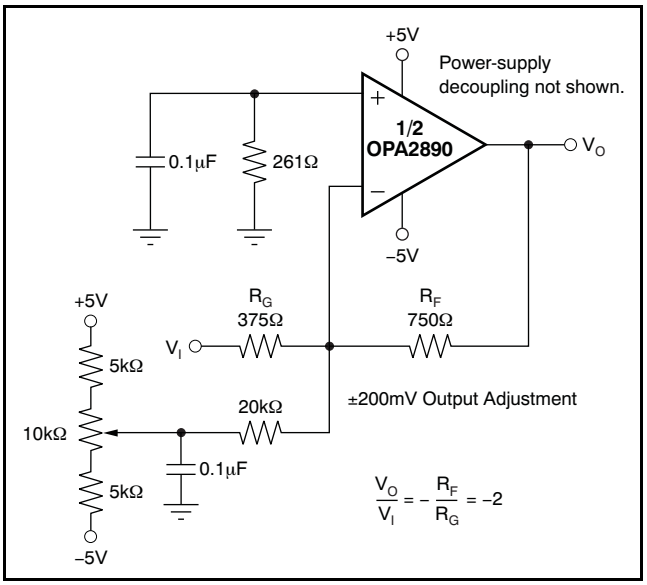

Figure 61. DC-Coupled, Inverting Gain of –2, with Offset Adjustment

DISABLE OPERATION (MSOP-10 Package Only)

The OPA2890IDGS provides an optional disable feature that can be used either to reduce system power or to implement a simple channel multiplexing operation. If the $\overline{DIS}$ control pin is left unconnected, the OPA2890IDGS operates normally. To disable, the control pin must be asserted LOW. Figure 62 shows a simplified internal circuit for the disable control feature.

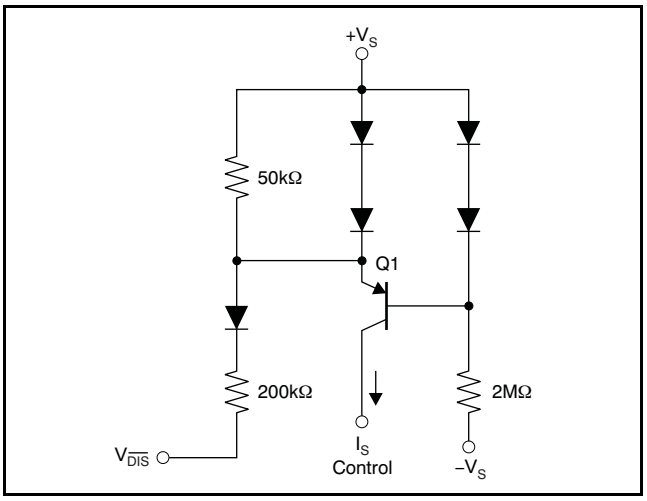

Figure 62. Simplified Disable Control Circuit

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In normal operation, base current to Q1 is provided through the 2MΩ resistor, while the emitter current through the 50kΩ resistor sets up a voltage drop that is inadequate to turn on the two diodes in the Q1 emitter. As $V_{\overline{DIS}}$ is pulled LOW, additional current is pulled through the 50kΩ resistor, eventually turning on those two diodes (30µA). At this point, any further current pulled out of $V_{\overline{DIS}}$ goes through those diodes holding the emitter-base voltage of Q1 at approximately 0V. This current shuts off the collector current out of Q1, turning the amplifier off. The supply currents in the disable mode are only those required to operate the circuit of Figure 62. Additional circuitry ensures that turn-on time occurs faster than turn-off time (make-before-break).

When disabled, the output and input nodes go to a high-impedance state. If the OPA2890 is operating at a gain of +1V/V, the device shows a very high impedance at the output and exceptional signal isolation. If operating at a gain greater than +1V/V, the total feedback network resistance (R_F + R_G) appears as the impedance looking back into the output, but the circuit still shows very high forward and reverse isolation. If configured as an inverting amplifier, the input and output are connected through the feedback network resistance (R_F + R_G) and the isolation is very poor as a result.

THERMAL ANALYSIS

Maximum desired junction temperature sets the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed +150°C.

Operating junction temperature (T_J) is given by T_A + $P_D \times \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load; for a grounded resistive load, P_{DL} is at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for equal bipolar supplies). Under this condition, $P_{DL} = V_S{}^2/(4 \times R_L)$, where R_L includes feedback network loading.

Note that it is the power in the output stage and not into the load that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA2890ID (SO-8 package) in the circuit of Figure 49 operating at the maximum specified ambient temperature of +85°C and with both outputs driving a grounded 20Ω load to +2.5V.

$P_D = 10V \times 2.5mA + 2[5^2/(4 \times (75\Omega \parallel 1.5k\Omega))] = 200mW$

Maximum $T_J = +85°C + (0.2W \times 125°C/W) = 110°C$

This absolute worst-case condition does not exceed the specified maximum junction temperature. Actual P_{DL} is normally less than that considered here. Carefully consider maximum T_J in your application.

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BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier such as the OPA2890 requires careful attention to board layout parasitics and external component types. Recommendations that optimize performance include:

a) Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability: on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25in, or 6.35mm) from the power-supply pins to high-frequency 0.1µF decoupling capacitors. At the device pins, the ground and power-plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. An optional supply decoupling capacitor (0.1µF) across the two power supplies (for bipolar operation) improves 2nd-harmonic distortion performance. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequencies, should also be used on the main supply pins. These capacitors may be placed somewhat farther from the device and may be shared among several devices in the same area of the printed circuit board (PCB).

c) Careful selection and placement of external components preserves the high-frequency performance of the OPA2890. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film or carbon composition axially-leaded resistors can also provide good high-frequency performance. Again, keep the leads and PCB traces as short as possible. Never use wirewound type resistors in a high-frequency application. Because the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal film or surface-mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values > 1.5kΩ, this parasitic capacitance can add a pole and/or zero below 500MHz that can effect circuit operation. Keep resistor values as low as possible consistent with load driving considerations. The 750Ω feedback used in the Electrical Characteristics is a good starting point for design. Note that a 0Ω feedback resistor is suggested for the unity-gain follower application.

d) Connections to other wideband devices on the board may be made with short, direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils, or 1.27mm to 2.54mm) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plots of Figure 15 and Figure 36. Low parasitic capacitive loads (< 3pF) may not need an R_S because the OPA2890 is nominally compensated to operate with a 2pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed as the signal gain increases (increasing the unloaded phase margin; see **Figure 61**). If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary on board, and in fact, a higher impedance environment improves distortion as shown in the distortion versus load plots. With a characteristic board trace impedance defined (based on board material and trace dimensions), a matching series resistor into the trace from the output of the OPA2890 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device; this total effective impedance should be set to match the trace impedance.

e) Socketing a high-speed part such as the OPA2890 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network that can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA2890 onto the board.

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INPUT AND ESD PROTECTION

The OPA2890 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 63.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±15V supply parts driving into the OPA2890), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response.

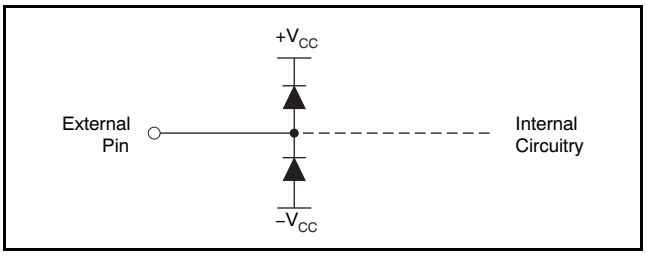

Figure 63. Internal ESD Protection

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May 2008) to Revision C **Page**

- Changed min/max over temperature specifications for the Input, *Common-mode input range (CMIR)* parameter of the ±5V electrical characteristics table 3
- Changed min/max over temperature specifications for the Input, *Most positive input voltage* parameter of the +5V electrical characteristics table 5
- Changed min/max over temperature specifications for the Input, *Least positive input voltage* parameter of the +5V electrical characteristics table 5
- Corrected x-axis of Figure 18 9

Changes from Revision A (December 2007) to Revision B **Page**

- Changed storage temperature range rating in *Absolute Maximum Ratings* table from –40°C to +125°C to –65°C to +125°C 2
- Changed typical specification from *15* to *±15* in minimum operating voltage parameter of *Power Supply* section of ±5V Electrical Characteristics 3

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2890ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2890	Samples
OPA2890IDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BPQ	Samples
OPA2890IDGST	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BPQ	Samples
OPA2890IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2890	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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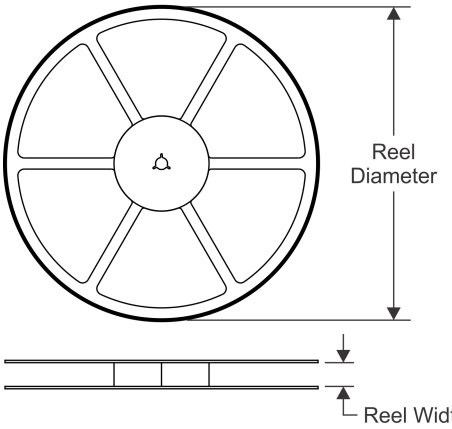
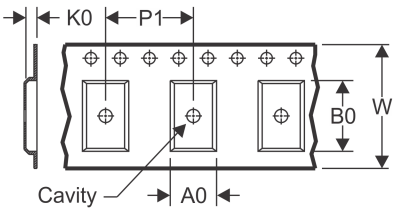
TAPE AND REEL INFORMATION

REEL DIMENSIONS

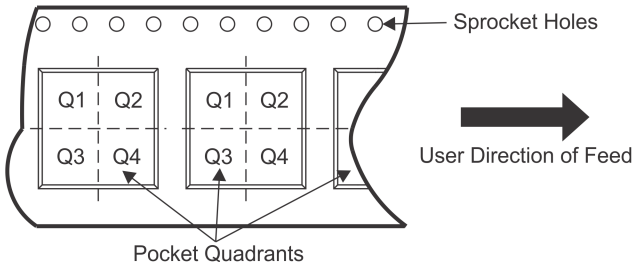


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

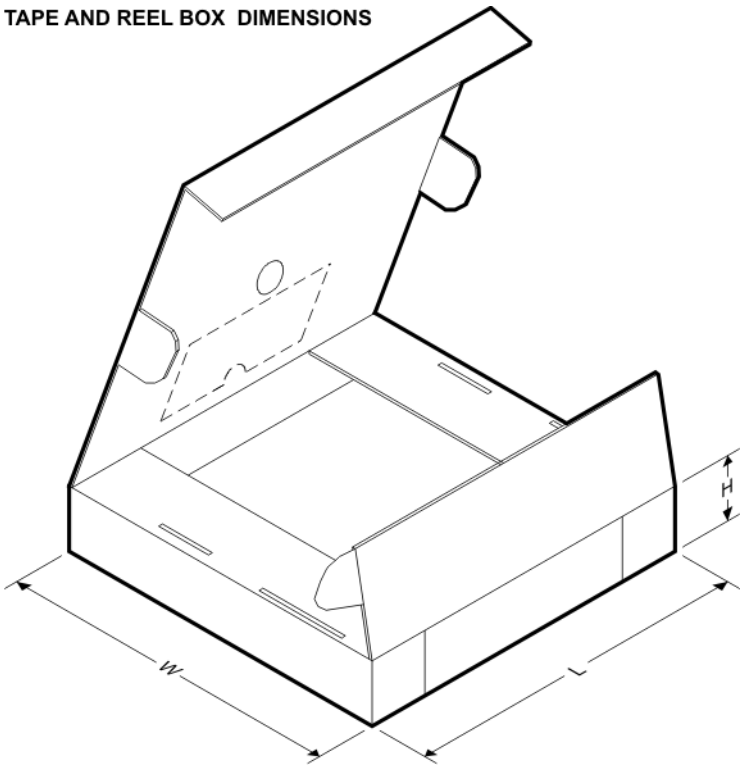
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2890IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2890IDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2890IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

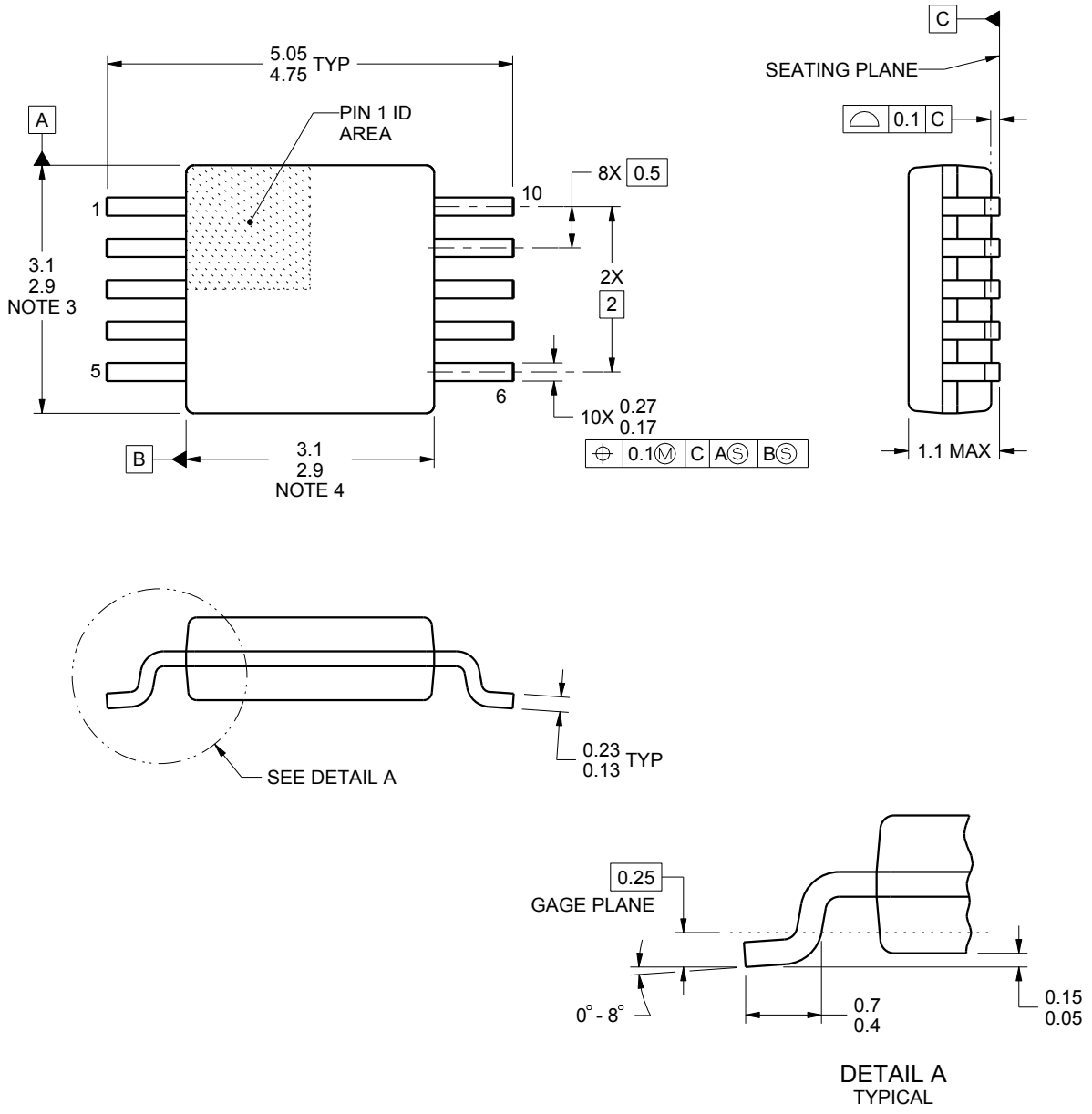
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2890IDGSR	VSSOP	DGS	10	2500	367.0	367.0	35.0
OPA2890IDGST	VSSOP	DGS	10	250	210.0	185.0	35.0
OPA2890IDR	SOIC	D	8	2500	367.0	367.0	35.0

PACKAGE OUTLINE

DGS0010A

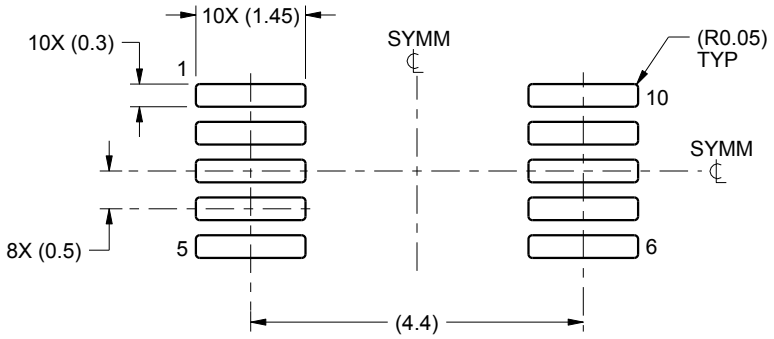
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

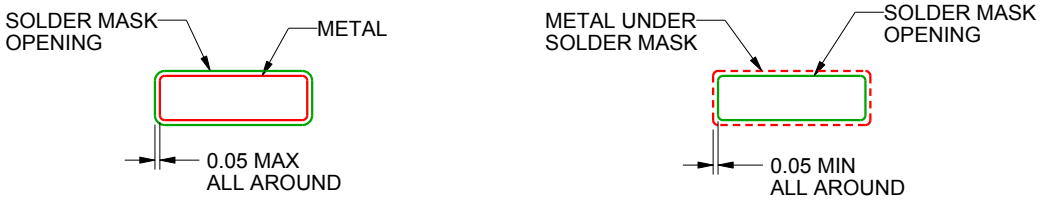


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

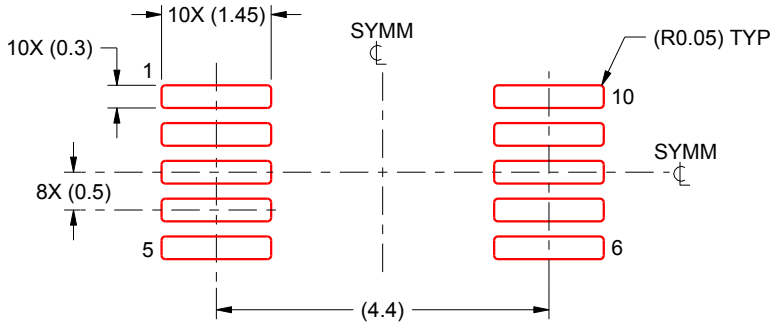


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

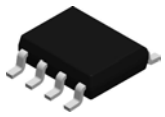


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

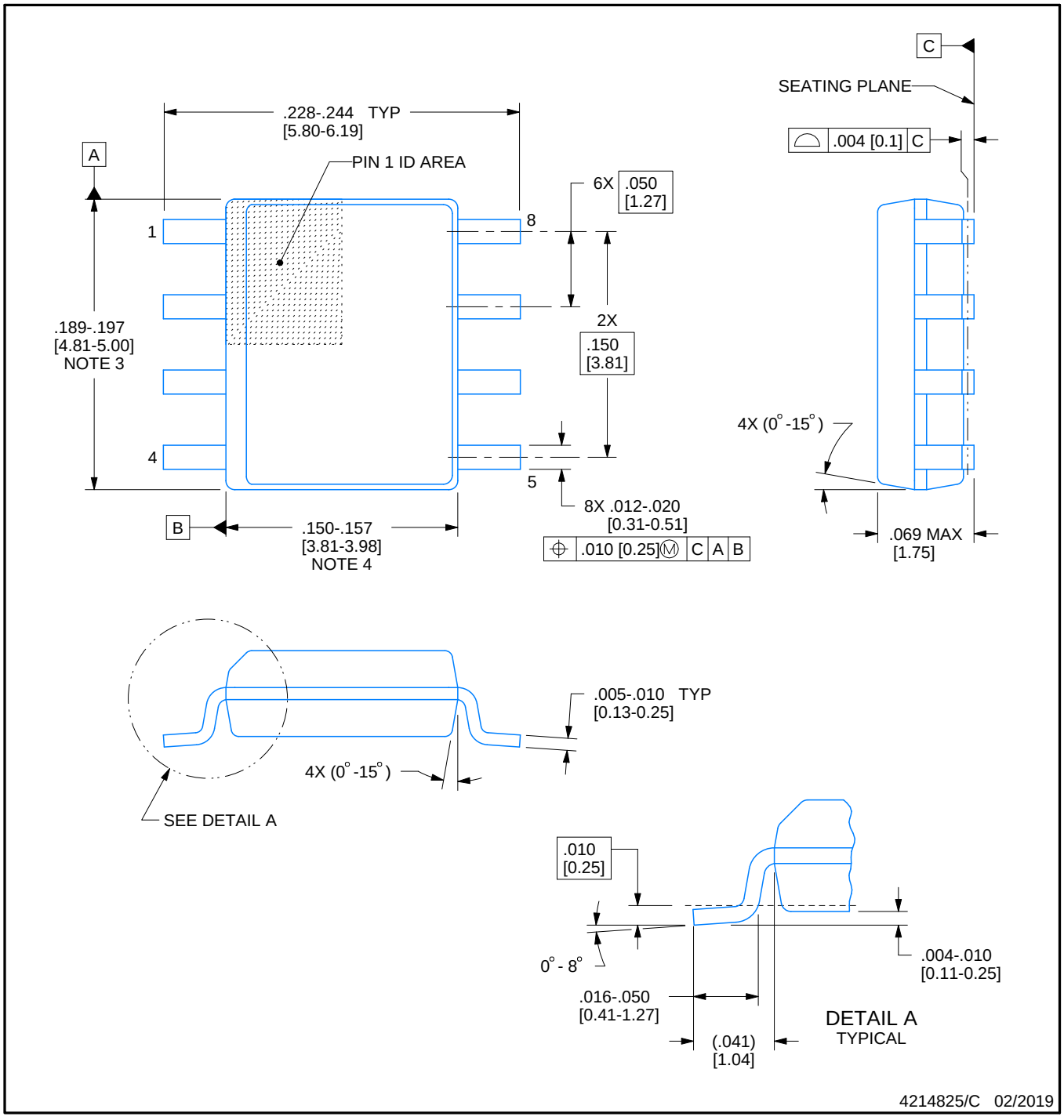


PACKAGE OUTLINE

D0008A

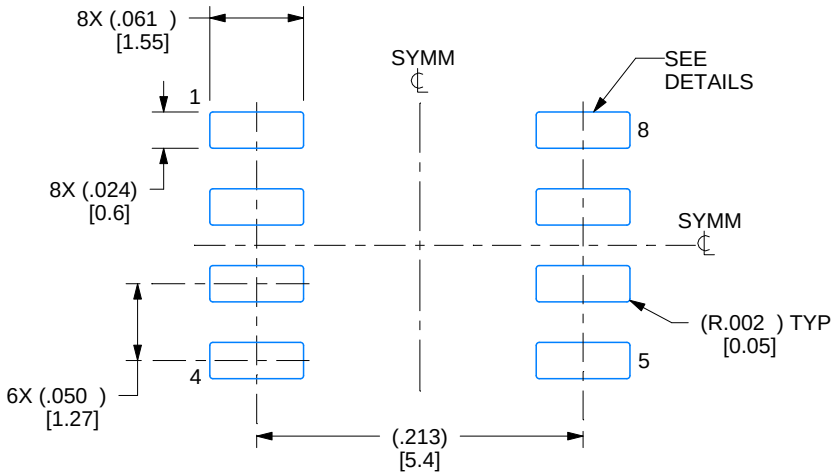
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

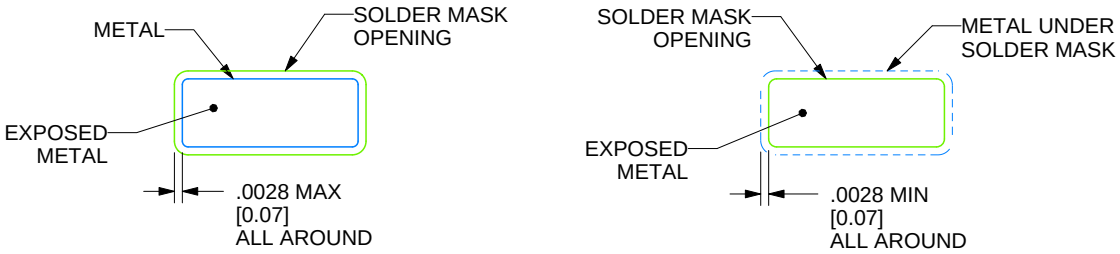


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

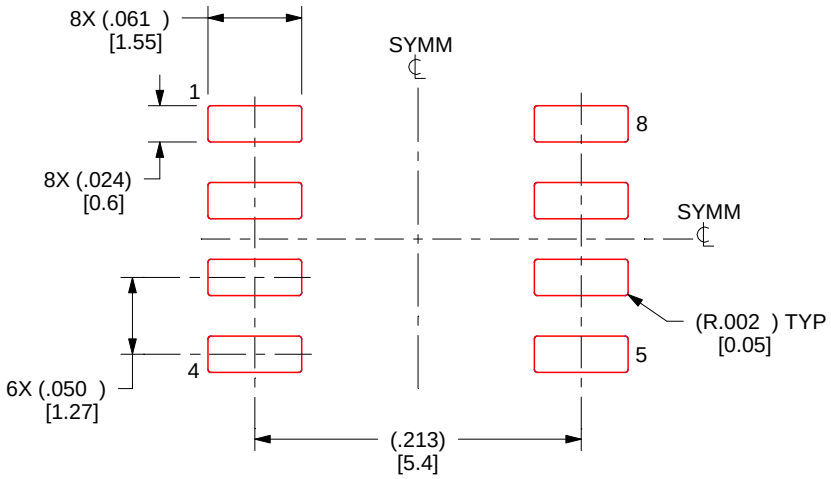
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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