

Dual, Wideband, High Output Current Operational Amplifier

FEATURES

- WIDEBAND +12V OPERATION: 200MHz (G = +4)
- UNITY-GAIN STABLE: 220MHz (G = +1)
- HIGH OUTPUT CURRENT: 500mA
- OUTPUT VOLTAGE SWING: ±5V
- HIGH SLEW RATE: 1800V/μs
- LOW SUPPLY CURRENT: 18mA
- FLEXIBLE SUPPLY RANGE:
  +5 to +12V Single Supply
  ±2.5 to ±6V Dual Supplies

APPLICATIONS

- xDSL LINE DRIVER
- CABLE MODEM DRIVER
- MATCHED I/Q CHANNEL AMPLIFIER
- BROADBAND VIDEO LINE DRIVER
- ARB LINE DRIVER
- POWER LINE MODEM
- HIGH CAP LOAD DRIVER

DESCRIPTION

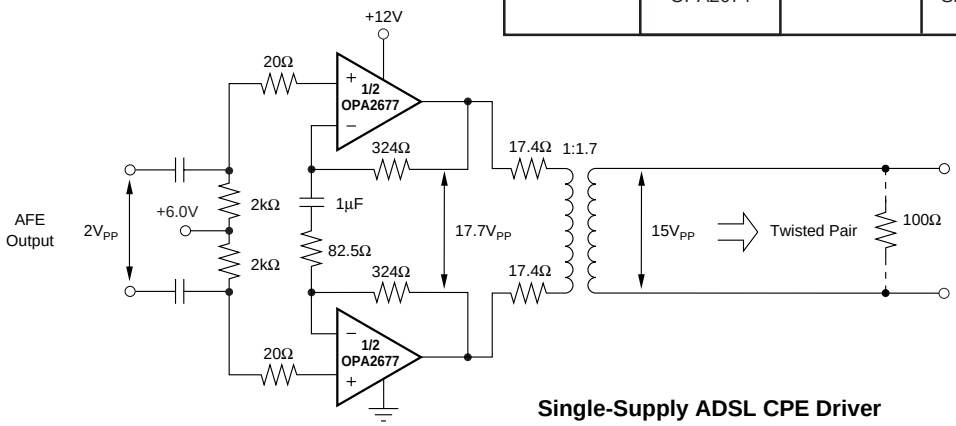
The OPA2677 provides the high output current and low distortion required in emerging xDSL and Power Line Modem driver applications. Operating on a single +12V supply, the OPA2677 consumes a low 9mA/ch quiescent current to deliver a very high 500mA output current. This output current supports even the most demanding ADSL CPE requirements with > 380mA minimum output current (+25°C minimum value) with low harmonic distortion. Differential driver applications will deliver < –85dBc distortion at the peak upstream power levels of full rate ADSL. The high 200MHz bandwidth will also support the most demanding VDSL line driver requirements.

Specified on ±6V supplies (to support +12V operation), the OPA2677 will also support a single +5V or dual ±5V supply. Video applications will benefit from its very high output current to drive up to 10 parallel video loads (15Ω) with < 0.1%/0.1° dG/dP nonlinearity.

The OPA2677 is available in either an SO-8 or QFN-16 and an HSOP-8 PowerPAD™ package.

OPA2677 RELATED PRODUCTS

SINGLES	DUALS	TRIPLES	NOTES
OPA691	OPA2691	OPA3691	Single +12V Capable
—	THS6042	—	±15V Capable
—	OPA2674	—	Single +12V Capable with current limit



Single-Supply ADSL CPE Driver

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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ABSOLUTE MAXIMUM RATINGS(1)

Power Supply	±6.5V_{DC}
Internal Power Dissipation	See Thermal Characteristics
Differential Input Voltage	±1.2V
Input Common-Mode Voltage Range	±V_S
Storage Temperature Range: U, DDA, RGV	–65°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature (T_J)	+150°C
ESD Rating:	
Human Body Model (HBM)(2)	2000V
Charge Device Model (CDM)	1000V
Machine Model (MM)	100V

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.
(2) Pins 2 and 6 on SO-8 and HSOP-8 packages, and pins 2 and 11 on QFN-16 package > 500V HBM.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

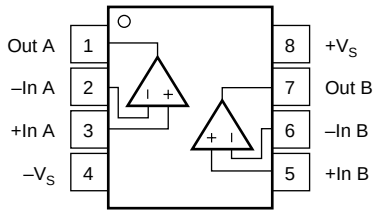
PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA2677	SO-8	D	–40°C to +85°C	OPA2677U	OPA2677U	Rails, 100
"	"	"	"	"	OPA2677U/2K5	Tape and Reel, 2500
OPA2677	HSOP-8	DDA	–40°C to +85°C	OP2677	OPA2677IDDA	Rails, 75
"	"	"	"	"	OPA2677IDDAR	Tape and Reel, 2500
OPA2677	QFN-16	RGV	–40°C to +85°C	OPA2677	OPA2677IRGVT	Tape and Reel, 250
					OPA2677IRGVR	Tape and Reel, 2500

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

PIN CONFIGURATIONS

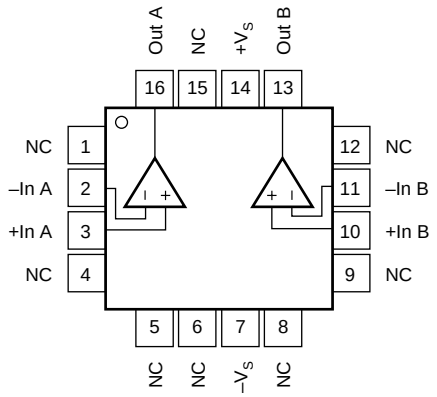
Top View

OPA2677U, DDA



SO-8, HSOP-8

OPA2677RGV



QFN-16

NOTE: Exposed thermal pad on HSOP-8 and QFN-16 must be tied to –V_S.

ELECTRICAL CHARACTERISTICS: V_S = ±6V

Boldface limits are tested at **+25°C.**

At T_A = +25°C, G = +4, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted. See Figure 1 for AC performance only.

PARAMETER	CONDITIONS	OPA2677U, DDA, RGV						
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	0°C to 70°C(2)	–40°C to +85°C(2)	UNITS	MIN/ MAX	TEST LEVEL(3)
AC PERFORMANCE (see Figure 1)								
Small-Signal Bandwidth (V_O = 0.5V_{PP})	G = +1, R_F = 511Ω	220				MHz	min	B
	G = +2, R_F = 475Ω	200	170	168	165	MHz	min	B
	G = +4, R_F = 402Ω	200	170	168	165	MHz	min	B
	G = +8, R_F = 250Ω	250	225	205	200	MHz	min	B
Peaking at a Gain of +1	G = +1, R_F = 511Ω	0				dB	typ	C
Bandwidth for 0.1dB Gain Flatness	G = +4, V_O = 0.5V_{PP}	80	36	32	30	MHz	min	B
Large-Signal Bandwidth	G = +4, V_O = 5V_{PP}	200				MHz	typ	C
Slew Rate	G = +4, 5V Step	2000	1500	1450	1400	V/µs	min	B
Rise-and-Fall Time	G = +4, V_O = 2V Step	1.75				ns	typ	C
Harmonic Distortion	G = +4, f = 5MHz, V_O = 2V_{PP}							
2nd-Harmonic	R_L = 100Ω	–72	–70	–69	–68	dBc	max	B
	R_L ≥ 500Ω	–82	–80	–79	–78	dBc	max	B
3rd-Harmonic	R_L = 100Ω	–81	–80	–79	–78	dBc	max	B
	R_L ≥ 500Ω	–93	–91	–90	–89	dBc	max	B
Input Voltage Noise	f > 1MHz	2	2.6	2.9	3.1	nV/√Hz	max	B
Noninverting Input Current Noise	f > 1MHz	16	20	21	22	pA/√Hz	max	B
Inverting Input Current Noise	f > 1MHz	24	29	30	31	pA/√Hz	max	B
NTSC Differential Gain	NTSC, G = +2, R_L = 150Ω	0.03				%	typ	C
	NTSC, G = +2, R_L = 37.5Ω	0.05				%	typ	C
NTSC Differential Phase	NTSC, G = +2, R_L = 150Ω	0.01				degrees	typ	C
	NTSC, G = +2, R_L= 37.5Ω	0.04				degrees	typ	C
Channel-to-Channel Crosstalk	f = 5MHz, Input Referred	–92				dB	typ	C
DC PERFORMANCE(4)								
Open-Loop Transimpedance Gain	V_O = 0V, R_L = 100Ω	135	**80**	76	75	kΩ	min	A
Input Offset Voltage	V_{CM} = 0V	±1.0	**±4.5**	±5	±5.3	mV	max	A
Average Offset Voltage Drift	V_{CM} = 0V	±4	±10	±10	±12	µV/°C	max	B
Noninverting Input Bias Current	V_{CM} = 0V	±10	**±30**	±32	±35	µA	max	A
Average Noninverting Input Bias Current Drift	V_{CM} = 0V	±5	±50	±50	±75	nA/°C	max	B
Inverting Input Bias Current	V_{CM} = 0V	±10	**±35**	±40	±45	µA	max	A
Average Inverting Input Bias Current Drift	V_{CM} = 0V	±10	±100	±100	±150	nA°/C	max	B
INPUT(4)								
Common-Mode Input Range (CMIR)(5)		±4.5	**±4.1**	±4.0	±3.9	V	min	A
Common-Mode Rejection Ratio (CMRR)	V_{CM} = 0V, Input Referred	55	**51**	50	49	dB	min	A
Noninverting Input Impedance		250 || 2				kΩ || pF	typ	C
Minimum Inverting Input Resistance	Open-Loop	22	12			Ω	min	B
Maximum Inverting Input Resistance	Open-Loop	22	35			Ω	max	B
OUTPUT(4)								
Voltage Output Swing	No Load	±5.1	**±4.9**	±4.8	±4.7	V	min	A
	R_L = 100Ω	±5.0	**±4.8**	±4.7	±4.5	V	min	A
	R_L = 25Ω	±4.8				V	typ	C
Current Output	V_O = 0	±500	**±380**	±350	±320	mA	min	A
Peak Current Output, Sourcing(6)	V_O = 0	1.2				A	typ	C
Peak Current Output, Sinking(6)	V_O = 0	–1.6				A	typ	C
Closed-Loop Output Impedance	G = +4, f ≤ 100kHz	0.003				Ω	typ	C
POWER SUPPLY								
Specified Operating Voltage		±6				V	typ	C
Maximum Operating Voltage			**±6.3**	±6.3	±6.3	V	max	A
Minimum Operating Voltage		±2				V	typ	C
Maximum Quiescent Current	V_S = ±6V, Both Channels	18	**18.6**	18.8	19.5	mA	max	A
Minimum Quiescent Current	V_S = ±6V, Both Channels	18	**17.4**	16.5	16.0	mA	min	A
Power-Supply Rejection Ratio (PSRR)	f = 100kHz, Input Referred	56	**51**	49	48	dB	min	A
THERMAL CHARACTERISTICS								
Specification: U, DDA, RGV		–40 to +85				°C		
Thermal Resistance, θ_{JA}	Junction-to-Ambient							
U SO-8		125				°C/W	typ	C
DDA HSOP-8	Exposed Slug Soldered to Board	55				°C/W	typ	C
RGV QFN-16	Exposed Slug Soldered to Board	50(7)				°C/W	typ	C

NOTES: (1) Junction temperature = ambient for +25°C specifications.
(2) Junction temperature = ambient at low temperature limit; junction temperature = ambient +23°C at high temperature limit for over temperature specifications.
(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(4) Current is considered positive out of node. V_{CM} is the input common-mode voltage.
(5) Tested < 3dB below minimum CMRR specifications at ±CMIR limits.
(6) Peak output duration should not exceed junction temperature +150°C for extended periods.
(7) Not connecting the exposed slug to the $–V_J$ plane gives 75°C/W thermal impedance (θ_{JA}).

ELECTRICAL SPECIFICATIONS: V_S = +5V

Boldface limits are tested at **+25°C.**

At T_A = +25°C, G = +4, R_F = 453Ω, and R_L = 100Ω, unless otherwise noted. See Figure 3 for AC performance only.

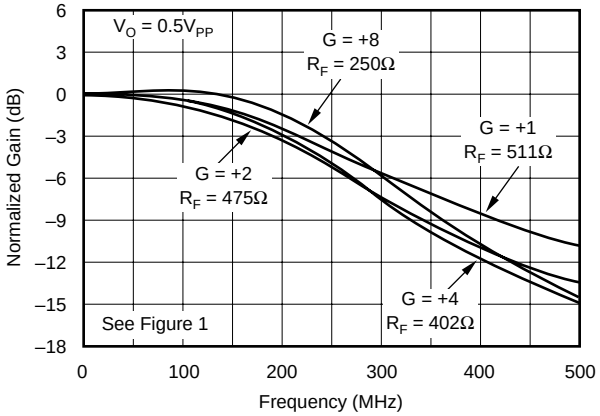
PARAMETER	CONDITIONS	OPA2677U, DDA, RGV						
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C[1]	0°C to 70°C[2]	–40°C to +85°C[2]	UNITS	MIN/ MAX	TEST LEVEL[3]
AC PERFORMANCE (see Figure 3)								
Small-Signal Bandwidth (V_O = 0.5V_{PP})	G = +1, R_F = 536Ω	160				MHz	min	B
	G = +2, R_F = 511Ω	150	120	118	115	MHz	min	B
	G = +4, R_F = 453Ω	150	130	128	125	MHz	min	B
	G = +8, R_F = 332Ω	160	130	128	125	MHz	min	B
Peaking at a Gain of +1	G = +1, R_F = 511Ω	0				dB	typ	C
Bandwidth for 0.1dB Gain Flatness	G = +4, V_O = 0.5V_{PP}	70	23	20	19	MHz	min	B
Large-Signal Bandwidth	G = +4, V_O = 2V_{PP}	100				MHz	typ	C
Slew Rate	G = +4, 2V Step	1100	830	827	825	V/µs	min	B
Rise-and-Fall Time	G = +4, V_O = 2V Step	2				ns	typ	C
Harmonic Distortion	G = +4, f = 5MHz, V_O = 2V_{PP}							
2nd-Harmonic	R_L = 100Ω	–67	–65	–64	–63	dBc	max	B
	R_L ≥ 500Ω	–71	–68	–67	–66	dBc	max	B
3rd-Harmonic	R_L = 100Ω	–72	–70	–69	–68	dBc	max	B
	R_L ≥ 500Ω	–74	–71	–70	–69	dBc	max	B
Input Voltage Noise	f > 1MHz	2	2.6	2.9	3.1	nV/√Hz	max	B
Noninverting Input Current Noise	f > 1MHz	16	20	21	22	pA/√Hz	max	B
Inverting Input Current Noise	f > 1MHz	24	29	30	31	pA/√Hz	max	B
Channel-to-Channel Crosstalk	f = 5MHz, Input Referred	–92				dB	typ	C
DC PERFORMANCE								
Open-Loop Transimpedance Gain	V_O = 0V, R_L = 100Ω	110	**72**	70	68	kΩ	min	A
Input Offset Voltage	V_{CM} = 0V	±0.8	**±3.5**	±4.0	±4.3	mV	max	A
Average Offset Voltage Drift	V_{CM} = 0V	±4	±10	±10	±12	µV/°C	max	B
Noninverting Input Bias Current	V_{CM} = 0V	±10	**±30**	±32	±35	µA	max	A
Average Noninverting Input Bias Current Drift	V_{CM} = 0V	±5	±50	±50	±75	nA/°C	max	B
Inverting Input Bias Current	V_{CM} = 0V	±10	**±30**	±40	±45	µA	max	A
Average Inverting Input Bias Current Drift	V_{CM} = 0V	±10	±100	±100	±150	nA°/C	max	B
INPUT								
Most Positive Input Voltage		3.7	**3.3**	3.2	3.1	V	min	A
Most Negative Input Voltage		1.3	**1.7**	1.8	1.9	V	min	A
Common-Mode Rejection Ratio (CMRR)	V_{CM} = 2.5V, Input Referred	52	**49**	48	47	dB	min	A
Noninverting Input Impedance		250 || 2				kΩ || pF	typ	C
Minimum Inverting Input Resistance	Open-Loop	25	15			kΩ	min	B
Maximum Inverting Input Resistance	Open-Loop	25	40			kΩ	max	B
OUTPUT								
Most Positive Output Voltage	No Load	4.1	**3.9**	3.8	3.6	V	min	A
	R_L = 100Ω	3.5	**3.8**	3.7	3.5	V	min	A
Least Positive Output Voltage	No Load	0.8	**1.0**	1.1	1.3	V	min	A
	R_L = 100Ω	1.0	**1.1**	1.2	1.5	V	min	A
Current Output	V_O = 0	±300	**±200**	±180	±100	mA	min	A
Closed-Loop Output Impedance	G = +4, f ≤ 100kHz	0.02				Ω	typ	C
POWER SUPPLY								
Specified Operating Voltage		+5				V	typ	C
Maximum Operating Voltage			**12.6**	12.6	12.6	V	max	A
Minimum Operating Voltage		+4				V	typ	C
Maximum Quiescent Current	V_S = ±5V, Both Channels	13.6	**14.8**	15.2	15.6	mA	max	A
Minimum Quiescent Current	V_S = ±5V, Both Channels	13.6	**12.0**	11.7	11.4	mA	min	A
Power-Supply Rejection Ratio (PSRR)	f = 100kHz, Input Referred	52				dB	typ	C
THERMAL CHARACTERISTICS								
Specification: U, DDA, RGV		–40 to +85				°C		
Thermal Resistance, θ_{JA}	Junction-to-Ambient							
U SO-8		125				°C/W	typ	C
DDA HSOP-8	Exposed Slug Soldered to Board	55				°C/W	typ	C
RGV QFN-16	Exposed Slug Soldered to Board	50[4]				°C/W	typ	C

NOTES: (1) Junction temperature = ambient for +25°C specifications.
(2) Junction temperature = ambient at low temperature limit; junction temperature = ambient +9°C at high temperature limit for over temperature specifications.
(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(4) Not connecting the exposed slug to the –V_J plane gives 75°C/W thermal impedance (θ_{JA}).

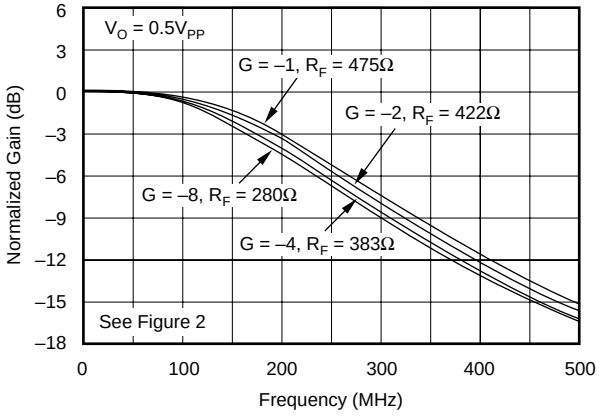
TYPICAL CHARACTERISTICS: $V_S = \pm 6V$

At T_A = +25°C, G = +4, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted.

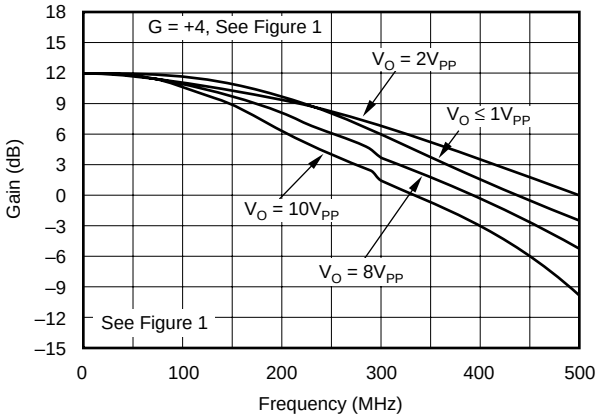
NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE



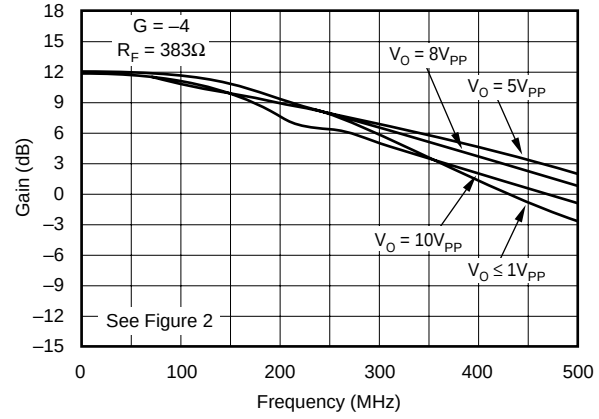
INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



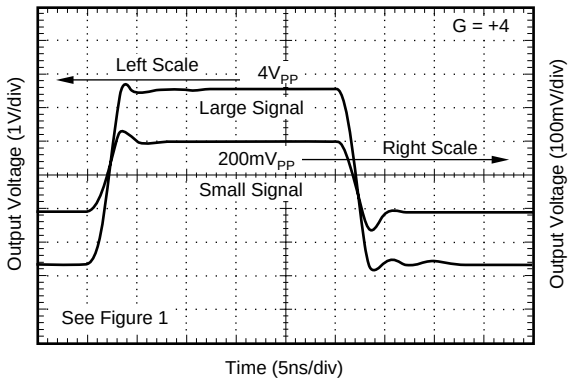
NONINVERTING LARGE-SIGNAL FREQUENCY RESPONSE



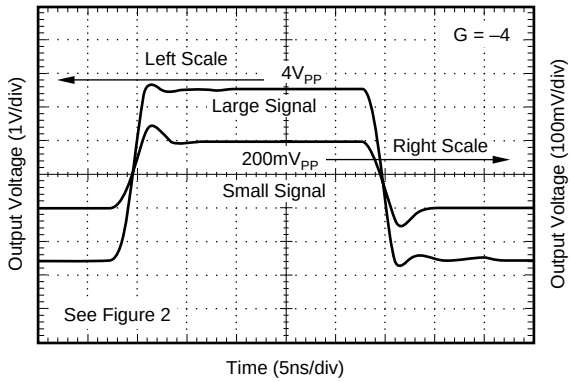
INVERTING LARGE-SIGNAL FREQUENCY RESPONSE



NONINVERTING PULSE RESPONSE



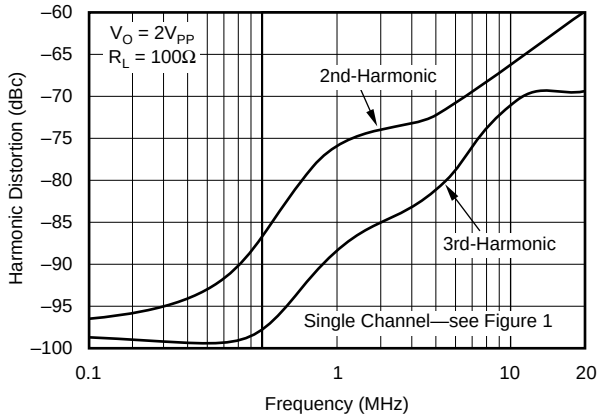
INVERTING PULSE RESPONSE



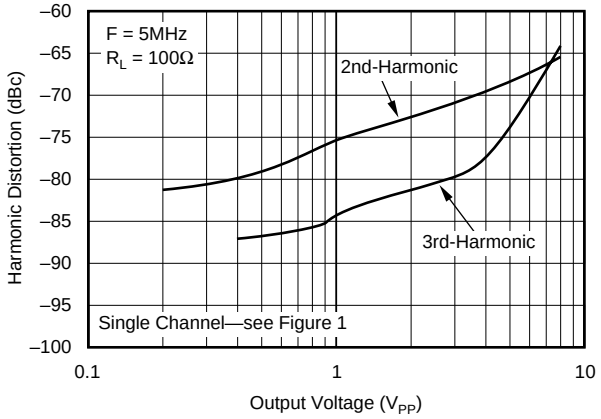
TYPICAL CHARACTERISTICS: $V_S = \pm 6V$ (Cont.)

At T_A = +25°C, G = +4, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted.

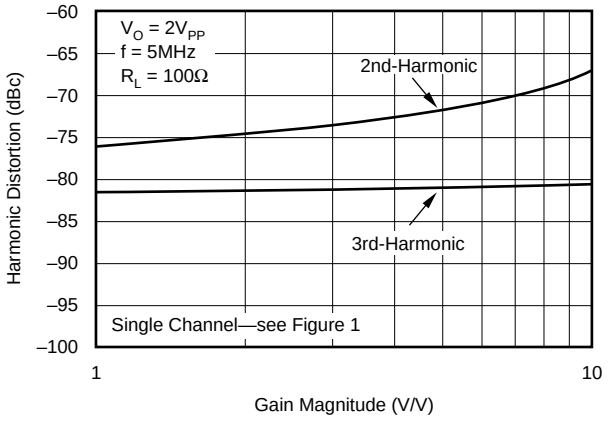
HARMONIC DISTORTION vs FREQUENCY



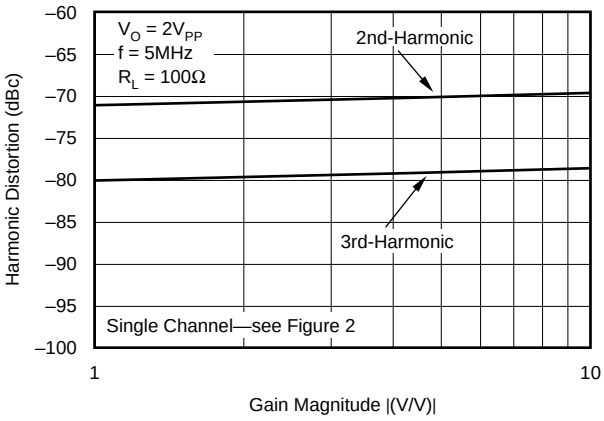
HARMONIC DISTORTION vs OUTPUT VOLTAGE



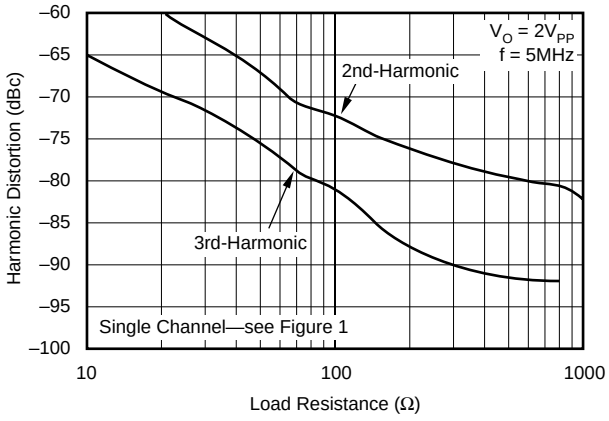
HARMONIC DISTORTION vs NONINVERTING GAIN



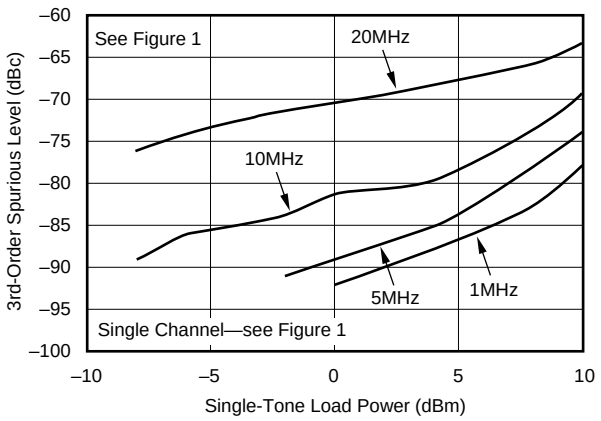
HARMONIC DISTORTION vs INVERTING GAIN



HARMONIC DISTORTION vs LOAD RESISTANCE



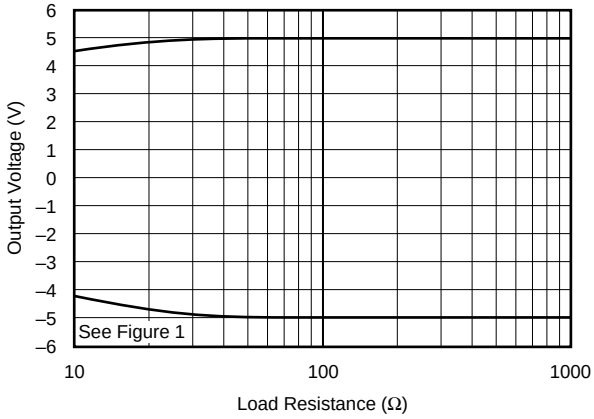
2-TONE, 3rd-ORDER
INTERMODULATION SPURIOUS



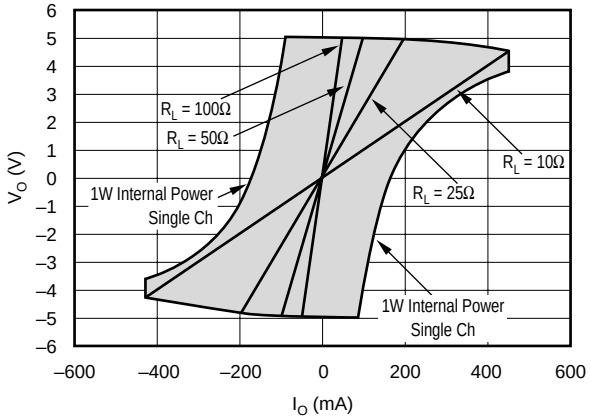
TYPICAL CHARACTERISTICS: $V_S = \pm 6V$ (Cont.)

At T_A = +25°C, G = +4, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted.

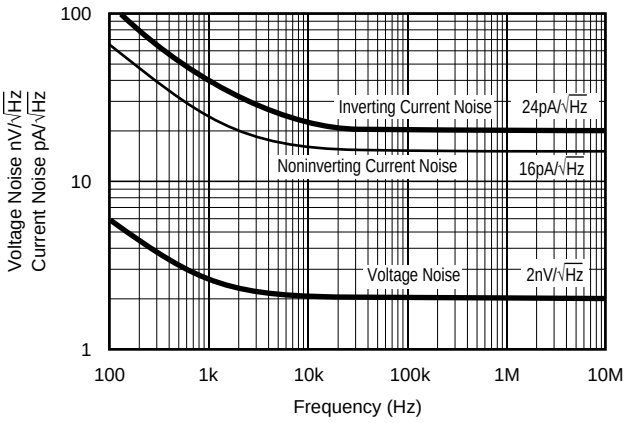
MAXIMUM OUTPUT SWING
vs LOAD RESISTANCE



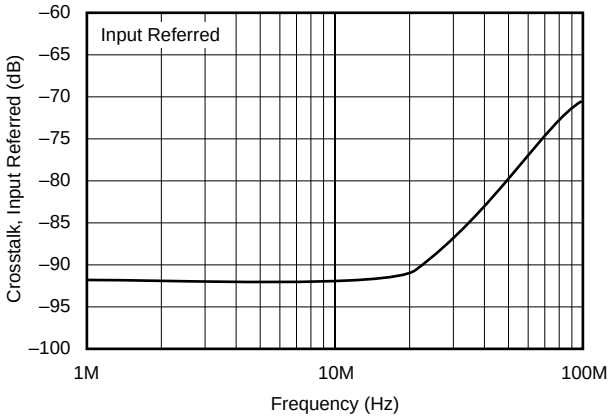
OUTPUT VOLTAGE AND CURRENT LIMITATIONS



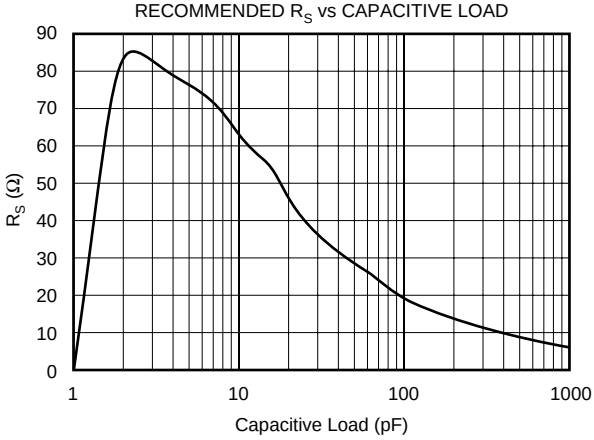
INPUT VOLTAGE AND CURRENT NOISE DENSITY



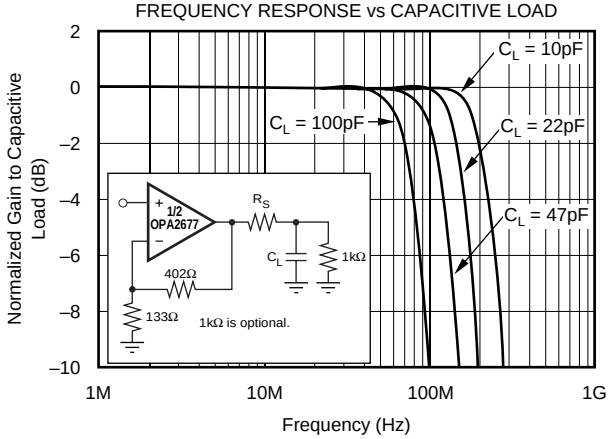
CHANNEL-TO-CHANNEL CROSSTALK



RECOMMENDED R_S vs CAPACITIVE LOAD



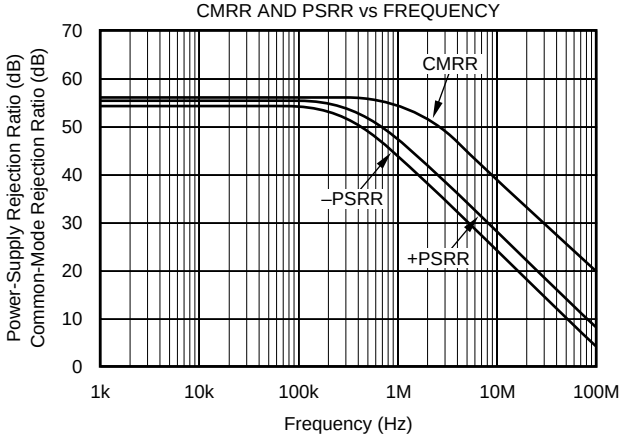
FREQUENCY RESPONSE vs CAPACITIVE LOAD



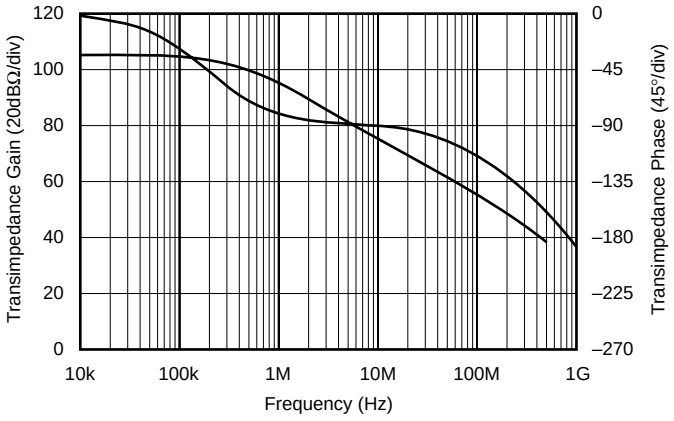
TYPICAL CHARACTERISTICS: $V_S = \pm 6V$ (Cont.)

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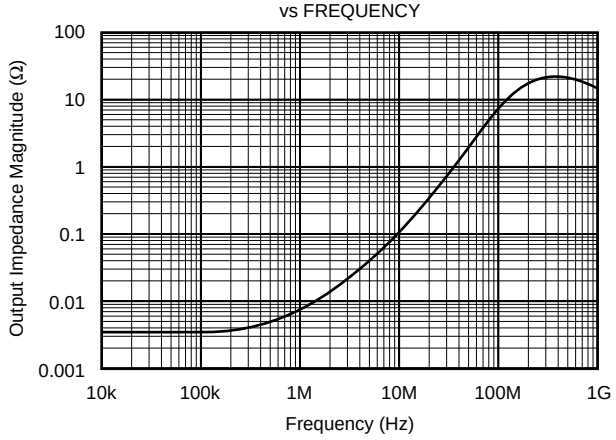
CMRR AND PSRR vs FREQUENCY



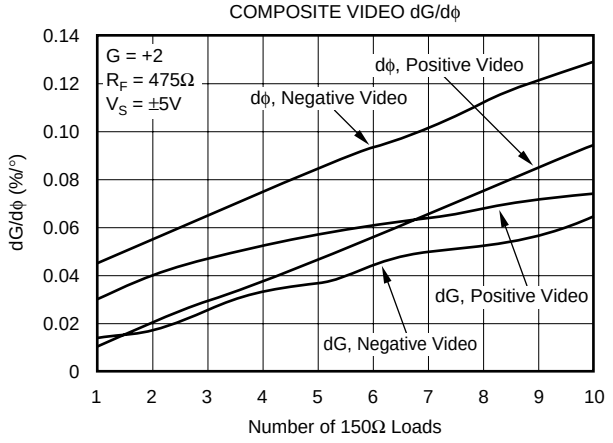
OPEN-LOOP TRANSIMPEDANCE GAIN AND PHASE



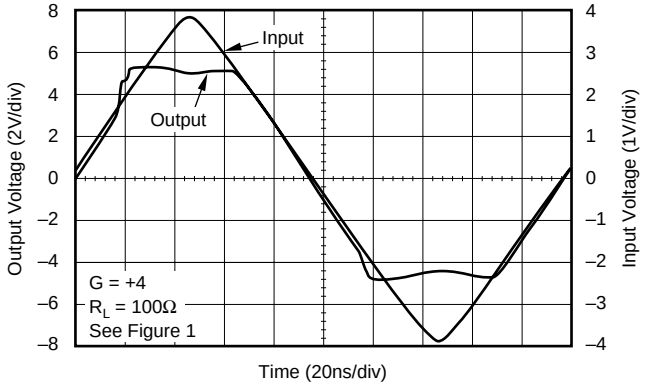
CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY



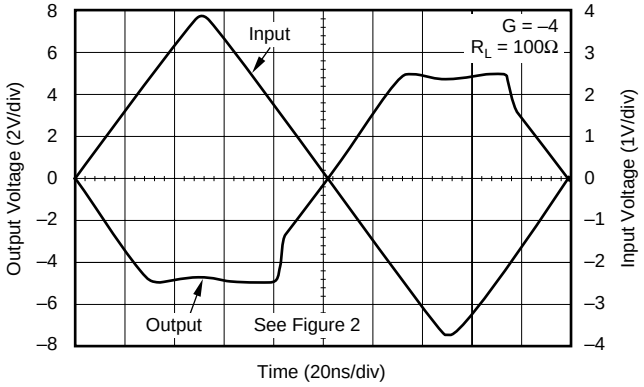
COMPOSITE VIDEO dG/dϕ



NONINVERTING OVERDRIVE RECOVERY



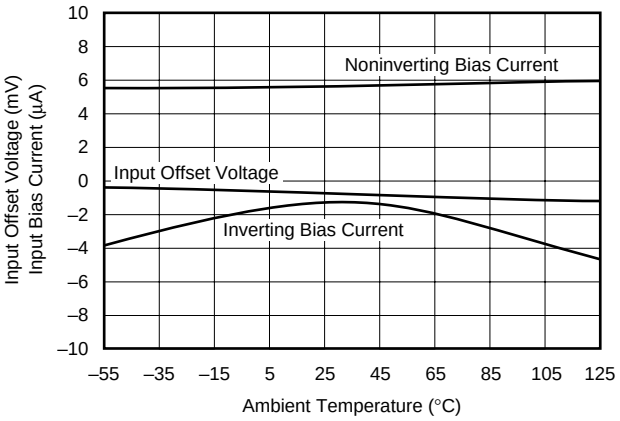
INVERTING OVERDRIVE RECOVERY



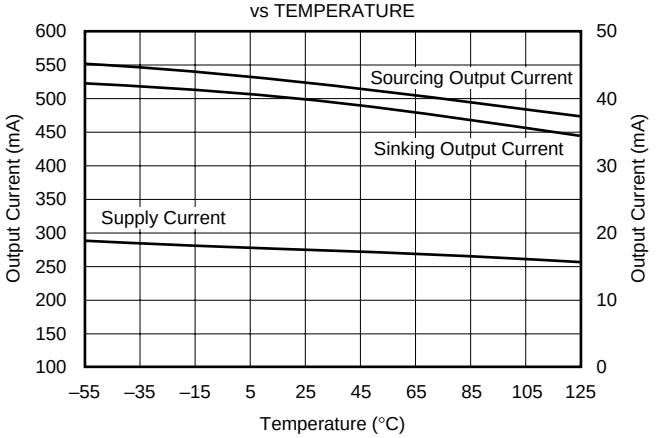
TYPICAL CHARACTERISTICS: $V_S = \pm 6V$ (Cont.)

At T_A = +25°C, G = +4, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted.

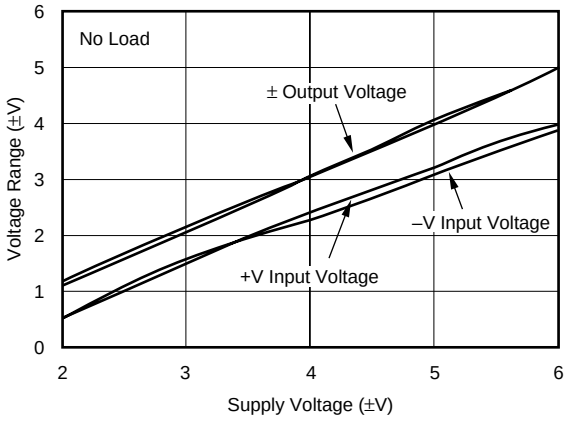
TYPICAL DC ERROR DRIFT
vs TEMPERATURE



SUPPLY AND OUTPUT CURRENT
vs TEMPERATURE



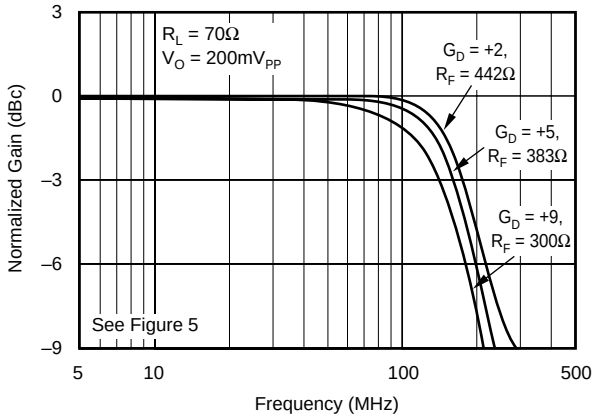
CMIR AND OUTPUT VOLTAGE
vs SUPPLY VOLTAGE



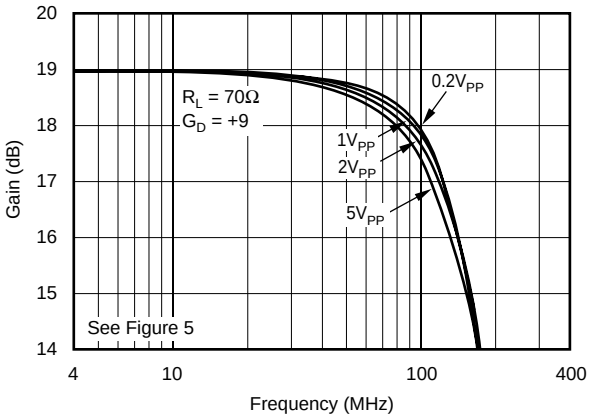
TYPICAL CHARACTERISTICS: $V_S = \pm 6V$ (Cont.)

At T_A = +25°C, Differential Gain = +9, R_F = 300Ω, and R_L = 70Ω, unless otherwise noted. See Figure 5 for AC performance only.

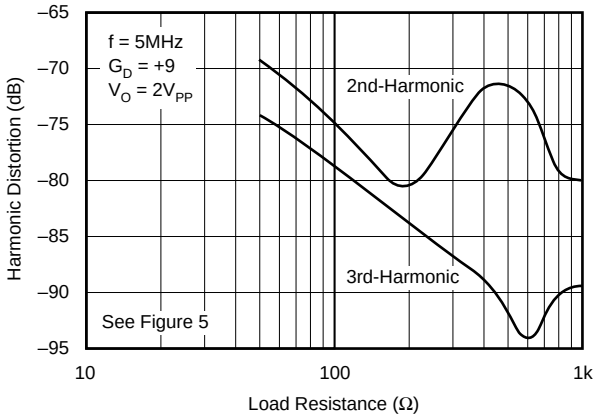
DIFFERENTIAL SMALL-SIGNAL FREQUENCY RESPONSE



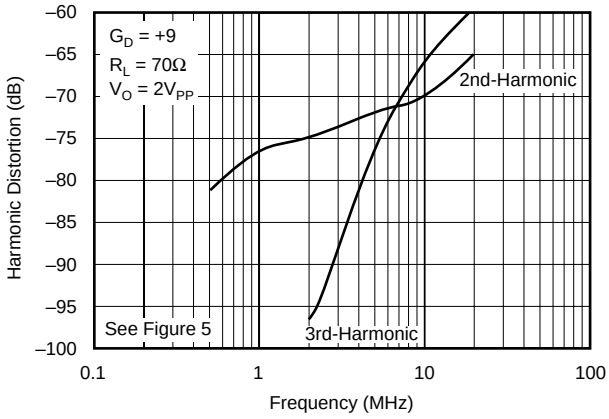
DIFFERENTIAL LARGE-SIGNAL FREQUENCY RESPONSE



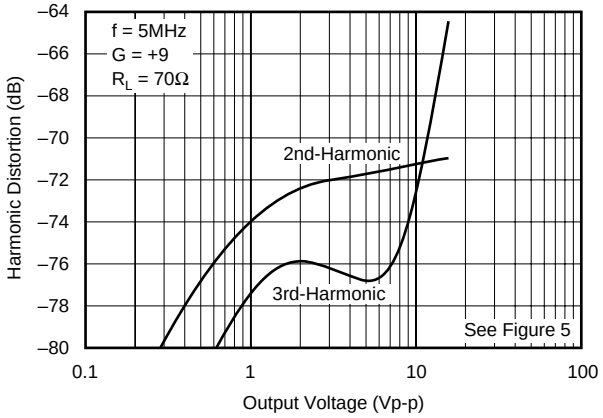
HARMONIC DISTORTION vs LOAD RESISTANCE



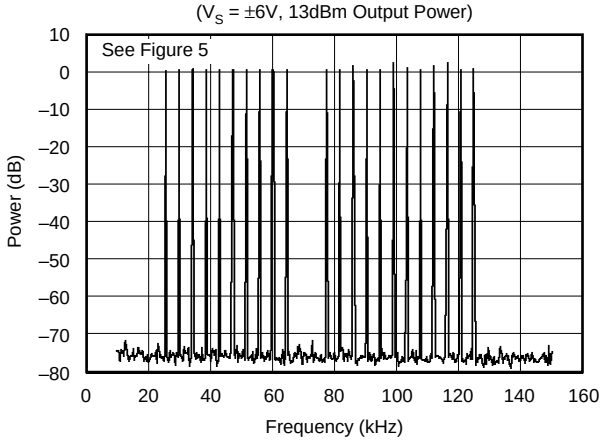
HARMONIC DISTORTION vs FREQUENCY



HARMONIC DISTORTION vs OUTPUT VOLTAGE



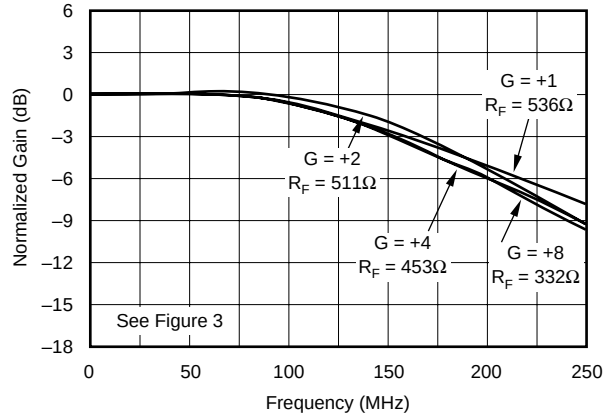
MULTITONE POWER RATIO (V_S = ±6V, 13dBm Output Power)



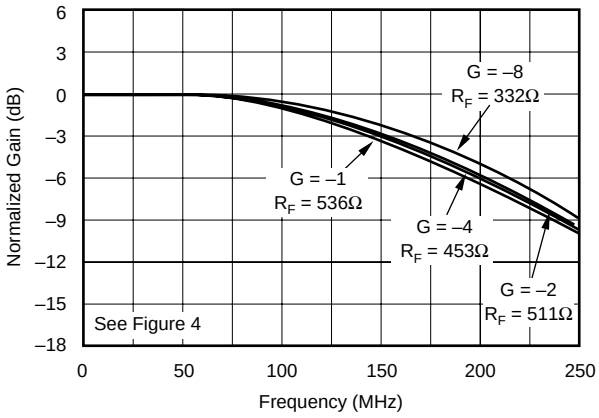
TYPICAL CHARACTERISTICS: V_S = +5V

At T_A = +25°C, G = +4, R_F = 453Ω, and R_L = 100Ω to V_S/2, unless otherwise noted.

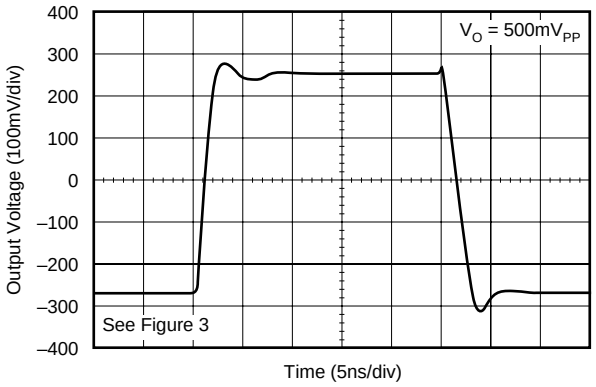
NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE



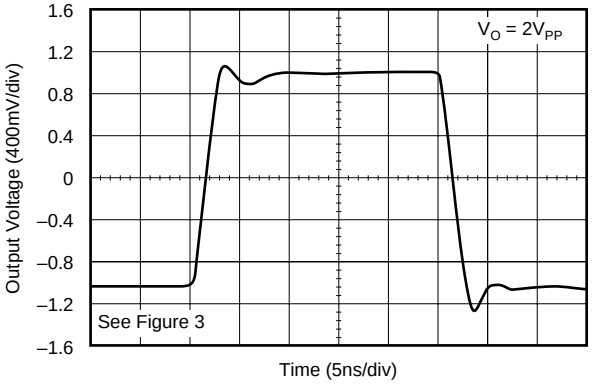
INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



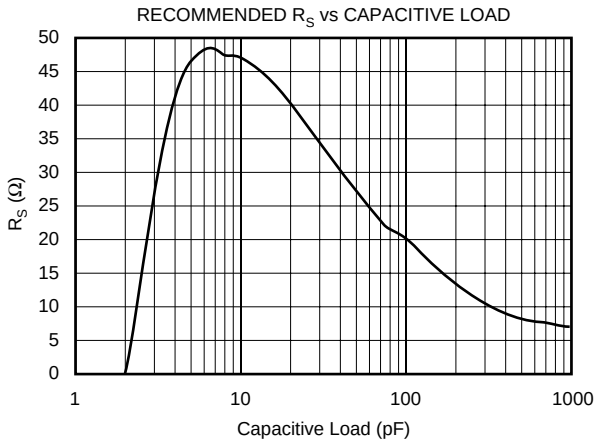
SMALL-SIGNAL PULSE RESPONSE



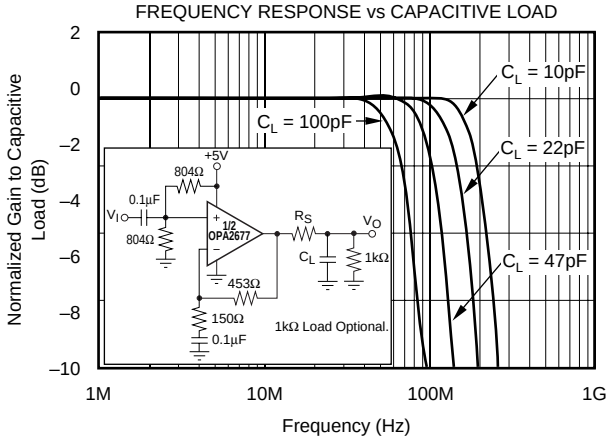
LARGE-SIGNAL PULSE RESPONSE



RECOMMENDED R_S vs CAPACITIVE LOAD



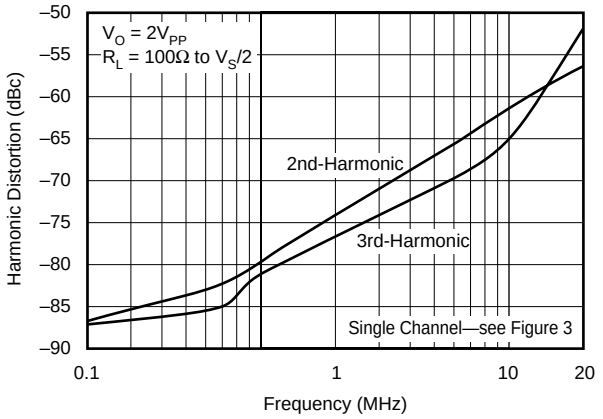
FREQUENCY RESPONSE vs CAPACITIVE LOAD



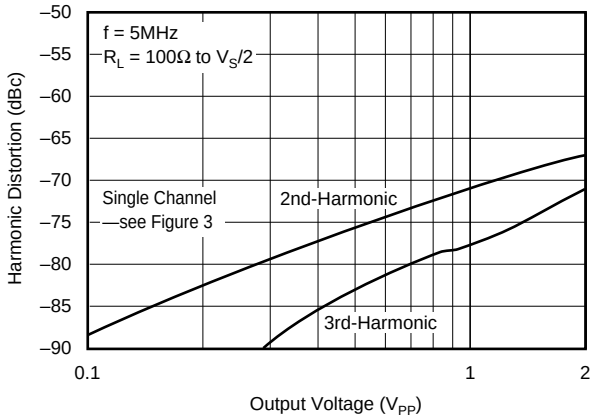
TYPICAL CHARACTERISTICS: V_S = +5V (Cont.)

At T_A = +25°C, G = +4, R_F = 453Ω, and R_L = 100Ω to V_S/2, unless otherwise noted.

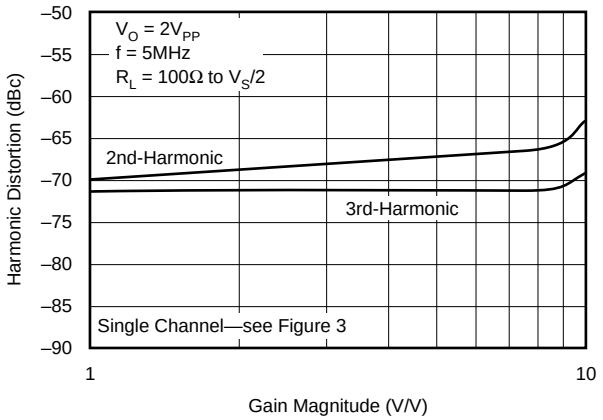
HARMONIC DISTORTION vs FREQUENCY



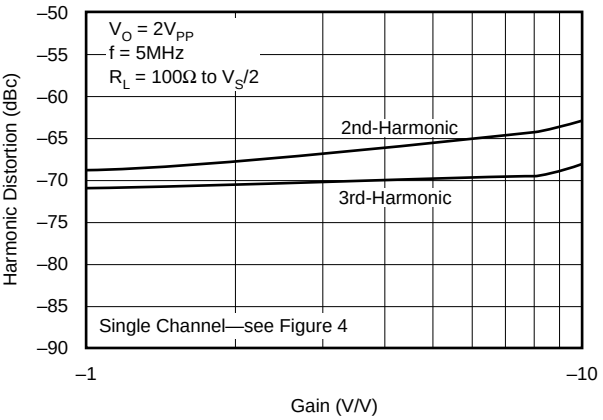
HARMONIC DISTORTION vs OUTPUT VOLTAGE



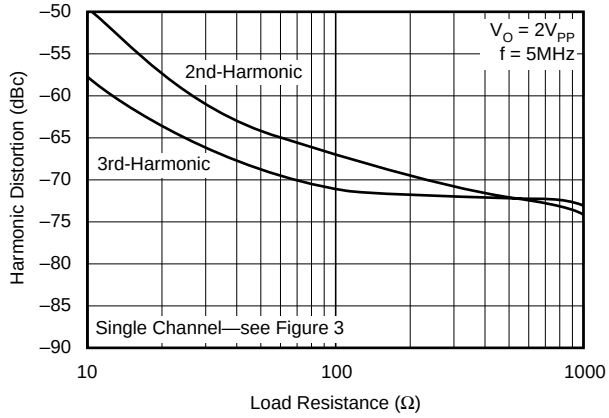
HARMONIC DISTORTION vs NONINVERTING GAIN



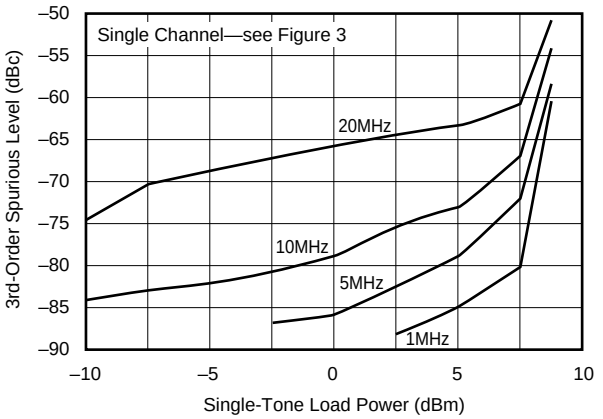
HARMONIC DISTORTION vs INVERTING GAIN



HARMONIC DISTORTION vs LOAD RESISTANCE



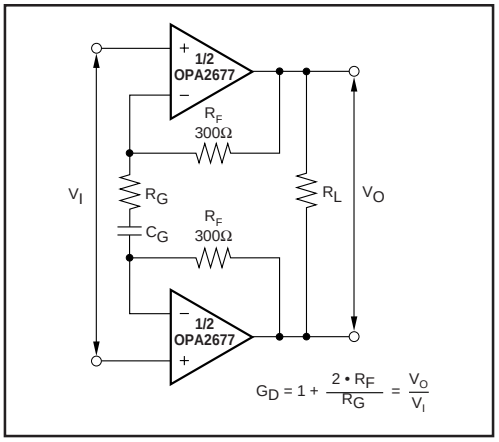
2-TONE, 3rd-ORDER SPURIOUS LEVEL



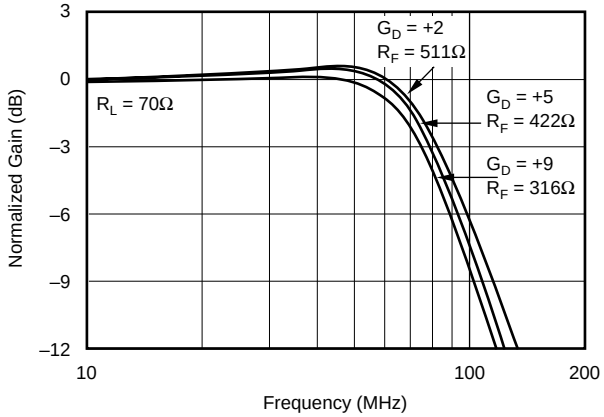
TYPICAL CHARACTERISTICS: V_S = +5V (Cont.)

At T_A = +25°C, Differential Gain = +9, R_F = 316Ω, and R_L = 70Ω, unless otherwise noted.

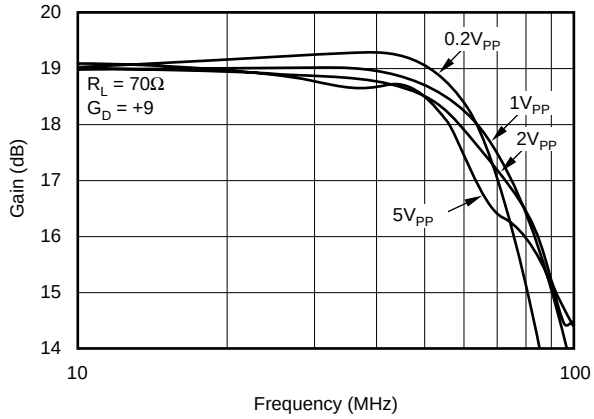
DIFFERENTIAL PERFORMANCE
TEST CIRCUIT



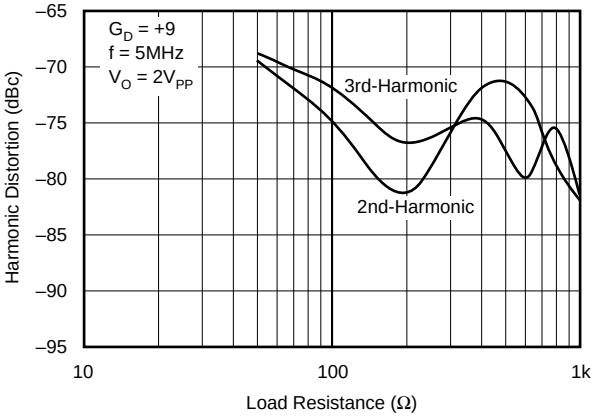
DIFFERENTIAL SMALL-SIGNAL
FREQUENCY RESPONSE



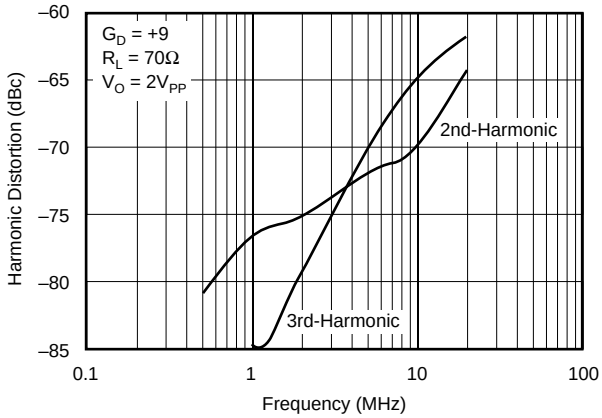
DIFFERENTIAL LARGE-SIGNAL
FREQUENCY RESPONSE



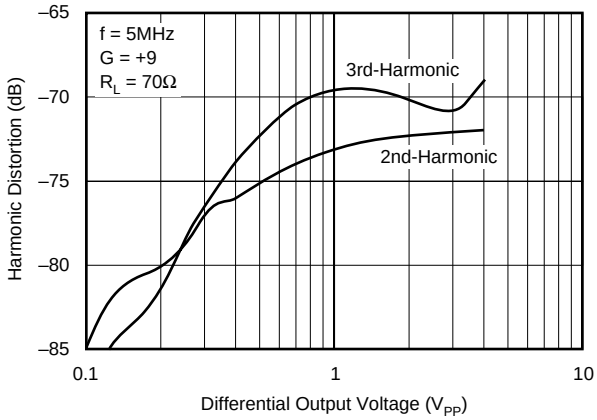
HARMONIC DISTORTION vs LOAD RESISTANCE



HARMONIC DISTORTION vs FREQUENCY



HARMONIC DISTORTION vs OUTPUT VOLTAGE



APPLICATION INFORMATION

WIDEBAND CURRENT-FEEDBACK OPERATION

The OPA2677 gives the exceptional AC performance of a wideband current-feedback op amp with a highly linear, high-power output stage. Requiring only 9mA/ch quiescent current, the OPA2677 swings to within 1V of either supply rail and delivers in excess of 380mA at room temperature. This low-output headroom requirement, along with supply voltage independent biasing, gives remarkable single (+5V) supply operation. The OPA2677 delivers greater than 150MHz bandwidth driving a $2V_{PP}$ output into 100Ω on a single +5V supply. Previous boosted output stage amplifiers typically suffer from very poor crossover distortion as the output current goes through zero. The OPA2677 achieves a comparable power gain with much better linearity. The primary advantage of a current-feedback op amp over a voltage-feedback op amp is that AC performance (bandwidth and distortion) is relatively independent of signal gain. Figure 1 shows the DC-coupled, gain of +4, dual power-supply circuit configuration used as the basis of the ±6V Electrical and Typical Characteristics. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 50Ω with a series output resistor. Voltage swings reported in the electrical characteristics are taken directly at the input and output pins, whereas load powers (dBm) are defined at a matched 50Ω load. For the circuit of Figure 1, the total effective load is 100Ω || 535Ω = 84Ω.

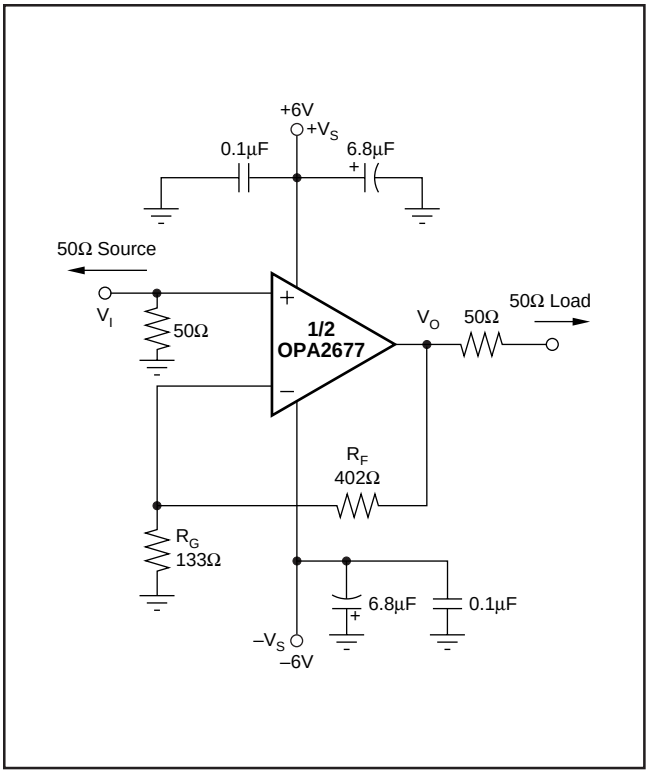


FIGURE 1. DC-Coupled, G = +4, Bipolar Supply, Specification and Test Circuit.

Figure 2 shows the DC-coupled, bipolar supply circuit configuration used as the basis for the Inverting Gain ±6V Typical Characteristics. Key design considerations of the inverting configuration are developed in the *Inverting Amplifier Operation* section.

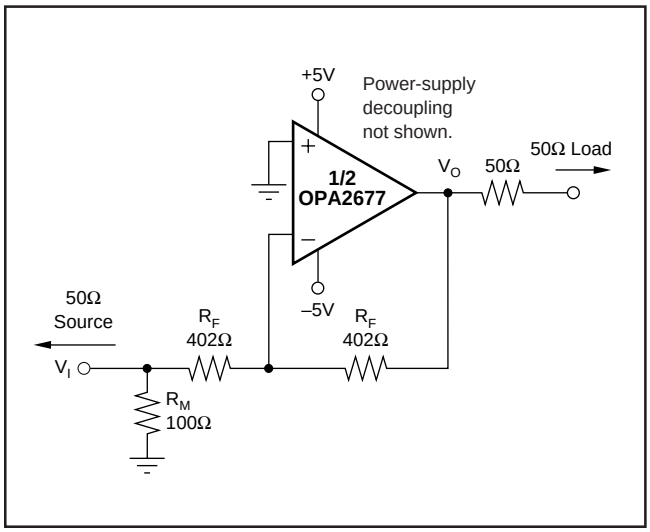


FIGURE 2. DC-Coupled, G = –4, Bipolar Supply, Specification and Test Circuit.

Figure 3 shows the AC-coupled, gain of +4, single-supply circuit configuration used as the basis of the +5V Electrical and Typical Characteristics. Though not a rail-to-rail design, the OPA2677 requires minimal input and output voltage headroom compared to other very wideband current-feedback op amps. It will deliver a $3V_{PP}$ output swing on a single +5V supply with greater than 100MHz bandwidth. The key requirement of broadband single-supply operation is to maintain input and output signal swings within the usable voltage ranges at both the input and the output. The circuit of Figure 3 establishes an input midpoint bias using a simple resistive divider from the +5V supply (two 806Ω resistors). The input signal is then AC-coupled into this midpoint voltage bias. The input voltage can swing to within 1.3V of either supply pin, giving a $2.4V_{PP}$ input signal range centered between the supply pins. The input impedance matching resistor (57.6Ω) used for testing is adjusted to give a 50Ω input match when the parallel combination of the biasing divider network is included. The gain resistor (R_G) is AC-coupled, giving the circuit a DC gain of +1—which puts the input DC bias voltage (2.5V) on the output as well. The feedback resistor value is adjusted from the bipolar supply condition to re-optimize for a flat frequency response in +5V, gain of +4, operation. Again, on a single +5V supply, the output voltage can swing to within 1V of either supply pin while delivering more than 200mA output current. A demanding 100Ω load to a midpoint bias is used in this characterization circuit. The new output stage used in the OPA2677 can deliver large bipolar output currents into this midpoint load with minimal crossover distortion, as shown by the +5V supply, harmonic distortion plots.

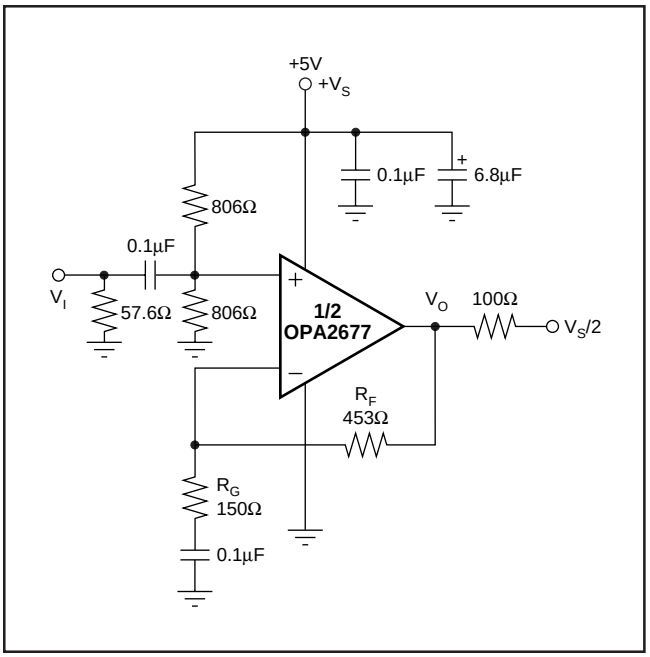


FIGURE 3. AC-Coupled, G = +4, Single-Supply, Specification and Test Circuit.

The last configuration used as the basis of the +5V Electrical and Typical Characteristics is shown in Figure 4. Design considerations for this inverting, bipolar supply configuration are covered either in single-supply configuration (as shown in Figure 3) or in the *Inverting Amplifier Operation* section.

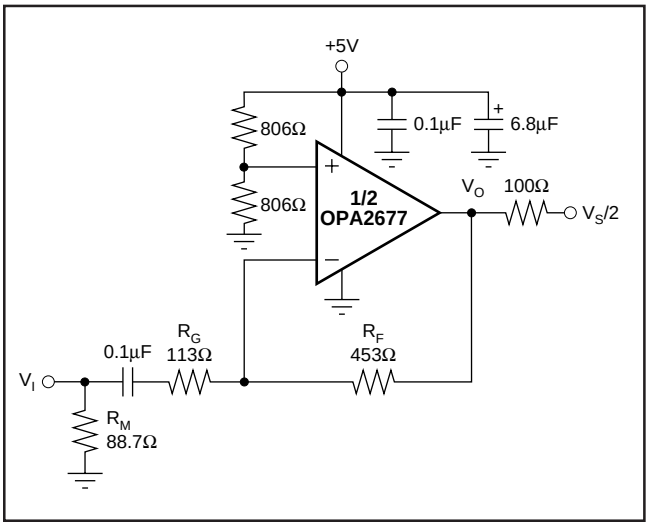


FIGURE 4. AC-Coupled, G = –4, Single-Supply, Specification and Test Circuit.

DIFFERENTIAL INTERFACE APPLICATIONS

Dual op amps are particularly suitable to differential input to differential output applications. Typically, these fall into either Analog-to-Digital Converter (ADC) input interface or line driver applications. Two basic approaches to differential I/O are noninverting or inverting configurations. Since the output is differential, the signal polarity is somewhat meaningless—the noninverting and inverting terminology applies here to where the input is brought into the OPA2677. Each has its advantages and disadvantages. Figure 5 shows a basic starting point for noninverting differential I/O applications.

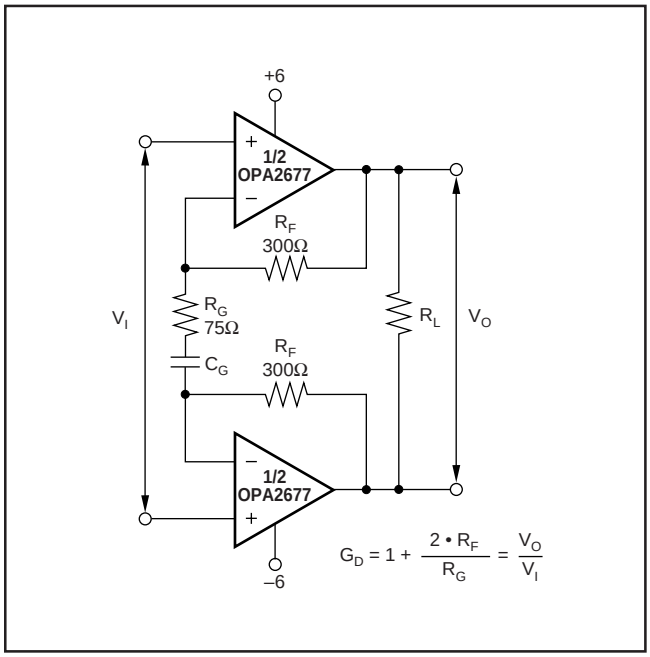


FIGURE 5. Noninverting Differential I/O Amplifier.

This approach provides for a source termination impedance that is independent of the signal gain. For instance, simple differential filters may be included in the signal path right up to the noninverting inputs without interacting with the gain setting. The differential signal gain for the circuit of Figure 5 is:

$$A_D = 1 + 2 \bullet R_F/R_G$$

Since the OPA2677 is a current feedback (CFB) amplifier, its bandwidth is principally controlled with the feedback resistor value; Figure 5 shows a value of 300Ω for the A_D = +9 design. The differential gain, however, may be adjusted with considerable freedom using just the R_G resistor. In fact, R_G may be a reactive network providing a very isolated shaping to the differential frequency response.

Various combinations of single-supply or AC-coupled gain can also be delivered using the basic circuit of Figure 5. Common-mode bias voltages on the two noninverting inputs pass on to the output with a gain of 1 since an equal DC voltage at each inverting node creates no current through R_G. This circuit does show a common-mode gain of 1 from input to output. The source connection should either remove this common-mode signal if undesired (using an input transformer can provide this function), or the common-mode voltage at the inputs can be used to set the output common-mode bias. If the low common-mode rejection of this circuit is a problem, the output interface may also be used to reject that common-mode. For instance, most modern differential input ADCs reject common-mode signals very well, while a line driver application through a transformer will also attenuate the common-mode signal through to the line.

SINGLE-SUPPLY ADSL UPSTREAM DRIVER

Figure 6 shows an example of a single-supply ADSL upstream driver. The dual OPA2677 is configured as a differential gain stage to provide signal drive to the primary winding of the transformer (here, a step-up transformer with a turns ratio of 1:1.7). The main advantage of this configuration is the cancellation of all even harmonic distortion products. Another important advantage for ADSL is that each amplifier needs only to swing half of the total output required driving the load.

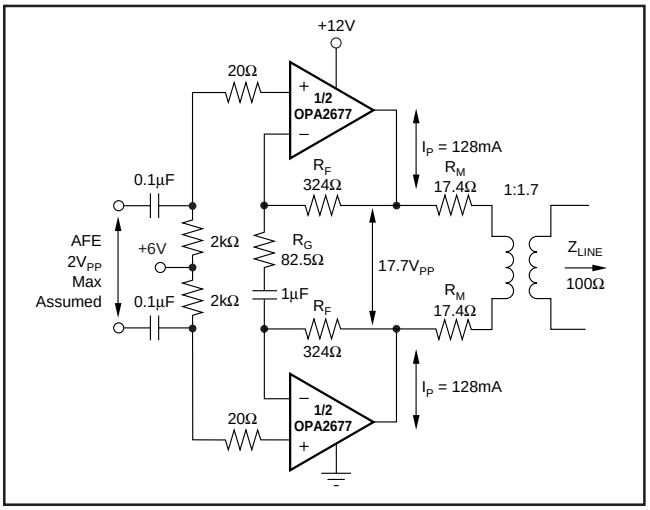


FIGURE 6. Single-Supply ADSL Upstream Driver.

The analog front end (AFE) signal is AC-coupled to the driver, and the noninverting input of each amplifier is biased to the mid-supply voltage (+6V in this case). In addition to providing the proper biasing to the amplifier, this approach also provides a high-pass filtering with a corner frequency, set here at 5kHz. As the upstream signal bandwidth starts at 26kHz, this high-pass filter does not generate any problem and has the advantage of filtering out unwanted lower frequencies.

The input signal is amplified with a gain set by the following equation:

$$G_D = 1 + \frac{2 \bullet R_F}{R_G} \qquad (1)$$

With R_F = 324Ω and R_G = 82.5Ω, the gain for this differential amplifier is 8.85. This gain boosts the AFE signal, assumed to be a maximum of $2V_{PP}$, to a maximum of $17.3V_{PP}$.

Refer to the *Setting Resistor Values to Optimize Bandwidth* section for a discussion on which feedback resistor value to choose.

The two back-termination resistors (17.4Ω each) added at each terminal of the transformer make the impedance of the modem match the impedance of the phone line, and also provide a means of detecting the received signal for the receiver. The value of these resistors (R_M) is a function of the line impedance and the transformer turns ratio (n), given by the following equation:

$$R_M = \frac{Z_{LINE}}{2n^2} \qquad (2)$$

OPA2677 HDSL2 UPSTREAM DRIVER

Figure 7 shows an HDSL2 implementation of a single-supply upstream driver.

The two designs differ by the values of their matching impedance, the load impedance, and the ratio turns of the transformers. All these differences are reflected in the higher peak current and thus, the higher maximum power dissipation in the output of the driver.

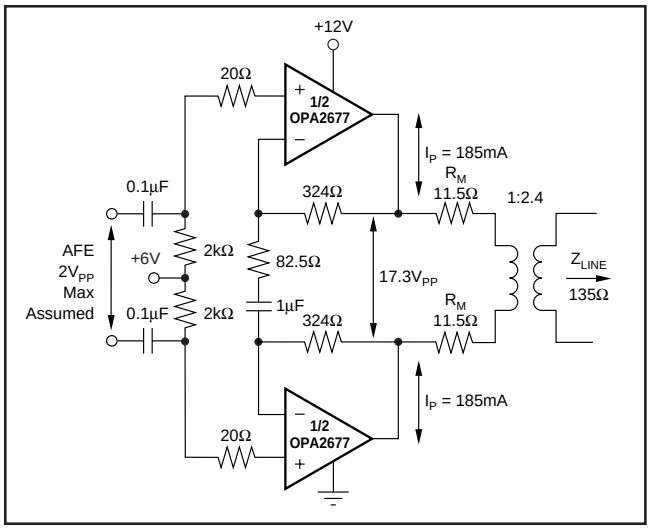


FIGURE 7. HDSL2 Upstream Driver.

LINE DRIVER HEADROOM MODEL

The first step in a transformer-coupled, twisted-pair driver design is to compute the peak-to-peak output voltage from the target specifications. This is done using the following equations:

$$P_L = 10 \bullet \log \frac{V_{RMS}^2}{(1mW) \bullet R_L} \qquad (3)$$

with P_L power at the load, V_{RMS} voltage at the load, and R_L load impedance; this gives the following:

$$V_{RMS} = \sqrt{(1mW) \bullet R_L \bullet 10^{\frac{P_L}{10}}} \qquad (4)$$

$$V_P = \text{Crest Factor} \bullet V_{RMS} = C_F \bullet V_{RMS} \qquad (5)$$

with V_P peak voltage at the load and CF Crest Factor.

$$V_{LPP} = 2 \bullet CF \bullet V_{RMS} \qquad (6)$$

with V_{LPP}: peak-to-peak voltage at the load.

Consolidating Equations 3 through 6 allows expressing the required peak-to-peak voltage at the load as a function of the crest factor, the load impedance, and the power at the load.

Thus,
$$V_{LPP} = 2 \bullet CF \bullet \sqrt{(1mW) \bullet R_L \bullet 10^{\frac{P_L}{10}}} \qquad (7)$$

This V_{LPP} is usually computed for a nominal line impedance and may be taken as a fixed design target.

The next step in the design is to compute the individual amplifier output voltage and currents as a function of V_{PP} on

the line and transformer turns ratio. As this turns ratio changes, the minimum allowed supply voltage changes along with it. The peak current in the amplifier output is given by:

$$\pm I_P = \frac{1}{2} \bullet \frac{2 \bullet V_{LPP}}{n} \bullet \frac{1}{4R_M} \quad (8)$$

with V_{PP} as defined in Equation 7, and R_M as defined in Equation 2 and shown in Figure 8.

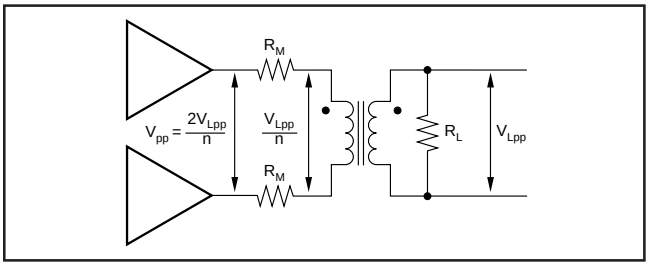


FIGURE 8. Driver Peak Output Voltage.

With the previous information available, it is now possible to select a supply voltage and the turns ratio desired for the transformer as well as calculate the headroom for the OPA2677.

The model, shown in Figure 9, can be described with the following set of equations:

1) As available output swing:

$$V_{PP} = V_{CC} - (V_1 + V_2) - I_P \bullet (R_1 + R_2) \quad (9)$$

2) Or as required supply voltage:

$$V_{CC} = V_{PP} + (V_1 + V_2) + I_P \bullet (R_1 + R_2) \quad (10)$$

The minimum supply voltage for a power and load requirement is given by Equation 10.

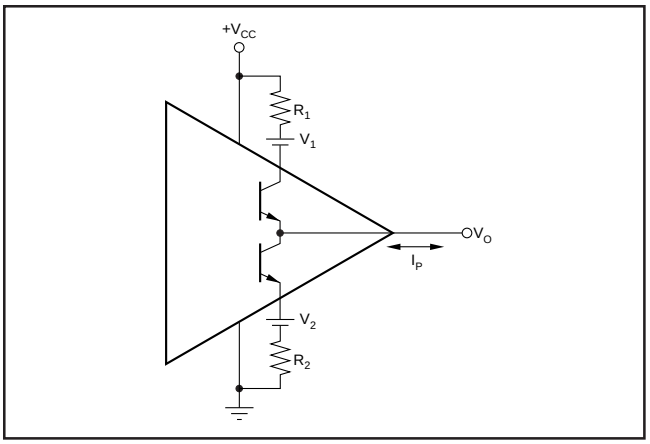


FIGURE 9. Line Driver Headroom Model.

V_1, V_2, R_1, and R_2 are given in Table I for both +12V and +5V operation.

	V_1	R_1	V_2	R_2
+5V	0.9V	5Ω	0.8V	5Ω
+12V	0.9V	2Ω	0.9V	2Ω

TABLE I. Line Driver Headroom Model Values.

TOTAL DRIVER POWER FOR xDSL APPLICATIONS

The total internal power dissipation for the OPA2677 in an xDSL line driver application will be the sum of the quiescent power and the output stage power. The OPA2677 holds a relatively constant quiescent current versus supply voltage—giving a power contribution that is simply the quiescent current times the supply voltage used (the supply voltage will be greater than the solution given in Equation 10). The total output stage power may be computed with reference to Figure 10.

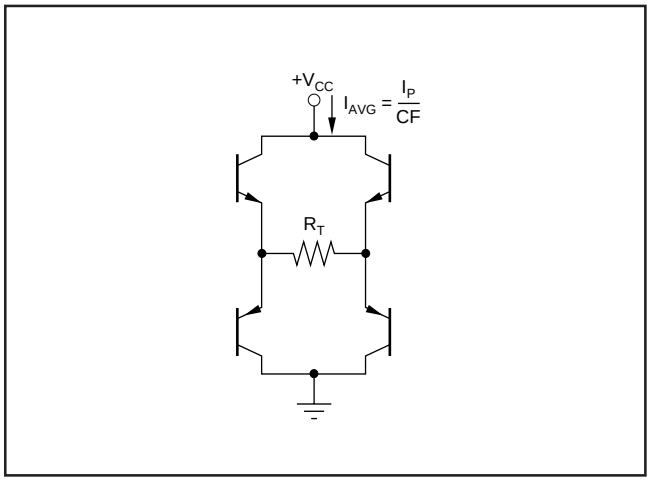


FIGURE 10. Output Stage Power Model.

The two output stages used to drive the load of Figure 8 can be seen as an H-Bridge in Figure 10. The average current drawn from the supply into this H-Bridge and load will be the peak current in the load given by Equation 8 divided by the crest factor (CF) for the xDSL modulation. This total power from the supply is then reduced by the power in R_T to leave the power dissipated internal to the drivers in the four output stage transistors. That power is simply the target line power used in Equation 3 plus the power lost in the matching elements (R_M). In the examples here, a perfect match is targeted giving the same power in the matching elements as in the load. The output stage power is then set by Equation 11.

$$P_{OUT} = \frac{I_P}{CF} \times V_{CC} - 2P_L \quad (11)$$

The total amplifier power is then:

$$P_{TOT} = I_q \times V_{CC} + \frac{I_P}{CF} \times V_{CC} - 2P_L \quad (12)$$

For the ADSL CPE upstream driver design of Figure 6, the peak current is 128mA for a signal that requires a crest factor of 5.33 with a target line power of 13dBm into 100Ω (20mW). With a typical quiescent current of 18mA and a nominal supply voltage of +12V, the total internal power dissipation for the solution of Figure 6 will be:

(13)

$$P_{TOT} = 18mA(12V) + \frac{128mA}{5.33}(12V) - 2(20mW) = 464mW$$

DESIGN-IN TOOLS

DEMONSTRATION FIXTURES

A printed circuit board (PCB) is available to assist in the initial evaluation of circuit performance using the OPA2677. The fixture is offered free of charge as unpopulated PCB, delivered with a user's guide. The summary information for this fixture is shown in Table II.

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA2677U	SO-8	DEM-OPA-SO-2A	SBOU003
OPA2677IDDA	HSOP-8	Not Available	Not Available
OPA2677T	SO-16	Not Available	Not Available
OPA2677IRGV	QFN-16	Not Available	Not Available

TABLE II. Demonstration Fixtures by Package.

This demonstration fixture can be requested at the Texas Instruments web site (www.ti.com) through the OPA2677 product folder.

MACROMODELS AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the OPA2677 is available through the TI web site (www.ti.com). This model does a good job of predicting small-signal AC and transient performance under a wide variety of operating conditions, but does not do as well in predicting the harmonic distortion or dG/dP characteristics. This model does not attempt to distinguish between the package types in small-signal AC performance, nor does it attempt to simulate channel-to-channel coupling.

OPERATING SUGGESTIONS

SETTING RESISTOR VALUES TO OPTIMIZE BANDWIDTH

A current-feedback op amp like the OPA2677 can hold an almost constant bandwidth over signal gain settings with the proper adjustment of the external resistor values, which is shown in the Typical Characteristics; the small-signal bandwidth decreases only slightly with increasing gain. These curves also show that the feedback resistor is changed for each gain setting. The resistor values on the inverting side of the circuit for a current-feedback op amp can be treated as frequency response compensation elements, whereas their ratios set the signal gain. Figure 11 shows the small-signal frequency response analysis circuit for the OPA2677.

The key elements of this current-feedback op amp model are:

$\alpha \rightarrow$ Buffer gain from the noninverting input to the inverting input

$R_I \rightarrow$ Buffer output impedance

$i_{ERR} \rightarrow$ Feedback error current signal

$Z_{(S)} \rightarrow$ Frequency dependent open-loop transimpedance gain from i_{ERR} to V_O

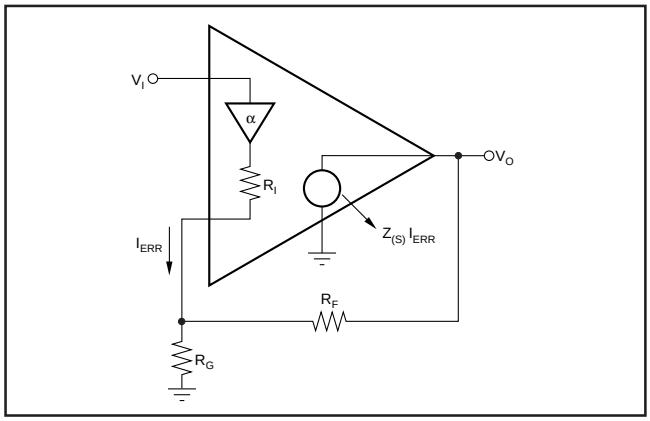


FIGURE 11. Current Feedback Transfer Function Analysis Circuit.

The buffer gain is typically very close to 1.00 and is normally neglected from signal gain considerations. It sets the CMRR, however, for a single op amp differential amplifier configuration. For a buffer gain $\alpha < 1.0$, the CMRR = $-20 \cdot \log(1 - \alpha)$dB.

R_I, the buffer output impedance, is a critical portion of the bandwidth control equation. The OPA2677 inverting input resistor is typically 22Ω.

A current-feedback op amp senses an error current in the inverting node (as opposed to a differential input error voltage for a voltage-feedback op amp) and passes this on to the output through an internal frequency dependent transimpedance gain. The Typical Characteristics show this open-loop transimpedance response, which is analogous to the open-loop voltage gain curve for a voltage-feedback op amp. Developing the transfer function for the circuit of Figure 11 gives Equation 14:

$$\frac{V_O}{V_I} = \frac{\alpha\left(1+\frac{R_F}{R_G}\right)}{1+\frac{R_F + R_I\left(1+\frac{R_F}{R_G}\right)}{Z(s)}} = \frac{\alpha \cdot NG}{1+\frac{R_F + R_I NG}{Z(s)}} \qquad \left[NG = \left(1+\frac{R_F}{R_G}\right)\right] \tag{14}$$

This is written in a loop-gain analysis format where the errors arising from a non-infinite open-loop gain are shown in the denominator. If Z(s) is infinite over all frequencies, the denominator of Equation 14 reduces to 1 and the ideal desired signal gain shown in the numerator is achieved. The fraction in the denominator of Equation 14 determines the frequency response. Equation 15 shows this as the loop-gain equation:

$$\frac{Z(s)}{R_F + R_I NG} = \text{Loop Gain} \tag{15}$$

If $20\log(R_F + NG \cdot R_I)$ is drawn on top of the open-loop transimpedance plot, the difference between the two would be the loop gain at a given frequency. Eventually, Z(s) rolls off to equal the denominator of Equation 15, at which point the loop gain has reduced to 1 (and the curves have intersected). This point of equality is where the amplifier closed-loop

frequency response given by Equation 14 starts to roll off, and is exactly analogous to the frequency at which the noise gain equals the open-loop voltage gain for a voltage-feedback op amp. The difference here is that the total impedance in the denominator of Equation 15 may be controlled somewhat separately from the desired signal gain (or NG). The OPA2677 is internally compensated to give a maximally flat frequency response for R_F = 402Ω at NG = 4 on ±6V supplies. Evaluating the denominator of Equation 15 (which is the feedback transimpedance) gives an optimal target of 490Ω. As the signal gain changes, the contribution of the NG • R_I term in the feedback transimpedance changes, but the total can be held constant by adjusting R_F. Equation 16 gives an approximate equation for optimum R_F over signal gain:

$$R_F = 490 - NG \bullet R_I \quad (16)$$

As the desired signal gain increases, this equation eventually predicts a negative R_F. A somewhat subjective limit to this adjustment can also be set by holding R_G to a minimum value of 20Ω. Lower values load both the buffer stage at the input and the output stage if R_F gets too low—actually decreasing the bandwidth. Figure 12 shows the recommended R_F versus NG for both ±6V and a single +5V operation. The values for R_F versus gain shown here are approximately equal to the values used to generate the Typical Characteristics. They differ in that the optimized values used in the Typical Characteristics are also correcting for board parasitic not considered in the simplified analysis leading to Equation 16. The values shown in Figure 12 give a good starting point for designs where bandwidth optimization is desired.

The total impedance going into the inverting input may be used to adjust the closed-loop signal bandwidth. Inserting a series resistor between the inverting input and the summing junction increases the feedback impedance (denominator of Equation 15), decreasing the bandwidth. The internal buffer output impedance for the OPA2677 is slightly influenced by the source impedance looking out of the noninverting input terminal. High-source resistors have the effect of increasing R_I, decreasing the bandwidth. For those single-supply applications which develop a midpoint bias at the noninverting input through high-valued resistors, the decoupling capacitor is essential for power-supply ripple rejection, noninverting input noise current shunting, and to minimize the high-frequency value for R_I in Figure 11.

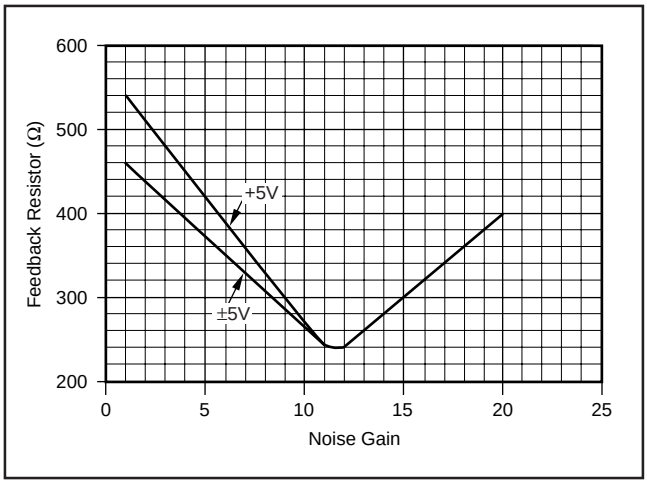


FIGURE 12. Feedback Resistor vs. Noise Gain.

INVERTING AMPLIFIER OPERATION

The OPA2677 is a general-purpose, wideband current-feedback op amp; most of the familiar op amp application circuits should be available to the designer. Those dual op amp applications that require considerable flexibility in the feedback element (for example, integrators, transimpedance, and some filters) should consider a unity-gain stable, voltage-feedback amplifier such as the OPA2822, because the feedback resistor is the compensation element for a current-feedback op amp. Wideband inverting operation (and especially summing) is particularly suited to the OPA2677. Figure 13 shows a typical inverting configuration where the I/O impedances and signal gain from Figure 1 are retained in an inverting circuit configuration.

In the inverting configuration, two key design considerations

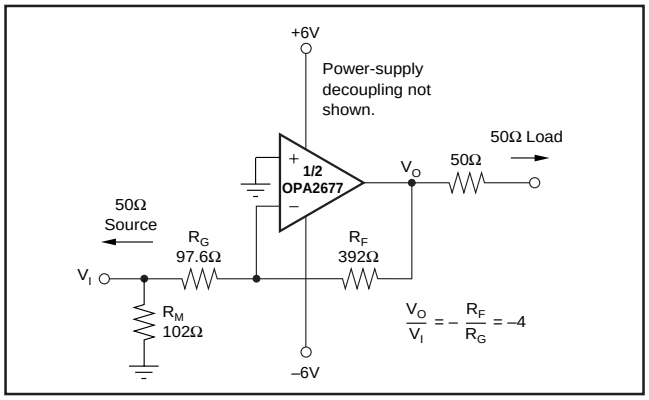


FIGURE 13. Inverting Gain of –4 with Impedance Matching.

must be noted. The first is that the gain resistor (R_G) becomes part of the signal source input impedance. If input impedance matching is desired (which is beneficial whenever the signal is coupled through a cable, twisted pair, long PC board trace or other transmission line conductor), it is normally necessary to add an additional matching resistor to ground. R_G, by itself, is not normally set to the required input impedance since its value, along with the desired gain, will determine an R_F, which may be non-optimal from a frequency response standpoint. The total input impedance for the source becomes the parallel combination of R_G and R_M.

The second major consideration, touched on in the previous paragraph, is that the signal source impedance becomes part of the noise gain equation and has a slight effect on the bandwidth through Equation 15. The values shown in Figure 12 have accounted for this by slightly decreasing R_F (from the optimum values) to re-optimize the bandwidth for the noise gain of Figure 12 (NG = 3.98). In the example of Figure 13, the R_M value combines in parallel with the external 50Ω source impedance, yielding an effective driving impedance of 50Ω || 102Ω = 33.5Ω. This impedance is added in series with R_G for calculating the noise gain—which gives NG = 3.98. This value, along with the inverting input impedance of 22Ω, are inserted into Equation 16 to get a feedback

transimpedance nearly equal to the 402Ω optimum value. Note that the noninverting input in this bipolar supply inverting application is connected directly to ground. It is often suggested that an additional resistor be connected to ground on the noninverting input to achieve bias current error cancellation at the output. The input bias currents for a current-feedback op amp are not generally matched in either magnitude or polarity. Connecting a resistor to ground on the noninverting input of the OPA2677 in the circuit of Figure 13 actually provides additional gain for that input bias and noise currents, but does not decrease the output DC error since the input bias currents are not matched.

OUTPUT CURRENT AND VOLTAGE

The OPA2677 provides output voltage and current capabilities that are unsurpassed in a low-cost dual monolithic op amp. Under no-load conditions at 25°C, the output voltage typically swings closer than 1V to either supply rail; tested at +25°C swing limit is within 1.1V of either rail. Into a 6Ω load (the minimum tested load), it delivers more than ±380mA continuous and > ±1.2A peak output current.

The specifications described above, though familiar in the industry, consider voltage and current limits separately. In many applications, it is the voltage times current (or V-I product) that is more relevant to circuit operation. Refer to the *Output Voltage and Current Limitations* plot in the Typical Characteristics. The X and Y axes of this graph show the zero-voltage output current limit and the zero-current output voltage limit, respectively. The four quadrants give a more detailed view of the OPA2677 output drive capabilities, noting that the graph is bounded by a safe operating area of 1W maximum internal power dissipation (in this case for 1 channel only). Superimposing resistor load lines onto the plot shows that the OPA2677 can drive ±4V into 10Ω or ±4.5V into 25Ω without exceeding the output capabilities or the 1W dissipation limit. A 100Ω load line (the standard test circuit load) shows the full ±5.0V output swing capability, as shown in the Electrical Characteristics tables. The minimum specified output voltage and current over temperature are set by worst-case simulations at the cold temperature extreme. Only at cold startup will the output current and voltage decrease to the numbers shown in the Electrical Characteristics tables. As the output transistors deliver power, the junction temperatures increases, decreasing the V_{BE}s (increasing the available output voltage swing), and increasing the current gains (increasing the available output current). In steady-state operation, the available output voltage and current will always be greater than that shown in the over-temperature specifications, since the output stage junction temperatures will be higher than the minimum specified operating ambient. To maintain maximum output stage linearity, no output short-circuit protection is provided. This is normally not a problem because most applications include a series-matching resistor at the output that limits the internal power dissipation if the output side of this resistor is shorted to ground. However, shorting the output pin directly to the adjacent positive power-supply pin (8-pin package), will in most cases, destroy the amplifier. If additional short-circuit protection is required, consider using the equivalent OPA2674 that includes output current limiting. Alternatively, a small series resistor may be included in the supply lines. Under heavy output loads this will reduce the available output voltage swing. A 5Ω series resistor in each power-supply lead will limit the internal power dissipation to less than 1W for an output short circuit while decreasing the available output voltage swing only 0.5V for up to 100mA desired load currents. Always place the 0.1µF power-supply decoupling capacitors after these supply current limiting resistors directly on the supply pins.

DRIVING CAPACITIVE LOADS

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an analog-to-digital (A/D) converter—including additional external capacitance that may be recommended to improve the A/D converter linearity. A high-speed, high open-loop gain amplifier such as the OPA2677 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested.

When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability. The Typical Characteristics show the recommended R_S vs Capacitive Load and the resulting frequency response at the load. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA2677. Long PC board traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA2677 output pin (see the Board Layout Guidelines section).

DISTORTION PERFORMANCE

The OPA2677 provides good distortion performance into a 100Ω load on ±6V supplies. Relative to alternative solutions, it provides exceptional performance into lighter loads and/or operation on a single +5V supply. Generally, until the fundamental signal reaches very high frequency or power levels, the 2nd-harmonic dominates the distortion with a negligible 3rd-harmonic component. Focusing then on the 2nd-harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network—in the noninverting configuration (see Figure 1), this is the sum of $R_F + R_G$, whereas in the inverting configuration it is just R_F. Also, providing an additional supply decoupling capacitor (0.01µF) between the supply pins (for bipolar operation) improves the 2nd-order distortion slightly (3dB to 6dB).

In most op amps, increasing the output voltage swing increases harmonic distortion directly. The Typical Characteristics show the 2nd-harmonic increasing at a little less than the expected 2x rate whereas the 3rd-harmonic increases at a little less than the expected 3x rate. Where the test power doubles, the difference between it and the 2nd-harmonic decreases less than the expected 6dB, whereas the difference between it and the 3rd-harmonic decreases by less than the expected 12dB. This also shows up in the 2-tone, 3rd-order intermodulation spurious (IM3) response curves. The 3rd-order spurious levels are extremely low at low-output power levels. The output stage continues to hold them low even as the fundamental power reaches very high levels. As the Typical Characteristics show, the spurious intermodulation powers do not increase as predicted by a traditional intercept model. As the fundamental power level increases, the dynamic range does not decrease significantly. For 2-tone centered at 20MHz, with 10dBm/tone into a matched 50Ω load (that is, $2V_{PP}$ for each tone at the load, which requires $8V_{PP}$ for the overall 2-tone envelope at the output pin), the Typical Characteristics show 63dBc difference between the test-tone power and the 3rd-order intermodulation spurious levels. This exceptional performance improves further when operating at lower frequencies.

NOISE PERFORMANCE

Wideband current-feedback op amps generally have a higher output noise than comparable voltage-feedback op amps. The OPA2677 offers an excellent balance between voltage and current noise terms to achieve low output noise. The inverting current noise (24pA/$\sqrt{Hz}$) is significantly lower than earlier solutions whereas the input voltage noise (2.0nV/$\sqrt{Hz}$) is lower than most unity-gain stable, wideband voltage-feedback op amps. This low input voltage noise is achieved at the price of higher noninverting input current noise (16pA/$\sqrt{Hz}$). As long as the AC source impedance looking out of the noninverting node is less than 100Ω, this current noise does not contribute significantly to the total output noise. The op amp input voltage noise and the two input current noise terms combine to give low output noise under a wide variety of operating conditions. Figure 14 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/$\sqrt{Hz}$ or pA/$\sqrt{Hz}$.

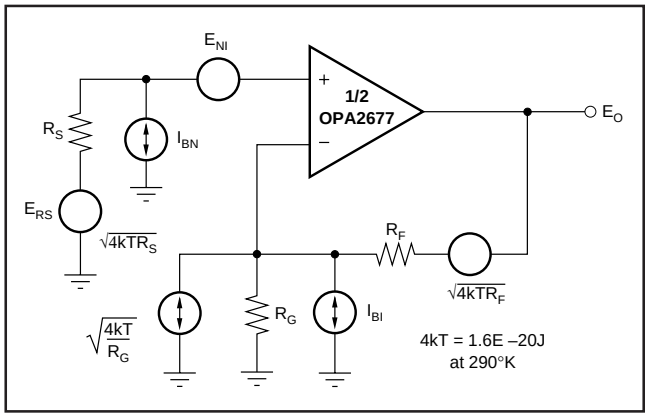


FIGURE 14. Op Amp Noise Analysis Model.

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 17 shows the general form for the output noise voltage using the terms shown in Figure 13.

(17)

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN} \bullet R_S\right)^2 + 4kTR_S + \left(I_{BI} \bullet R_F\right)^2 + 4kTR_FNG\right)}$$

Dividing this expression by the noise gain (NG = $(1 + R_F/R_G)$) gives the equivalent input referred spot noise voltage at the noninverting input, as shown in Equation 18.

(18)

$$E_N = \sqrt{\left(E_{NI}^2 + \left(I_{BN} \bullet R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI} \bullet R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}\right)}$$

Evaluating these two equations for the OPA2677 circuit and component values (see Figure 1) gives a total output spot noise voltage of 13.5nV/$\sqrt{Hz}$ and a total equivalent input spot noise voltage of 3.3nV/$\sqrt{Hz}$. This total input referred spot noise voltage is higher than the 2.0nV/$\sqrt{Hz}$ specification for the op amp voltage noise alone. This reflects the noise added to the output by the inverting current noise times the feedback resistor. If the feedback resistor is reduced in high-gain configurations (as suggested previously), the total input referred voltage noise given by Equation 18 approaches just the 2.0nV/$\sqrt{Hz}$ of the op amp. For example, going to a gain of +10 using R_F = 298Ω gives a total input referred noise of 2.3nV/$\sqrt{Hz}$.

DIFFERENTIAL NOISE PERFORMANCE

As the OPA2677 is used as a differential driver in xDSL applications, it is important to analyze the noise in such a configuration. Figure 15 shows the op amp noise model for the differential configuration.

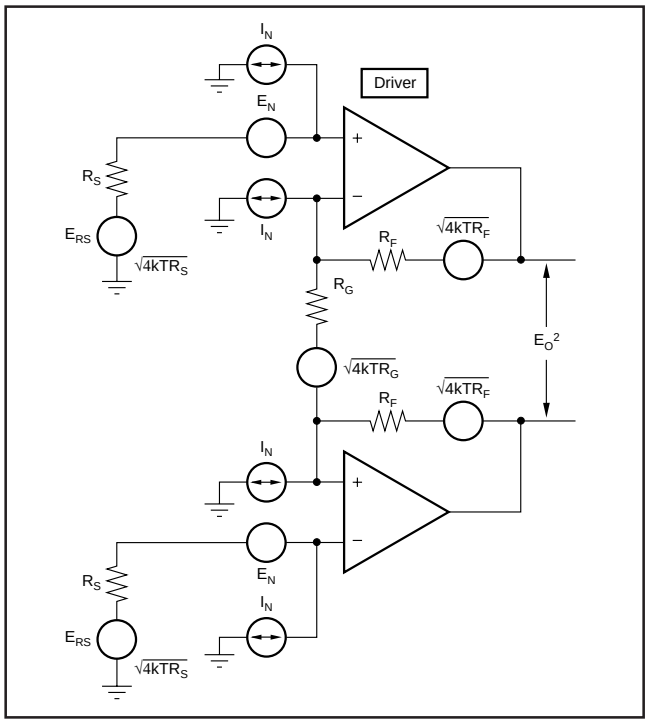


FIGURE 15. Differential Op Amp Noise Analysis Model.

As a reminder, the differential gain is expressed as:

$$G_D = 1 + \frac{2 \bullet R_F}{R_G} \quad (19)$$

The output noise can be expressed as shown below:

(20)

$$E_O = \sqrt{2 \bullet G_D^2 \bullet \left(e_N^2 + (i_N \bullet R_S)^2 + 4kTR_S \right) + 2(i_I R_F)^2 + 2(4kTR_F G_D)}$$

Dividing this expression by the differential noise gain ($G_D = (1 + 2R_F/R_G)$) gives the equivalent input referred spot noise voltage at the noninverting input, as shown in Equation 21.

(21)

$$E_O = \sqrt{2 \bullet \left(e_N^2 + (i_N \bullet R_S)^2 + 4kTR_S \right) + 2\left(\frac{i_I R_F}{G_D} \right)^2 + 2\left(\frac{4kTR_F}{G_D} \right)}$$

Evaluating these equations for the OPA2677 ADSL circuit and component values of Figure 6 gives a total output spot noise voltage of 31.8nV/$\sqrt{Hz}$ and a total equivalent input spot noise voltage of 3.6nV/$\sqrt{Hz}$.

In order to minimize the output noise due to the noninverting input bias current noise, it is recommended to keep the noninverting source impedance as low as possible.

DC ACCURACY AND OFFSET CONTROL

A current-feedback op amp such as the OPA2677 provides exceptional bandwidth in high gains, giving fast pulse settling but only moderate DC accuracy. The Electrical Characteristics show an input offset voltage comparable to high-speed, voltage-feedback amplifiers; however, the two input bias currents are somewhat higher and are unmatched. While bias current cancellation techniques are very effective with most voltage-feedback op amps, they do not generally reduce the output DC offset for wideband current-feedback op amps. Because the two input bias currents are unrelated in both magnitude and polarity, matching the input source impedance to reduce error contribution to the output is ineffective. Evaluating the configuration of Figure 1, using worst-case +25°C input offset voltage and the two input bias currents, gives a worst-case output offset range equal to:

$V_{OFF} = \pm (NG \bullet V_{OS(MAX)}) + (I_{BN} \bullet R_S/2 \bullet NG) \pm (I_{BI} \bullet R_F)$

where NG = noninverting signal gain

$= \pm (4 \bullet 4.5mV) + (30\mu A \bullet 25\Omega \bullet 4) \pm (402\Omega \bullet 30\mu A)$

$= \pm 18mV + 3mV \pm 12.06mV$

$V_{OFF} = -29.06mV$ to $+35.06mV$

THERMAL ANALYSIS

Due to the high output power capability of the OPA2677, heatsinking or forced airflow may be required under extreme operating conditions. Maximum desired junction temperature sets the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed 175°C. Operating junction temperature (T_J) is given by $T_A + P_D \bullet \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipation in the output stage (P_{DL}) to deliver load power. Quiescent power is the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load, but for a grounded resistive load, P_{DL} is at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for equal bipolar supplies). Under this condition, $P_{DL} = V_S^2/(4 \bullet R_L)$ where R_L includes feedback network loading. Note that it is the power in the output stage and not into the load that determines internal power dissipation. As a worst-case example, compute the maximum T_J using an OPA2677 SO-8 in the circuit of Figure 1 operating at the maximum specified ambient temperature of +85°C with both outputs driving a grounded 20Ω load to +2.5V.

$P_D = 12V \bullet 18mA + 2 \bullet [6^2 / (4 \bullet (20\Omega \parallel 534\Omega))] = 882mW$

Maximum $T_J = +85°C + (0.83 \bullet 125°C/W) = 170°C$

This absolute worst-case condition exceeds specified maximum junction temperature. This extreme case is not normally encountered. Where high internal power dissipation is anticipated, consider the thermal slug package version.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier like the OPA2677 requires careful attention to board layout parasitic and external component types. Recommendations that optimize performance include:

a) Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability; on the noninverting input, it can react with the source impedance to cause unintentional band limiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the power-supply pins to high-frequency 0.1µF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections (on pins 4 and 7) should always be decoupled with these capacitors. An optional supply decoupling capacitor across the two power supplies (for bipolar operation) improves 2nd-harmonic distortion performance. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These can be placed somewhat farther from the device and may be shared among several devices in the same area of the PCB.

c) Careful selection and placement of external components preserve the high-frequency performance of the OPA2677. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film and carbon composition axially leaded resistors can also provide good high-frequency performance.

Again, keep leads and PCB trace length as short as possible. Never use wire-wound type resistors in a high-frequency application. Although the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. The frequency response is primarily determined by the feedback resistor value as described previously. Increasing the value reduces the bandwidth, whereas decreasing it gives a more peaked frequency response. The 402Ω feedback resistor used in the Typical Characteristics at a gain of +4 on ±6V supplies is a good starting point for design. Note that a 511Ω feedback resistor, rather than a direct short, is recommended for the unity-gain follower application. A current-feedback op amp requires a feedback resistor even in the unity-gain follower configuration to control stability.

d) Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of Recommended R_S vs Capacitive Load. Low parasitic capacitive loads (< 5pF) may not need an R_S because the OPA2677 is nominally compensated to operate with a 2pF parasitic load. If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary on board; in fact, a higher impedance environment improves distortion (see the distortion versus load plots). With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA2677 is used, as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device.

This total effective impedance should be set to match the trace impedance. The high output voltage and current capability of the OPA2677 allows multiple destination devices to be handled as separate transmission lines, each with their own series and shunt terminations. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of R_S vs Capacitive Load. However, this does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there is some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high-speed part like the OPA2677 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network, which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA2677 directly onto the board.

f) Use the $-V_S$ plane to conduct heat out of the HSOP-8 PowerPAD package (OPA2677IDDA) or the QFN-16 (OPA2677IRGV). These packages attach the die directly to an exposed thermal pad on the bottom, which should be soldered to the board. This pad must be connected electrically to the same voltage plane as the most negative supply applied to the OPA2677 (in Figure 6, this would be ground), which must have a minimum area of 3.5" x 3.5" (88.9mm x 88.9mm) to produce the θ_{JA} values in the *Electrical Characteristics* tables.

INPUT AND ESD PROTECTION

The OPA2677 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices and are reflected in the absolute maximum ratings table. All device pins have limited ESD protection using internal diodes to the power supplies, as shown in Figure 16.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±15V supply parts driving into the OPA2677), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible, since high values degrade both noise performance and frequency response.

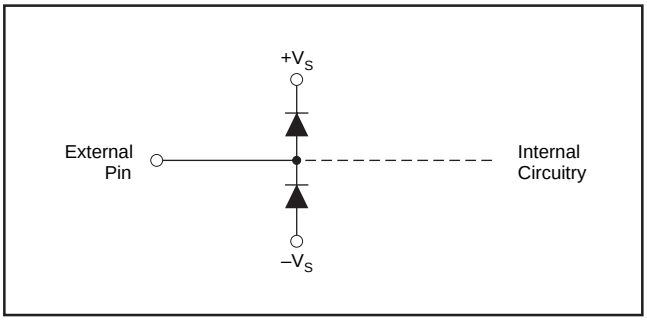


FIGURE 16. Internal ESD Protection.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
7/08	I	2	Abs Max Ratings	Changed Storage Temperature Range from –40°C to +125°C to –65°C to +125°C.
3/08	H	3	Electrical Characteristics	Added Both Channels; Power Supply section under Conditions.
		4	Electrical Characteristics	Added +5V and Both Channels; Power Supply section under Conditions.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2677IDDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	OP2677	Samples
OPA2677IDDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	OP2677	Samples
OPA2677IRGVT	ACTIVE	VQFN	RGV	16	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2677	Samples
OPA2677U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR		OPA 2677U	Samples
OPA2677U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2677U	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

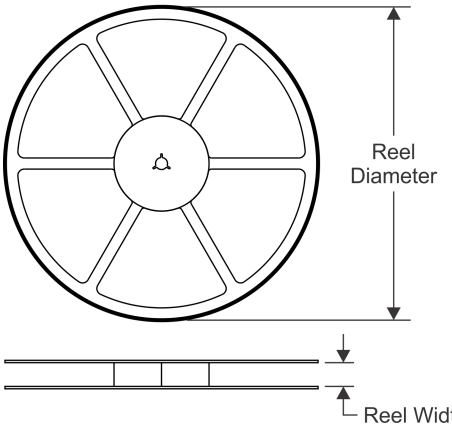
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

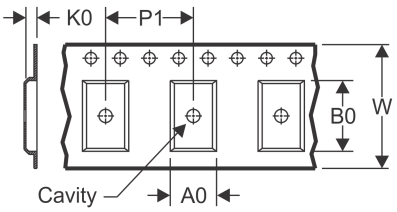
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

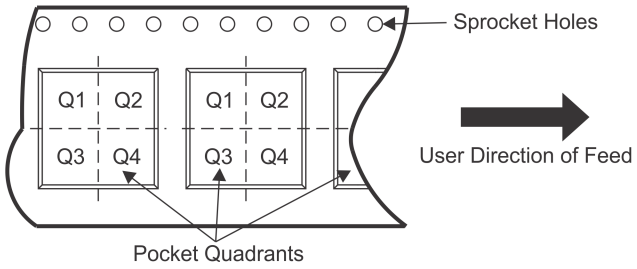


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

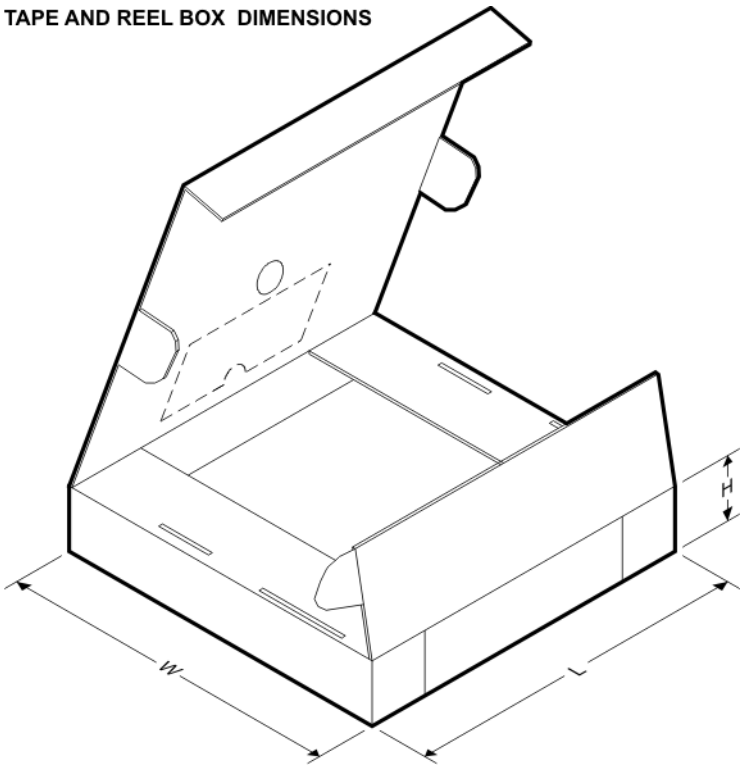
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2677IDDAR	SO Power PAD	DDA	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2677IRGVT	VQFN	RGV	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
OPA2677U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

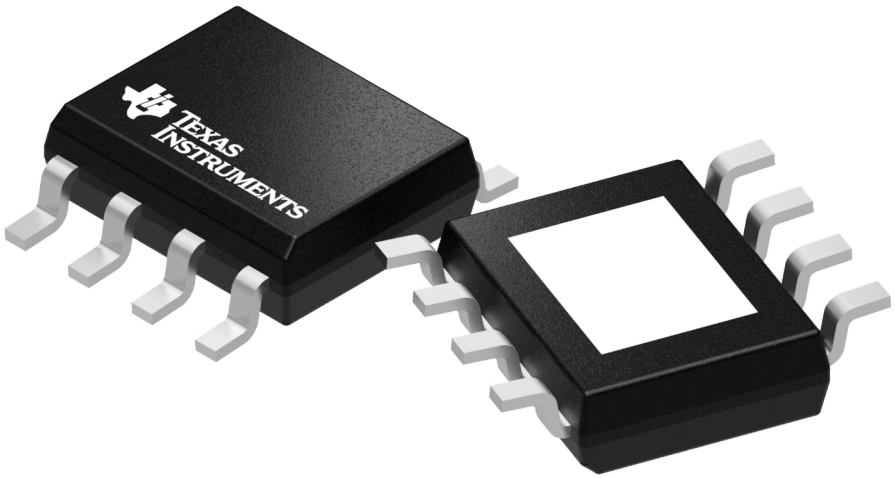


*All dimensions are nominal

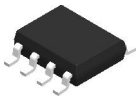
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2677IDDAR	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0
OPA2677IRGVT	VQFN	RGV	16	250	210.0	185.0	35.0
OPA2677U/2K5	SOIC	D	8	2500	367.0	367.0	35.0

DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

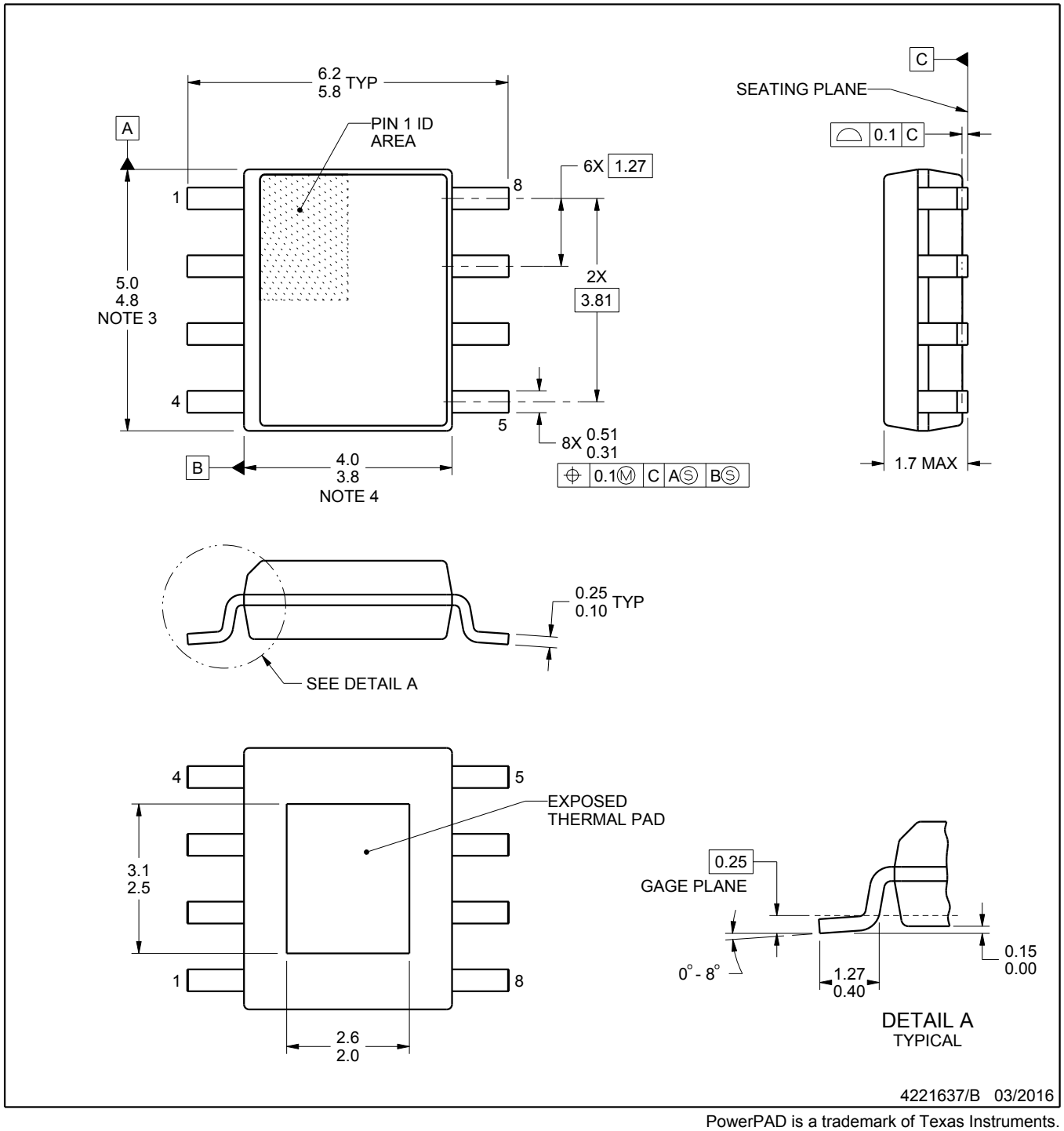


PACKAGE OUTLINE

DDA0008J

PowerPAD™ SOIC - 1.7 mm max height

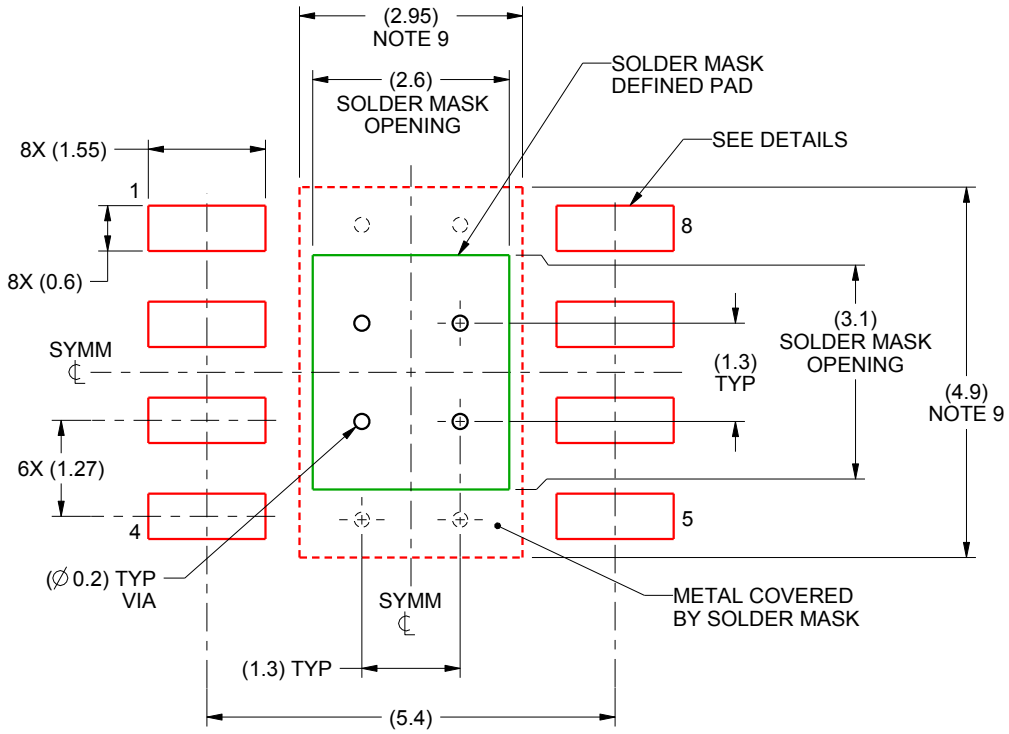
PLASTIC SMALL OUTLINE



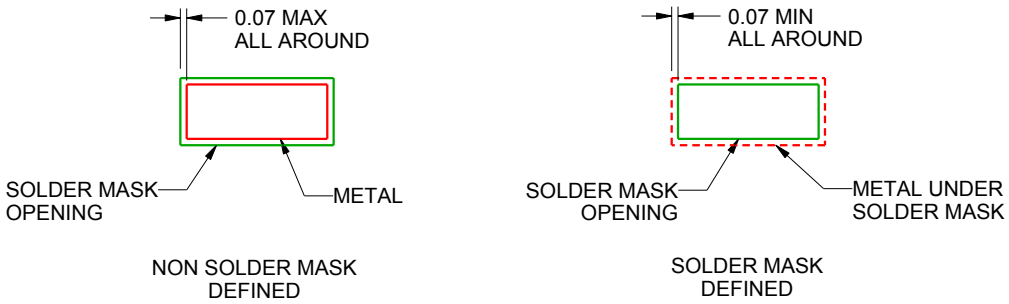
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

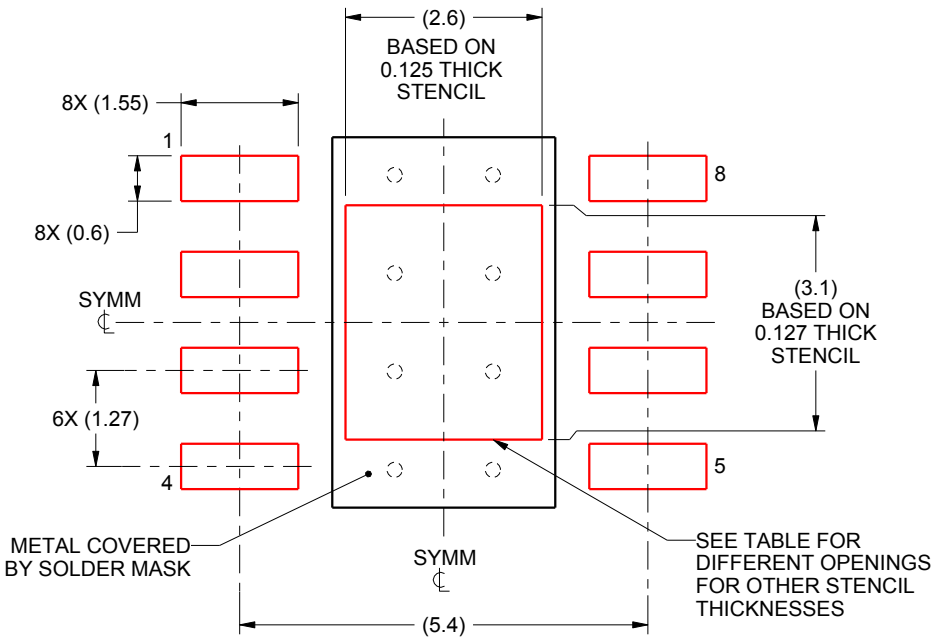


SOLDER MASK DETAILS

4221637/B 03/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

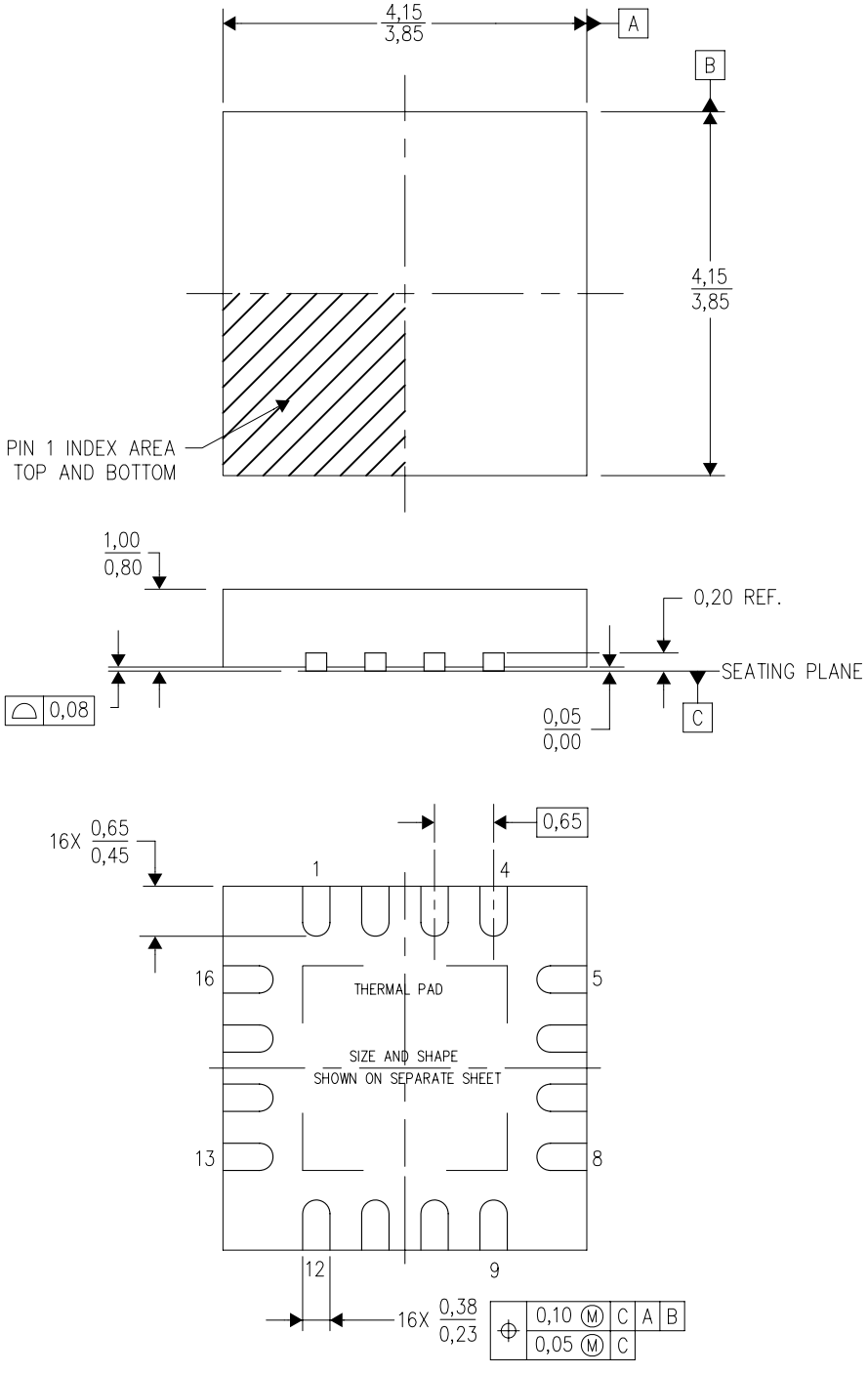
STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 3.47
0.125	2.6 X 3.1 (SHOWN)
0.150	2.37 X 2.83
0.175	2.20 X 2.62

4221637/B 03/2016

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

RGV (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

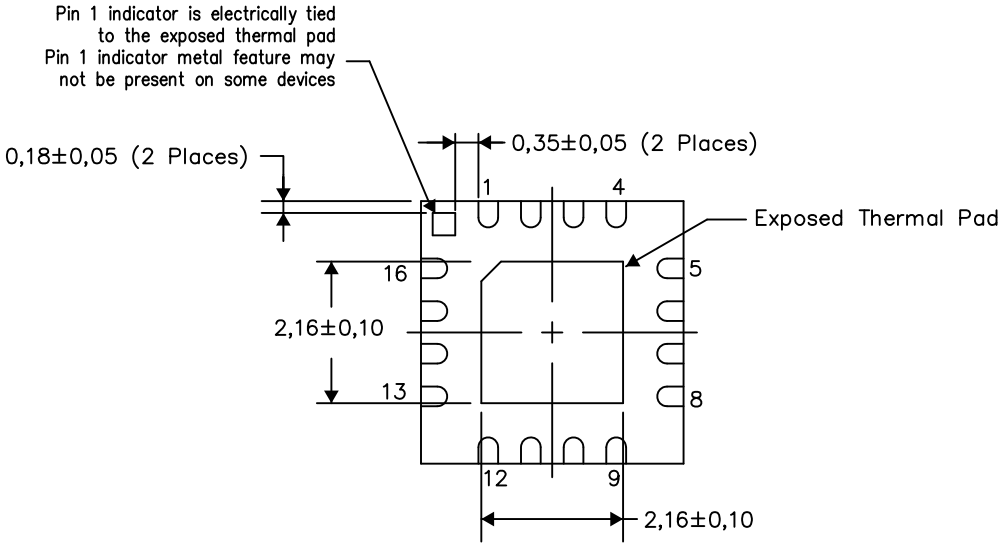
RGV (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



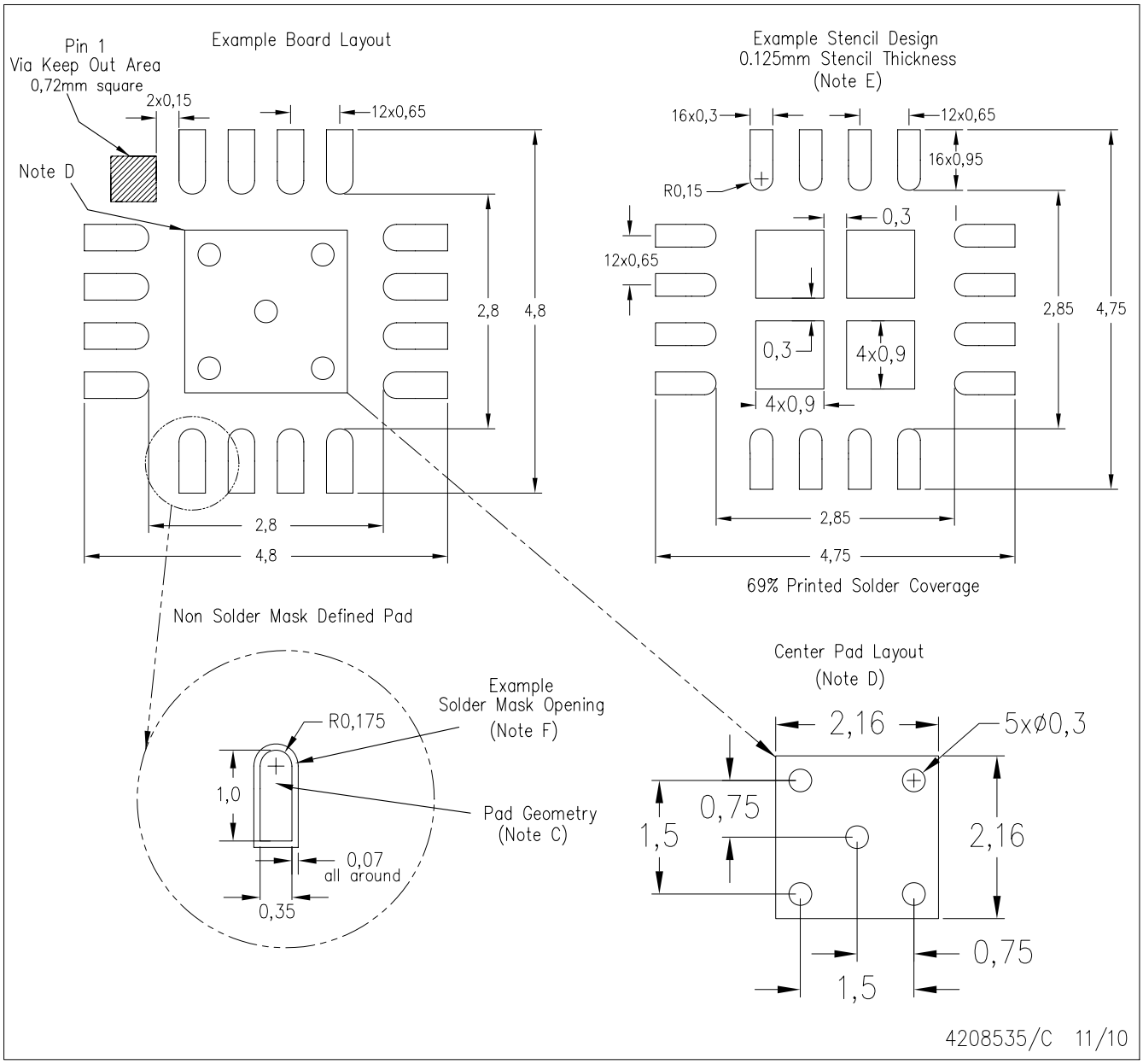
Bottom View

Exposed Thermal Pad Dimensions

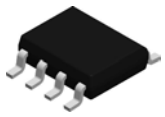
4206351–2/L 05/13

NOTE: All linear dimensions are in millimeters

RGV (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

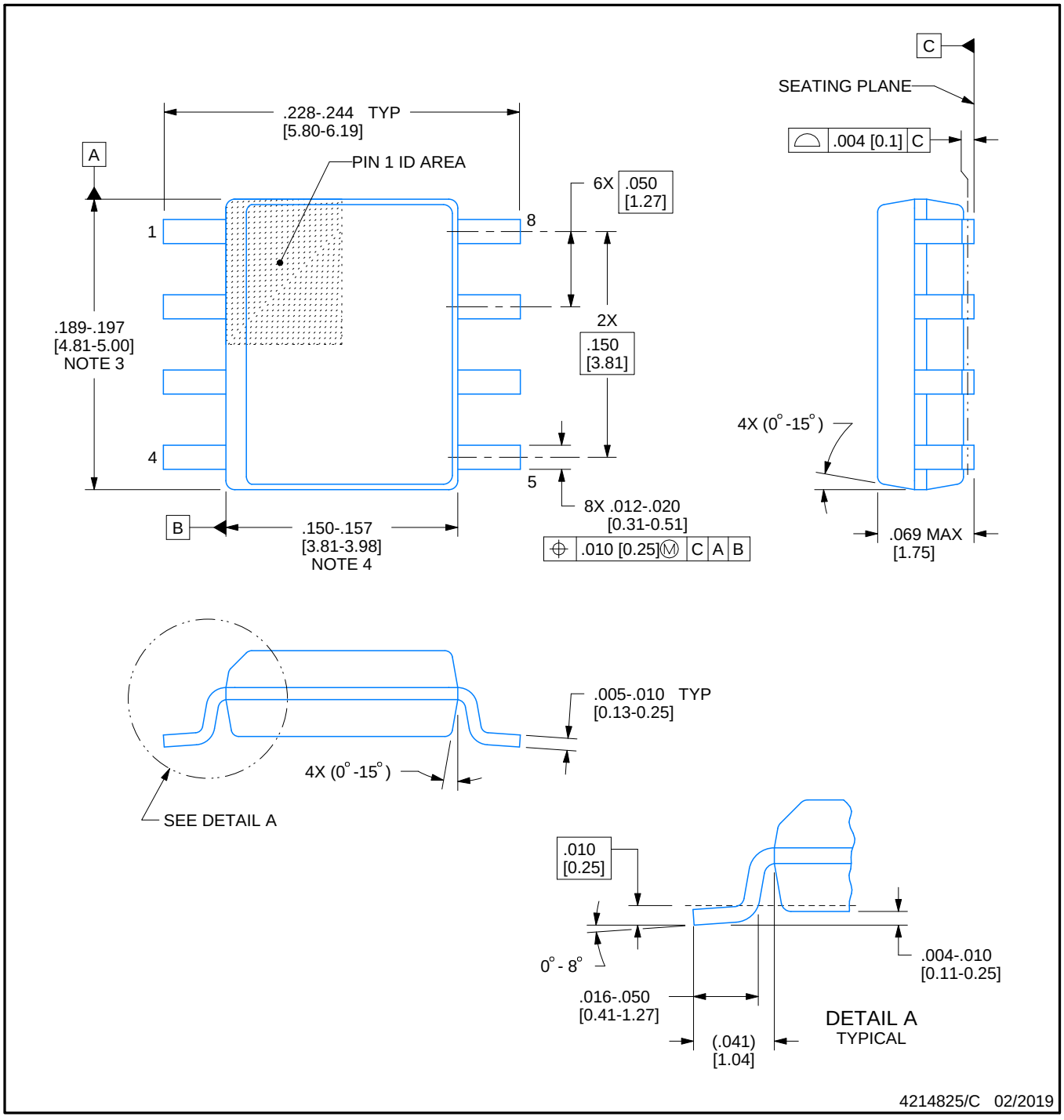


PACKAGE OUTLINE

D0008A

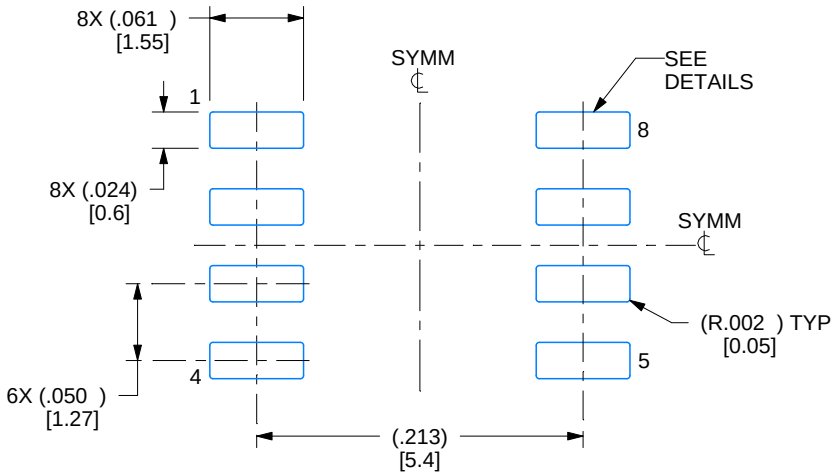
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

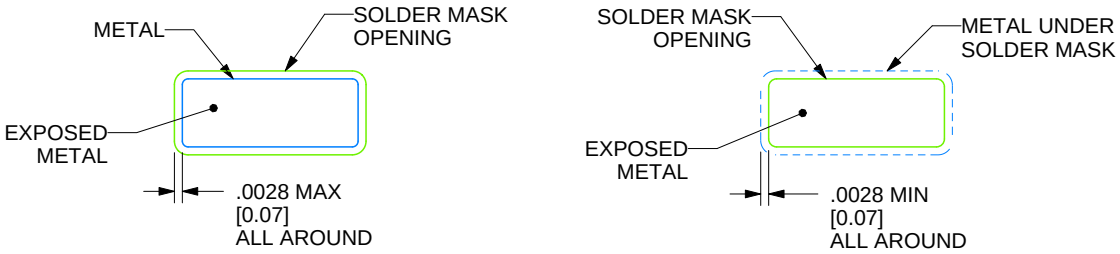


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

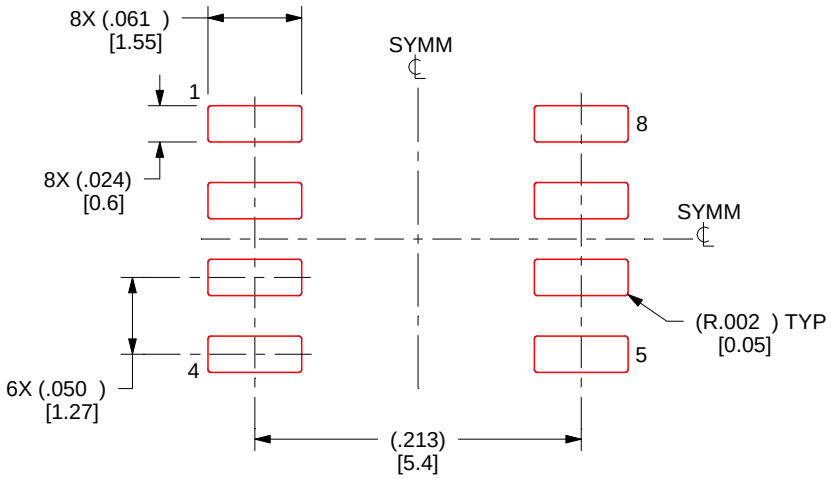
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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