

### FEATURES

- High slew rate: 9 V/ $\mu$ s
- Wide bandwidth: 4 MHz
- Low supply current: 250  $\mu$ A/amplifier maximum
- Low offset voltage: 3 mV maximum
- Low bias current: 100 pA maximum
- Fast settling time
- Common-mode range includes V+
- Unity-gain stable
- 14-ball wafer level chip scale for quad

### APPLICATIONS

- Active filters
- Fast amplifiers
- Integrators
- Supply current monitoring

### GENERAL DESCRIPTION

The **OP282/OP482** dual and quad operational amplifiers feature excellent speed at exceptionally low supply currents. The slew rate is typically 9 V/ $\mu$ s with a supply current of less than 250  $\mu$ A per amplifier. These unity-gain stable amplifiers have a typical gain bandwidth of 4 MHz.

The JFET input stage of the **OP282/OP482** ensures that the bias current is typically a few picoamps and is less than 500 pA over the full temperature range. The offset voltage is less than 3 mV for the dual amplifier and less than 4 mV for the quad amplifier.

With a wide output swing (within 1.5 V of each supply), low power consumption, and high slew rate, the **OP282/OP482** are ideal for battery-powered systems or power-restricted applications. An input common-mode range that includes the positive supply makes the **OP282/OP482** an excellent choice for high-side signal conditioning.

The **OP282/OP482** are specified over the extended industrial temperature range. The **OP282** is available in the standard 8-lead, narrow SOIC and MSOP packages. The **OP482** is available in the PDIP and narrow SOIC packages, as well as a 14-ball WLCSP.

### PIN CONNECTIONS

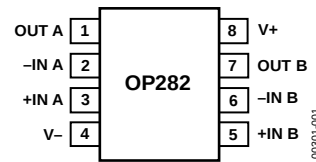


Figure 1. 8-Lead, Narrow-Body SOIC (S-Suffix) [R-8]



Figure 2. 8-Lead MSOP [RM-8]

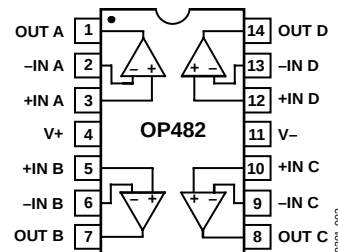


Figure 3. 14-Lead PDIP (P-Suffix) [N-14]

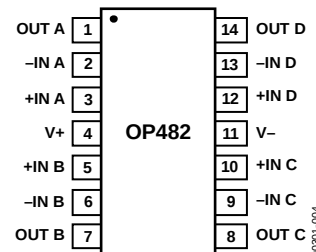


Figure 4. 14-Lead, Narrow-Body SOIC (S-Suffix) [R-14]

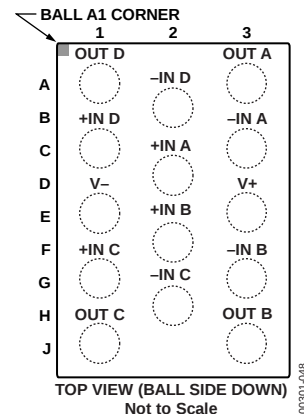


Figure 5. 14-Ball WLCSP [CB-14-2]

Rev. I

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## REVISION HISTORY

### 9/13—Rev. H to Rev. I

|                                  |    |
|----------------------------------|----|
| Changes to Figure 5.....         | 1  |
| Updated Outline Dimensions ..... | 14 |
| Changes to Ordering Guide .....  | 16 |

### 9/10—Rev. G to Rev. H

|                                                                 |           |
|-----------------------------------------------------------------|-----------|
| Added WLCSP .....                                               | Universal |
| Changes to Features Section.....                                | 1         |
| Changes to General Description Section .....                    | 1         |
| Added Figure 5; Renumbered Sequentially .....                   | 1         |
| Changes to Large-Signal Voltage Gain Parameter, Table 1 .....   | 3         |
| Changes to Table 2, Thermal Resistance Section, and Table 3 ... | 4         |
| Change to Figure 30 .....                                       | 9         |
| Added Figure 53.....                                            | 16        |
| Changes to Ordering Guide .....                                 | 16        |

### 7/08—Rev. F to Rev. G

|                                          |    |
|------------------------------------------|----|
| Changes to Phase Inversion Section ..... | 12 |
| Deleted Figure 45.....                   | 12 |
| Added Figure 45 and Figure 46.....       | 12 |
| Updated Outline Dimensions .....         | 14 |
| Changes to Ordering Guide .....          | 16 |

### 10/04—Rev. E to Rev. F

|                                           |           |
|-------------------------------------------|-----------|
| Deleted 8-Lead PDIP .....                 | Universal |
| Added 8-Lead MSOP .....                   | Universal |
| Changes to Format and Layout.....         | Universal |
| Changes to Features.....                  | 1         |
| Changes to Pin Configurations.....        | 1         |
| Changes to General Description .....      | 1         |
| Changes to Specifications .....           | 3         |
| Changes to Absolute Maximum Ratings ..... | 4         |
| Changes to Table 3.....                   | 4         |

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### Added Figure 5 through Figure 20; Renumbered

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| Updated Figure 21 and Figure 22 .....               | 7  |
| Updated Figure 23 and Figure 27 .....               | 8  |
| Updated Figure 29 .....                             | 9  |
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| Deleted OP282/OP482 Spice Macro Model Section ..... | 9  |
| Deleted Figure 4.....                               | 9  |
| Deleted OP282 Spice Marco Model .....               | 10 |
| Updated Outline Dimensions.....                     | 14 |
| Changes to Ordering Guide .....                     | 14 |

### 10/02—Rev. D to Rev. E

|                                               |    |
|-----------------------------------------------|----|
| Edits to 8-Lead Epoxy DIP (P-Suffix) Pin..... | 1  |
| Edits to Ordering Guide .....                 | 3  |
| Edits to Outline Dimensions.....              | 11 |

### 9/02—Rev. C to Rev. D

|                                            |    |
|--------------------------------------------|----|
| Edits to 14-Lead SOIC (S-Suffix) Pin ..... | 1  |
| Replaced 8-Lead SOIC (S-Suffix) .....      | 11 |

### 4/02—Rev. B to Rev. C

|                                                    |    |
|----------------------------------------------------|----|
| Wafer Test Limits Deleted .....                    | 2  |
| Edits to Absolute Maximum Ratings .....            | 3  |
| Dice Characteristics Deleted.....                  | 3  |
| Edits to Ordering Guide .....                      | 3  |
| Edits to Figure 1.....                             | 7  |
| Edits to Figure 3.....                             | 8  |
| 20-Position Chip Carrier (RC Suffix) Deleted ..... | 11 |

## SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS

At  $V_S = \pm 15.0\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted; applies to both A and G grades.

Table 1.

| Parameter                    | Symbol                   | Test Conditions/Comments                                                                                                                                                 | Min       | Typ   | Max      | Unit                         |
|------------------------------|--------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|----------|------------------------------|
| INPUT CHARACTERISTICS        |                          |                                                                                                                                                                          |           |       |          |                              |
| Offset Voltage               | $V_{OS}$                 | <b>OP282</b><br><b>OP282</b> , $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$<br><b>OP482</b><br><b>OP482</b> , $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ |           | 0.2   | 3        | mV                           |
|                              |                          |                                                                                                                                                                          |           |       | 4.5      | mV                           |
|                              |                          |                                                                                                                                                                          |           | 0.2   | 4        | mV                           |
|                              |                          |                                                                                                                                                                          |           |       | 6        | mV                           |
| Input Bias Current           | $I_B$                    | $V_{CM} = 0\text{ V}$<br>$V_{CM} = 0\text{ V}^1$                                                                                                                         |           | 3     | 100      | pA                           |
|                              |                          |                                                                                                                                                                          |           |       | 500      | pA                           |
| Input Offset Current         | $I_{OS}$                 | $V_{CM} = 0\text{ V}$<br>$V_{CM} = 0\text{ V}^1$                                                                                                                         |           | 1     | 50       | pA                           |
|                              |                          |                                                                                                                                                                          |           |       | 250      | pA                           |
|                              |                          |                                                                                                                                                                          |           |       |          |                              |
| Input Voltage Range          |                          |                                                                                                                                                                          | -11       |       | +15      | V                            |
| Common-Mode Rejection Ratio  | CMRR                     | $-11\text{ V} \leq V_{CM} \leq +15\text{ V}$ , $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$                                                                       | 70        | 90    |          | dB                           |
| Large-Signal Voltage Gain    | $A_{VO}$                 | $R_L = 10\text{ k}\Omega$ , $V_O = \pm 13.5\text{ V}$<br>$R_L = 10\text{ k}\Omega$ , $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$                                 | 20        |       |          | V/mV                         |
|                              |                          |                                                                                                                                                                          |           |       |          | V/mV                         |
| Offset Voltage Drift         | $\Delta V_{OS}/\Delta T$ |                                                                                                                                                                          |           | 10    |          | $\mu\text{V}/^\circ\text{C}$ |
| Bias Current Drift           | $\Delta I_B/\Delta T$    |                                                                                                                                                                          |           | 8     |          | $\text{pA}/^\circ\text{C}$   |
| OUTPUT CHARACTERISTICS       |                          |                                                                                                                                                                          |           |       |          |                              |
| Output Voltage High          | $V_{OH}$                 | $R_L = 10\text{ k}\Omega$                                                                                                                                                | 13.5      | 13.9  |          | V                            |
| Output Voltage Low           | $V_{OL}$                 | $R_L = 10\text{ k}\Omega$                                                                                                                                                |           | -13.9 | -13.5    | V                            |
| Short-Circuit Limit          | $I_{SC}$                 | Source                                                                                                                                                                   | 3         | 10    |          | mA                           |
|                              |                          | Sink                                                                                                                                                                     |           | -12   | -8       | mA                           |
| Open-Loop Output Impedance   | $Z_{OUT}$                | $f = 1\text{ MHz}$                                                                                                                                                       |           | 200   |          | $\Omega$                     |
| POWER SUPPLY                 |                          |                                                                                                                                                                          |           |       |          |                              |
| Power Supply Rejection Ratio | PSRR                     | $V_S = \pm 4.5\text{ V}$ to $\pm 18\text{ V}$ , $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$                                                                      |           | 25    | 316      | $\mu\text{V}/\text{V}$       |
| Supply Current/Amplifier     | $I_{SY}$                 | $V_O = 0\text{ V}$ , $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$                                                                                                  |           | 210   | 250      | $\mu\text{A}$                |
| Supply Voltage Range         | $V_S$                    |                                                                                                                                                                          | $\pm 4.5$ |       | $\pm 18$ | V                            |
| DYNAMIC PERFORMANCE          |                          |                                                                                                                                                                          |           |       |          |                              |
| Slew Rate                    | SR                       | $R_L = 10\text{ k}\Omega$                                                                                                                                                | 7         | 9     |          | $\text{V}/\mu\text{s}$       |
| Full-Power Bandwidth         | $BW_P$                   | 1% distortion                                                                                                                                                            |           | 125   |          | kHz                          |
| Settling Time                | $t_s$                    | To 0.01%                                                                                                                                                                 |           | 1.6   |          | $\mu\text{s}$                |
| Gain Bandwidth Product       | GBP                      |                                                                                                                                                                          |           | 4     |          | MHz                          |
| Phase Margin                 | $\phi_M$                 |                                                                                                                                                                          |           | 55    |          | Degrees                      |
| NOISE PERFORMANCE            |                          |                                                                                                                                                                          |           |       |          |                              |
| Voltage Noise                | $e_n$ p-p                | 0.1 Hz to 10 Hz                                                                                                                                                          |           | 1.3   |          | $\mu\text{V}$ p-p            |
| Voltage Noise Density        | $e_n$                    | $f = 1\text{ kHz}$                                                                                                                                                       |           | 36    |          | $\text{nV}/\sqrt{\text{Hz}}$ |
| Current Noise Density        | $i_n$                    |                                                                                                                                                                          |           | 0.01  |          | $\text{pA}/\sqrt{\text{Hz}}$ |

<sup>1</sup> The input bias and offset currents are characterized at  $T_A = T_J = 85^\circ\text{C}$ . Bias and offset currents are guaranteed but not tested at  $-40^\circ\text{C}$ .

## ABSOLUTE MAXIMUM RATINGS

Table 2.

| Parameter                               | Rating                                          |
|-----------------------------------------|-------------------------------------------------|
| Supply Voltage                          | $\pm 18\text{ V}$                               |
| Input Voltage                           | $\pm 18\text{ V}$                               |
| Differential Input Voltage <sup>1</sup> | 36 V                                            |
| Output Short-Circuit Duration           | Indefinite                                      |
| Storage Temperature Range               | $-65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$ |
| Operating Temperature Range             | $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$  |
| Junction Temperature Range              | $-65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$ |
| Lead Temperature (Soldering 60 sec)     | $300^{\circ}\text{C}$                           |

<sup>1</sup> For supply voltages less than  $\pm 18\text{ V}$ , the absolute maximum input voltage is equal to the supply voltage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions, that is, a device in socket for PDIP.  $\theta_{JA}$  is specified for a device soldered in the circuit board for SOIC\_N, MSOP, and WLCSP packages. This was measured using a standard 4-layer board.

Table 3.

| Package Type                      | $\theta_{JA}$ | $\theta_{JC}$ | Unit                 |
|-----------------------------------|---------------|---------------|----------------------|
| 8-Lead MSOP [RM]                  | 142           | 45            | $^{\circ}\text{C/W}$ |
| 8-Lead SOIC_N (S-Suffix) [R]      | 120           | 45            | $^{\circ}\text{C/W}$ |
| 14-Lead PDIP (P-Suffix) [N]       | 83            | 39            | $^{\circ}\text{C/W}$ |
| 14-Lead SOIC_N (S-Suffix) [R]     | 112           | 35            | $^{\circ}\text{C/W}$ |
| 14-Ball WLCSP [CB] <sup>1,2</sup> | 70            | 16            | $^{\circ}\text{C/W}$ |

<sup>1</sup> Simulated thermal numbers per JESD51-9.

<sup>2</sup> Junction-to-board thermal resistance.

## ESD CAUTION



### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## TYPICAL PERFORMANCE CHARACTERISTICS

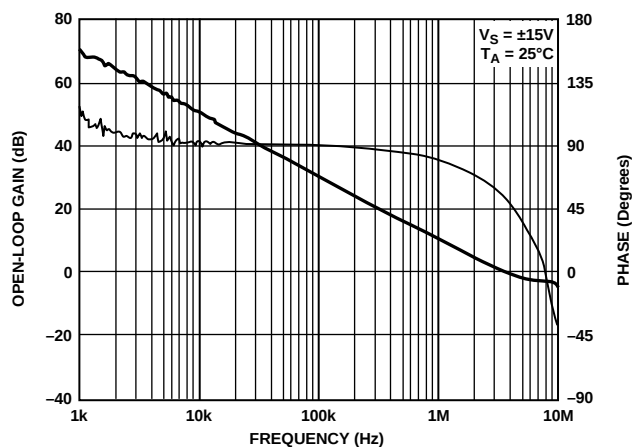


Figure 6. OP282 Open-Loop Gain and Phase vs. Frequency

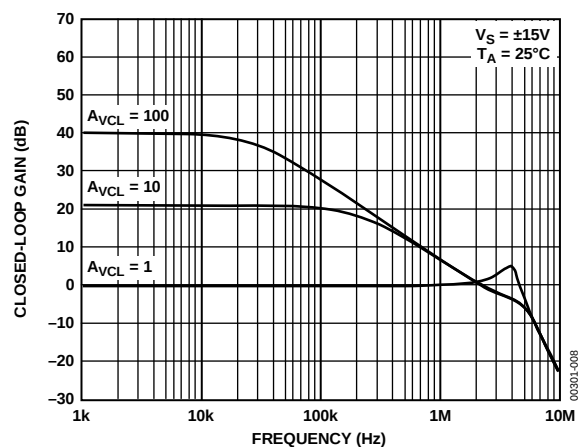


Figure 9. OP282 Closed-Loop Gain vs. Frequency

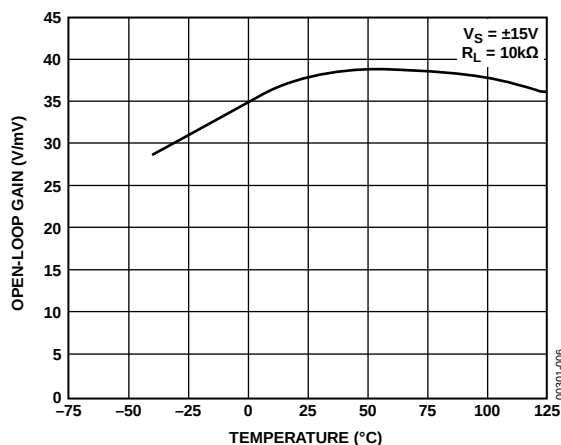


Figure 7. OP282 Open-Loop Gain vs. Temperature

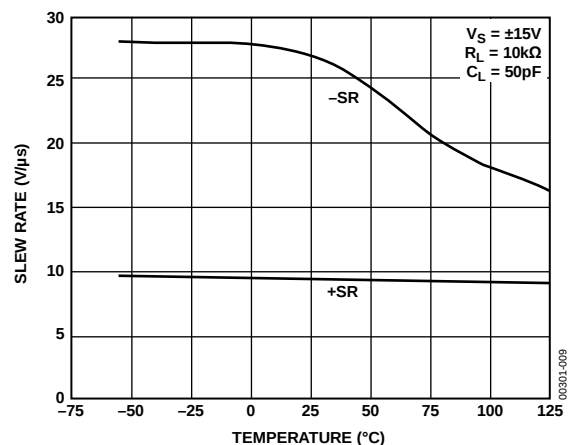


Figure 10. OP282 Slew Rate vs. Temperature

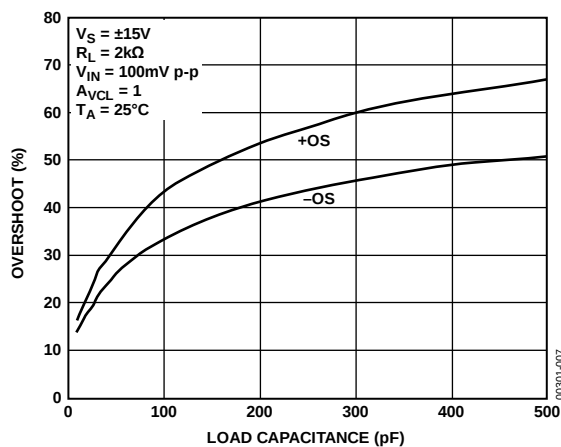


Figure 8. OP282 Small-Signal Overshoot vs. Load Capacitance

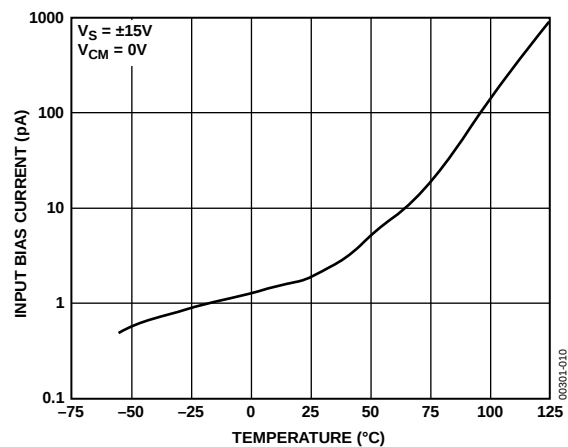


Figure 11. OP282 Input Bias Current vs. Temperature

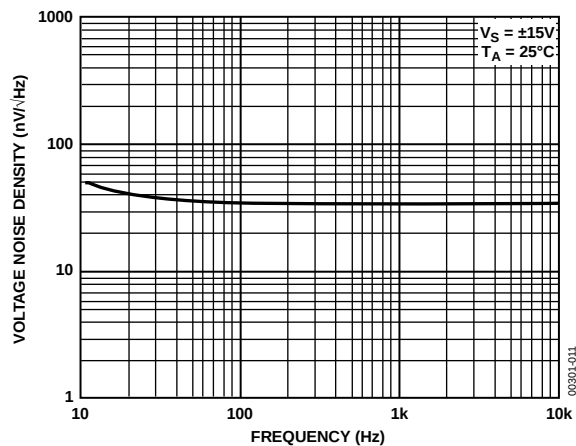


Figure 12. OP282 Voltage Noise Density vs. Frequency

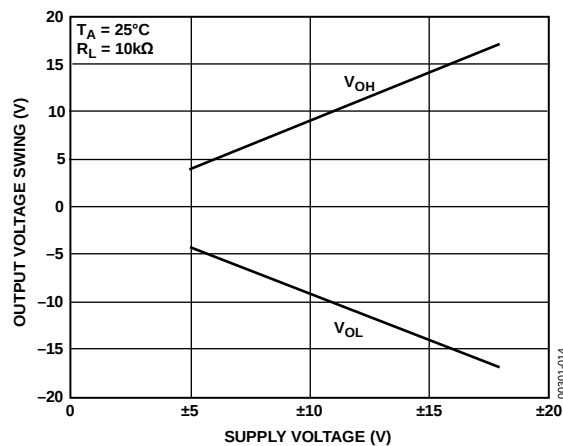


Figure 15. OP282 Output Voltage Swing vs. Supply Voltage

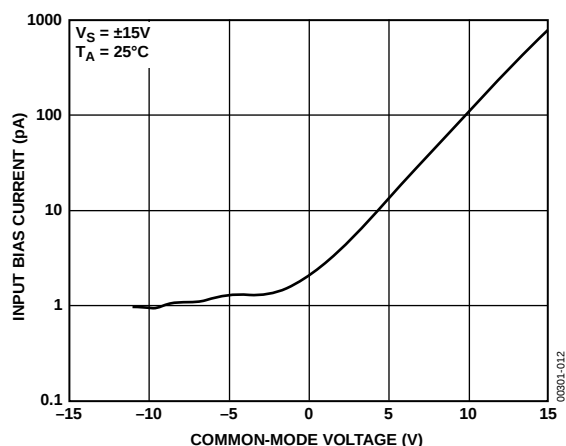


Figure 13. OP282 Input Bias Current vs. Common-Mode Voltage

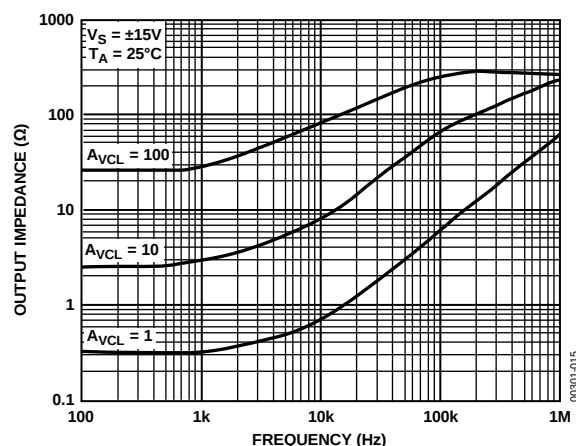


Figure 16. OP282 Closed-Loop Output Impedance vs. Frequency

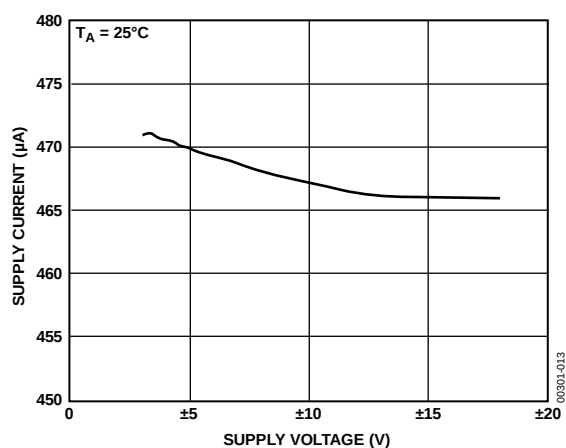


Figure 14. OP282 Supply Current vs. Supply Voltage

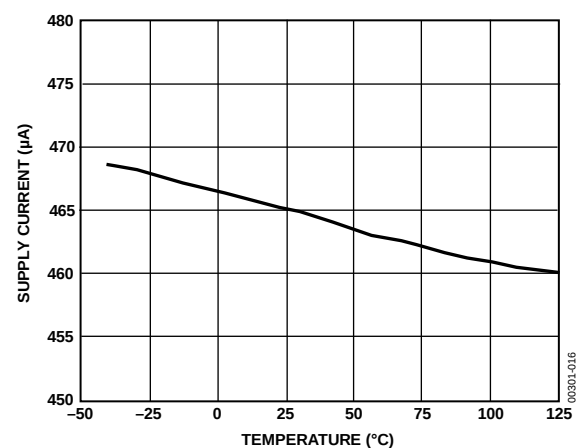


Figure 17. OP282 Supply Current vs. Temperature

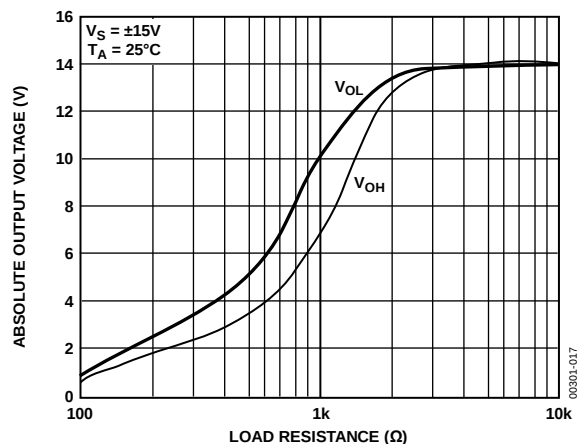


Figure 18. OP282 Absolute Output Voltage vs. Load Resistance

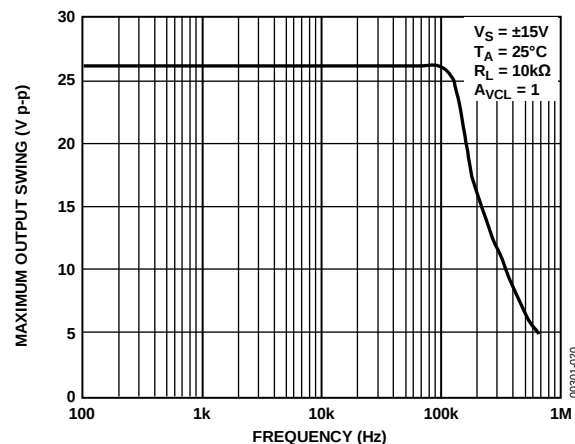


Figure 21. OP282 Maximum Output Swing vs. Frequency

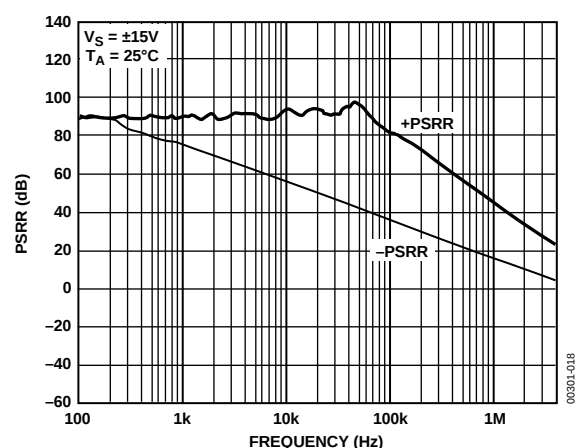


Figure 19. OP282 PSRR vs. Frequency

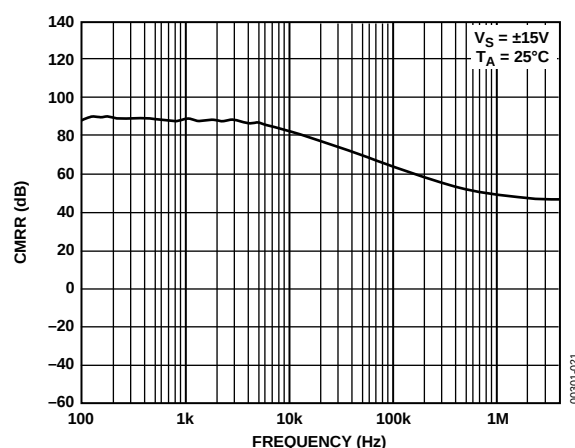


Figure 22. OP282 CMRR vs. Frequency

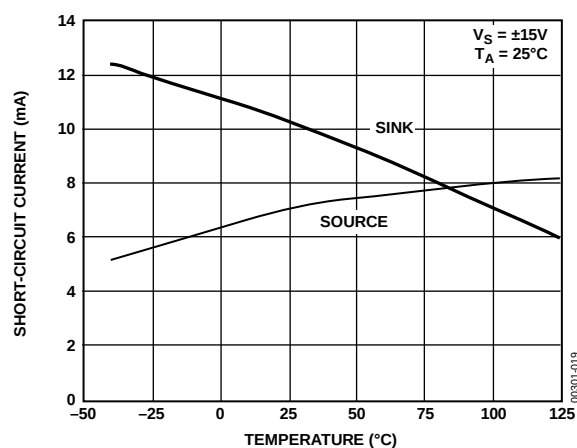


Figure 20. OP282 Short-Circuit Current vs. Temperature

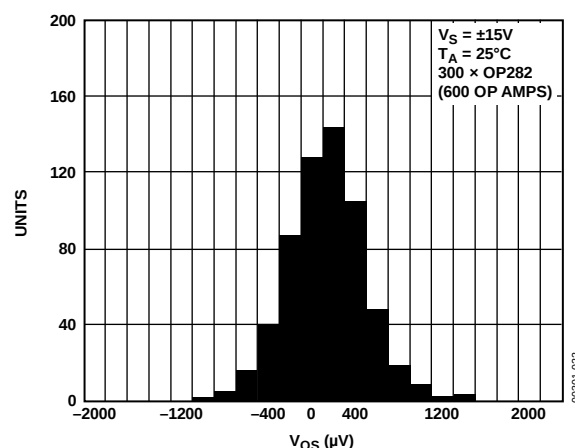


Figure 23. OP282 VOS Distribution, SOIC\_N Package

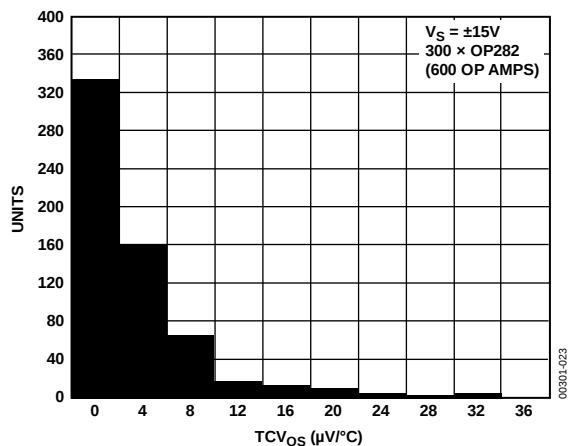


Figure 24. OP282 TCVOS Distribution, SOIC\_N Package

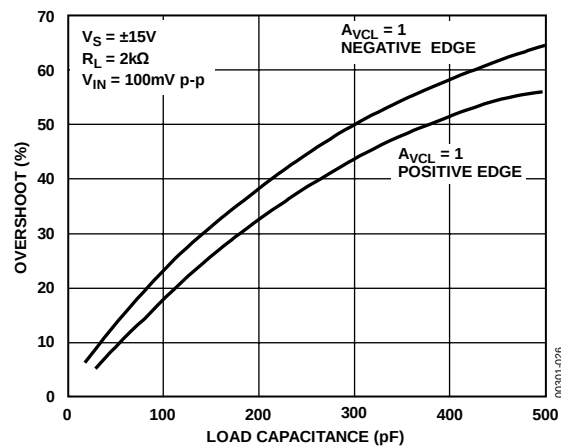


Figure 27. OP482 Small-Signal Overshoot vs. Load Capacitance

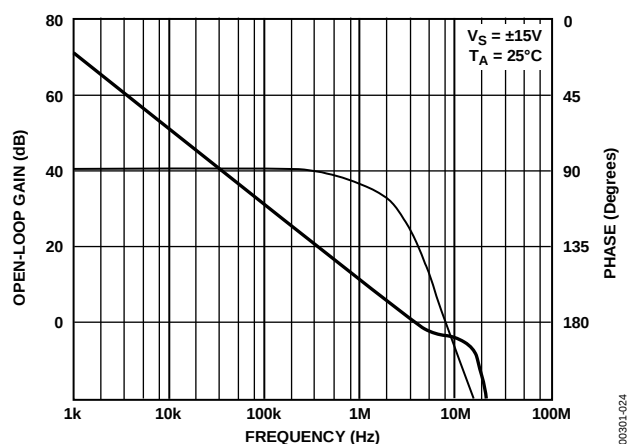


Figure 25. OP482 Open-Loop Gain and Phase vs. Frequency

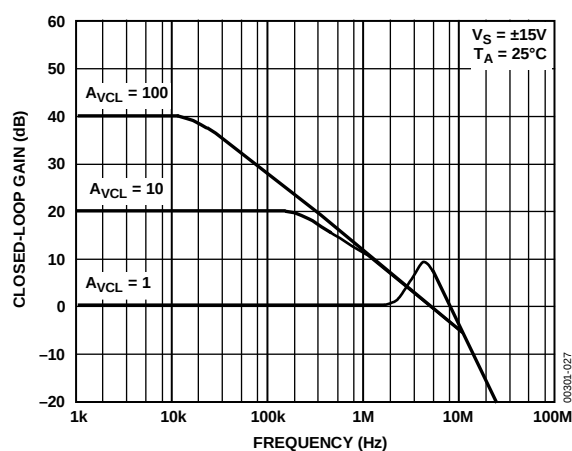


Figure 28. OP482 Closed-Loop Gain vs. Frequency

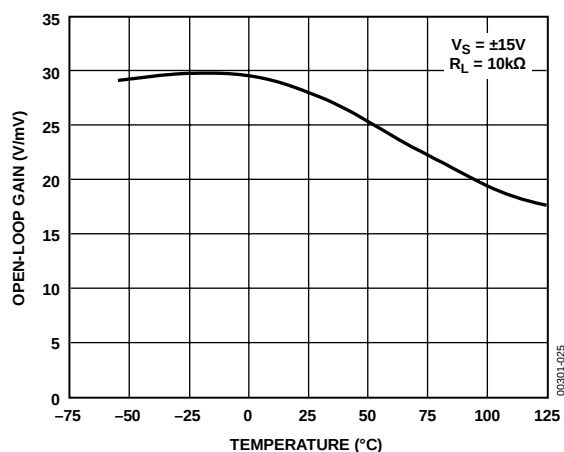


Figure 26. OP482 Open-Loop Gain vs. Temperature

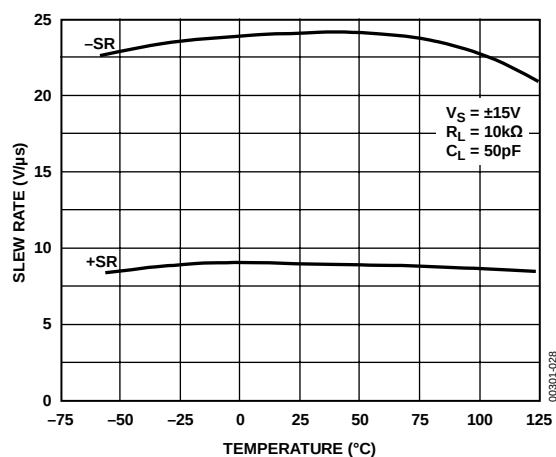


Figure 29. OP482 Slew Rate vs. Temperature

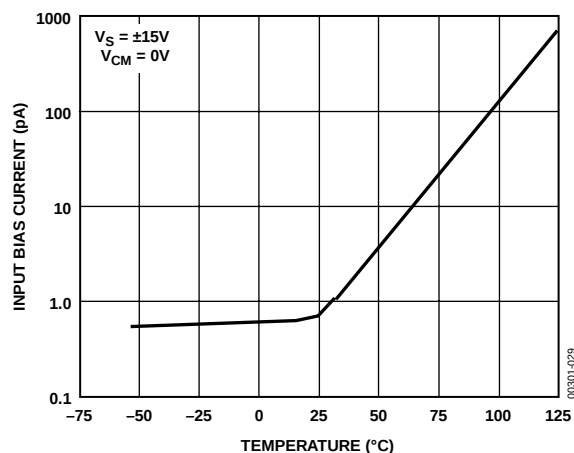


Figure 30. OP482 Input Bias Current vs. Temperature

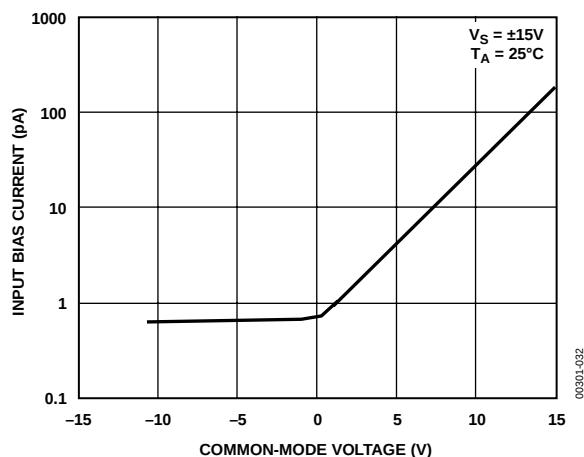


Figure 33. OP482 Input Bias Current vs. Common-Mode Voltage

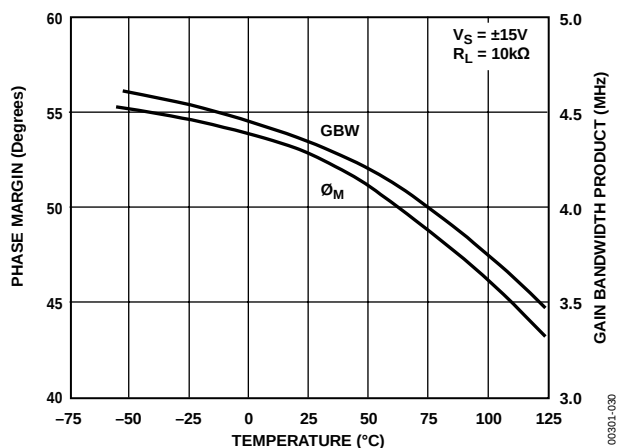


Figure 31. OP482 Phase Margin and Gain Bandwidth Product vs. Temperature

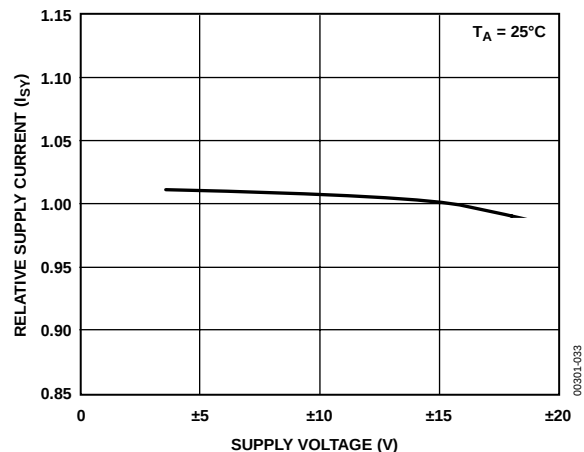


Figure 34. OP482 Relative Supply Current vs. Supply Voltage

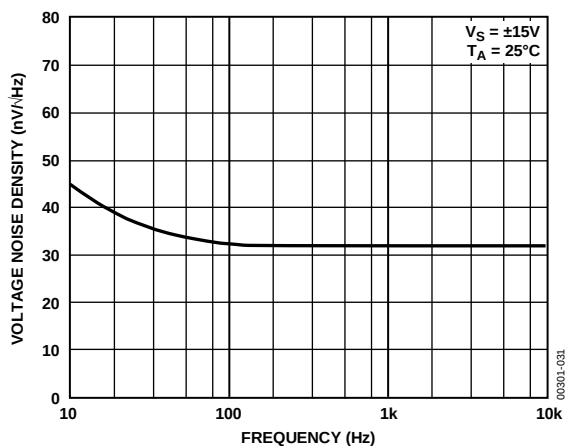


Figure 32. OP482 Voltage Noise Density vs. Frequency

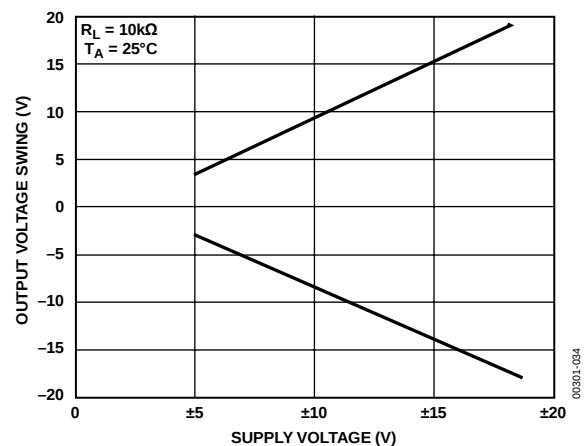


Figure 35. OP482 Output Voltage Swing vs. Supply Voltage

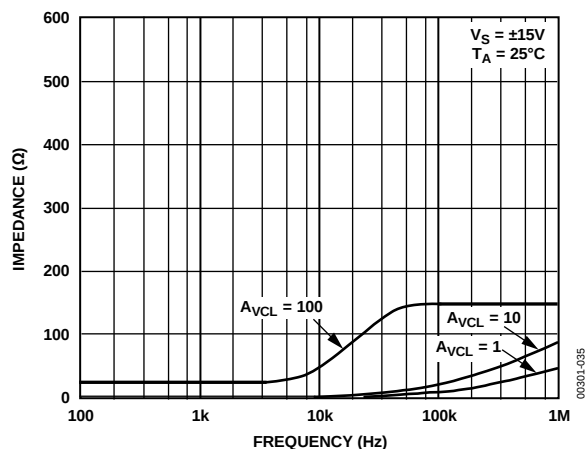


Figure 36. OP482 Closed-Loop Output Impedance vs. Frequency

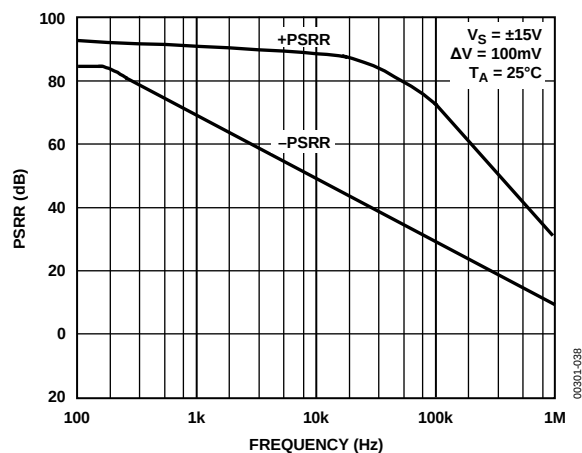


Figure 39. OP482 Power Supply Rejection Ratio (PSRR) vs. Frequency

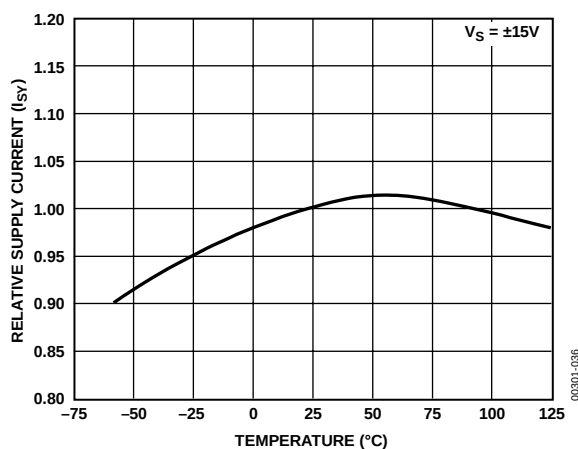


Figure 37. OP482 Relative Supply Current vs. Temperature

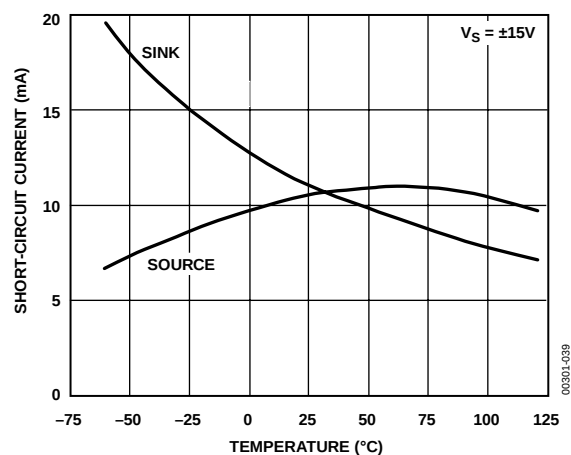


Figure 40. OP482 Short-Circuit Current vs. Temperature

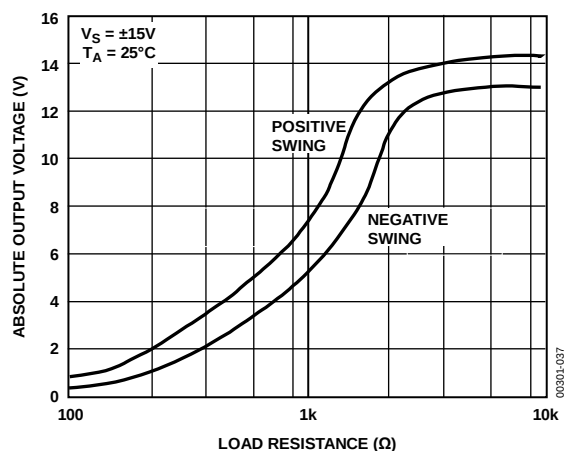


Figure 38. OP482 Maximum Output Voltage vs. Load Resistance

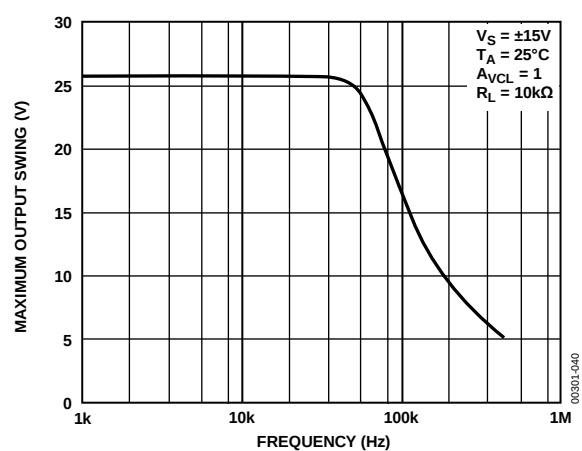


Figure 41. OP482 Maximum Output Swing vs. Frequency

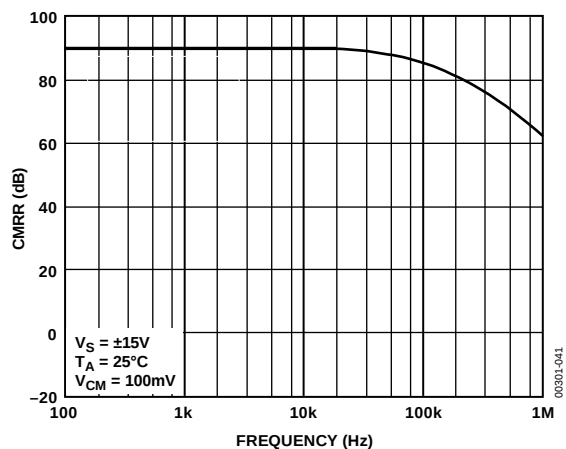
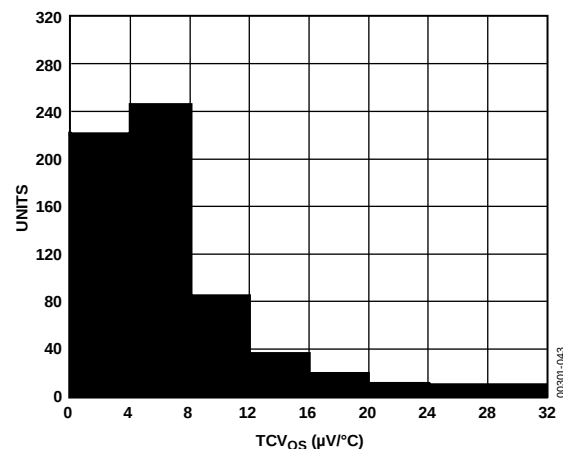
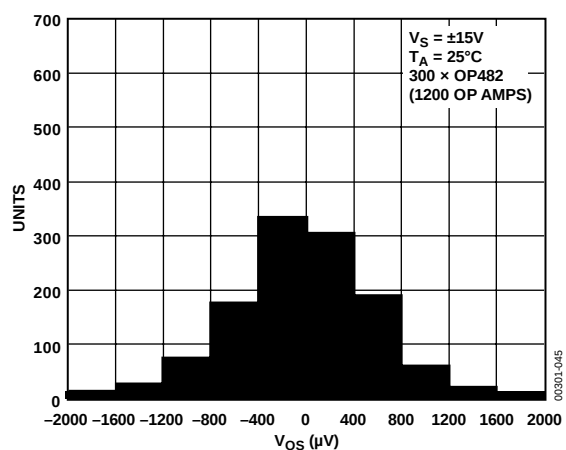


Figure 42. OP482 Common-Mode Rejection Ratio (CMRR) vs. Frequency

Figure 44. OP482 TCV<sub>OS</sub> Distribution, PDIP PackageFigure 43. OP482 V<sub>OS</sub> Distribution, PDIP Package

# APPLICATIONS INFORMATION

The **OP282** and **OP482** are dual and quad JFET op amps that are optimized for high speed at low power. This combination makes these amplifiers excellent choices for battery-powered or low power applications that require above average performance. Applications benefiting from this performance combination include telecommunications, geophysical exploration, portable medical equipment, and navigational instrumentation.

## HIGH-SIDE SIGNAL CONDITIONING

Many applications require the sensing of signals near the positive rail. **OP282** and **OP482** were tested and are guaranteed over a common-mode range ( $-11\text{ V} \leq V_{CM} \leq +15\text{ V}$ ) that includes the positive supply.

One application where such sensing is commonly used is in the sensing of power supply currents. Therefore, the **OP282/OP482** can be used in current sensing applications, such as the partial circuit shown in Figure 45. In this circuit, the voltage drop across a low value resistor, such as the  $0.1\ \Omega$  shown here, is amplified and compared to  $7.5\text{ V}$ . The output can then be used for current limiting.

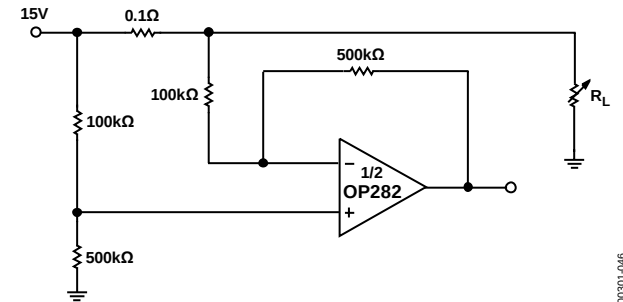


Figure 45. High-Side Signal Conditioning

## PHASE INVERSION

Most JFET input amplifiers invert the phase of the input signal if either input exceeds the input common-mode range. For the **OP282/OP482**, a negative signal in excess of  $11\text{ V}$  causes phase inversion. This is caused by saturation of the input stage, leading to the forward-biasing of a gate-drain diode. Phase reversal in the **OP282/OP482** can be prevented by using Schottky diodes to clamp the input terminals to each other and to the supplies. In the simple buffer circuit shown in Figure 46, D1 protects the op

amp against phase reversal. R1, D2, and D3 limit the input current when the input exceeds the supply rail. The resistor should be selected to limit the amount of input current below the absolute maximum rating.

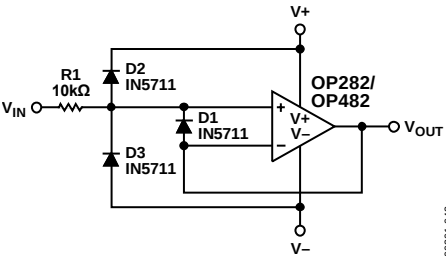


Figure 46. Phase Reversal Solution Circuit

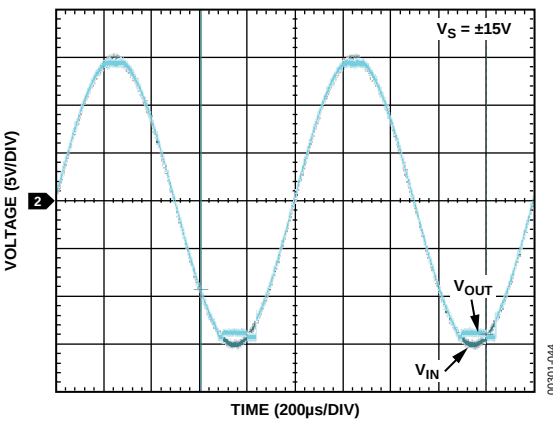


Figure 47. No Phase Reversal

## ACTIVE FILTERS

The wide bandwidth and high slew rates of the **OP282/OP482** make either one an excellent choice for many filter applications.

There are many active filter configurations, but the four most popular configurations are Butterworth, elliptic, Bessel, and Chebyshev. Each type has a response that is optimized for a given characteristic, as shown in Table 4.

Table 4. Active Filter Configurations

| Type              | Selectivity | Overshoot | Phase     | Amplitude (Pass Band) | Amplitude (Stop Band) |
|-------------------|-------------|-----------|-----------|-----------------------|-----------------------|
| Butterworth       | Moderate    | Good      | Nonlinear | Maximum flat          | Equal ripple          |
| Chebyshev         | Good        | Moderate  |           | Equal ripple          |                       |
| Elliptic          | Best        | Poor      |           | Equal ripple          |                       |
| Bessel (Thompson) | Poor        | Best      | Linear    |                       |                       |

## PROGRAMMABLE STATE VARIABLE FILTER

The circuit shown in Figure 48 can be used to accurately program the Q, the cutoff frequency ( $f_c$ ), and the gain of a two-pole state variable filter. OP482 devices have been used in this design because of their high bandwidths, low power, and low noise. This circuit takes only three packages to build because of the quad configuration of the op amps and DACs.

The DACs shown are used in the voltage mode; therefore, many values are dependent on the accuracy of the DAC only and not on the absolute values of the DAC's resistive ladders. This makes this circuit unusually accurate for a programmable filter.

Adjusting DAC 1 changes the signal amplitude across R1; therefore, the DAC attenuation times R1 determines the amount of signal current that charges the integrating capacitor, C1.

This cutoff frequency can now be expressed as

$$f_c = \frac{1}{2\pi R1C1} \left( \frac{D1}{256} \right)$$

where  $D1$  is the digital code for the DAC.

The gain of this circuit is set by adjusting D3. The gain equation is

$$Gain = \frac{R4}{R5} \left( \frac{D3}{256} \right)$$

DAC 2 is used to set the Q of the circuit. Adjusting this DAC controls the amount of feedback from the band-pass node to the input summing node. Note that the digital value of the DAC is in the numerator; therefore, zero code is not a valid operating point.

$$Q = \frac{R2}{R3} \left( \frac{256}{D2} \right)$$

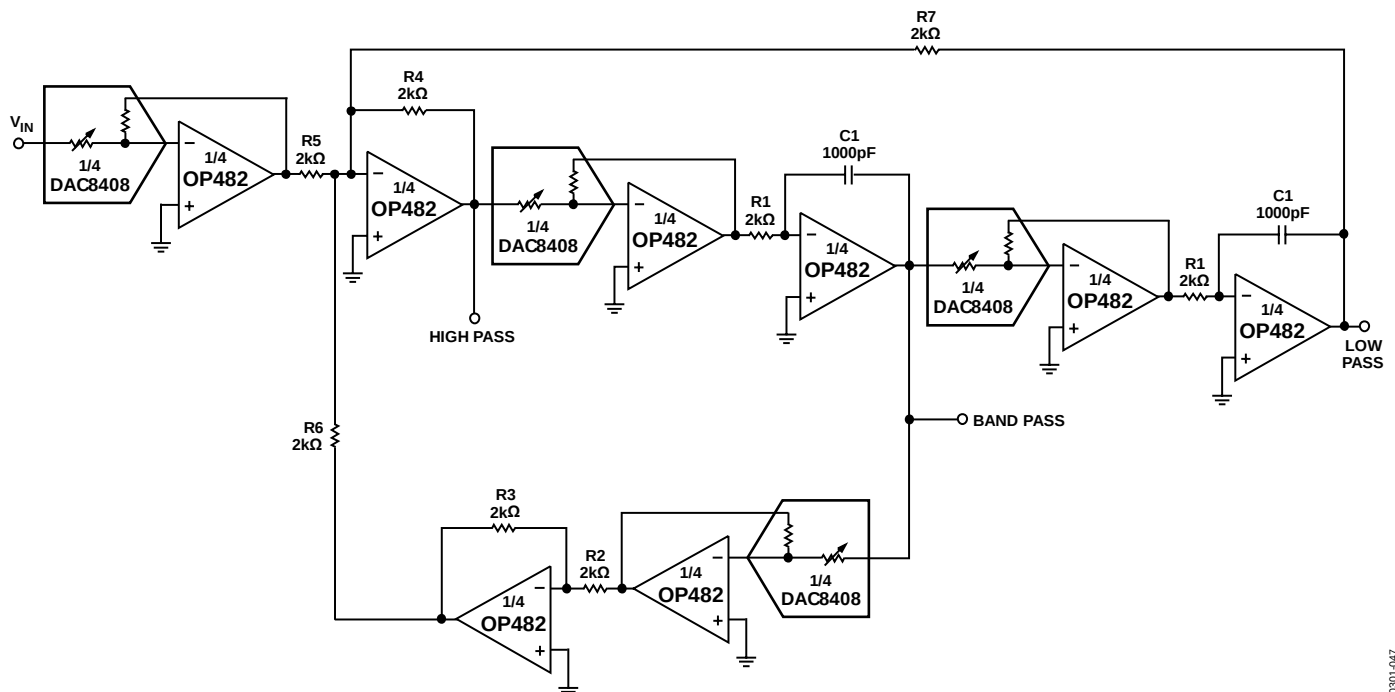


Figure 48. Programmable State Variable Filter

# OUTLINE DIMENSIONS

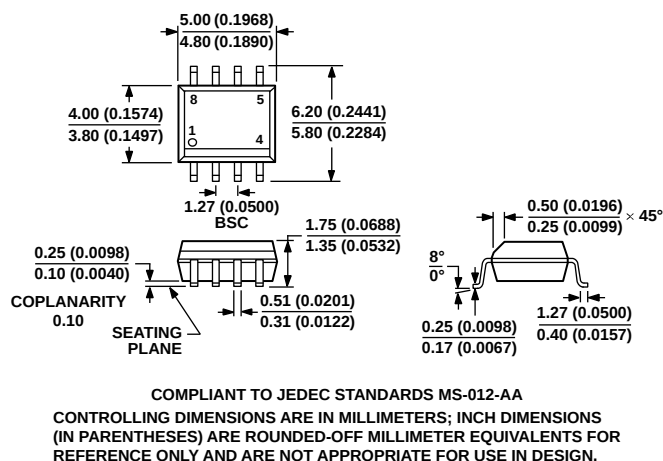
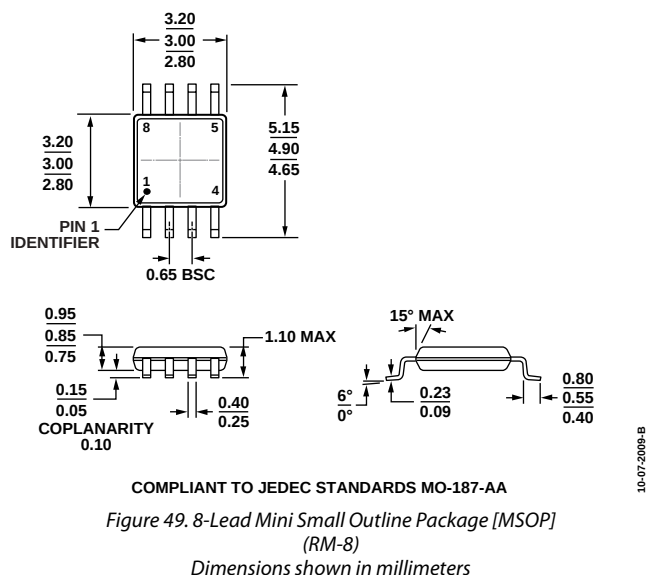




Figure 51. 14-Lead Plastic Dual In-Line Package [PDIP]  
P-Suffix (N-14)



Figure 52. 14-Lead Standard Small Outline Package [SOIC\_N]  
Narrow Body  
S-Suffix (R-14)

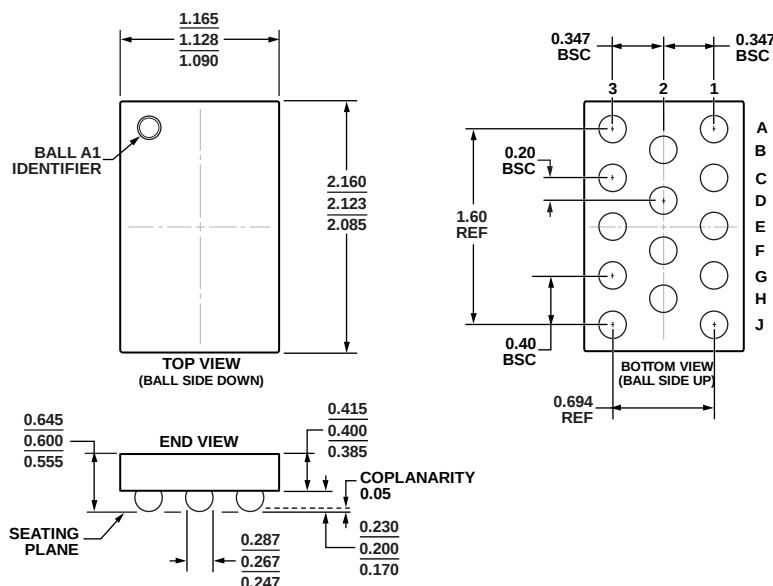


Figure 53. 14-Ball Wafer Level Chip Scale Package [WLCSP]  
CB-14-2  
Controlling dimensions are millimeters

## ORDERING GUIDE

| Model <sup>1</sup> | Temperature Range | Package Description | Package Option  | Branding |
|--------------------|-------------------|---------------------|-----------------|----------|
| OP282ARMZ          | −40°C to +85°C    | 8-Lead MSOP         | RM-8            | A0B      |
| OP282ARMZ-REEL     | −40°C to +85°C    | 8-Lead MSOP         | RM-8            | A0B      |
| OP282GS            | −40°C to +85°C    | 8-Lead SOIC_N       | S-Suffix (R-8)  |          |
| OP282GS-REEL       | −40°C to +85°C    | 8-Lead SOIC_N       | S-Suffix (R-8)  |          |
| OP282GS-REEL7      | −40°C to +85°C    | 8-Lead SOIC_N       | S-Suffix (R-8)  |          |
| OP282GSZ           | −40°C to +85°C    | 8-Lead SOIC_N       | S-Suffix (R-8)  |          |
| OP282GSZ-REEL      | −40°C to +85°C    | 8-Lead SOIC_N       | S-Suffix (R-8)  |          |
| OP282GSZ-REEL7     | −40°C to +85°C    | 8-Lead SOIC_N       | S-Suffix (R-8)  |          |
| OP482ACBZ-RL       | −40°C to +85°C    | 14-Ball WLCSP       | CB-14-2         | A2J      |
| OP482ACBZ-R7       | −40°C to +85°C    | 14-Ball WLCSP       | CB-14-2         | A2J      |
| OP482GPZ           | −40°C to +85°C    | 14-Lead PDIP        | P-Suffix (N-14) |          |
| OP482GS            | −40°C to +85°C    | 14-Lead SOIC_N      | S-Suffix (R-14) |          |
| OP482GS-REEL       | −40°C to +85°C    | 14-Lead SOIC_N      | S-Suffix (R-14) |          |
| OP482GS-REEL7      | −40°C to +85°C    | 14-Lead SOIC_N      | S-Suffix (R-14) |          |
| OP482GSZ           | −40°C to +85°C    | 14-Lead SOIC_N      | S-Suffix (R-14) |          |
| OP482GSZ-REEL      | −40°C to +85°C    | 14-Lead SOIC_N      | S-Suffix (R-14) |          |
| OP482GSZ-REEL7     | −40°C to +85°C    | 14-Lead SOIC_N      | S-Suffix (R-14) |          |

<sup>1</sup> Z = RoHS Compliant Part.