OP-260

DUAL, HIGH-SPEED, CURRENT FEEDBACK, OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

FEATURES

- **Very High Slew Rate** ..... **1000V/μs Typ**
- **–3dB Bandwidth (A_V=+1)** ..... **90MHz Typ**
- **Bandwidth Independent of Gain**
- **Unity-Gain Stable**
- **Low Supply Current** ..... **4.5mA per amp Typ**
- **Available in Die Form**

ORDERING INFORMATION †

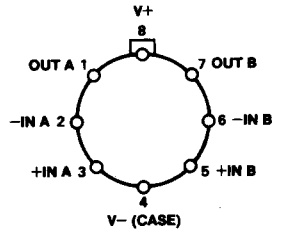
T_A = +25°C V_{OS} MAX (mV)	PACKAGE CERDIP 8-PIN	TO-99	PLASTIC	LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
3.5	OP260AZ*	OP260AJ*	–	OP260ARC/883	MIL
3.5	OP260EZ	OP260EJ	–	–	XIND
5.0	OP260FZ	OP260FJ	–	–	XIND
7.0	–	–	OP260GP	–	XIND
7.0	–	–	OP260GS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

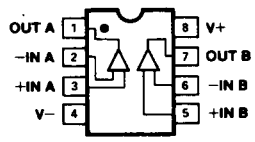
† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages. For ordering information, see PMI's Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

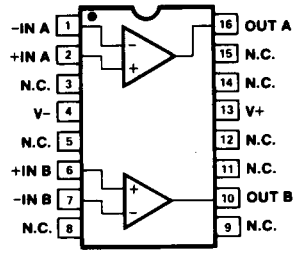
PIN CONNECTIONS



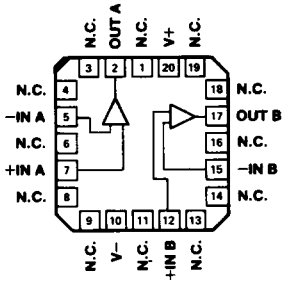
TO-99
(J-Suffix)



EPOXY MINI-DIP
(P-Suffix)
CERDIP
(Z-Suffix)



16-PIN SOL
(S-Suffix)



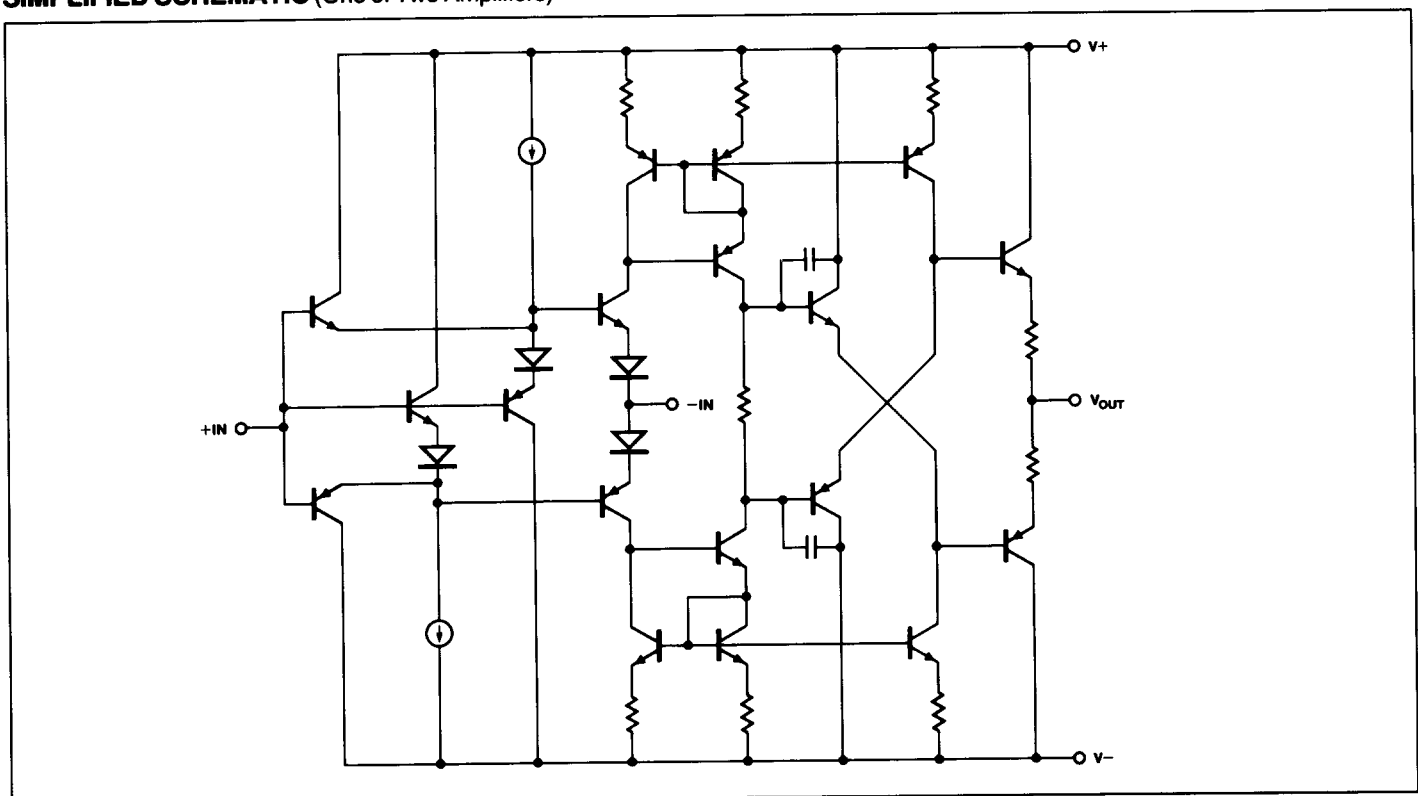
20-CONTACT
HERMETIC LCC
(RC-Suffix)

GENERAL DESCRIPTION

The dual OP-260 represents a new concept in monolithic operational amplifiers. Built on PMI's high-speed bipolar process, the OP-260

continued

SIMPLIFIED SCHEMATIC (One of Two Amplifiers)



GENERAL DESCRIPTION *Continued*

employs current feedback to provide consistently wideband operation regardless of gain. The OP-260's –3dB bandwidth of 90MHz at A_V=+1 combines with a slew rate of 1000V/µs for extremely high-speed operation. For its high-speed bandwidth, the OP-260 requires only 4.5mA of supply current per amplifier, a considerable power savings over other high-speed operational amplifiers.

The OP-260 is easy to design with, since most of the circuit assumptions for voltage feedback amplifiers can also be used for current feedback amplifiers. The two independent amplifiers of the OP-260 allow two channel amplification with matched AC performance. It is also ideal for high-speed instrumentation amplifiers. Other applications for the OP-260 include ultrasound and sonar systems, video amplifiers and high-speed data acquisition systems.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Input Voltage ..... Supply Voltage
Differential Input Voltage ..... ±1V
Inverting Input Current ..... ±7mA Continuous
..... ±20mA Peak
Output Short-Circuit Duration ..... 10 sec
Operating Temperature Range
OP-260A, (J, RC, Z) ..... –55°C to +125°C
OP-260E/F (J, Z) ..... –40°C to +85°C
OP-260G (P, S) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +175°C
Junction Temperature Range (J, RC) ..... –65°C to +175°C
Junction Temperature Range (P, S) ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
TO-99 (J)	145	16	°C/W
8-Pin Hermetic DIP (Z)	134	12	°C/W
8-Pin Plastic DIP (P)	96	37	°C/W
20-Contact LCC (RC)	88	33	°C/W
16-Pin SOL (S)	92	27	°C/W

NOTES:

1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, V_{CM} = 0V, R_F = 2.5kΩ, T_A = +25°C, unless otherwise noted.

			OP-260A/E			OP-260F			OP-260G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{IOS}		–	1	3.5	–	2	5	–	3	7	mV
Input Bias Current	I_{B+} I_{B-}	Noninverting Input Inverting Input	– –	0.2 3	1 8	– –	0.3 4	2 10	– –	0.5 5	3 15	µA
Input Bias Current Common-Mode Rejection Ratio	$CMRRI_{B-}$	Inverting Input V_{CM} = ±11V	–	0.04	0.1	–	0.06	0.2	–	0.1	0.5	µA/V
Input Bias Current Power Supply Rejection Ratio	$PSRRI_{B-}$ $PSRRI_{B+}$	Inverting Input Noninverting Input V_S = ±9V to ±18V	– –	0.02 0.002	0.1 0.02	– –	0.04 0.004	0.2 0.04	– –	0.05 0.01	0.5 0.1	µA/V
Common-Mode Rejection	CMR	V_{CM} = ±11V	56	62	–	50	60	–	50	60	–	dB
Power Supply Rejection	PSR	V_S = ±9V to ±18V	66	72	–	60	66	–	60	66	–	dB
Open-Loop Transimpedance	R_T	R_L = 1kΩ V_O = ±10V	5	7	–	4	5	–	4	5	–	MΩ
Input Voltage Range	IVR		±11	–	–	±11	–	–	±11	–	–	V
Output Voltage Swing	V_O	R_L = 1kΩ I_{OUT} = ±20mA	±12 ±11	±12.6 ±11.5	–	±12 ±11	±12.6 ±11.5	–	±12 ±11	±12.6 ±11.5	–	V
Supply Current	I_{SY}	No Load, Both Amplifiers	–	9	10.5	–	9	10.5	–	9	10.5	mA
Slew Rate	SR	A_V = +1, V_O = ±10V, R_L = 1kΩ, Test at V_O = ±5V	–	1000	–	–	1000	–	–	1000	–	V/µs
		A_V = +10, V_O = ±10V, R_L = 1kΩ, Test at V_O = ±5V	375	550	–	300	550	–	300	550	–	
		A_V = +10, V_O = ±10V, R_L = 1kΩ, Test at V_O = ±5V 8-pin Hermetic DIP (Z) Package	300	–	–	300	–	–	–	–	–	

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $V_{CM} = 0V$, $R_F = 2.5k\Omega$, $T_A = 25°C$, unless otherwise noted. *Continued*

			OP-260A/E			OP-260F			OP-260G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
–3dB Bandwidth	BW	–3dB point, $A_V = -1$	–	55	–	–	55	–	–	55	–	MHz
		$R_L = 500\Omega$, $A_V = +1$	–	90	–	–	90	–	–	90	–	
		$A_V = +10$	–	40	–	–	40	–	–	40	–	
Settling Time	t_S	$A_V = -1$, 10V step, 0.1%	–	250	–	–	250	–	–	250	–	ns
Input Capacitance	C_{IN}	Noninverting and Inverting Inputs	–	4.5	–	–	4.5	–	–	4.5	–	pF
Channel Separation	CS	$f_O = 100kHz$, $V_O = 10Vp\text{-}p$, $R_L = 100\Omega$	–	100	–	–	100	–	–	100	–	dB

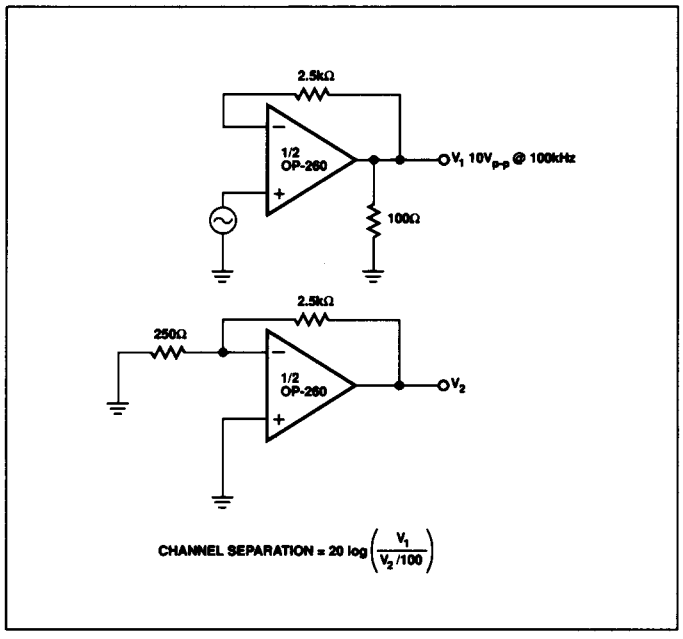
ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $V_{CM} = 0V$, $R_F = 2.5k\Omega$, $-55°C \le T_A \le +125°C$, for the OP-260A, unless otherwise noted.

			OP-260A			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{IOS}		–	1.8	6	mV
Average Input Offset Voltage Drift	TCV_{IOS}		–	8	–	µV/°C
Input Bias Current	I_{B+}	Noninverting Input	–	0.3	2	µA
	I_{B-}	Inverting Input	–	4	12	
Input Bias Current Common Mode Rejection Ratio	$CMRRI_{B-}$	Inverting Input, $V_{CM} = \pm11V$	–	0.05	0.2	µA/V
Input Bias Current Power Supply Rejection Ratio	$PSRRI_{B-}$	Inverting Input, $V_S = \pm9V$ to $\pm18V$	–	0.03	0.2	µA/V
	$PSRRI_{B+}$	Noninverting Input, $V_S = \pm9V$ to $\pm18V$	–	0.003	0.05	
Common Mode Rejection	CMR	$V_{CM} = \pm11V$	52	58	–	dB
Power Supply Rejection	PSR	$V_S = \pm9V$ to $\pm18V$	62	70	–	dB
Open-Loop Transimpedance	R_T	$R_L = 1k\Omega$, $V_O = \pm10V$	3	4.8	–	MΩ
Input Voltage Range	IVR		±11	–	–	V
Output Voltage Swing	V_O	$R_L = 1k\Omega$	±11.5	±12.4	–	V
		$I_{OUT} = \pm20mA$	±10.5	±11.1	–	
Supply Current	I_{SY}	No load, Both Amplifiers	–	9	11.5	mA

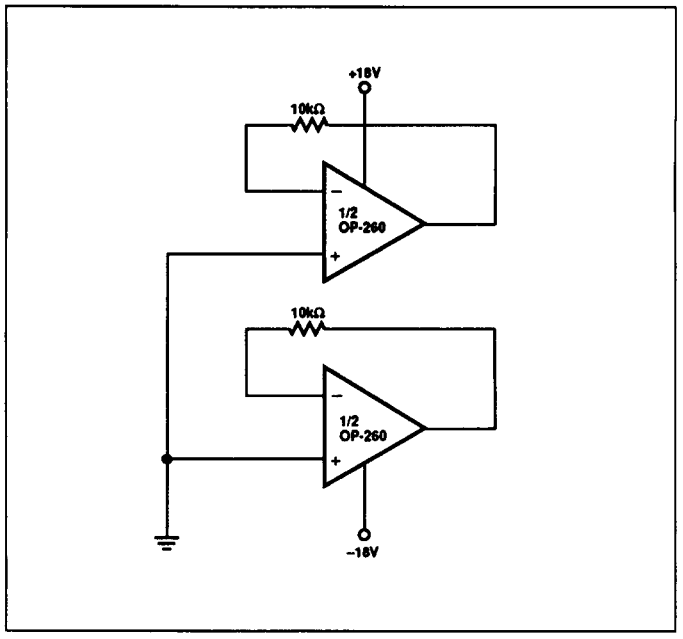
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $V_{CM} = 0V$, $R_F = 2.5k\Omega$, $-40°C \leq T_A \leq +85°C$ for the OP-260E/F/G, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-260E MIN	OP-260E TYP	OP-260E MAX	OP-260F MIN	OP-260F TYP	OP-260F MAX	OP-260G MIN	OP-260G TYP	OP-260G MAX	UNITS
Input Offset Voltage	V_{IOS}		–	1.4	6	–	2.5	8	–	3.7	10	mV
Average Input Offset Voltage Drift	TCV_{IOS}		–	6	–	–	8	–	–	10	–	µV/°C
Input Bias Current	I_{B+} I_{B-}	Noninverting Input Inverting Input	– –	0.3 4	2 12	– –	0.4 5	3 15	– –	0.6 7	5 20	µA
Input Bias Current Common Mode Rejection Ratio	$CMRRI_{B-}$	Inverting Input $V_{CM} = \pm 11V$	–	0.05	0.2	–	0.7	0.4	–	0.15	1.0	µA/V
Input Bias Current Power Supply Rejection Ratio	$PSRRI_{B-}$ $PSRRI_{B+}$	Inverting Input Noninverting Input	– –	0.03 0.003	0.2 0.05	– –	0.05 0.005	0.4 0.1	– –	0.1 0.01	1.0 0.2	µA/V
Common Mode Rejection	CMR	$V_{CM} = \pm 11V$	52	60	–	50	58	–	50	58	–	dB
Power Supply Rejection	PSR	$V_S = \pm 9V$ to $\pm 15V$	62	70	–	60	64	–	60	64	–	dB
Open-Loop Transimpedance	R_T	$R_L = 1k\Omega$, $V_O = \pm 10V$	3	5	–	2	4	–	2	4	–	MΩ
Input Voltage Range	IVR		±11	–	–	±11	–	–	±11	–	–	V
Output Voltage Swing	V_O	$R_L = 1k\Omega$ $I_{OUT} = \pm 20mA$	±11.5 ±10.5	±12.5 ±11.1	–	±11.5 ±10.5	±12.5 ±11.1	–	±11.5 ±10.5	±12.5 ±11.1	–	V
Supply Current	I_{SY}	No Load, Both Amplifiers	–	9	11.5	–	9	11.5	–	9	11.5	mA

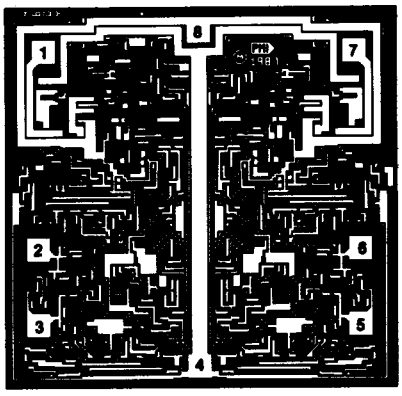
CHANNEL SEPARATION TEST CIRCUIT



BURN-IN CIRCUIT



DICE CHARACTERISTICS



DIE SIZE 0.089 x 0.086 inch, 7,654 sq. mils
(2.26 x 2.18 mm, 4.93 sq. mm)

1. OUT A
2. - IN A
3. + IN A
4. V-
5. + IN B
6. - IN B
7. OUT B
8. V +

For additional DICE ordering information, refer to PMI's Data Book, Section 2.

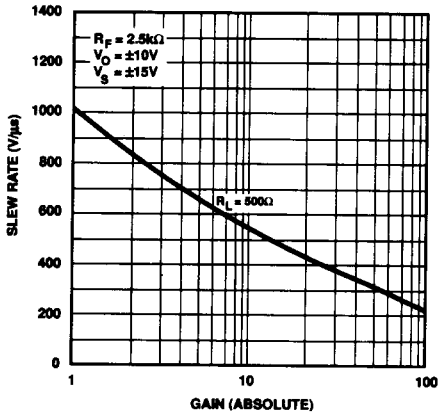
WAFER TEST LIMITS at V_S = ±15V, V_{CM} = 0V, R_F = 2.5kΩ, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-260GBC LIMITS	UNITS
Input Offset Voltage	V_{IOS}		5	mV MAX
Input Bias Current	I_{B+} I_{B-}	Noninverting Input Inverting Input	2 10	µA MAX
Input Bias Current Common Mode Rejection Ratio	$CMRRI_B$	Inverting Input V_{CM} = +11V	0.2	µA/V MAX
Input Bias Current Power Supply Rejection Ratio	$PSRRI_{B-}$ $PSRRI_{B+}$	Inverting Input Noninverting Input V_S = ±9V to ±18V	0.2 0.04	µA/V MAX
Common Mode Rejection	CMR	V_{CM} = ±11V	50	dB MIN
Power Supply Rejection	PSR	V_S = ±9V to ±18V	60	dB MIN
Open-Loop Transimpedance	R_T	R_L = 1kΩ, V_O = ±10V	4	MΩ MIN
Input Voltage Range	IVR		±11	V MIN
Output Voltage Swing	V_O	R_L = 1kΩ I_{OUT} = ±20mA	±12 ±11	V MIN
Supply Current	I_{SY}	No Load, Both Amplifiers	10.5	mA MAX

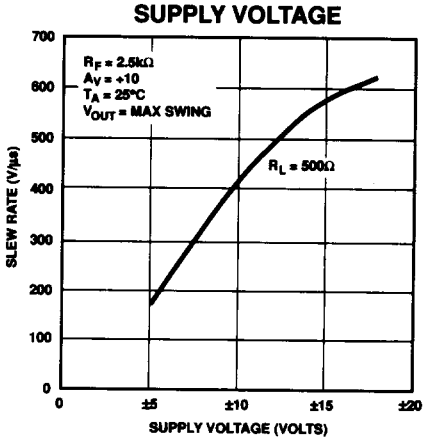
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS

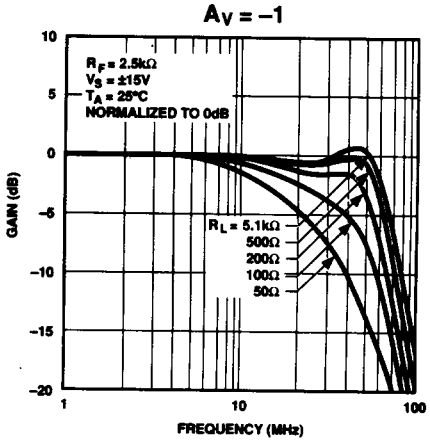
SLEW RATE vs GAIN



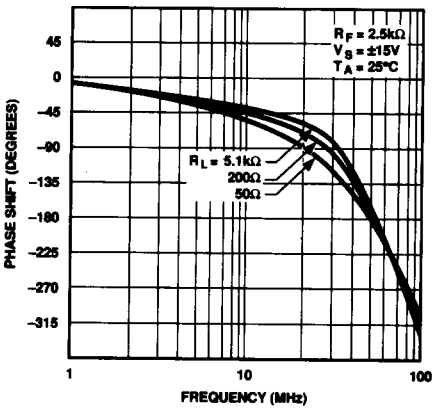
SLEW RATE vs SUPPLY VOLTAGE



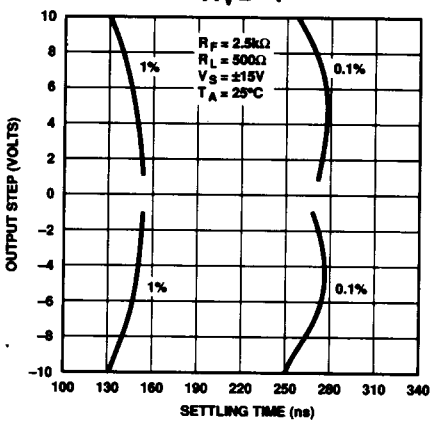
GAIN vs FREQUENCY A_V = –1



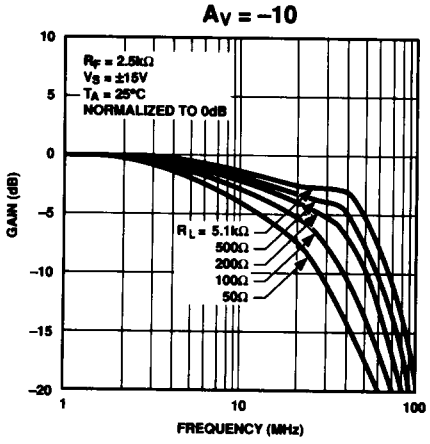
PHASE SHIFT vs FREQUENCY A_V = –1



SETTLING TIME vs OUTPUT STEP A_V = –1



GAIN vs FREQUENCY A_V = –10



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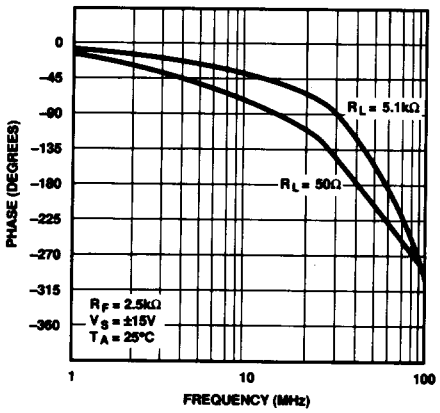

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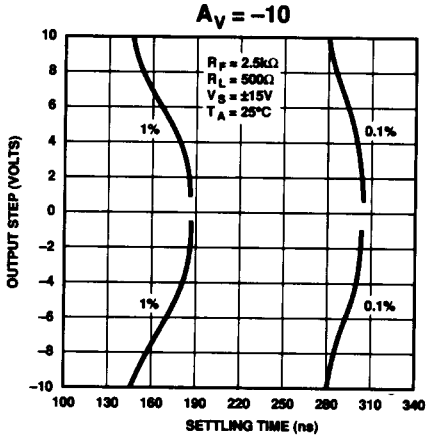
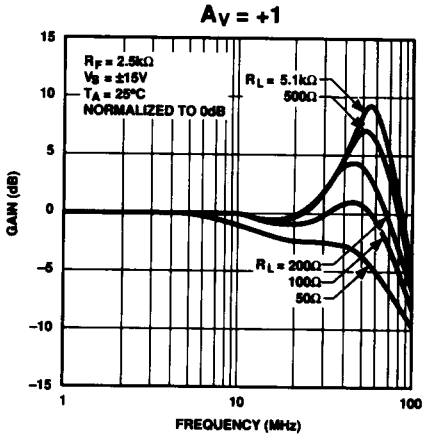
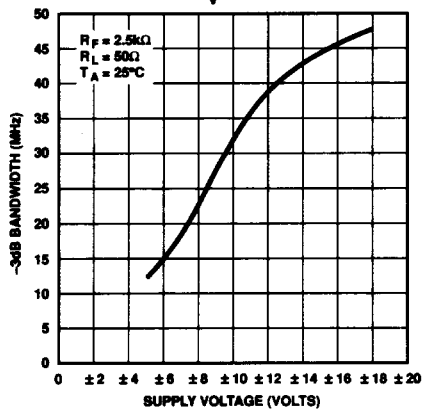


GAIN vs FREQUENCY A_V = +1

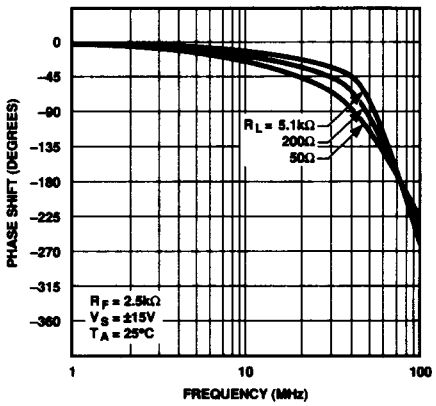


TYPICAL ELECTRICAL CHARACTERISTICS *Continued*

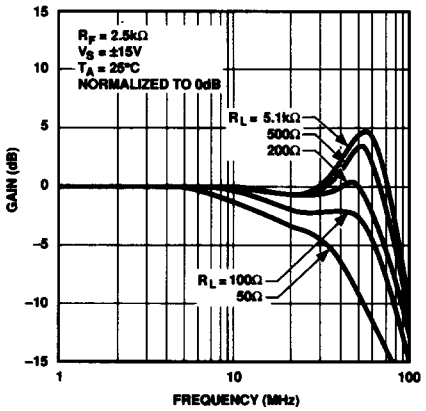
SMALL-SIGNAL –3dB BANDWIDTH vs SUPPLY VOLTAGE A_V = +1



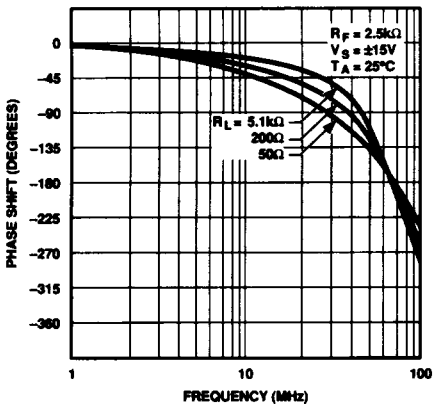
PHASE SHIFT vs FREQUENCY A_V = +1



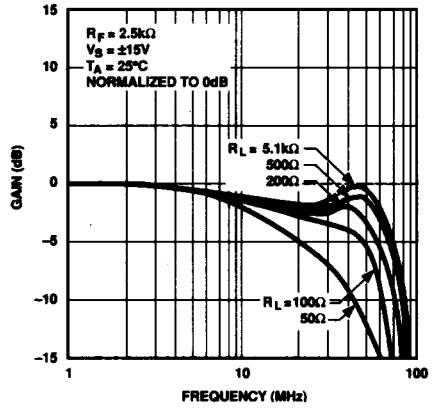
GAIN vs FREQUENCY A_V = +2



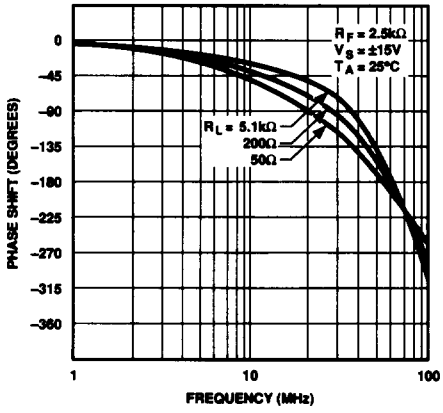
PHASE SHIFT vs FREQUENCY A_V = +2



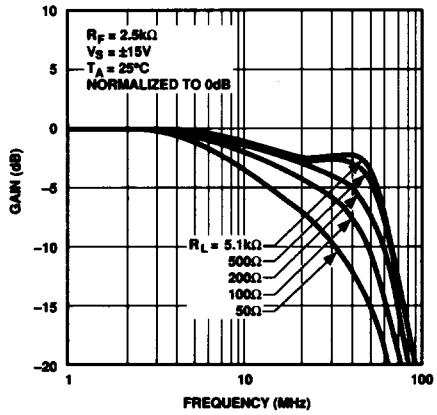
GAIN vs FREQUENCY A_V = +5



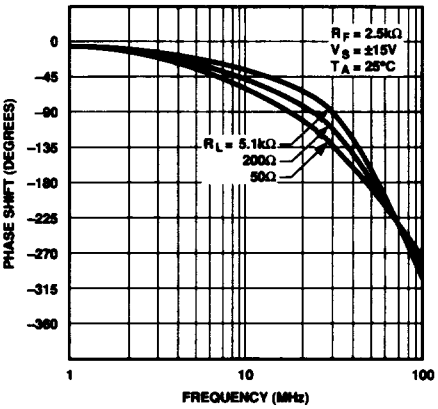
PHASE SHIFT vs FREQUENCY A_V = +5



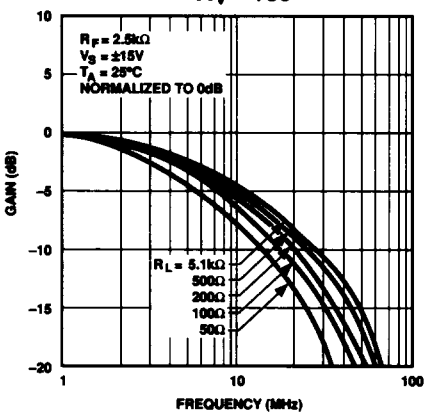
GAIN vs FREQUENCY A_V = +10



PHASE SHIFT vs FREQUENCY A_V = +10

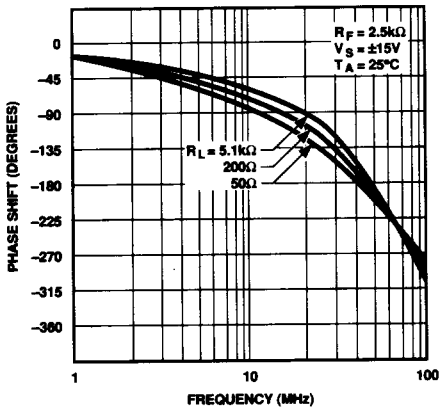


GAIN vs FREQUENCY A_V = +50

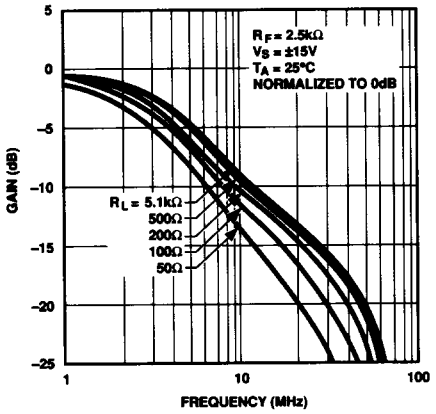


TYPICAL ELECTRICAL CHARACTERISTICS *Continued*

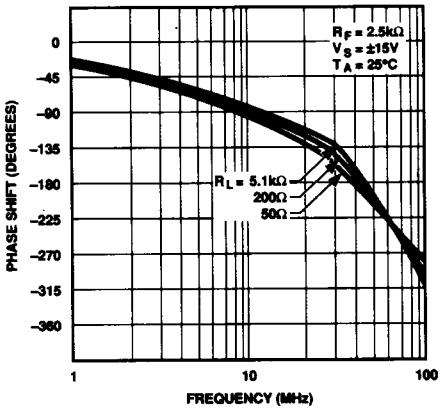
PHASE SHIFT vs FREQUENCY
A_V = +50



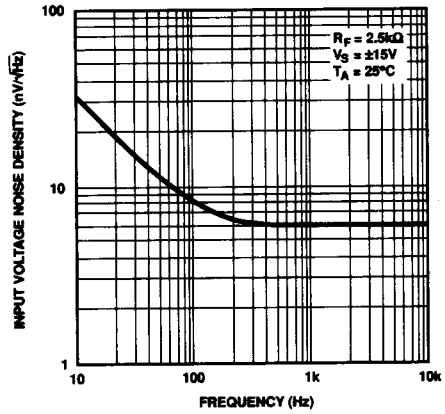
GAIN vs FREQUENCY
A_V = +100



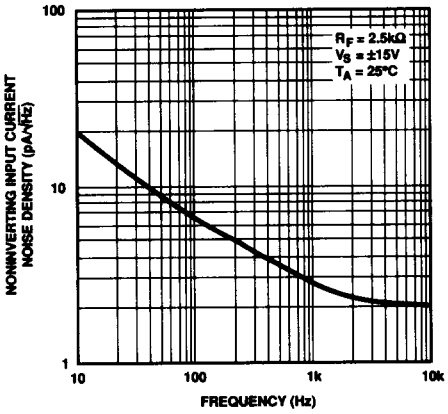
PHASE SHIFT vs FREQUENCY
A_V = +100



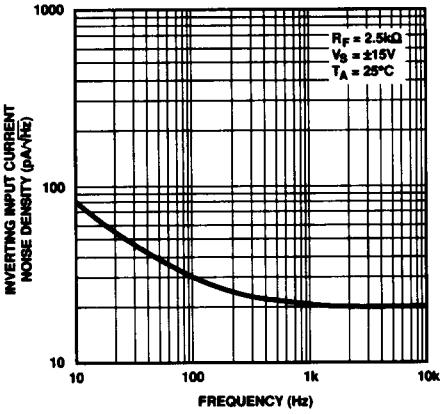
INPUT VOLTAGE NOISE DENSITY vs FREQUENCY



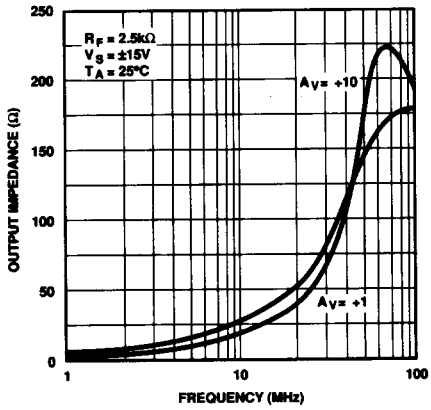
NONINVERTING INPUT CURRENT NOISE DENSITY vs FREQUENCY



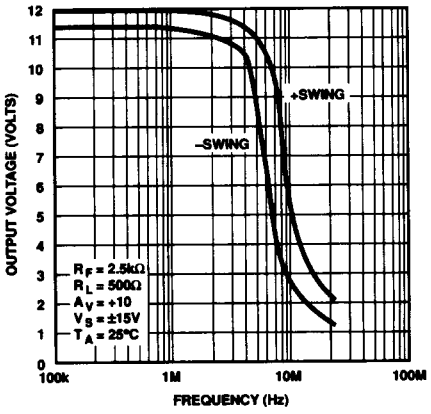
INVERTING INPUT CURRENT NOISE DENSITY vs FREQUENCY



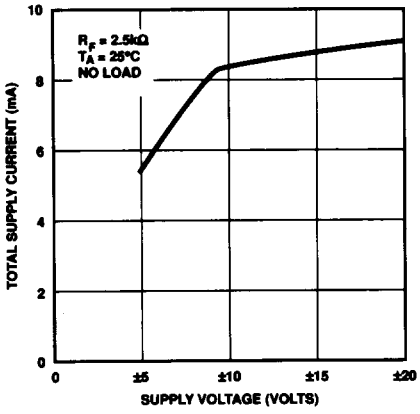
OUTPUT IMPEDANCE vs FREQUENCY



MAXIMUM OUTPUT SWING vs FREQUENCY

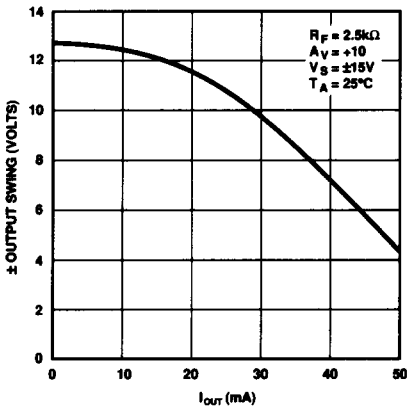


TOTAL SUPPLY CURRENT vs SUPPLY VOLTAGE

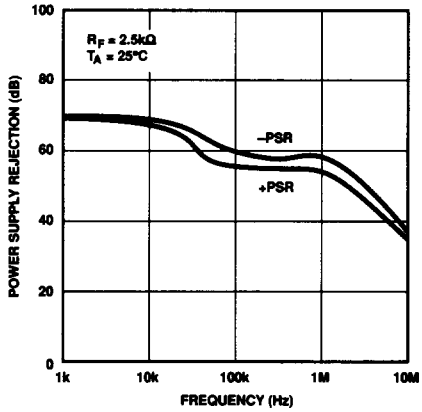


TYPICAL ELECTRICAL CHARACTERISTICS *Continued*

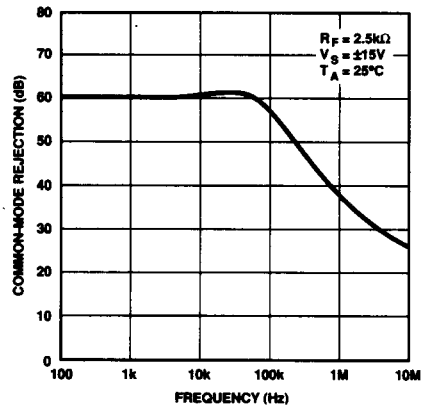
OUTPUT SWING vs OUTPUT CURRENT @ 1kHz



POWER SUPPLY REJECTION vs FREQUENCY



COMMON-MODE REJECTION vs FREQUENCY



APPLICATIONS INFORMATION

CURRENT VERSUS VOLTAGE FEEDBACK AMPLIFIERS

The dual OP-260 employs a unique circuit topology that sets it apart from conventional op amps. By using a transimpedance amplifier configuration, the OP-260 provides substantial improvements in bandwidth and slew rate over voltage feedback op amps. Figure 1 compares models of these two different amplifier configurations.

A voltage feedback op amp multiplies the differential voltage at its inputs by its open-loop gain. The feedback loop forces the output to a voltage that, when divided by R_1 and R_2, equalizes the input voltages. Unlike a voltage feedback op amp, which has high impedance inputs, the current feedback amplifier has a high and a low impedance input. The current feedback amplifier's input stage consists of a unity-gain voltage buffer between the noninverting and inverting inputs. The inverting "input" is in reality a low impedance output. Current can flow into or out of the inverting input. A transimpedance stage follows the input buffer that converts the buffer output current into a linearly proportional amplifier output voltage.

The current feedback amplifier loop works in the following fashion (Figure 1b). As the noninverting input voltage rises, the inverting input follows and the buffer sources current through R_1. This current, multiplied by the transimpedance stage, causes the amplifier's output voltage to rise until the current flowing into R_2 from the amplifier's output equalizes the current through R_1, replacing the buffer's output current. At steady state, only a very small buffer output current must flow to sustain the proper output voltage. The ratio $(1 + R_2/R_1)$ determines the

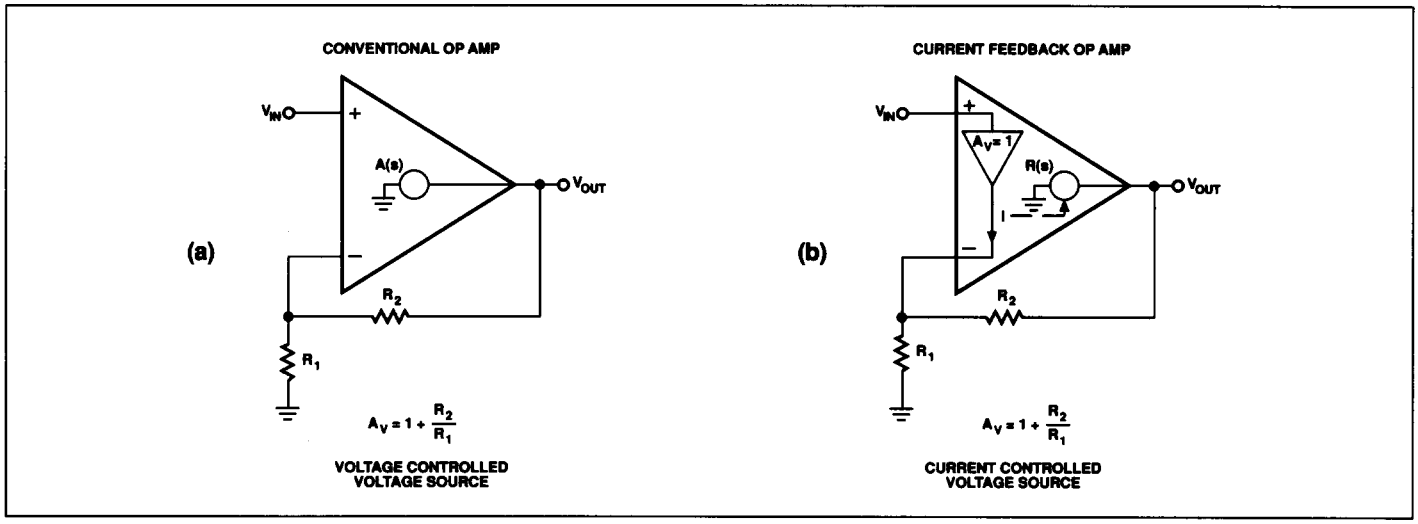


FIGURE 1: *The conventional op amp (a) can be modelled as a voltage-controlled voltage source. In contrast, the current feedback op amp (b), resembles a current-controlled voltage source.*

closed-loop gain of the circuit. The result is that when designing with current feedback amplifiers the familiar op amp assumptions can still be used for circuit analysis:

1. The voltage across the inputs equals zero.
2. The current into the inputs equals zero.

BANDWIDTH VERSUS GAIN

A unique feature of the current feedback amplifier design is that the closed-loop bandwidth remains relatively constant as a function of closed-loop gain. Voltage feedback op amps suffer from a bandwidth reduction as closed-loop gain increases, as quantified by the gain-bandwidth product (GBWP). This is illustrated in Figure 2 which shows the frequency response of the OP-260 for various closed-loop gains and the frequency response of a voltage feedback op amp with a gain-bandwidth product of 30MHz. The bandwidth of the OP-260 is much less dependent upon closed-loop gain than the voltage feedback op amp.

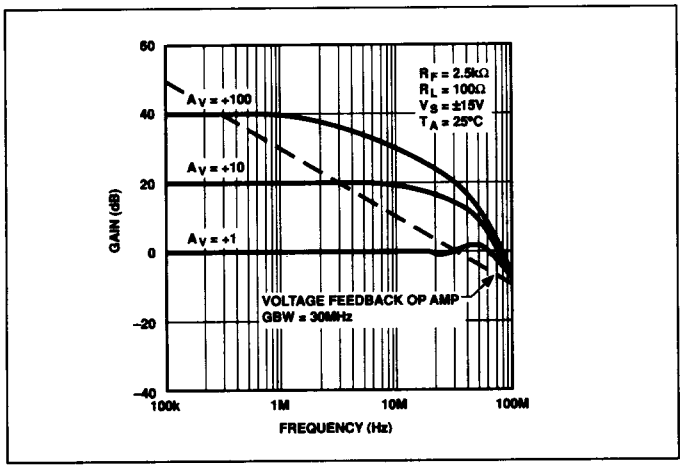


FIGURE 2: *Frequency response of the OP-260 when connected in various closed-loop gains with R_F = 2.5kΩ and R_L = 100Ω. Note that the frequency response of the OP-260 does not follow the asymptotic roll-off characteristic of a voltage feedback op-amp.*

FEEDBACK RESISTANCE AND BANDWIDTH

The closed-loop frequency response of the OP-260 shown in Figure 2 applies for a fixed feedback resistor of 2.5kΩ. The frequency response of a current feedback amplifier is primarily dependent on the value of the feedback resistor. The design of the OP-260 has been optimized for a feedback resistance of 2.5kΩ. By holding the feedback resistor value constant, the –3dB frequency point will also remain constant within a moderate range of closed-loop gain.

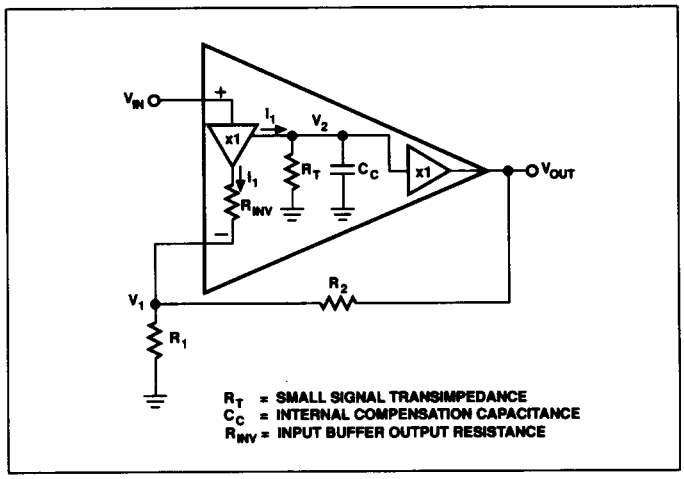


FIGURE 3: *Simple frequency response model of the current feedback amplifier.*

The model shown in Figure 3 can be used to determine the frequency response of a current feedback amplifier. With this model, the frequency response dependency on the value of the feedback resistance is easily seen.

From the model of Figure 3, nodal equations may be written for V_1 and V_2.

$$V_1 = \frac{V_{IN}\left(\frac{R_2}{R_{INV}}\right) + V_{OUT}}{1 + \frac{R_2}{R_1} + \frac{R_2}{R_{INV}}}$$

$$V_2 = \frac{R_T}{1 + sR_TC_C} I_1$$

where $I_1 = \frac{V_{IN} - V_1}{R_{INV}} = V_1\left(\frac{1}{R_1} + \frac{1}{R_2}\right) - \frac{V_{OUT}}{R_2}$, and $V_{OUT} = V_2$.

Combining these equations yields:

$$V_{OUT} = \left[\left(\frac{V_{IN}\left(\frac{R_2}{R_{INV}}\right) + V_{OUT}}{1 + \frac{R_2}{R_1} + \frac{R_2}{R_{INV}}}\right)\left(\frac{1}{R_1} + \frac{1}{R_2}\right) - \frac{V_{OUT}}{R_2}\right] \frac{R_T}{1 + sR_TC_C}$$

If the transimpedance of the amplifier, R_T, is » R_2 and R_{INV}, then the transfer function may be simplified to:

$$\frac{V_{OUT}}{V_{IN}} \approx \frac{1 + \frac{R_2}{R_1}}{1 + s\left[R_2 + \left(1 + \frac{R_2}{R_1}\right)R_{INV}\right]C_C}$$

The transfer function shows that the dominant closed-loop pole is mainly dependent on the value of the feedback resistance, R_2, and the internal compensation capacitor, C_C. For example, at unity gain, where R_1 is infinite, R_2 determines the –3dB frequency.

$$\frac{V_{OUT}}{V_{IN}} \approx \frac{1}{1 + sR_2C_C}$$

$$f_{-3dB} = \frac{1}{2\pi R_2 C_C}$$

where $R_2 \gg R_{INV}$.

For higher gains, the –3dB frequency is determined by R_2 plus the output resistance of the buffer, R_{INV} (typically 100Ω), which is multiplied by the closed-loop gain. As the closed-loop gain increases, the multiplying effect on R_{INV} becomes dominant, causing the bandwidth to decrease. However, the closed-loop bandwidth of a current feedback amplifier still far exceeds that of a voltage feedback op amp for moderate values of gain.

Figure 4 shows the effect of the feedback resistance on the bandwidth of the OP-260 for various closed-loop gains.

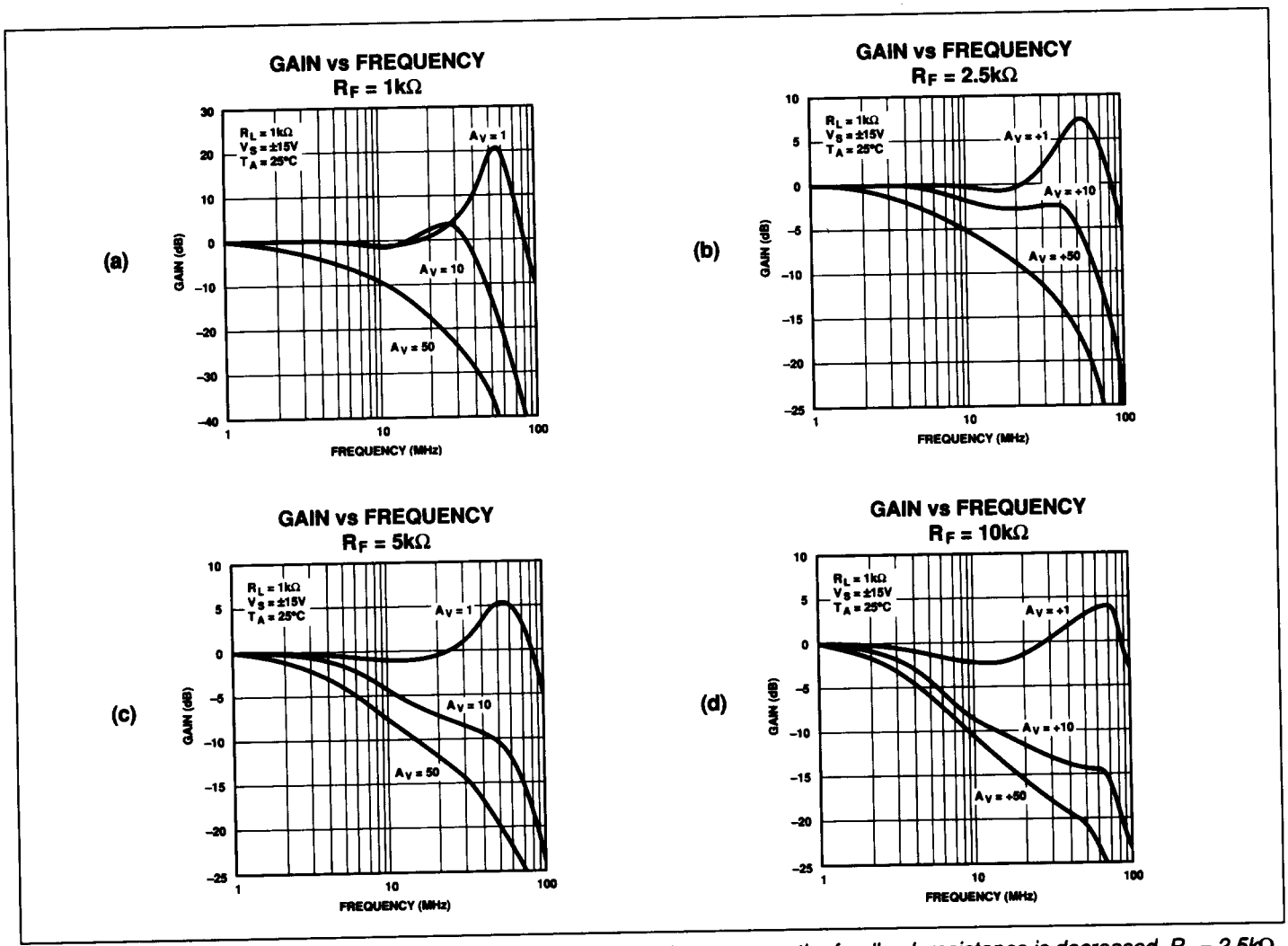


FIGURE 4: *Bandwidth will vary with feedback resistance. Peaking increases as the feedback resistance is decreased. R_F = 2.5kΩ is the recommended value. All graphs are normalized to 0dB.*

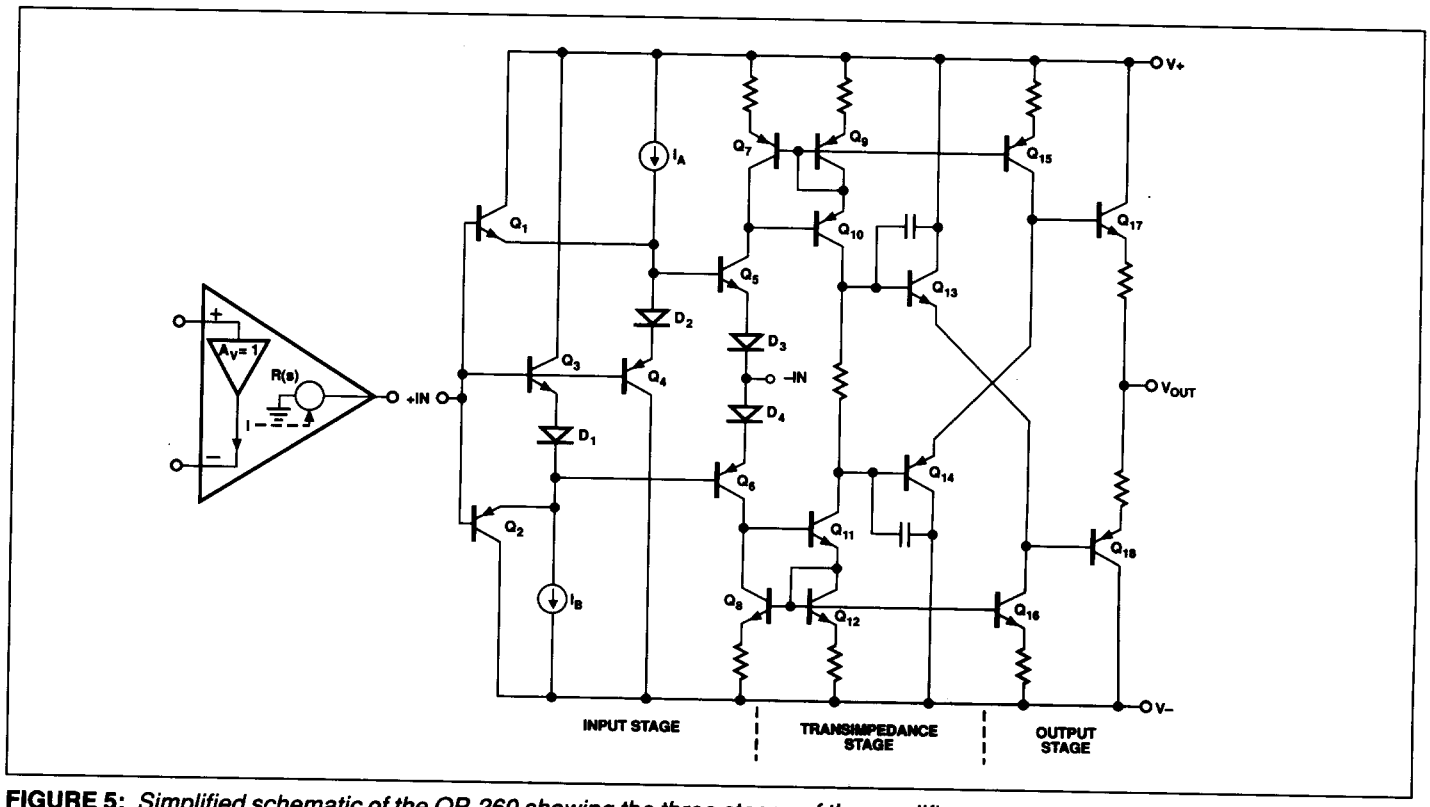


FIGURE 5: *Simplified schematic of the OP-260 showing the three stages of the amplifier.*

SLEW RATE AND GAIN

The simplified schematic in Figure 5 shows the three stages of the OP-260. The input stage consists of a unity-gain emitter-follower amplifier. Q_5 and Q_6 form a class AB output stage at the inverting input which can source or sink current. The current flowing through the inverting input is sensed by the top current mirror, formed by Q_7, Q_9, and Q_{10}, or the bottom current mirror, formed by Q_8, Q_{11}, and Q_{12}. When the buffer sources current to a load, current flows out of the inverting input, increasing Q_5's collector current and causing more current to flow through Q_9 and Q_{15}. This increases the base drive to the output transistor Q_{17}. Simultaneously, the increased current in Q_9 drives Q_{13} which reduces base drive to the complementary output transistor Q_{18}. This push-pull action produces a very fast output slew rate. For a small voltage step, the OP-260's slew rate is dependent on the available current from the two current sources (I_A and I_B) that drive Q_5 and Q_6.

To increase the slew rate, transistors Q_1 and Q_2 have been added to boost the base drive to Q_5 and Q_6. In closed-loop gains below 10, a large input step will turn on Q_1 or Q_2 increasing the slew rate dramatically as illustrated in Figure 6.

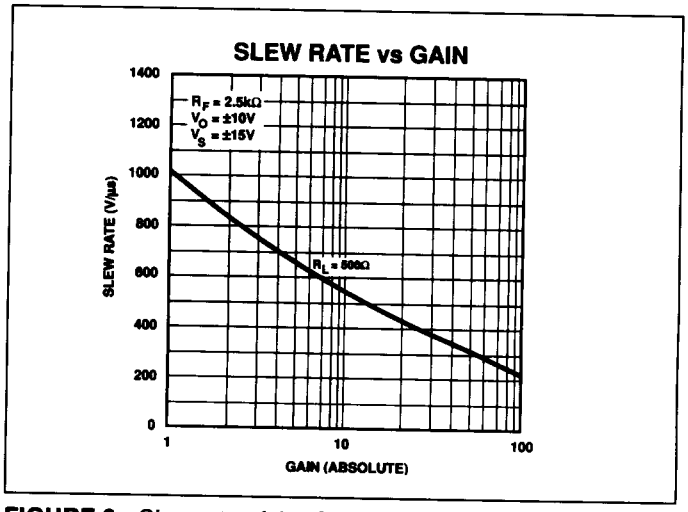


FIGURE 6: *Slew rate of the OP-260 is highest in gains below ±10.*

AMPLIFIER NOISE PERFORMANCE

Simplified noise models of the OP-260 in the noninverting and inverting amplifier configurations are shown in Figure 7. All resistors are assumed to be noiseless.

For the noninverting amplifier, the equivalent input voltage noise, referred to the input, is:

$$E_N = \sqrt{(R_S\, i_{nn})^2 + e_n^2 + (R_2\, i_{ni})^2 / A_{VCL}}$$

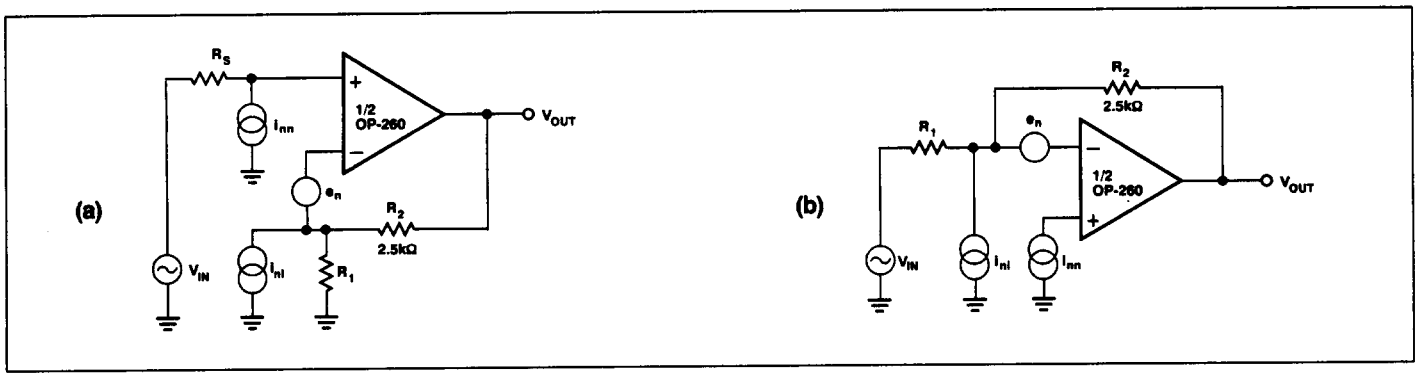


FIGURE 7: *Simplified noise models for the OP-260 in noninverting (a) and inverting (b) gain.*

where:

E_N = total input referred noise
e_n = amplifier voltage noise
i_{nn} = noninverting input current noise
i_{ni} = inverting input current noise
R_S = source resistance
A_{VCL} = closed loop gain = $1 + R_2/R_1$

For the inverting amplifier, the equivalent input voltage noise, referred to the input, is:

$$E_N = \sqrt{e_n^2 \left(\frac{1+|A_{VCL}|}{|A_{VCL}|}\right) + \frac{(R_2 i_{ni})^2}{|A_{VCL}|}}$$

assuming $R_S \ll R_1$. A_{VCL} = closed loop gain = $-R_2/R_1$.

Typical values @ 1kHz for the noise parameters of the OP-260 are:

e_n = 5.0nV/$\sqrt{Hz}$
i_{nn} = 3.0pA/$\sqrt{Hz}$
i_{ni} = 20.0pA/$\sqrt{Hz}$

SHORT CIRCUIT PERFORMANCE

To avoid sacrificing bandwidth and slew rate performance the OP-260's output is **not** short circuit protected. Do not short the amplifier's output to ground or to the supplies. Also, the buffer output current should not exceed a value of ±20mA peak or ±7mA continuous.

POWER SUPPLY BYPASSING AND LAYOUT CONSIDERATIONS

Proper power supply bypassing is critical in all high-frequency circuit applications. For stable operation of the OP-260, the power supplies must maintain a low impedance-to-ground over an extremely wide bandwidth. This is most critical when driving a low resistance or large capacitance, since the current required to drive the load comes from the power supplies. A 10µF and 0.1µF bypass capacitor are recommended for each supply, as shown in Figure 8, and will provide adequate high-frequency bypassing in most applications. The bypass capacitors should be placed at the supply pins of the OP-260. As with all high frequency amplifiers, circuit layout is a critical factor in obtaining optimum performance from the OP-260. Proper high frequency layout reduces unwanted signal coupling in the circuit. When breadboarding a high frequency circuit, use direct point-to-point wiring, keeping all lead lengths as short as possible. Do not use wire-wrap boards or "plug-in" prototyping boards.

During PC board layout, keep all lead lengths and traces as short as possible to minimize inductance. The feedback and gain-setting resistors should be as close as possible to the inverting input to reduce stray capacitance at that point. To further reduce stray capacitance, remove the ground plane from the area around the inputs of the OP-260. Elsewhere, the use of a solid unbroken ground plane will insure a good high-frequency ground.

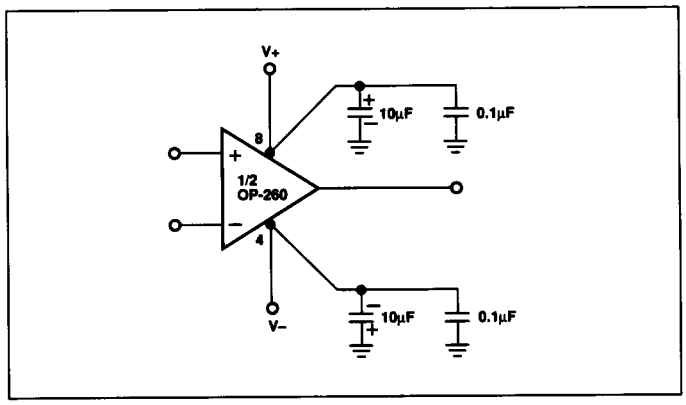


FIGURE 8: *Proper power supplying bypassing is required to obtain optimum performance with the OP-260.*

APPLICATIONS

NONINVERTING AMPLIFIER

The OP-260 can be used as a voltage-follower or noninverting amplifier as shown in Figure 9. A current feedback amplifier in this configuration yields the same transfer function as a voltage feedback op amp:

$$\frac{V_{OUT}}{V_{IN}} = 1 + \frac{R_2}{R_1}.$$

Remember to use a 2.5kΩ feedback resistor in voltage-follower application.

In noninverting applications, stray capacitance at the inverting input of a current feedback amplifier will cause peaking which will increase as the closed-loop gain decreases. The gain setting resistor, R_1, is in parallel with this stray capacitance creating a zero in the closed-loop response. For large noninverting gains, R_1 is small, creating a very high frequency open-loop pole which has limited effect on the closed-loop response. As the noninverting gain is decreased, R_1 becomes larger and the stray zero becomes lower in frequency, having a much greater effect on the closed-loop response. To reduce peaking at low noninverting gains, place a series resistor, R_C, in series with the noninverting input as shown in Figure 9. This resistor combines with the stray capacitance at the noninverting input to form a low-pass filter that will reduce the peaking. The value of R_C should be determined experimentally in the actual PCB layout. Less peaking will occur in inverting gain configurations since the inverting input is a virtual ground which forces a constant voltage across the stray capacitance.

A common practice to stabilize voltage feedback op amps is to use a capacitor across the feedback resistance. This creates a zero in the voltage feedback amplifier response to offset the loss of phase margin due to a parasitic pole. In current feedback amplifiers, this technique will cause the amplifier to become unstable because the closed-loop bandwidth will increase beyond the stable operating frequency. For the same reason, current feedback amplifiers will not be stable in integrator applications.

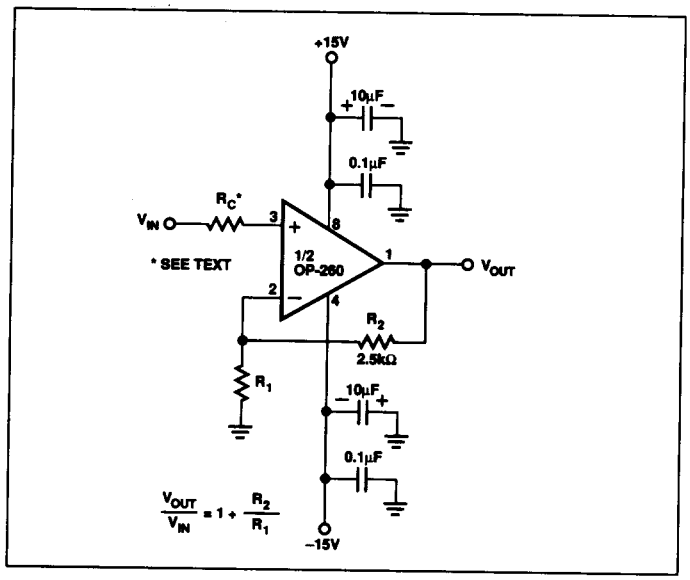


FIGURE 9: *The OP-260 as a voltage follower or noninverting amplifier.*

INVERTING AMPLIFIER

The OP-260 is also capable of operation as an inverting amplifier (see Figure 10). The transfer function of this circuit is identical to that using a voltage feedback op amp:

$$\frac{V_{OUT}}{V_{IN}} = -\frac{R_2}{R_1}.$$

An optional offset voltage trim is shown in Figure 11.

AUTOMATIC GAIN CONTROL AMPLIFIER

One of the shortcomings of using voltage feedback op amps in an Automatic-Gain-Control amplifier is that its bandwidth drops off rapidly as gain increases, limiting the useful bandwidth. However, for current feedback amplifiers, bandwidth is relatively independent of gain,

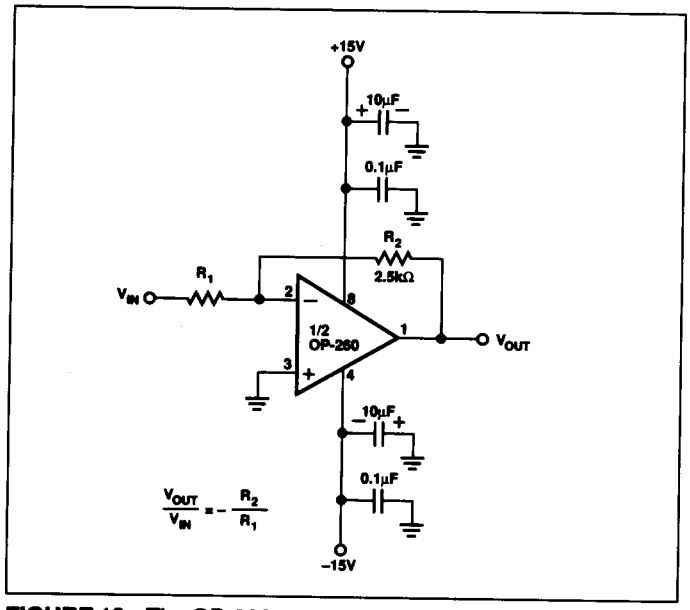


FIGURE 10: *The OP-260 as an inverting amplifier.*

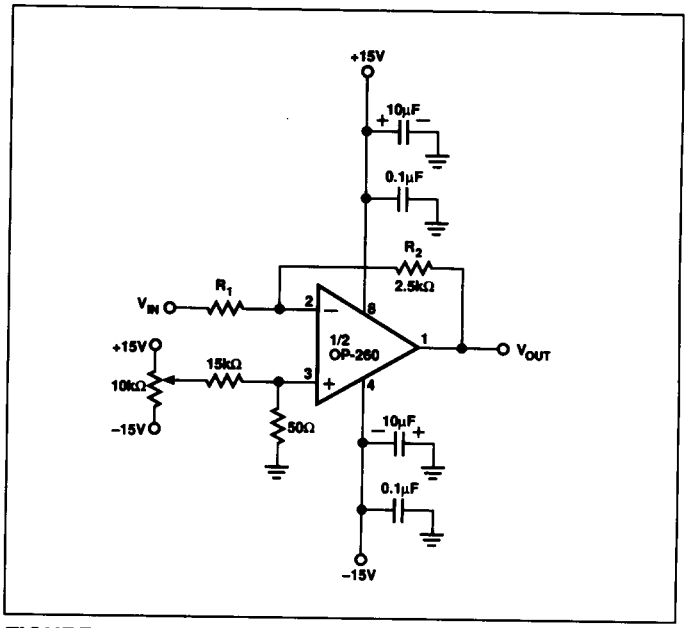


FIGURE 11: *Optional offset voltage trim circuit for the OP-260.*

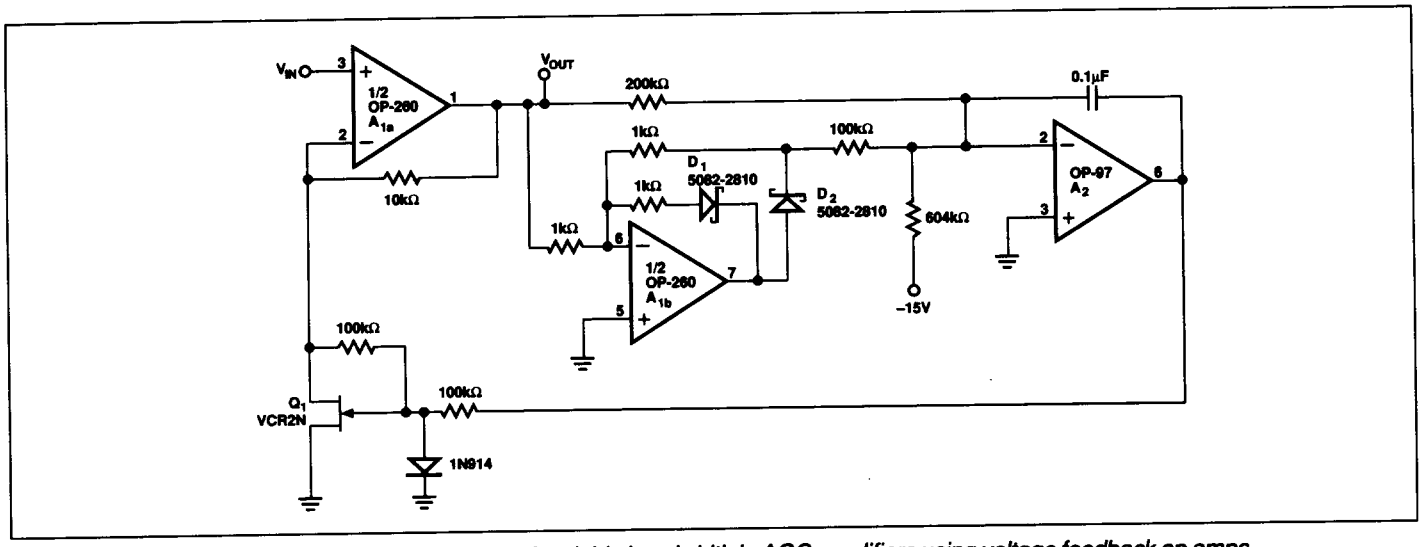


FIGURE 12: *The OP-260 eliminates the problem of variable bandwidth in AGC amplifiers using voltage feedback op amps.*

eliminating this problem. Figure 12 shows a simple AGC amplifier design using the OP-260. Amplifier A_{1a} is used as the gain stage. Its output is rectified by the second amplifier A_{1b}. If the output voltage swings more negative, diode D_2 forward biases and D_1 reverse biases, closing the loop on amplifier A_{1b}. A positive voltage appears on the anode of D_2; but, if the output voltage swings positive, D_2 reverse biases and D_1 forward biases, keeping the loop closed on A_{1b}. This prevents the amplifier from saturating to the negative rail. The result is an accurate positive rectification of the output signal.

The output of the rectifier is then compared with a reference current set up by the 604kΩ resistor which is biased to −15V. The output of the error amplifier A_2 will drive the FET (Q_1) to the proper voltage necessary to achieve a zero voltage at the inverting input of A_2. If there is insufficient signal, the error amplifier will detect an imbalance. This causes the error amp to drive more positive, turning FET Q_1 on harder, reducing the channel resistance and increasing the gain. Figure 13 shows the pulse response of the AGC amplifier. The AGC loop maintains a constant peak output amplitude for a square wave input signal range of ±20mV$_{p-p}$ to ±6.0V$_{p-p}$.

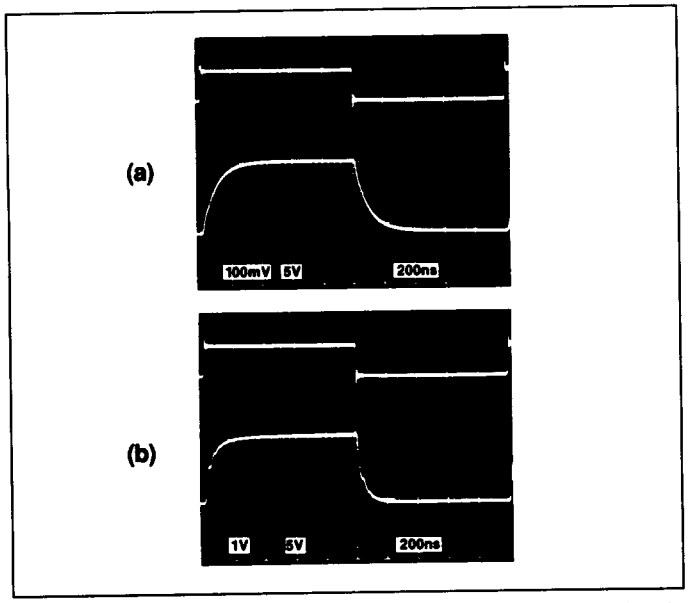


FIGURE 13: *Pulse response of the AGC amplifier at (a) low level input signal, and (b) large input signal.*

LOW PHASE ERROR AMPLIFIER

The simple amplifier depicted in Figure 14 utilizes the monolithic dual OP-260 and a few resistors to substantially reduce phase error over a wide frequency range compared to conventional amplifier

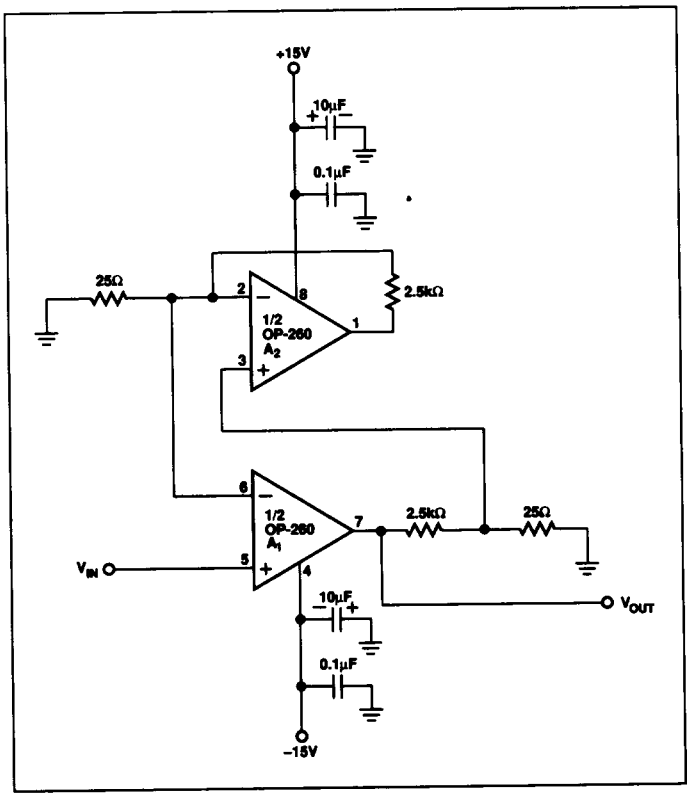


FIGURE 14: *Active feedback allows cancellation of the dominant pole, therefore reducing the phase shift significantly.*

designs. This technique relies on the matched frequency characteristics of the two current feedback amplifiers in the OP-260. Referring to the circuit, notice that each amplifier has the same feedback resistor network, corresponding to a gain of 100. Since these two amplifiers are set at equal gain and are matched due to the monolithic construction of the OP-260, they will have an identical frequency response. A pole in the feedback loop of an amplifier becomes a zero in the closed loop response. With one amplifier in the feedback loop of the other, the pole and zero are at the same frequency, thus cancelling and reducing low phase error. Figure 15 shows that the low phase error amplifier at a gain of 100 exhibits 1° of phase error up to a frequency of 1MHz. For a single voltage feedback op amp to match this performance, it would require a gain-bandwidth product exceeding 10GHz!

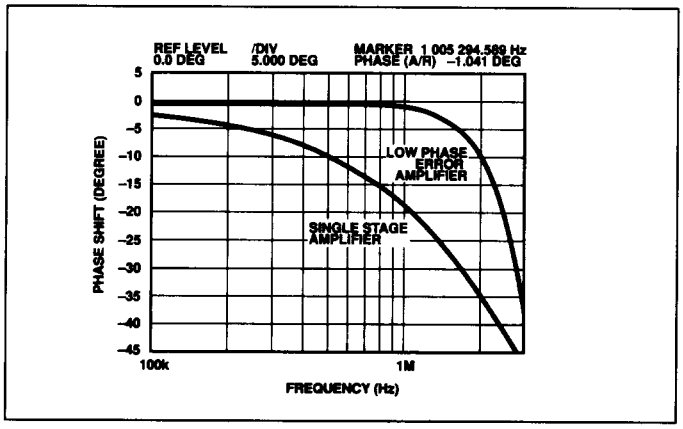


FIGURE 15: *Phase response of the ultra-low phase error amplifier compared to that of a single current feedback amplifier. Note that there is only one degree of phase error over a 1MHz bandwidth at a gain of 100.*

HIGH-SPEED INSTRUMENTATION AMPLIFIER

The circuit of Figure 16 is a high-speed instrumentation amplifier constructed with a single OP-260. Gain of the amplifier is set by resistor R_G according to the following formula:

$$\frac{V_{OUT}}{V_{IN}} = \frac{10k\Omega}{R_G} + 2.$$

The advantages of the two op amp instrumentation amplifier is that the errors in the individual amplifiers tend to cancel one another. Common-mode rejection is limited by the matching of resistors R_1 to R_4. For the best CMR performance, these resistors should be matched to 0.01% or a CMR trim can be performed on R_1. A CMRR of 90dB (measured at 60Hz) is achievable at all gains. Input offset voltage of the instrumentation amplifier is determined by the V_{IOS} matching of the OP-260, which is typically under 0.5mV.

Figure 17 shows the relationship between gain and bandwidth for the instrumentation amplifier. Reducing resistors R_1 to R_4 to 2.5kΩ increases the bandwidth but makes circuit performance more dependent on board layout.

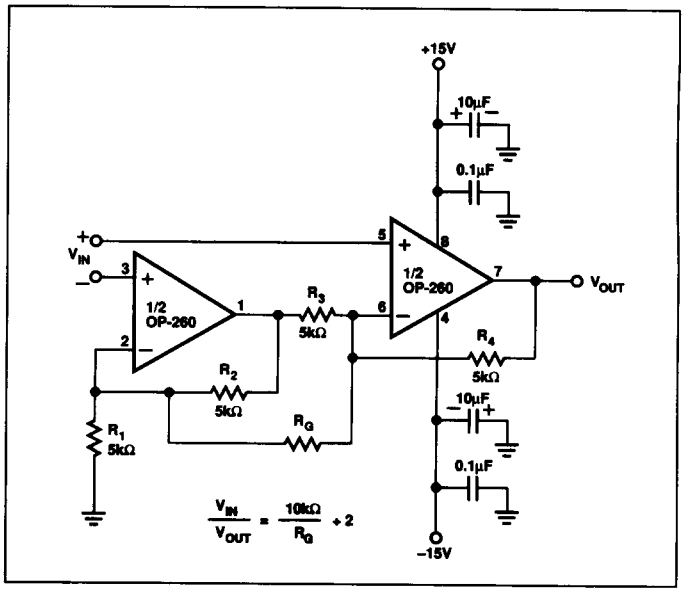


FIGURE 16: *High Speed Instrumentation Amplifier*

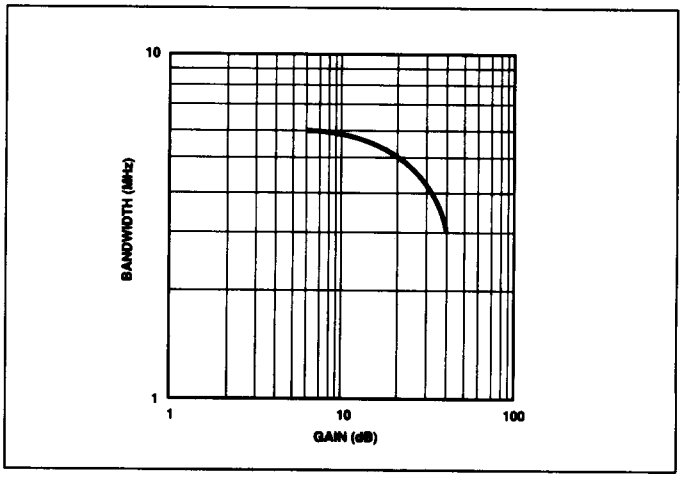


FIGURE 17: *Bandwidth versus gain for the high speed instrumentation amplifier.*