UM10541

NVT2008PW and NVT2010PW demo boards

Rev. 1 — 7 March 2012 **User manual**

Document information

Info	Content
Keywords	NVT, voltage translator, level translator, level shift, passive voltage translator, passive level translator, passive level shift, I2C-bus, SMBus, SPI, NVT2008, NVT2010
Abstract	NXP Voltage Translators (NVT) are used in bidirectional signaling voltage level translation applications for I/O buses with incompatible logic levels. The NVT2008 and NVT2010 are eight- and ten-channel voltage translators, operational from 1.0 V to 3.6 V at $V_{CC(A)}$ (low voltage side) and 1.8 V to 5.5 V at $V_{CC(B)}$ (high voltage side) without direction control for open-drain or push-pull I/O devices.

Revision history

Rev	Date	Description
v.1	20120307	user manual; initial release

Contact information

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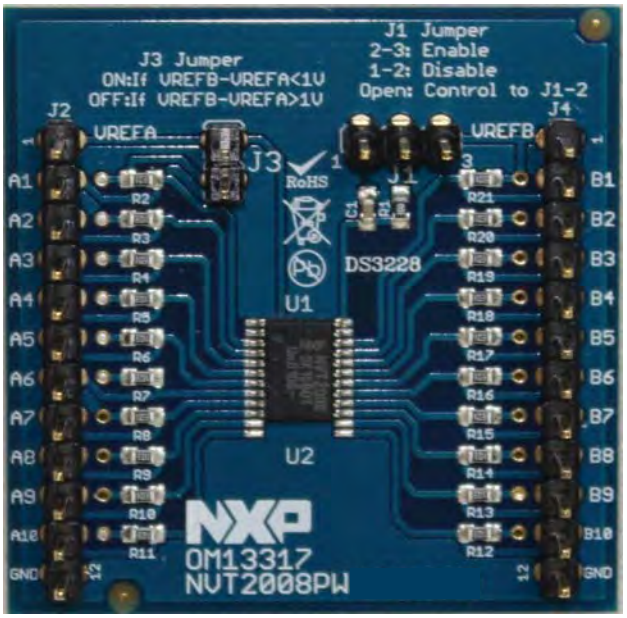
1. Introduction

The NVT2008PW (OM13317) and NVT2010PW (OM13324) demo boards are designed to let customers evaluate the NXP 8-channel and 10-channel bidirectional voltage level translators. The demo boards interface between device I/Os operating at different voltage levels. Since the NVT2008PW and NVT2010PW devices are passive devices, pull-up resistors may be needed depending on the I/O interface type (totem pole or open-drain), difference in translation voltage, and the translation direction (high-to-low voltage, low-to-high voltage, or bidirectional). The NVT2008PW and NVT2010PW devices allow translations between any voltages from 1.0 V to 5.5 V.

Please refer to NVT2008/NVT2010 data sheet (Ref. 1) and application note *AN11127* (Ref. 2) for more detailed information.



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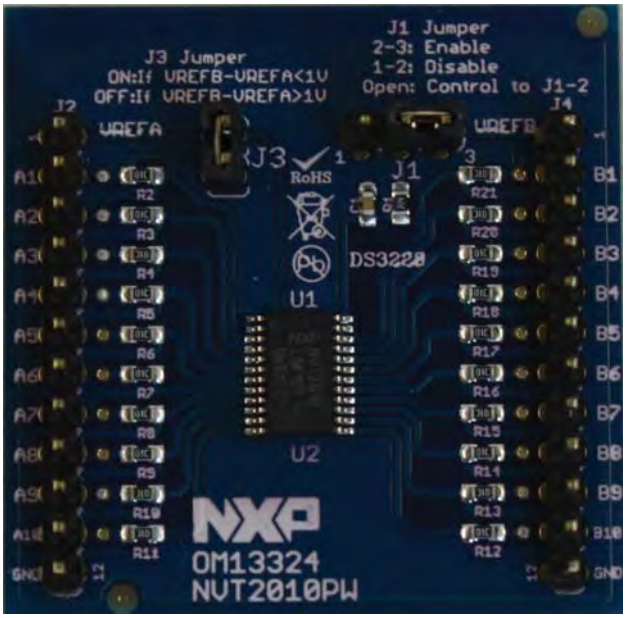
a. NVT2008PW (OM13317)



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b. NVT2010PW (OM13324)

Fig 1. Bidirectional voltage level translators demo boards

2. Hardware description

2.1 Schematic

The demo boards contain footprints for the NVT2008PW and NVT2010PW devices, the jumpers, headers, and passive components are shared. The NVT2008PW and NVT2010PW demo board schematic is shown in Figure 2. Pins 2 and 3 on J1 must be shorted to enable the part. Pins 1 and 12 on J2 are power and GND for the low voltage side. Pins 1 and 12 on J4 are power and GND for the high voltage side. All Bn I/O pins on the right side have 10 kΩ pull-up resistors to VREFB and all An I/O pins on the left side have 10 kΩ pull-up resistors to VREFA through jumper J3. A shunt must be installed at J3 if VREFB − VREFA < 1 V. If VREFB − VREFA ≥ 1 V, then the J3 jumper should be open and resistors R2 through R11 must be removed. If they are not removed, then a resistive path exists between the A-side I/Os that can impact the efficiency and signal integrity of the solution.

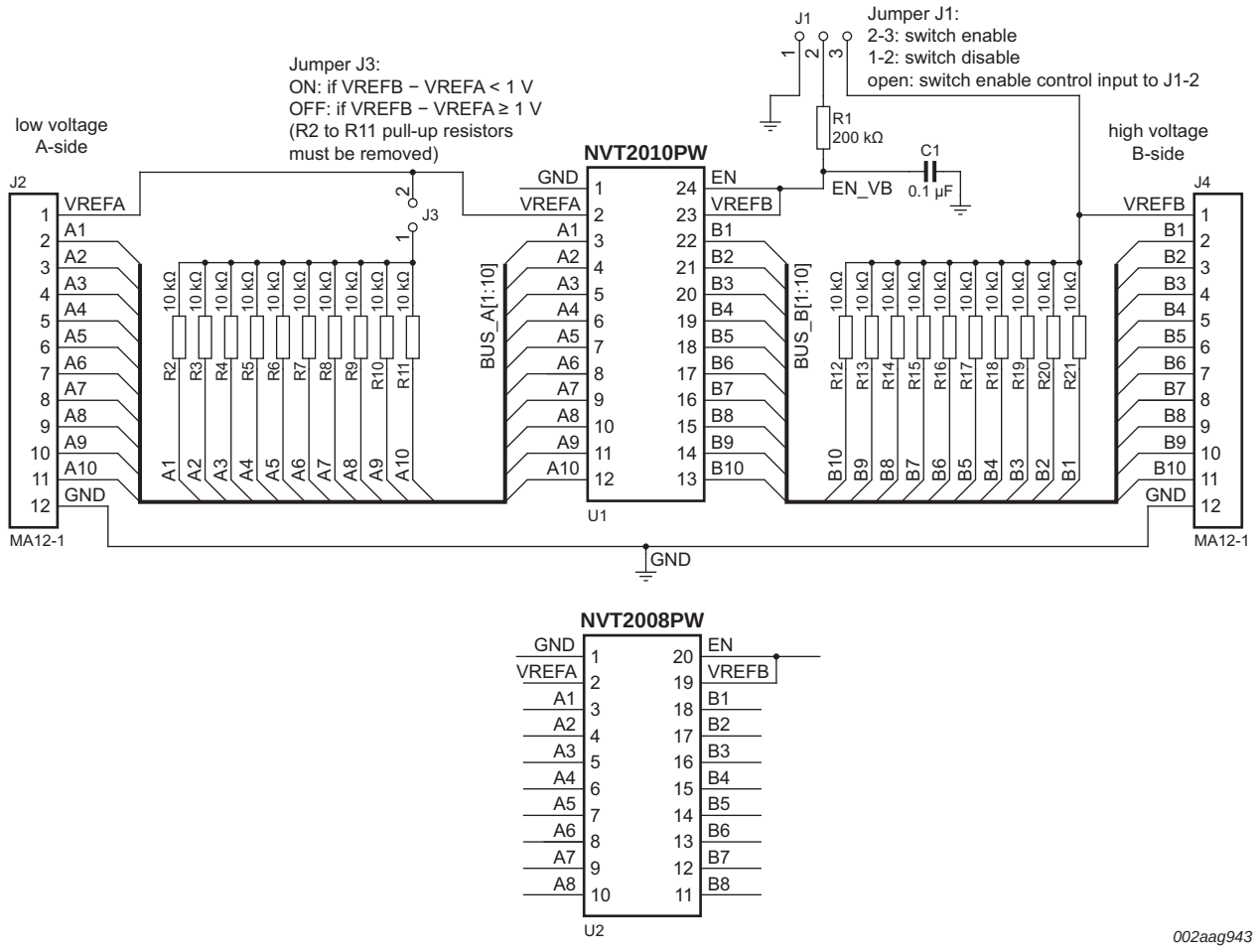

Fig 2. NVT2008PW and NVT2010PW demo board schematic

2.2 Jumper and header functions

The functions of the jumpers and headers on these demo boards are shown in Table 1.

Table 1. Header descriptions for NVT2008PW (OM13317) and NVT2010PW (OM13324) demo boards

Jumper/header	Function	Notes
J1 (3-pin)	Device switch enable or disable control	Short pins 2 and 3 to enable the NVT2008PW or NVT2010PW device (default). When pins 1 and 2 are shorted, the device is disabled.
J2 (12-pin)	Low voltage VREFA, GND and An I/O signal connect pins	Pin 1 = VREFA: low voltage power. Pin 12 = GND: low voltage ground. A[1:8] are low voltage signals for NVT2008PW. A[1:10] are low voltage signals for NVT2010PW.
J3 (3-pin)	Connects 10 kΩ pull-up resistors to VREFA on low voltage side for VREFB – VREFA < 1 V application required	Short pins 1 and 2 to connect 10 kΩ pull-up resistors to VREFA on low voltage side (default). **Remark:** Pins 1 and 2 must be open and 10 kΩ pull-up resistors must be removed when VREFB – VREFA ≥ 1 V.
J4 (12-pin)	High voltage VREFB, GND and Bn I/O signal connect pins	Pin 1 = VREFB: high voltage power. Pin 12 = GND: high voltage ground. B[1:8] are high voltage signals for NVT2008PW. B[1:10] are high voltage signals for NVT2010PW.

3. References

[1] **NVT2008; NVT2010, “Bidirectional voltage-level translator for open-drain and push-pull applications” —** Product data sheet; NXP Semiconductors; www.nxp.com/documents/data_sheet/NVT2008_NVT2010.pdf

[2] **AN11127, “Bidirectional voltage level translators NVT20xx, PCA9306, GTL2000, GTL2002, GTL2003, GTL2010” —** application note; NXP Semiconductors; www.nxp.com/documents/application_note/AN11127.pdf

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