TYPE II CALLER ID DECODER

NW6003

FEATURES

- 1200 baud Bell 202 and ITU-T V.23 Frequency Shift Keying (FSK) Demodulation
- Compliant with three specifications:
  Bellcore GR-30-CORE & SR-TSV-002476
  British Telecom (BT) SIN227 & SIN242
  Cable Communication Association (CCA) TW/P&E/312
- Bellcore "CPE Alerting Signal (CAS)" and British Telecom "Idle State and Loop State Tone Alert Signal" detection
- Ring and line reversal detection
- High sensitivity with -40 dBV input Tone and FSK Detection
- Serial data interface to microcontroller
- 3 V ±10% or 5 V ±10% operation
- Low power CMOS with powerdown mode
- Operating temperature range: -40 °C to +85 °C
- Packages available:
  NW6003-XS 24 pin SOIC
  (where 'X' is the revision ID)

DESCRIPTION

The NW6003 device is a single-chip, 3/5 Volt CMOS caller ID and call waiting detection circuit. It can receive signals following Bellcore GR-30-CORE & SR-TSV-002476, BT SIN227 & SIN242, and CCA TW/P&E/312 specifications.

The NW6003 provides 1200 baud Bell 202 and ITU-T V.23 FSK demodulation. It allows a microcontroller to extract data from it via a serial interface. In addition, the NW6003 offers Idle State and Loop State Tone Alert Signal and line reversal detection capability for BT CLIP, ring burst detection for the CCA CLIP, and ring and CAS detection for Bellcore CID.

The device can be used in feature or cordless phones for BT Calling Line Identity Presentation (CLIP), CCA CLIP and Bellcore Calling Identity Delivery (CID) systems. It can also be used in caller ID boxes, modem, fax machines, answering machines, database query systems and Computer Telephony Integration (CTI) systems.

FUNCTIONAL BLOCK DIAGRAM

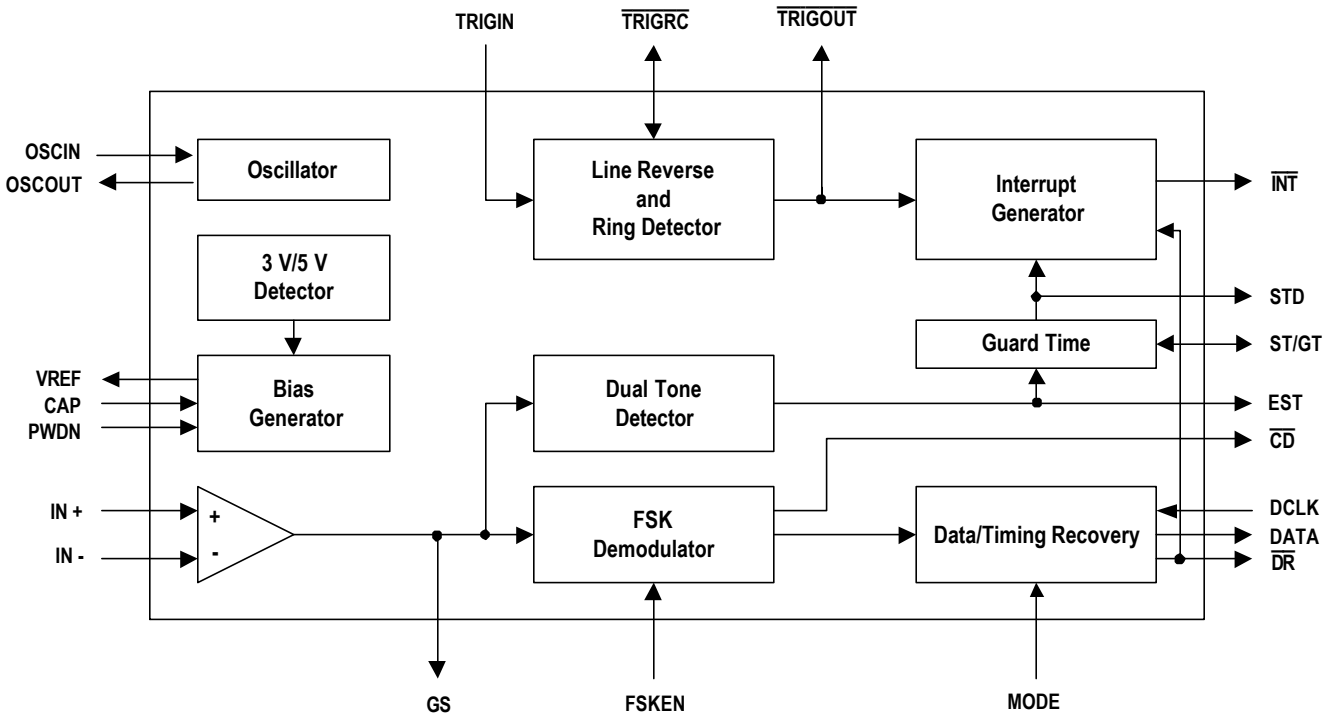


Figure 1. Block Diagram

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PIN INFORMATION

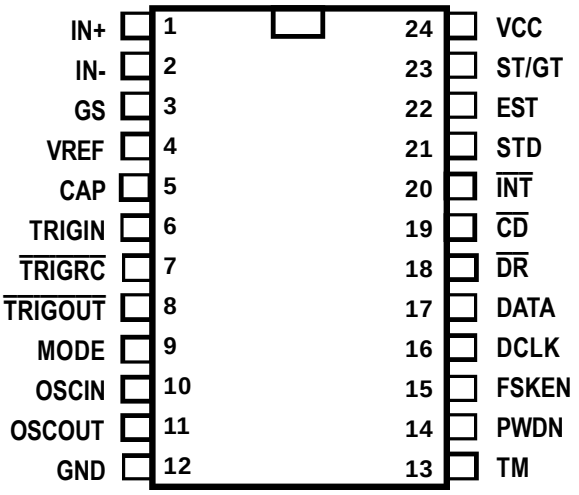


Figure 2. Pin Assignment

Name	Type	Pin No.	Description
IN+	I	1	**Non-inverting Input** of the gain adjustable op amp.
IN-	I	2	**Inverting Input** of the gain adjustable op amp.
GS	O	3	**Gain Select Output** of the gain adjustable op amp. Select the op amp gain by adjusting the resistor ratio in the feed-back resistor network.
VREF	O	4	**Reference Voltage.** This output is used to bias the input op amp. It is typically VCC/2.
CAP	O	5	**Capacitor Connector.** A 0.1μF decoupling capacitor should be connected between this pin and GND.
TRIGIN	I	6	**Trigger Input.** This is a Schmitt trigger input used for ring detection and line reversal detection.
$\overline{\text{TRIGRC}}$	I/O	7	**Trigger Resistor and Capacitor Connector.** This pin is connected to VCC and GND through resistor and capacitor. The RC value decides the time delay from TRIGIN going inactive (low) to $\overline{\text{TRIGOUT}}$ becoming inactive (high). See Fig.6 for reference.
$\overline{\text{TRIGOUT}}$	O	8	**Trigger Output.** This is a Schmitt trigger buffer output indicating the detection of line reversal and/or ringing.
MODE	I	9	**Serial FSK Interface MODE Select.** A low level on this pin sets the interface to mode '0', while a high level sets it to mode '1'.
OSCIN	I	10	**Oscillator Input.** A 3.579545 MHz crystal or ceramic resonator should be connected between this pin and the OSCOUT. It can also be driven by an external clock source.
OSCOUT	O	11	**Oscillator Output.** A 3.579545 MHz crystal or ceramic resonator should be connected between this pin and and OSCIN. When OSCIN is driven by an external clock, this pin should be left floating.
GND	--	12	**Ground.**
TM	I	13	**Test Mode.** Must be connected to GND for normal operation.

PIN INFORMATION (CONTINUED)

Name	Type	Pin No.	Description
PWDN	I	14	**Power Down.** This is an active high Schmitt trigger input. When active, the device enters a minimal power state by disabling all internal functional circuits except TRIGIN, $\overline{\text{TRIGRC}}$ and $\overline{\text{TRIGOUT}}$. It must be low for normal operation.
FSKEN	I	15	**FSK Enable.** When this pin is high, FSK demodulation is enabled. This pin should be set low to disable the FSK demodulator from reacting to extraneous signals such as speech, alert signal etc.
DCLK	I/NC	16	**Data Clock.** In mode '0' (MODE pin low), this pin is unused. In mode '1' (MODE pin high), this pin is an input, Data Clock is provided by microcontroller.
DATA	O	17	**Data Output.** In mode '0', data appears on this pin once demodulated. In mode '1', data is shifted out on the rising edge of DCLK, which is supplied by microcontroller.
$\overline{\text{DR}}$	O/NC	18	**Data Ready Output.** In mode '0', this pin is unused. In mode '1', this pin indicates to the microcontroller that 8-bit data is ready. Microcontroller initializes the DCLK signal to read out the data.
$\overline{\text{CD}}$	O	19	**FSK Carrier Detect .** This is an active low CMOS output signal to indicate the presence of in-band FSK signal.
$\overline{\text{INT}}$	OD	20	**Interrupt.** This is an active low open drain output. This pin is used to interrupt the microcontroller when $\overline{\text{TRIGOUT}}$ or $\overline{\text{DR}}$ is low, or STD is high. It remains low until all three signals become inactive.
STD	O	21	**Dual Tone Alert Signal Delayed Steering Output.** An active high signal to indicate the detection of a "guard time qualified" Dual Tone Alert Signal.
EST	O	22	**Dual Tone Alert Signal Early Steering Output.** This pin is an active high output to indicate the detection of Dual Tone Alert Signal.
ST/GT	I/O	23	**Dual Tone Alert Signal Steering Input/Guard Time.** It's a CMOS output and an input of voltage comparator. If the voltage at this pin is greater than voltage threshold (See Fig-6), STD is asserted high to indicate that a dual tone has been detected. A voltage less than threshold enables the device to accept a new dual tone. External RC are connected to EST and VCC pins.
VCC	--	24	**3/5 V Power Supply.**

Abbreviation Index

CAS ---------- CPE Alerting Signal
CDS ---------- Caller Display Service
CID ---------- Calling Identity Delivery
CIDCW ---------- Calling Identity Delivery on Call Waiting
CLIP ---------- Calling Line Identity Presentation
CNAM ---------- Calling Name Delivery
CND ---------- Calling Number Delivery
CNIC ---------- Calling Number Identification Circuit
CO ---------- Central Office
CTI ---------- Computer Telephony Integration
TE ---------- Terminal Equipment

FUNCTIONAL DESCRIPTION

CALLER ID SPECS SUPPORTED

The NW6003 is a type II Caller ID device with Call Waiting capability. It supports Bellcore, BT and CCA specifications. The major differences between above specs are as follows (refer to Figure 13, Figure 14, Figure 15, Figure 16 and Figure 17):

BELLCORE

Bellcore GR-30-CORE and SR-TSV-002476 define the requirement for the signaling services of Calling Number Delivery (CND), Calling Name Delivery (CNAM) and Calling Identity Delivery on Call Waiting (CIDCW).

In CND or CNAM service, information of the calling party is embedded in the silent interval between the first and second ringings. The NW6003 can detect the first ringing and then demodulate the incoming Bell-202 FSK data. In CIDCW service, information about an incoming caller is sent to the subscriber who is engaged in another call. A CPE Alerting Signal (CAS) indicates that a CIDCW data is incoming. The NW6003 can detect the alerting signal and demodulate the incoming FSK information which contains CIDCW data. The demodulated data is output onto the serial interface.

BRITISH TELECOM

BT SIN227 and SIN242 define the signal interface between the Central Office (CO) and the Terminal Equipment (TE) for the Caller Display Service (CDS). CDS provides CLIP (Calling Line Identity Presentation) that delivers to an idle state (on hook) TE the identity of an incoming caller before the first ring.

A polarity reversal on the A and B wires (see Figure 6) indicates the arrival of a CDS call. After that comes an Idle State Tone Alert Signal, and then Caller ID FSK information transmitted in ITU-T V.23 format. When the subscriber is engaged in a call, the arrival of information about another incoming call is indicated by a Loop State Tone Alert Signal. The NW6003 can detect the line reversal and tone alert signal, it can also demodulate the incoming ITU-T V.23 FSK signals.

CABLE COMMUNICATION ASSOCIATION

The CCA caller identity specification TW/P&E/312 defines a different CDS TE interface. In this specificaiton, data is transmitted after a single burst of ringing rather than before the first ringing cycle, as specified in the BT. The Idle State Tone Alert Signal is not required in this case. The CCA specifies that data can be transmitted in either Bell-202 or ITU-T V.23 format. The NW6003 can detect the ring burst, and then demodulate either of the FSK format.

BLOCK DESCRIPTION

The NW6003 requires a 3.579545 MHz system clock and consists of four major functional blocks: Analog Input Circuit, CLIP/CID Call Arrival Detection, Dual Tone Alert Signal Dectection, and FSK Demodulation.

ANALOG INPUT CIRCUIT

The input signal is processed by the Analog Input Circuit block, which is comprised of an operational amplifier and a bias source (VREF). VREF is the output of a low impedance voltage source used to bias the input op amp, and is typically equal to VCC/2. The gain adjustable op amp is also used to select the input gain by connecting a feedback resistor between GS and the IN- pin. Figure 3 shows the necessary connections with the A/B line inputs. In single-ended configuration, the gain adjustable op amp is connected as shown in Figure 4.

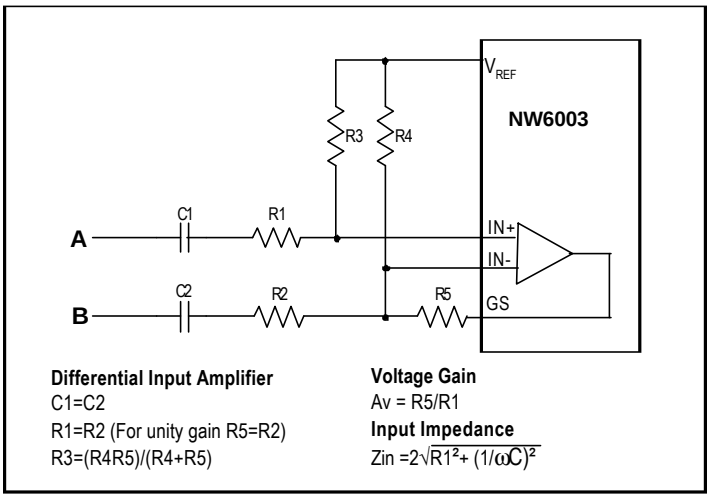


Figure 3. Differential Input Gain Control Circuit

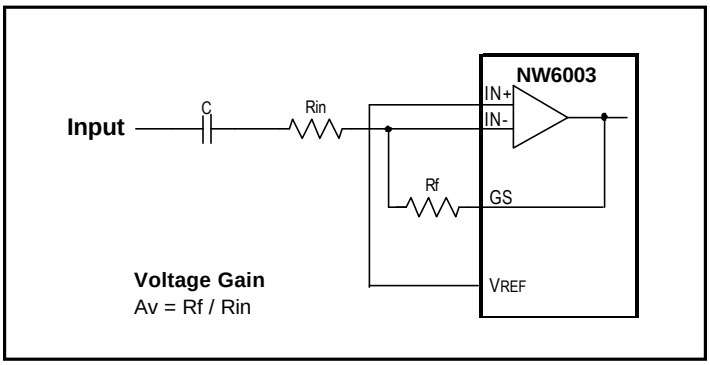


Figure 4. Single-ended Input Gain Control Circuit

CLIP/CID CALL ARRIVAL DETECTION

Figure 6 shows the typical application circuit to detect the CLIP/CID call arrival signals. The diode bridge works for both single ended and balanced ring signals. R1 and R2 are used to set the maximum loading and must be of some value to achieve balanced loading. The ring signal is attenuated by R1, R3 and R4 resistor devider before being applied to pin TRIGIN. The attenuation value is determined by the detection of minimal ring voltage and maximum noise tolerance between Ring/Tip and ground.

When no signal is applied to telephone line, TRIGIN will be at ground and pin $\overline{\text{TRIGOUT}}$ will stay inactive high. If TRIGIN increases from ground to VT+ (Schmitt trigger high going threshold voltage), C3 gets discharged, $\overline{\text{TRIGRC}}$ becomes low and $\overline{\text{TRIGOUT}}$ is asserted. The low going $\overline{\text{TRIGOUT}}$ can be used to interrupt or wake up the microcontroller. When TRIGIN signal drops below VT- (Schmitt trigger low going threshold voltage), C3 will start to charge up through R5C3 time constant. After $\overline{\text{TRIGRC}}$ pin reaches above the threshhold voltage (VT+), $\overline{\text{TRIGOUT}}$ becomes inactive high and it stops to interrupt the microcontroller. To ensure the minimum $\overline{\text{TRIGOUT}}$ low interval and to filter the ring signal to get a smooth envelope output, the RC time constant should be greater than the maximum cycle time of the Ring Signal.

Ring Detection for Bellcore: Bellcore recommends that the CID FSK data be transmitted between first and second ringings. The circuit in Figure 6 will generate a ring envelope signal at pin $\overline{\text{TRIGOUT}}$ for the ring voltage of 40 Vrms or greater. R5 and C3 are used to filter the ring signal to provide the envelope output.

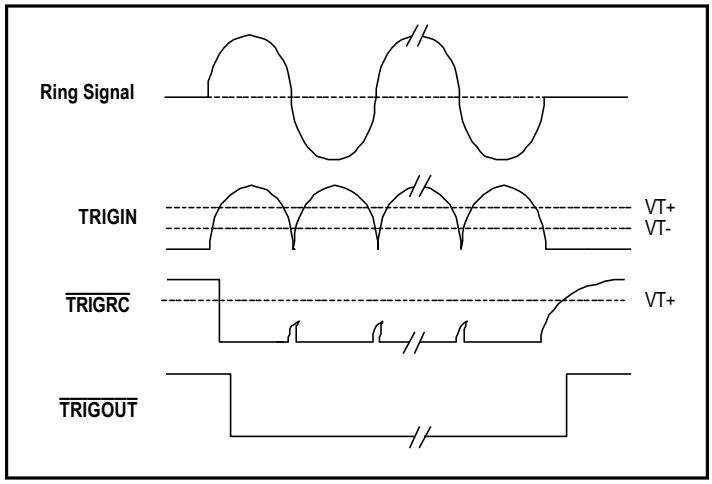


Figure 5. TRIGIN, $\overline{\text{TRIGRC}}$ and $\overline{\text{TRIGOUT}}$ Operation

Line Reversal Detection for BT: British Telecom uses the line polarity reverse (+15 V to -15V between the two lines slewing in 30 ms) to indicate the arrival of an incoming CDS call. When line reverse occurs, TRIGIN increases over VT+ and $\overline{\text{TRIGOUT}}$ signal becomes active low. When reversal is over, TRIGIN falls below VT- and $\overline{\text{TRIGOUT}}$ returns inactive high.

Ring Burst Detection for CCA: The CCA requires the TE to detect a single burst of ringing followed by the FSK data. The ring pulse may varies from 30 to 75 Vrms with pulse duration 200 - 450 ms.

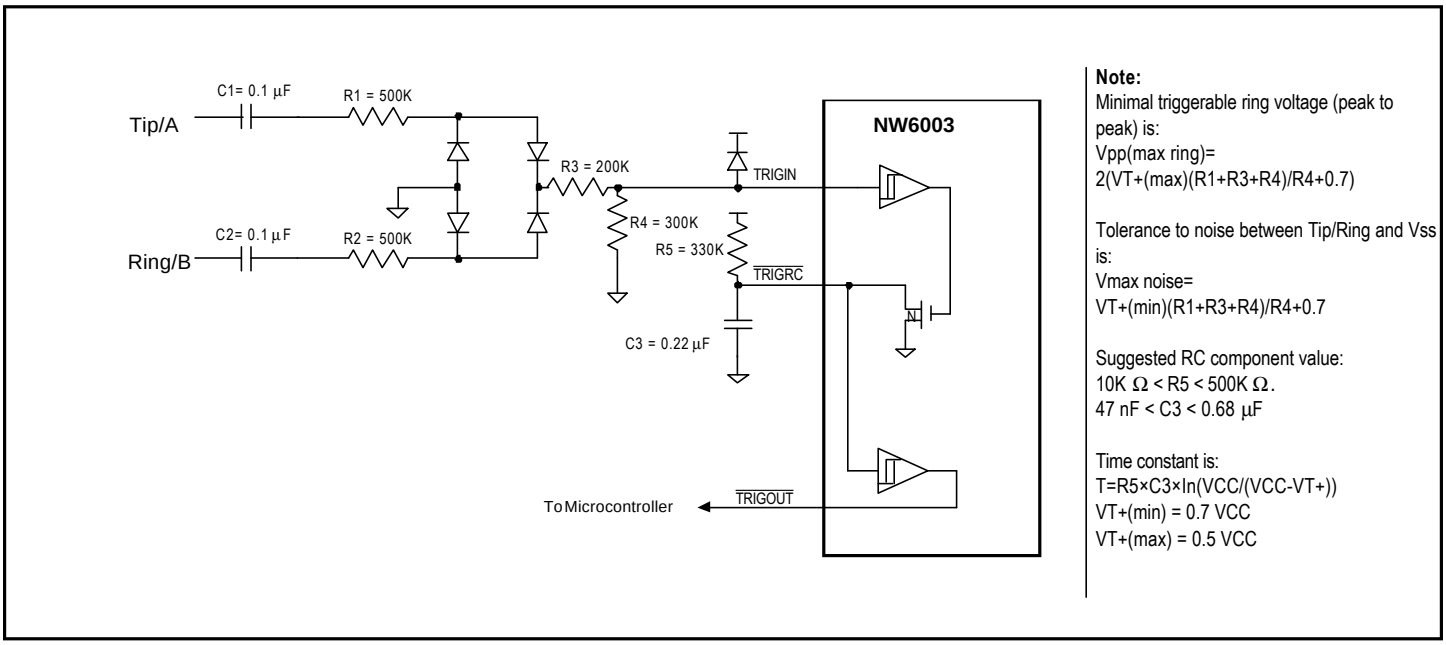


Figure 6. CLIP/CID Call Arrival Detection Circuit

DUAL TONE ALERT SIGNAL DETECTION

BT specifies a Dual Tone Alert Signal in both idle (on-hook) state and loop (off-hook) state, while Bellcore specifies a similar Dual Tone Alert Signal called CPE Alerting Signal (CAS) in off-hook state. The low and high tone frequencies of two different systems are as follows:

	BT	Bellcore
Low Tone Frequency	2130 Hz ± 1.1%	2130 Hz ± 0.5%
High Tone Frequency	2750 Hz ± 1.1%	2750 Hz ± 0.5%

The incoming Alert Signal goes through anti-alias filter and then is separated into high band and low band by two bandpass filters. The tone detection algorithm examines the filter outputs to validate the arrival of the Dual Tone Alert Signal. The EST pin becomes active when both tones are detected. The EST is only the preliminary indication, it must be qualified by the "guard time" as required by Bellcore and BT (a minimum duration for valid signals). STD is the guard time qualified CAS/Dual Tone Alert Signal detection output, it indicates the correct detection.

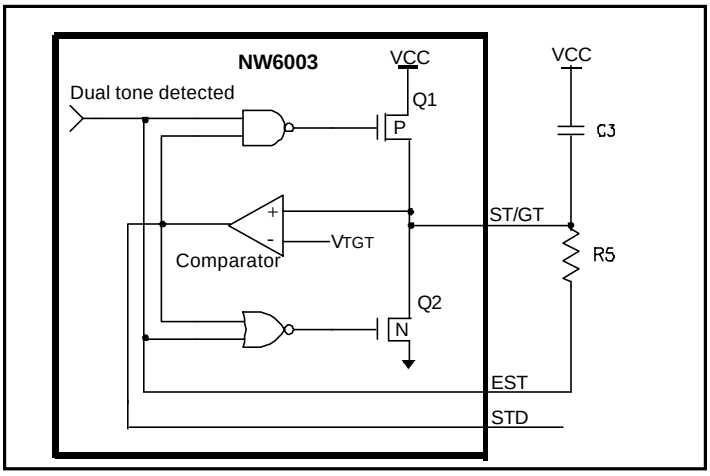


Figure 7. Guard Time Circuit of Dual Tone Alert Signal Detection

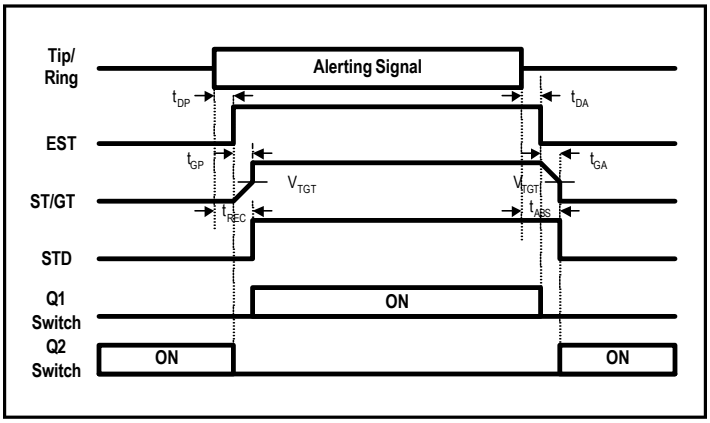


Figure 8. Guard Time Waveform

Figure 7 shows the operation of the guard time circuit and Figure 8 shows the waveform of the EST, ST/GT and STD pins. The total recognition time is $t_{REC} = t_{DP} + t_{GP}$, where t_{DP} is the tone present detection time and t_{GP} is the tone present guard time. The total absent time is $t_{ABS} = t_{DA} + t_{GA}$, where t_{DA} is the tone absent detection time and t_{GA} is the tone absent guard time. The guard time is the RC time constant for the capacitor charge to VCC or discharge to GND. To get the unequal present and absent guard time, a diode can be connected as shown in Figure 9 to provide different RC time constant (varying resistance value) during charging and discharging.

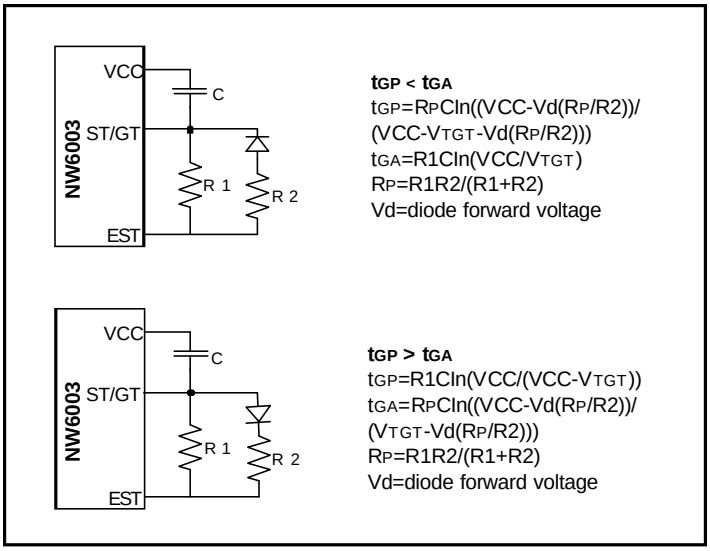


Figure 9. Guard Time Circuits with Unequal Present and Absent Times

FSK DEMODULATION

The key part among the functions offered by NW6003 is FSK demodulation. This function is implemented by several stages: first, the carrier detector provides an indication of the presence of signal at the bandpass filter output; second, the device's dual mode serial interface allows convenient extraction of the 8-bit data words in the demodulated FSK bit stream.

The FSK characteristics are different in BT and Bellcore specifications. The BT's signal frequencies correspond to ITU-T V.23; the Bellcore frequencies correspond to Bell 202. The CCA requires that TE be able to receive both ITU-T V.23 and Bell 202 signals. The NW6003 is compatible with both formats. It also meets the signal characteristics by setting the input op amp at unity gain in 5 V operation.

	ITU-T V.23	Bell 202
Mark Freq. ('1')	1300 Hz ± 1.5%	1200 Hz ± 1%
Space Freq. ('0')	2100 Hz ± 1.5%	2200 Hz ± 1%

The Dual Tone Alert Signal, speech and DTMF tones are in the same frequency band as FSK, they will be demodulated and generate false data. To avoid it, FSKEN pin is used to disable the FSK modulation when FSK signal is not expected.

FSK CARRIER DETECTION

The carrier detector provides an indication of the presence of a signal in the FSK frequency band. It detects the presence of a signal of sufficient amplitude at the output of the FSK bandpass filter. If the signal is qualified by a digital algorithm, the $\overline{CD}$ output becomes low to indicate carrier detection. An 8 ms hysteresis is provided to allow for momentary signal drop out once $\overline{CD}$ has been activated. And when there is no activity at the FSK bandpass filter output for 8 ms, $\overline{CD}$ is released.

When $\overline{CD}$ is inactive (high), the raw output of the FSK demodulator is ignored by the FSK data output interface. In mode '0', the DATA pin is forced high. In mode '1', the internal shift register is not updated. No $\overline{DR}$ is generated. If DCLK is clocked, DATA is undefined.

SERIAL FSK INTERFACE

The three wire DATA, DCLK and $\overline{DR}$ form the data interface of the FSK demodulation. The DATA pin is the serial data pin that outputs data to external devices. The DCLK pin is the data clock which is generated by an external device. The $\overline{DR}$ pin is the data ready signal, also an output from the NW6003 to external devices. This interface provides the mechanism to extract the 8-bit data words in the demodulated FSK bit stream. Two modes are selectable via control of the device's MODE pin: Mode '0' (MODE pin is low), where data transfer is initiated by the NW6003; Mode '1' (MODE pin is high), where the data transfer is initiated by an external microcontroller.

Mode '0'

In this mode, data transfer is initiated by the NW6003. The device demodulates the incoming FSK signal, and output the data directly to the DATA pin. Figure 24 shows the timing diagram of Mode '0' operation.

Mode '1'

In this mode, the microcontroller supplies read pulses (DCLK) to shift the 8-bit data words out of the NW6003, onto the DATA pin. The NW6003 asserts $\overline{DR}$ to denote the word boundary and indicate to the microprocessor that a new word has become available. Internal to the device, the demodulated data bits are sampled and stored. After the 8th bit, the word is parallelly loaded into an 8-bit shift register and $\overline{DR}$ goes low. The contents of shift register are shifted out to DATA pin on DCLK's rising edge with LSB (Least Significant Bit) out first. If DCLK begins while $\overline{DR}$ is low, $\overline{DR}$ will return to high upon the first DCLK. This feature allows the associated interrupt to be cleared by the first read pulse. Otherwise, $\overline{DR}$ stays low for half a nominal bit time (1/2400 sec) and then returns to high. After the last bit (Most Significant Bit) has been read, additional DCLKs are ignored. Figure 22 shows the timing diagram of Mode '1' operation.

OTHER FUNCTIONS

POWER-DOWN MODE

The device provides the power down feature to reduce the power consumption. By activating the PWDN pin (high), the gain adjustable op amp, oscillator and all other internal circuits besides the ring detection circuit are all disabled. The TRIGIN, $\overline{\text{TRIGRC}}$ and $\overline{\text{TRIGOUT}}$ pins are not affected, the device can still react to call arrival indicator and activate the interrupt to wake up the microcontroller.

CRYSTAL OSCILLATOR

A 3.579545 MHz crystal oscillator or other external clock source is required for NW6003. The crystal can be directly connected between OSCIN and OSCOUT pins without any external component. If an external clock source is used, OSCIN pin should be driven by the clock source and OSCOUT pin is left floating or is used to drive other devices. Figure 10 shows some applications.

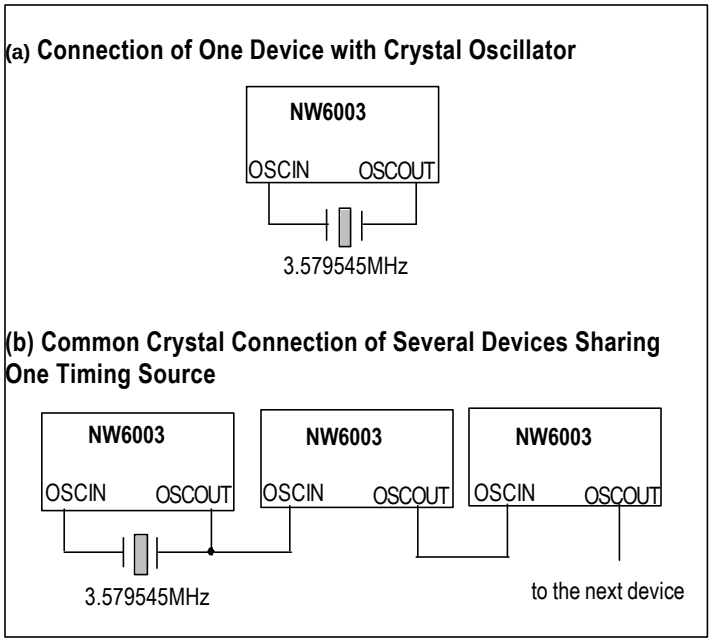


Figure 10. Applicaiton of Clock Driven Circuit

INTERRUPT

The NW6003 provides an open drain interrupt output $\overline{\text{INT}}$ to interrupt the microcontroller. Either $\overline{\text{TRIGOUT}}$ low, STD high or $\overline{\text{DR}}$ low will activate the $\overline{\text{INT}}$ and it will remain active 'low' until all of these three pins return to an inactive state. The microcontroller should read these pins through input ports to detect the interrupt type ($\overline{\text{TRIGOUT}}$, STD or $\overline{\text{DR}}$) and to make the correspondent response.

When the system is first powered up, $\overline{\text{TRIGOUT}}$ will be low (C3 at $\overline{\text{TRIGRC}}$ has no initial charge) and STD will be high if PWDN is low (no charge across the capacitor at ST/GT pin in Figure 7), interrupt signal will be generated. The microcontroller should ignore interrupts from these sources on the initial power up until there is sufficient time to charge the capacitors. Also, by asserting PWDN high immediately after system power up, STD will become low and no interrupt will be generated. In power-down mode, EST and comparator output are forced low, the charging switch will turn on, and the capacitor at ST/GT pin will charge up more rapidly.

BIAS VOLTAGE GENERATOR

The bias voltage generator provides a low impedance voltage source equal to VCC/2 on pin VREF and is used to bias the op amp. To reduce the noise, a 0.1 μF capacitor should be connected between CAP and GND pins.

APPLICATION INFORMATION

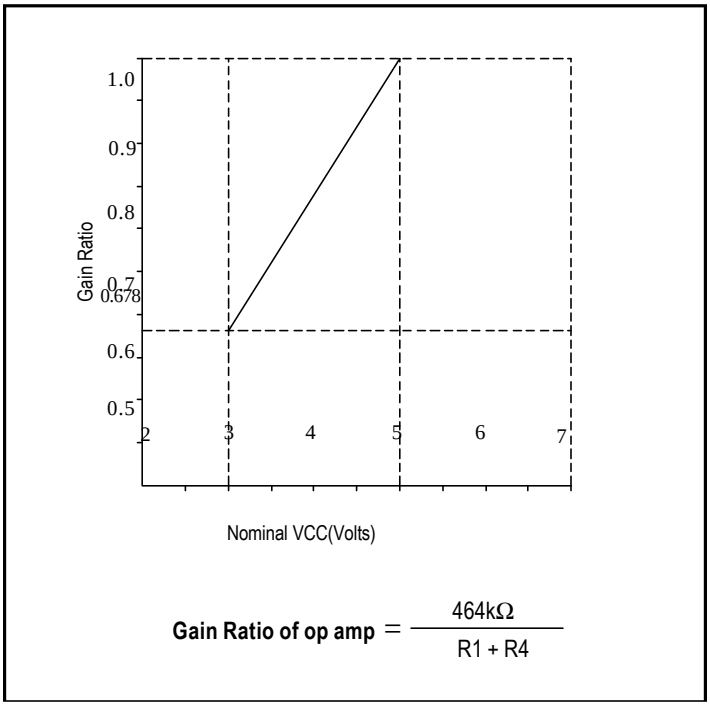
APPLICATION CIRCUITS

Figure 11 shows the typical NW6003 application circuit. For 5 V operation, the gain ratio of the op amp is set to unity to optimize the electrical characteristics. As the power supply voltage drops, the threshold of tone and FSK detectors will be lower. To meet the BT and Bellcore tone reject level requirements, the gain of the op amp should be adjusted according to the graph in Figure 12.

It should be noted that the glitch with sufficient amplitude appears on the tip and ring interface will be falsely detected. One way to avoid such false detection is to use the photo-coupler LED between the diode bridge and TRIGIN pin.

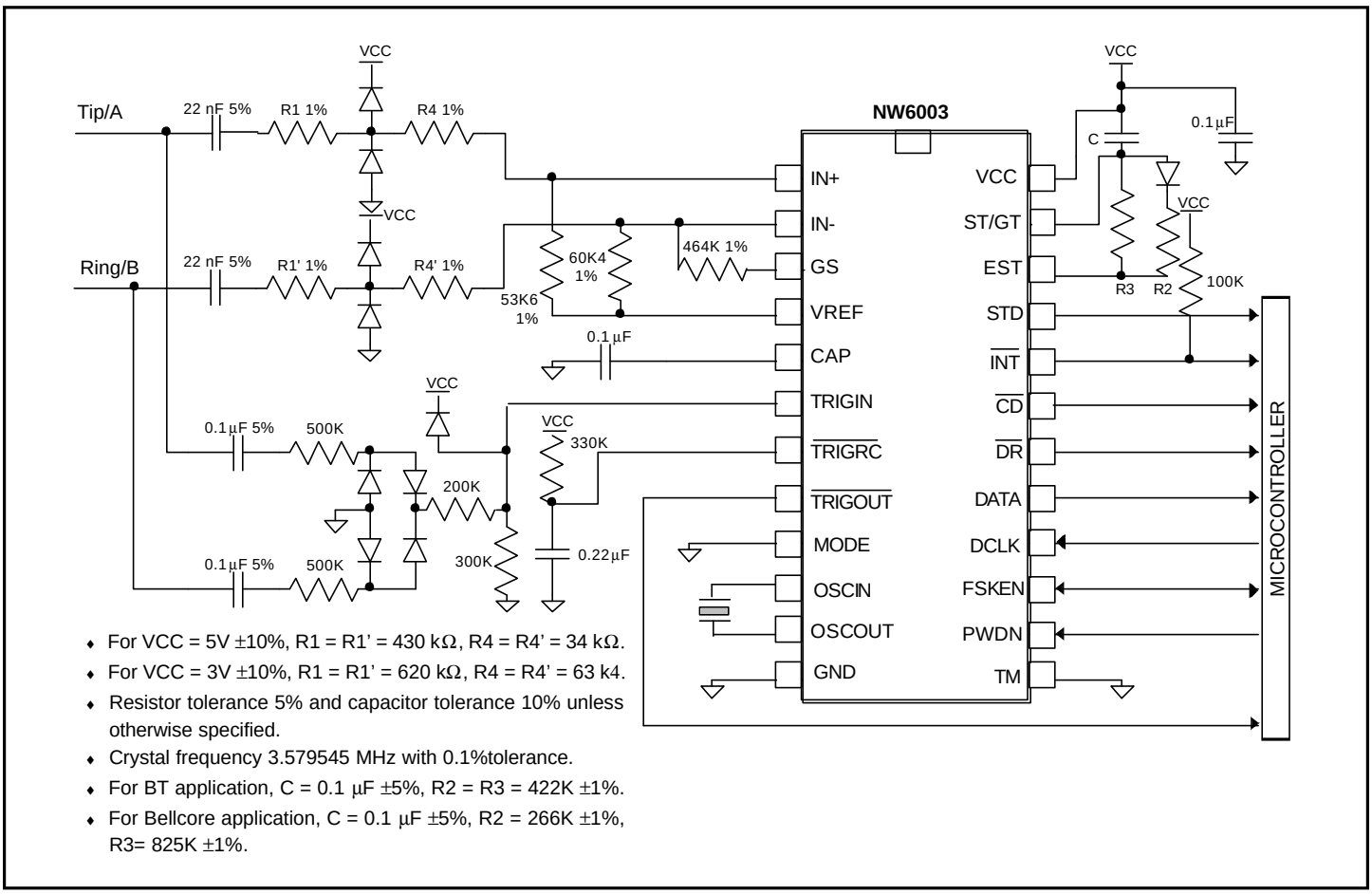
BELLCORE/BT/CCA APPLICATIONS

The NW6003 supports three specifications: Bellcore, BT and CCA. Figure 13 shows the timing diagram of Bellcore on-hook data transmission, and Figure 14 shows Bellcore off-hook data transmission. The BT operations are shown in Figure 15 and Figure 16, and the CCA operation in Figure 17.



$$\text{Gain Ratio of op amp} = \frac{464k\Omega}{R1 + R4}$$

Figure 12. Gain Ratio as a Function of Nominal VCC



- For VCC = 5V ±10%, R1 = R1' = 430 kΩ, R4 = R4' = 34 kΩ.
- For VCC = 3V ±10%, R1 = R1' = 620 kΩ, R4 = R4' = 63 k4.
- Resistor tolerance 5% and capacitor tolerance 10% unless otherwise specified.
- Crystal frequency 3.579545 MHz with 0.1%tolerance.
- For BT application, C = 0.1 µF ±5%, R2 = R3 = 422K ±1%.
- For Bellcore application, C = 0.1 µF ±5%, R2 = 266K ±1%, R3= 825K ±1%.

Figure 11. Typical Application Circuit

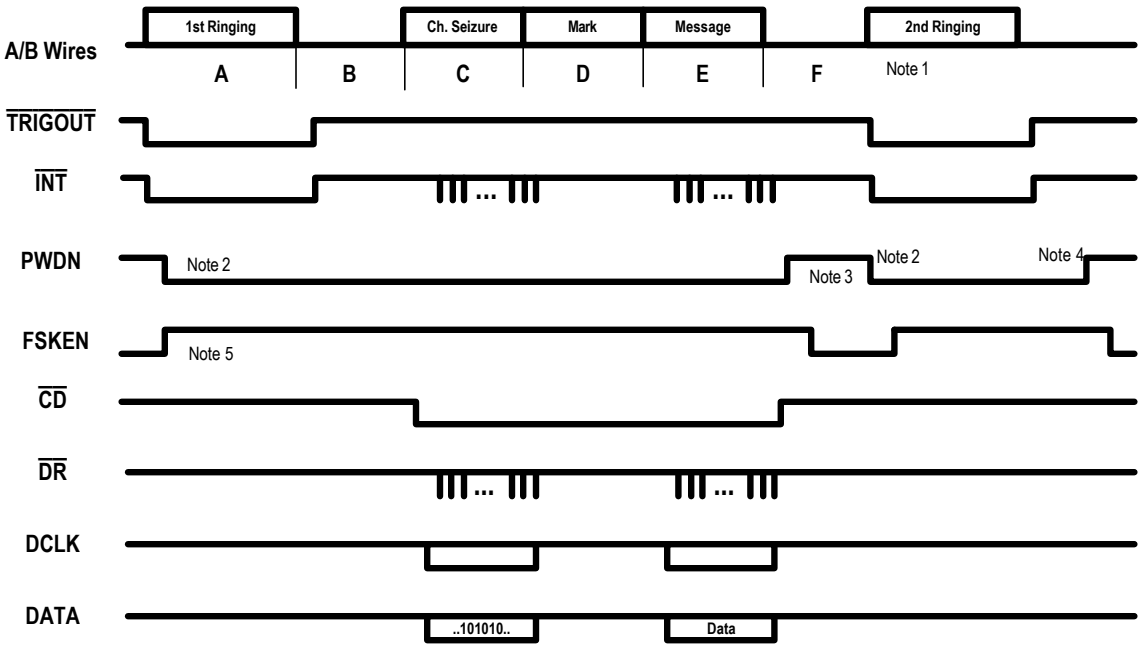


Figure 13. Bellcore On-hook Data Transmission Timing Diagram

Notes:

1) A= 2 sec typ., B= 250 - 500 ms, C= 250 ms, D= 150ms, E depends on data length, Max C+D+E = 2.9 - 3.7 sec, F ≥ 200 ms.

2) In a battery operated CPE, NW6003 may be enabled only after the end of ringing to conserve power.

3) The microcontroller in the CPE powers down the NW6003 after $\overline{CD}$ goes inactive.

4) The microcontroller times out if $\overline{CD}$ is not activated on the 2nd ring and puts the device into Power-down mode.

5) FSKEN may be set always high while the CPE is on-hook. To prevent the FSK demodulator from reacting to other inband signals such as speech, CAS or DTMT tones. The designer may choose to set FSKEN low during the period that FSK signal is not expected.

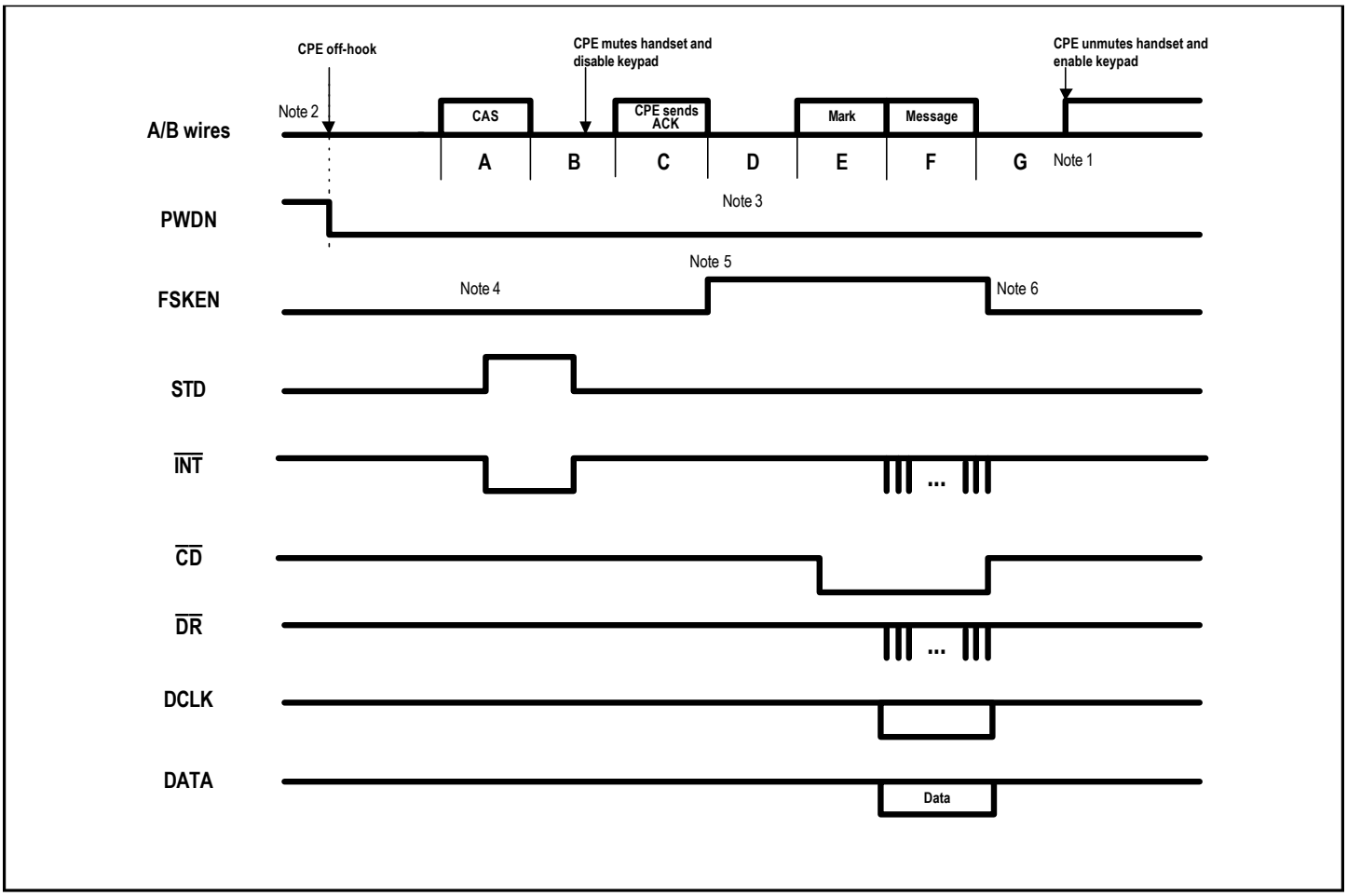


Figure 14. Bellcore Off-hook Data Transmission Timing Diagram

Notes:

1) A= 75 - 85 ms, B= 0 -100 ms, C= 55 - 65 ms, D= 0 - 500 ms, E= 58 - 75ms, F depends on data length, G≤ 50 ms.
2) If AC power is not available, the designer may use the line power when the CPE goes off-hook and use battery power while on-hook. The CPE should also be CID (on-hook) capable .
3) If the end office fails to send the FSK signal, the CPE should disable FSKEN to unmute the handset and enable the keypad after this interval.
4) When FSK signal is not expected, the FSKEN pin should be set low to disable the FSK demodulator.
5) FSKEN should be high as soon as the CPE has finished sending the acknowledgement signal ACK.
6) FSKEN should be low when $\overline{CD}$ become inactive.

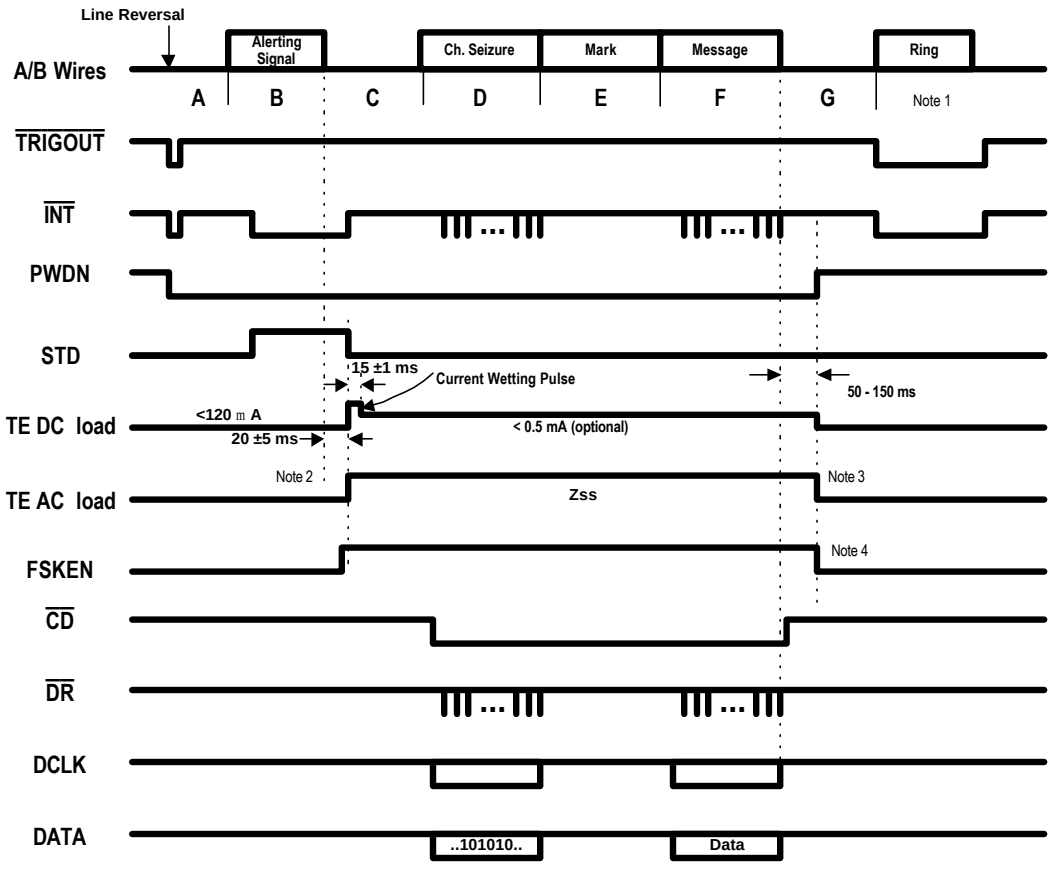


Figure 15. BT Idle State (on-hook) Data Transmission Timing Diagram

Notes:

1) A≥ 100ms, B=88 - 110 ms, C≥ 45 ms (up to 5 sec), D= 80 -262 ms, E= 45 - 75 ms, F≤ 2.5 sec (typ. 500 ms), G≥ 200 ms.

2) By choosing t_{GA}=15 ms, t_{ABS} will be 15-25 ms (refer to Figure 8). Current wetting pulse and AC/DC load should be applied right after the STD falling edge.

3) AC and DC loads should be removed between 50-150 ms after the end of the FSK signal. The NW6003 may go to power down mode to save power.

4) FSKEN should be set low to disable the FSK demodulator, when the FSK signal is not expected.

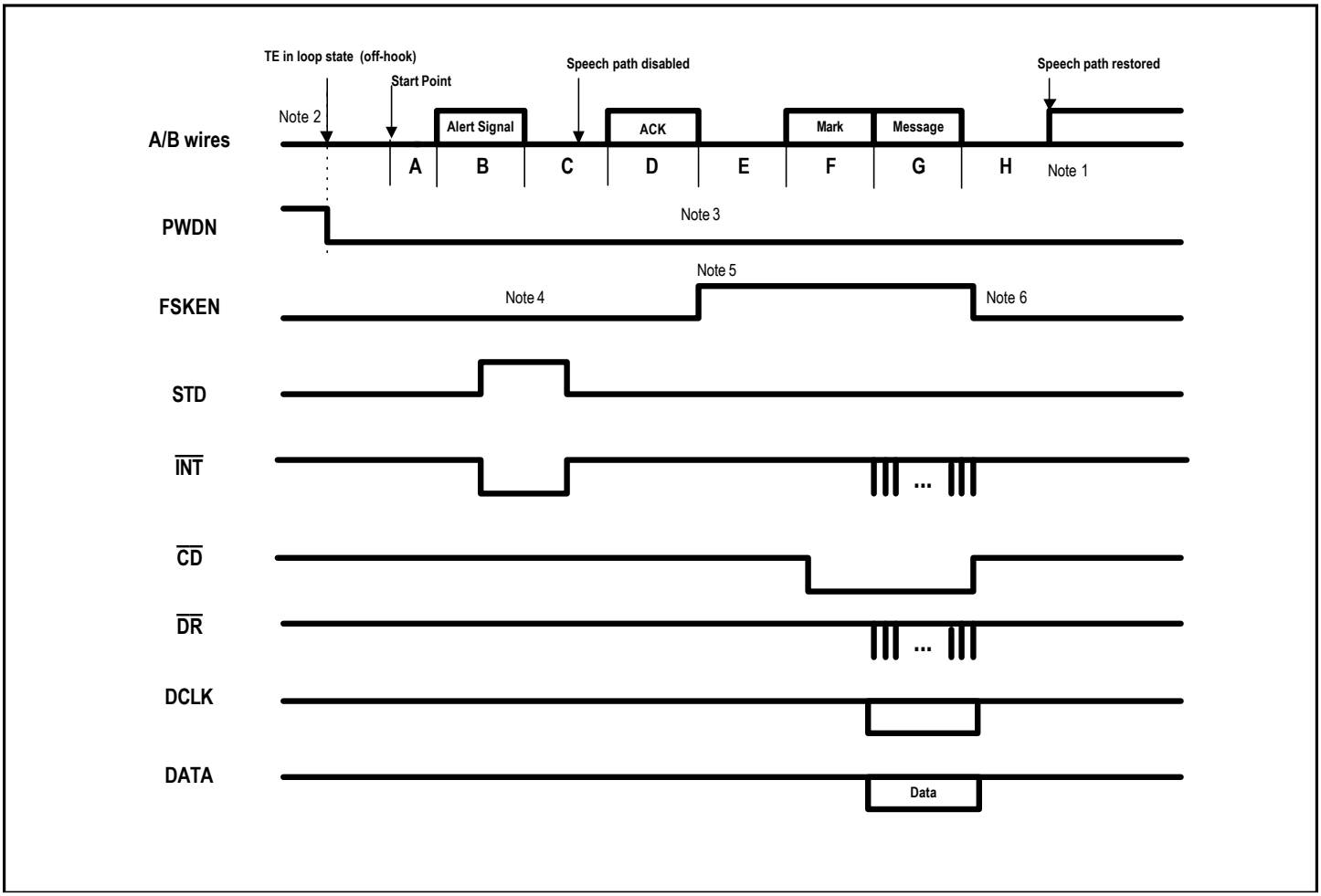


Figure 16. BT Loop State (Off-hook) Data Transmission Timing Diagram

Notes:

1) A= 40 - 50 ms, B= 80 - 85 ms, C≤ 100 ms, D= 65 - 75 ms, E= 5- 100ms, F = 45 - 75 ms, G depends on data length, H ≤ 100 ms.
2) If AC power is not available, the designer may use the line power when the TE goes into loop state (off-hook) and use battery power while on-hook.
3) If the end office fails to send the FSK signal, the TE should disable FSKEN to unmute the handset and enable the keypad after this interval.
4) When FSK signal is not expected, the FSKEN pin should be set low to disable the FSK demodulator.
5) FSKEN should be high as soon as the TE has finished sending the acknowledgement signal ACK.
6) FSKEN should be low when $\overline{CD}$ become inactive.

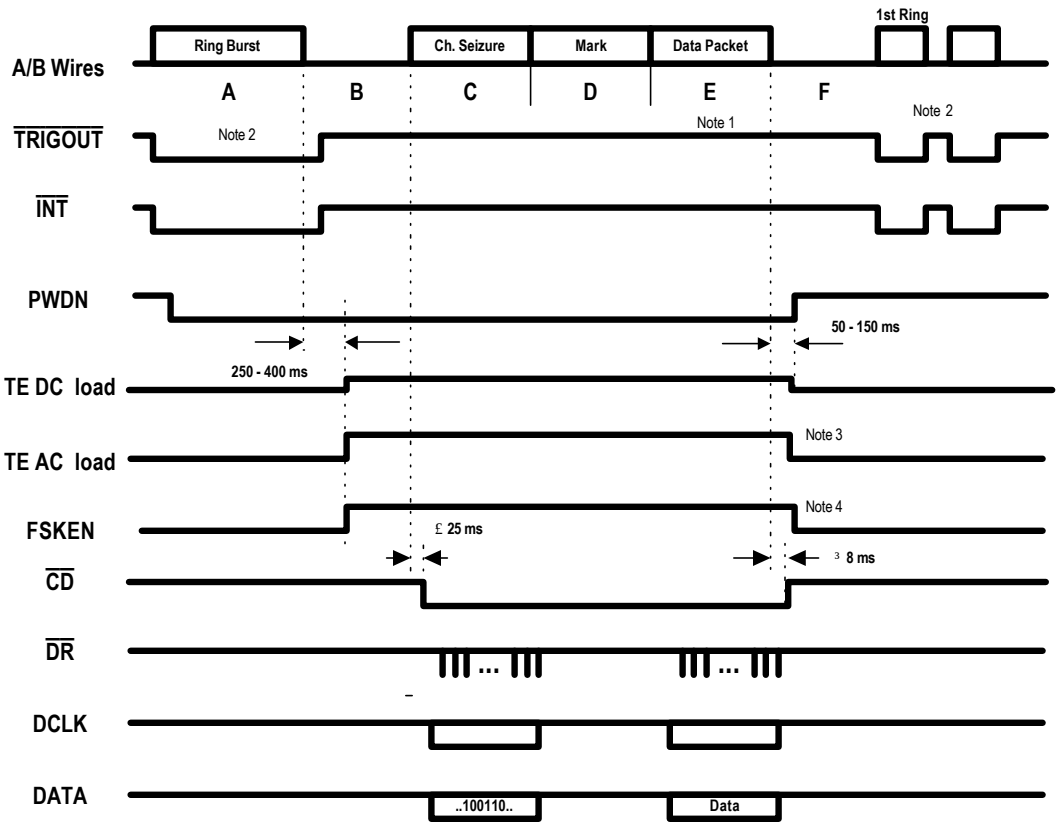


Figure 17. CCA Caller Display Service Timing Diagram

Notes:

1) A = 200 - 450 ms, B ≥ 500 ms, C= 80 - 262 ms, D= 45 -262 ms, E≤ 2.5 s (typ. 500 ms), F ≥ 200 ms.
2) $\overline{\text{TRIGOUT}}$ indicates the ring envelope.
3) AC and DC loads should be applied between 250 - 400 ms after the ring burst and should be removed between 50 to 150 ms after the end of FSK signal.
4) FSKEN should be set low when FSK signal is not expected.

MAXIMUM RATING - Exceeding the following listed values may cause permament damage.

Power Supply Voltage: -0.3 V to 7 V
Voltage on any pin other than supplies: GND - 0.3 V to VCC + 1 V
Current at any pin other than supplies: £ 20 mA
Storage Temperature: -65 °C to +150 °C

RECOMMENDED OPERATING CONDITIONS

Operating Temperature: -40 °C to +85 °C
Power Supply Voltage: 3 V ± 10% or 5 V ± 10%
Clock Frequency: 3.579545 MHz ± 0.1%
Input Voltage: 0 V to VCC

CRYSTAL SPECIFICATIONS

Frequency: 3.579545 MHz
Resonancy tolerance: ± 0.1%(-40°C to +85°C)
Resonance mode: Parallel
Load capacitance: 18 pF
Maximum series resistance: 150 Ω
Maximum drive level(mW): 2 mW

DC ELECTRICAL CHARACTERISTICS

Parameter	Pin	Description	Min	Typ	Max	Units	Test Conditions
I_{CCS}	VCC	Power Supply Standby Current		0.5	10	µA	Test 1
I_{CC}	VCC	Operating Supply Current VCC = 5 V ± 10% VCC = 3 V ± 10%		 2.5 1.8	 3.8 2.7	 mA mA	Test 2
V_{T+}	TRIGIN $\overline{\text{TRIGRC}}$ PWDN	Schmitt Trigger Input High Threshold	0.5VCC		0.7VCC	V	
V_{T-}		Schmitt Trigger Input Low Threshold	0.3VCC		0.5VCC	V	
V_{HYS}		Schmitt Hysteresis	0.2			V	
V_{IH}	DCLK MODE	CMOS Input High Voltage	0.7VCC		VCC	V	
V_{IL}	FSKEN	CMOS Input Low Voltage	GND		0.3VCC	V	
I_{OH}	$\overline{\text{TRIGOUT}}$, DCLK, DATA, $\overline{\text{DR}}$, $\overline{\text{CD}}$, STD, EST, ST/GT	Output High Sourcing Current	-0.8			mA	V_{OH}=0.9VCC

Test 1: All inputs are VCC/GND except for oscillator pins. No analog input. Output unloaded. PWDN = VCC.
Test 2: All inputs are VCC/GND except for oscillator pins. No analog input. Ouput unloaded. PWDN = GND, FEKEN = VCC.

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Parameter	Pin	Description	Min	Typ	Max	Units	Test Conditions
I_{OL}	$\overline{TRIGOUT}$, DCLK, DATA, $\overline{DR}$, $\overline{CD}$, STD, EST, ST/GT, $\overline{TRIGRC}$, $\overline{INT}$	Output Low Sinking Current	2			mA	V_{OL} = 0.1VCC
Iin1	IN+, IN-, TRIGIN	Input Current			1	µA	V_{in} = VCC to GND
Iin2	PWDN, DCLK MODE, FSKEN	Input Current			10	µA	
$I_{OZ}1$	$\overline{TRIGRC}$	Output High Impedance Current			1	µA	V_{out} = VCC to GND
$I_{OZ}2$	ST/GT				5	µA	
$I_{OZ}3$	$\overline{INT}$				10	µA	
VREF	VREF	Output Voltage	0.5VCC-0.05		0.5VCC+0.05	V	No Load
RREF		Output Resistance			2	kΩ	
V_{TGT}	ST/GT	Comparator Threshold Voltage	0.5VCC-0.05		0.5VCC+0.05	V	

AC ELECTRICAL CHARACTERISTICS

DUAL TONE ALERT SIGNAL DETECTION

Parameter	Description	Min	Typ	Max	Units	Notes
F_L	Low Tone Frequency		2130		Hz	Nominal frequency
F_H	High Tone Frequency		2750		Hz	Nominal frequency
FDA	Frequency Deviation Accept	1.1%				Within this range, tones are accepted.
FDR	Frequency Deviation Reject	3.5%				Outside this range, tones are rejected.
SIGAC	Accept Signal Level per tone	-40 -37.78		-2 0.22	dBV dBm	The gain setting as in Figure 3. Production tested at 3 V ±10%, or 5 V ±10%.
SIGRJ	Reject Signal Level per tone			-46 -43.78	dBV dBm	
TA	Positive and Negative Twist Accept #			7	dB	
SNR	Signal to Noise Ratio	20			dB	Both tones have the same amplitude and at nominal frequencies. Band limited random noise 300-3400 Hz. Measurement valid only when tone is present.

Twist = 20 log (f_H amplitude / f_L amplitude).

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

GAIN ADJUSTABLE OP AMP

Parameter	Description	Min	Typ	Max	Units	Test Conditions
I_{IN}	Input Leakage Current			0.8	μA	GND ≤ V_{IN} ≤ VCC
R_{IN}	Input Resistance	15			MΩ	
V_{OS}	Input Offset Voltage			25	mV	
PSRR	Power Supply Rejection Ratio	45			dB	1kHz ripple on VCC
CMRR	Common Mode Rejection	40			dB	V_{CMmin} ≤ V_{IN} ≤ V_{CMmax}
A_{VOL}	DC Open Loop Voltage Gain	40			dB	
f_C	Unity Gain Bandwidth	0.3			MHz	
V_O	Output Voltage Swing	0.4		VCC -0.4	V	Load ≥ 50 kΩ
C_L	Maximum Capacitive Load (GS)			100	pF	
R_L	Maximum Resistive Load (GS)	50			kΩ	
V_{CM}	Common Mode Range Voltage	1.0		VCC-1.0		

FSK DETECTION

Parameter	Description	Min	Typ	Max	Units	Notes
ID	Input Detection Level	-40 -37.78 10.0		-8 -5.78 398.1	dBV dBm mVrms	Production tested at VCC =3V ±10%, or 5V ±10%. Both mark and space have the same amplitude.
TR	Transmission Rate	1188	1200	1212	baud	
FMARK	Input Frequency Detection Bell 202 '1' (mark)	1188	1200	1212	Hz	
FSPACE	Input Frequency Detection Bell 202 '0' (space)	2178	2200	2222	Hz	
FMARK	Input Frequency Detection ITU-T V.23 '1' (mark)	1280.5	1300	1319.5	Hz	
FSPACE	Input Frequency Detection ITU-T V.23 0 (space)	2068.5	2100	2131.5	Hz	
TA	Positive and Negative Twist Accept *	-10		10	dB	
SNR	Signal to Noise Ratio	20			dB	Both mark and space have the same amplitude and at nominal frequencies. Band limited random noise: 200-3400 Hz. Present only when FSK signal is present. #

* Twist = 20 log (f_H amplitude / f_L amplitude).
# BT band is 200-3400 Hz, while Bellcore band is 0-4 kHz.

Notes:
dBV = decibels above or below a reference voltage of 1 Vrms.
dBm = decibels above or below a reference power of 1 mW into 600 ohms, 0 dBm = 0.7746 Vrms.

AC TIMING CHARACTERISTICS

POWER UP/DOWN AND FSK DETECTION

Parameter	Description	Min	Typ	Max	Units	Test Conditions
t1	Power Up Time			50	ms	
t2	Power Down Time			1	ms	
t3	Input FSK to $\overline{CD}$ low delay			25	ms	
t4	Input FSK to $\overline{CD}$ high delay	8			ms	
t5	Hysteresis	8			ms	

DUAL TONE ALERT SIGNAL

Parameter	Description	Min	Typ	Max	Units	Test Conditions
t6	Alert Signal Present Detect Time	0.5		10	ms	
t7	Alert Signal Absent Detect Time	0.1		8	ms	



Figure 18. Power Up/Down Timing

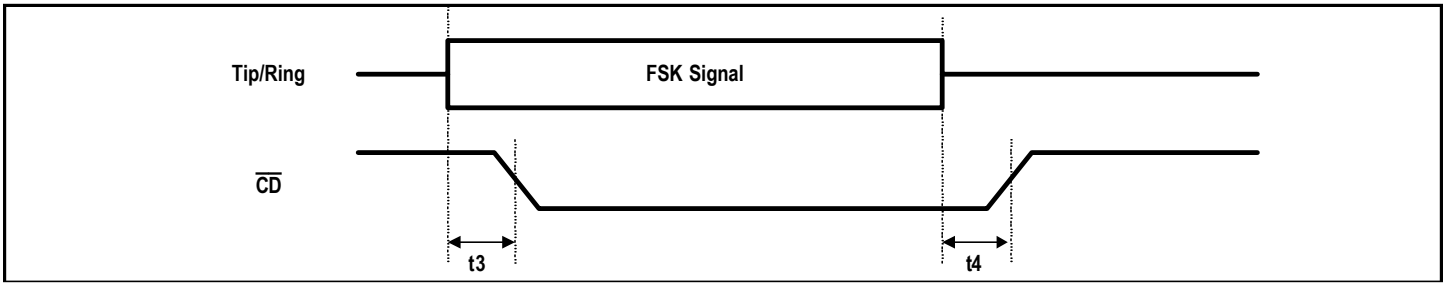


Figure 19. FSK Detection Time

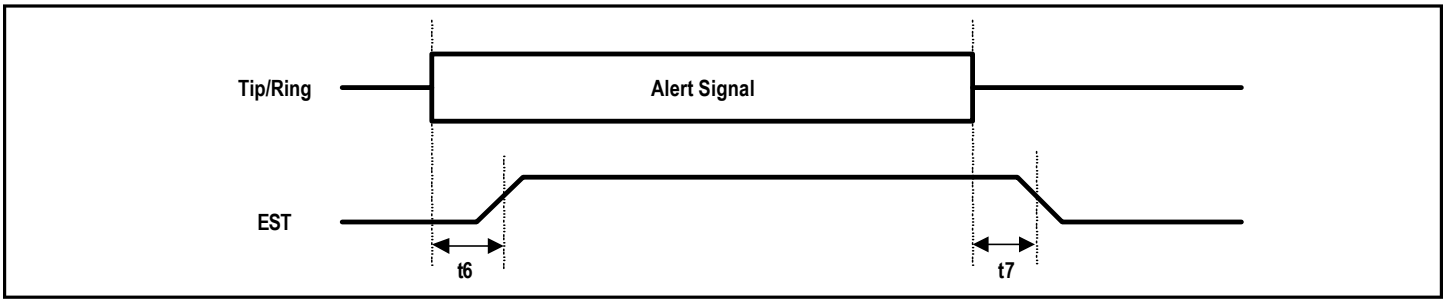


Figure 20. Dual Tone Alert Signal Detection Time

AC TIMING CHARACTERISTICS (CONTINUED)

SERIAL INTERFACE (MODE '1')

Parameter	Description	Min	Typ	Max	Units	Test Conditions
t11	DCLK Cycle Time	1			µs	
t12	DCLK High Time	0.3			µs	
t13	DCLK Low Time	0.3			µs	
t14	DCLK Rise Time			20	ns	
t15	DCLK Fall Time			20	ns	
t16	DCLK Low Setup to $\overline{DR}$	500			ns	
t17	DCLK Low Hold Time after $\overline{DR}$	500			ns	

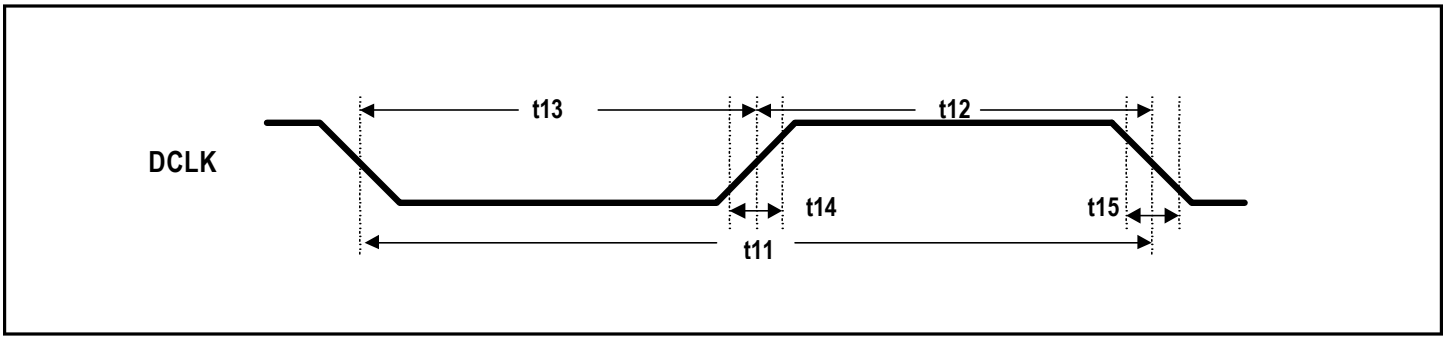


Figure 21. DCLK Timing in Mode '1'

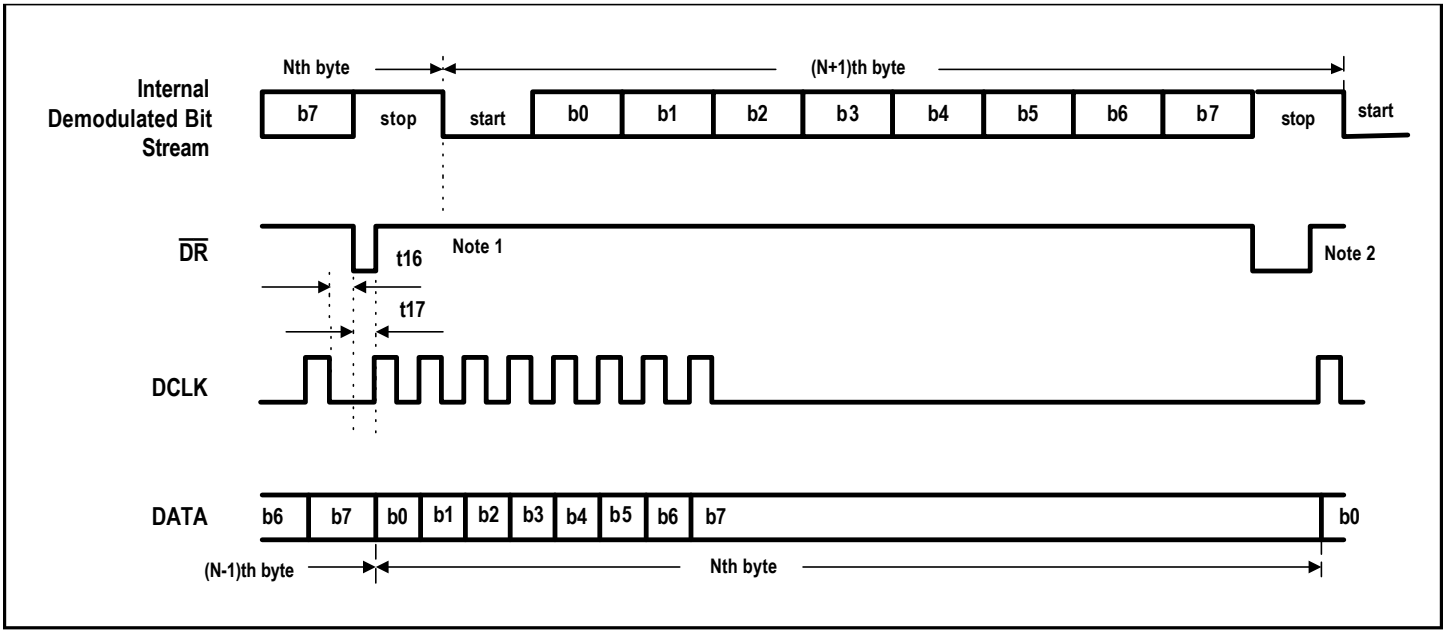


Figure 22. Serial Data Interface Timing in MODE '1'

Notes:
1. DCLK clears $\overline{DR}$.
2. $\overline{DR}$ not cleared by DCLK, low for a maximum time of 1/2 bit width.

SERIAL INTERFACE (MODE '0')

Parameter	Description	Min	Typ	Max	Units	Test Conditions
DR	Data Rate	1188	1200	1212	baud	1
t21	Input FSK to DATA Delay		1	5	ms	
t22	DATA Rise Time			200	ns	2
t23	DATA Fall Time			200	ns	2

Test conditions:
1. FSK input data at 1200 ± 12 buad.
2. Load of 50 pF.

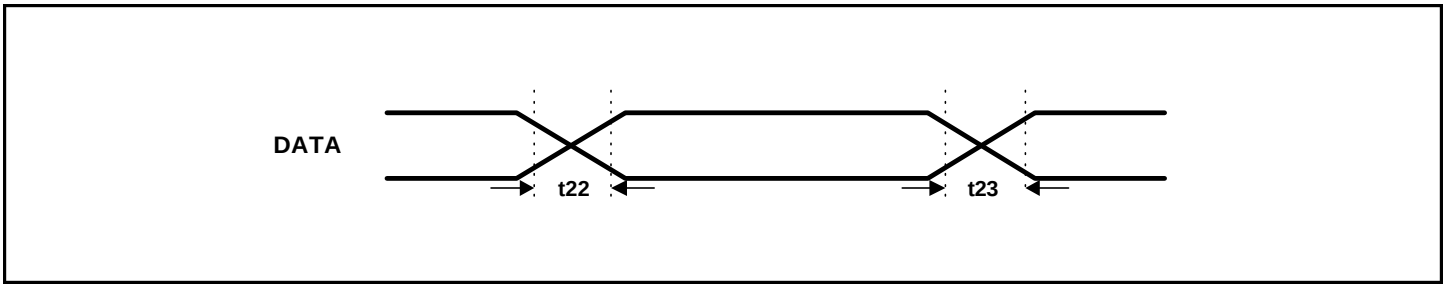


Figure 23. DATA Output Timing in Mode '0'

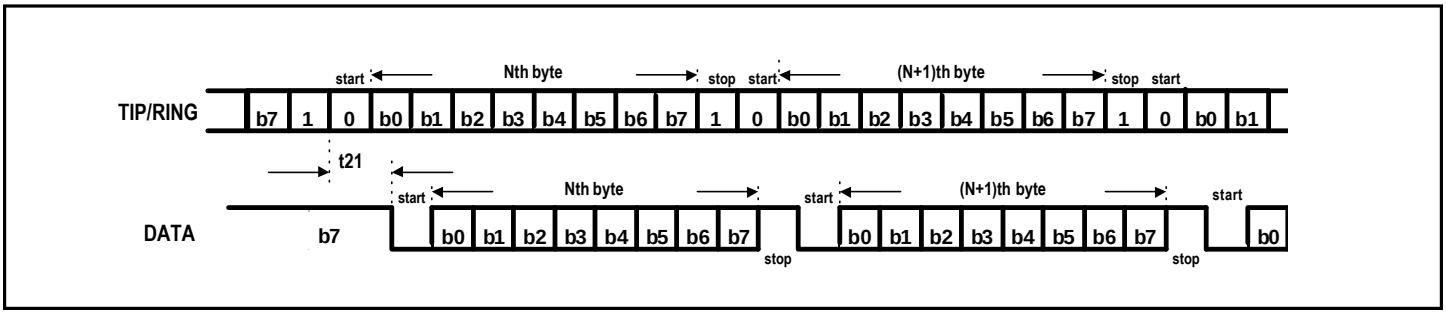


Figure 24. Serial Data Interface Timing in MODE '0'

PHYSICAL DIMENSIONS in Millimeters

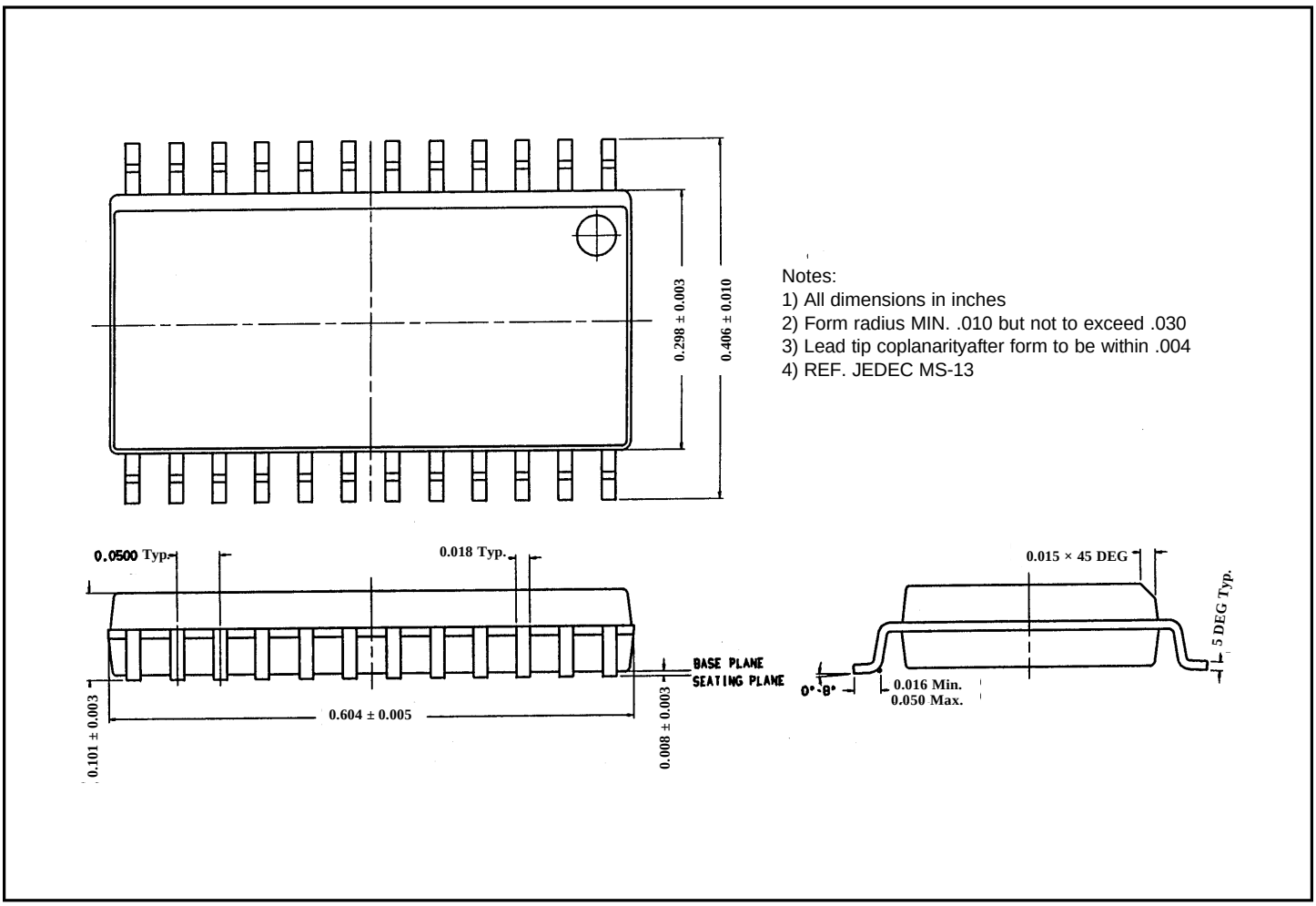


Figure 25. NW6003-XS 24 Pin SOIC Package Diagram

CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com

for Tech Support:
408-330-1552
email: telecomhelp@idt.com