



ARM Cortex™-M0
32-BIT MICROCONTROLLER

NuMicro™ Family
NUC140 Product Brief

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1 GENERAL DESCRIPTION

The NuMicro™ NUC100 Series is 32-bit microcontrollers with embedded ARM® Cortex™-M0 core for industrial control and applications which need rich communication interfaces. The Cortex™-M0 is the newest ARM® embedded processor with 32-bit performance and at a cost equivalent to traditional 8-bit microcontroller. NuMicro™ NUC100 Series includes NUC100, NUC120, NUC130 and NUC140 product line.

The NuMicro™ NUC140 Connectivity Line with USB 2.0 full-speed and CAN functions embeds Cortex™-M0 core running up to 50 MHz with 32K/64K/128K-byte embedded flash, 4K/8K/16K-byte embedded SRAM, and 4K-byte loader ROM for the ISP.. It also equips with plenty of peripheral devices, such as Timers, Watchdog Timer, RTC, PDMA, UART, SPI, I²C, I²S, PWM Timer, GPIO, LIN, CAN, PS/2, USB 2.0 FS Device, 12-bit ADC, Analog Comparator, Low Voltage Reset Controller and Brown-out Detector.

Product Line	UART	SPI	I ² C	USB	LIN	CAN	PS/2	I ² S
NUC100	•	•	•				•	•
NUC120	•	•	•	•			•	•
NUC130	•	•	•		•	•	•	•
NUC140	•	•	•	•	•	•	•	•

Table 1-1 Connectivity Supported Table

2 FEATURES

The equipped features are dependent on the product line and their sub products.

2.1 NuMicro™ NUC140 Features – Connectivity Line

- Core
 - ARM® Cortex™-M0 core runs up to 50 MHz
 - One 24-bit system timer
 - Supports low power sleep mode
 - Single-cycle 32-bit hardware multiplier
 - NVIC for the 32 interrupt inputs, each with 4-levels of priority
 - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Build-in LDO for wide operating voltage ranges from 2.5 V to 5.5 V
- Flash Memory
 - 32K/64K/128K bytes Flash for program code
 - 4KB flash for ISP loader
 - Support In-system program (ISP) application code update
 - 512 byte page erase for flash
 - Configurable data flash address and size for 128KB system, fixed 4KB data flash for the 32KB and 64KB system
 - Support 2 wire ICP update through SWD/ICE interface
 - Support fast parallel programming mode by external programmer
- SRAM Memory
 - 4K/8K/16K bytes embedded SRAM
 - Support PDMA mode
- PDMA (Peripheral DMA)
 - Support 9 channels PDMA for automatic data transfer between SRAM and peripherals
- Clock Control
 - Flexible selection for different applications
 - Built-in 22.1184 MHz high speed OSC for system operation
 - ◆ Trimmed to $\pm 1\%$ at $+25\text{ }^{\circ}\text{C}$ and $V_{DD} = 5\text{ V}$
 - ◆ Trimmed to $\pm 3\%$ at $-40\text{ }^{\circ}\text{C} \sim +85\text{ }^{\circ}\text{C}$ and $V_{DD} = 2.5\text{ V} \sim 5.5\text{ V}$
 - Built-in 10 KHz low speed OSC for Watchdog Timer and Wake-up operation
 - Support one PLL, up to 50 MHz, for high performance system operation
 - External 4~24 MHz high speed crystal input for USB and precise timing operation
 - External 32.768 kHz low speed crystal input for RTC function and low power system operation
- GPIO
 - Four I/O modes:
 - ◆ Quasi bi-direction
 - ◆ Push-Pull output
 - ◆ Open-Drain output
 - ◆ Input only with high impedance
 - TTL/Schmitt trigger input selectable
 - I/O pin can be configured as interrupt source with edge/level setting
 - High driver and high sink IO mode support



- Timer
 - Support 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
 - Independent clock source for each timer
 - Provides one-shot, periodic, toggle and continuous counting operation modes
 - Support event counting function
 - Support input capture function
- Watchdog Timer
 - Multiple clock sources
 - 8 selectable time out period from 1.6ms ~ 26.0sec (depends on clock source)
 - WDT can wake-up from power down or idle mode
 - Interrupt or reset selectable on watchdog time-out
- RTC
 - Support software compensation by setting frequency compensate register (FCR)
 - Support RTC counter (second, minute, hour) and calendar counter (day, month, year)
 - Support Alarm registers (second, minute, hour, day, month, year)
 - Selectable 12-hour or 24-hour mode
 - Automatic leap year recognition
 - Support periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
 - Support wake-up function
- PWM/Capture
 - Built-in up to four 16-bit PWM generators provide eight PWM outputs or four complementary paired PWM outputs
 - Each PWM generator equipped with one clock source selector, one clock divider, one 8-bit prescaler and one Dead-Zone generator for complementary paired PWM
 - Up to eight 16-bit digital Capture timers (shared with PWM timers) provide eight rising/falling capture inputs
 - Support Capture interrupt
- UART
 - Up to three UART controllers
 - UART ports with flow control (TXD, RXD, CTS and RTS)
 - UART0 with 64-byte FIFO is for high speed
 - UART1/2(optional) with 16-byte FIFO for standard device
 - Support IrDA (SIR) and LIN function
 - Support RS-485 9-bit mode and direction control.
 - Programmable baud-rate generator up to 1/16 system clock
 - Support PDMA mode
- SPI
 - Up to four sets of SPI controller
 - Master up to 32 MHz, and Slave up to 10 MHz (chip working @ 5V)
 - Support SPI master/slave mode
 - Full duplex synchronous serial data transfer
 - Variable length of transfer data from 1 to 32 bits
 - MSB or LSB first data transfer
 - Rx and Tx on both rising or falling edge of serial clock independently
 - 2 slave/device select lines when it is as the master, and 1 slave/device select line when it is as the slave
 - Support byte suspend mode in 32-bit transmission
 - Support PDMA mode
 - Support three wire, no slave select signal, bi-direction interface



- I²C

- Up to two sets of I²C device
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- Programmable clocks allow versatile rate control
- Support multiple address recognition (four slave address with mask option)

- I²S

- Interface with external audio CODEC
- Operate as either master or slave mode
- Capable of handling 8-, 16-, 24- and 32-bit word sizes
- Mono and stereo audio data supported
- I²S and MSB justified data format supported
- Two 8 word FIFO data buffers are provided, one for transmit and one for receive
- Generates interrupt requests when buffer levels cross a programmable boundary
- Support two DMA requests, one for transmit and one for receive

- CAN 2.0

- Supports CAN protocol version 2.0 part A and B
- Bit rates up to 1M bit/s
- 32 Message Objects
- Each Message Object has its own identifier mask
- Programmable FIFO mode (concatenation of Message Object)
- Maskable interrupt
- Disabled Automatic Re-transmission mode for Time Triggered CAN applications
- Support power down wake-up function

- PS/2 Device Controller

- Host communication inhibit and request to send detection
- Reception frame error detection
- Programmable 1 to 16 bytes transmit buffer to reduce CPU intervention
- Double buffer for data reception
- S/W override bus

- USB 2.0 Full-Speed Device

- One set of USB 2.0 FS Device 12Mbps
- On-chip USB Transceiver
- Provide 1 interrupt source with 4 interrupt events
- Support Control, Bulk In/Out, Interrupt and Isochronous transfers
- Auto suspend function when no bus signaling for 3 ms
- Provide 6 programmable endpoints
- Include 512 Bytes internal SRAM as USB buffer
- Provide remote wake-up capability

- EBI (External bus interface) support (100-pin and 64-pin Package Only)

- Accessible space: 64KB in 8-bit mode or 128KB in 16-bit mode
- Support 8-/16-bit data width

- Support byte write in 16-bit data width mode
- ADC
 - 12-bit SAR ADC with 700K SPS
 - Up to 8-ch single-end input or 4-ch differential input
 - Single scan/single cycle scan/continuous scan
 - Each channel with individual result register
 - Scan on enabled channels
 - Threshold voltage detection
 - Conversion start by software programming or external input
 - Support PDMA Mode
- Analog Comparator
 - Up to two analog comparators
 - External input or internal bandgap voltage selectable at negative node
 - Interrupt when compare result change
 - Power down wake-up
- One built-in temperature sensor with 1°C resolution
- Brown-Out detector
 - With 4 levels: 4.5 V/3.8 V/2.7 V/2.2 V
 - Support Brown-Out Interrupt and Reset option
- Low Voltage Reset
 - Threshold voltage levels: 2.0 V
- Operating Temperature: -40°C~85°C
- Packages:
 - All Green package (RoHS)
 - LQFP 100-pin / 64-pin / 48-pin

3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 NuMicro™ NUC140 Products Selection Guide

3.1.1 NuMicro™ NUC140 Connectivity Line Selection Guide

Part number	APROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer	Connectivity						I ² S	Comp.	PWM	ADC	RTC	EBI	ISP ICP	Package
							UART	SPI	I ² C	USB	LIN	CAN								
NUC140LC1CN	32 KB	4 KB	4 KB	4 KB	up to 31	4x32-bit	2	1	2	1	2	1	1	1	4	8x12-bit	v	-	v	LQFP48
NUC140LD2CN	64 KB	8 KB	4 KB	4 KB	up to 31	4x32-bit	2	1	2	1	2	1	1	1	4	8x12-bit	v	-	v	LQFP48
NUC140LE3CN	128 KB	16 KB	Definable	4 KB	up to 31	4x32-bit	2	1	2	1	2	1	1	1	4	8x12-bit	v	-	v	LQFP48
NUC140RC1CN	32 KB	4 KB	4 KB	4 KB	up to 45	4x32-bit	3	2	2	1	2	1	1	2	4	8x12-bit	v	v	v	LQFP64
NUC140RD2CN	64 KB	8 KB	4 KB	4 KB	up to 45	4x32-bit	3	2	2	1	2	1	1	2	4	8x12-bit	v	v	v	LQFP64
NUC140RE3CN	128 KB	16 KB	Definable	4 KB	up to 45	4x32-bit	3	2	2	1	2	1	1	2	4	8x12-bit	v	v	v	LQFP64
NUC140VE3CN	128 KB	16 KB	Definable	4 KB	up to 76	4x32-bit	3	4	2	1	2	1	1	2	8	8x12-bit	v	v	v	LQFP100

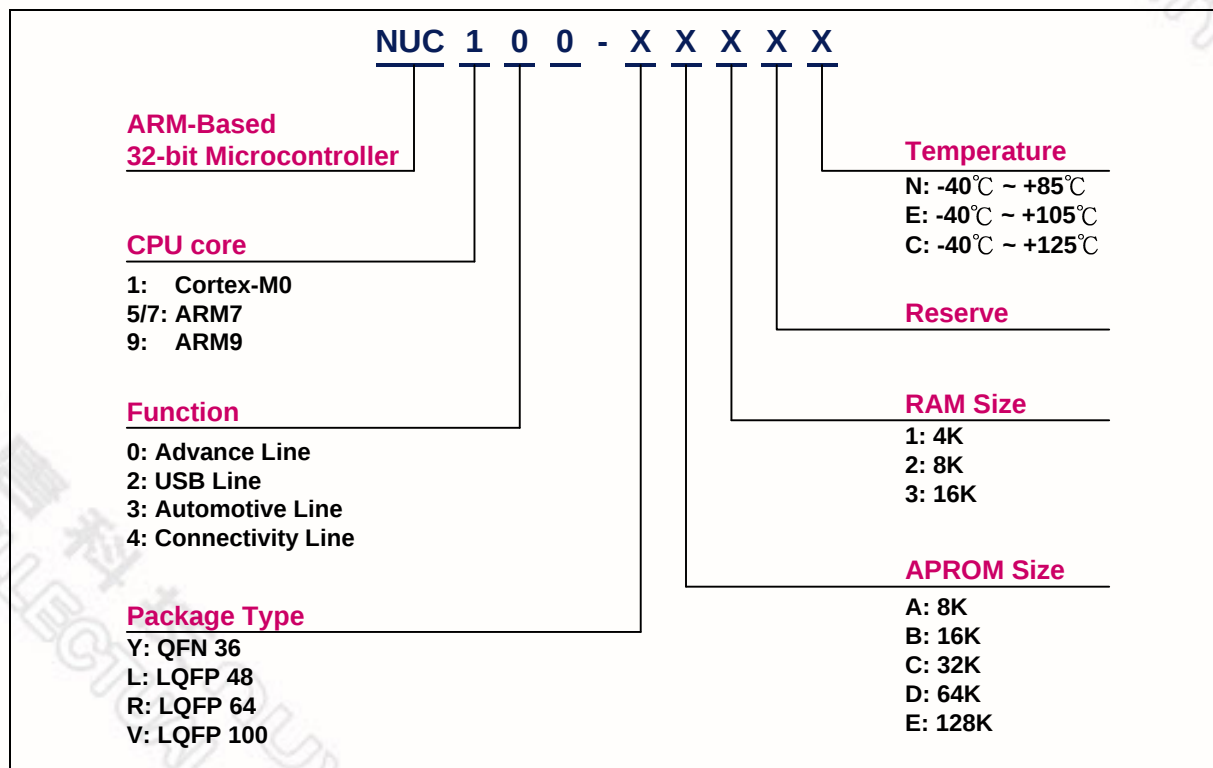


Figure 3-1 NuMicro™ NUC100 Series selection code

3.2 Pin Configuration

3.2.1 NuMicro™ NUC140 Pin Diagram

3.2.1.1 NuMicro™ NUC140 LQFP 100 pin

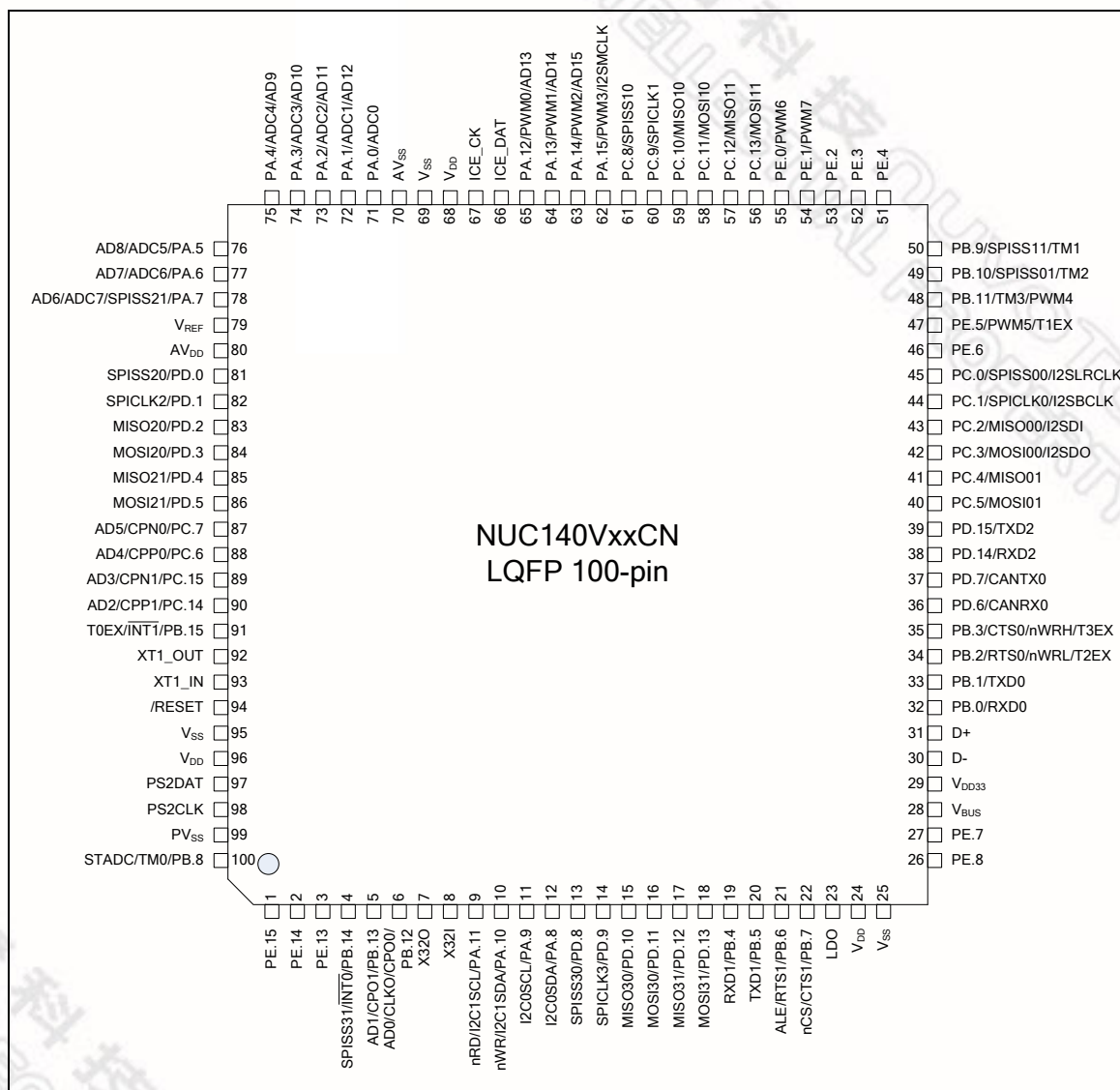


Figure 3-2 NuMicro™ NUC140 LQFP 100-pin Pin Diagram

3.2.1.2 NuMicro™ NUC140 LQFP 64 pin

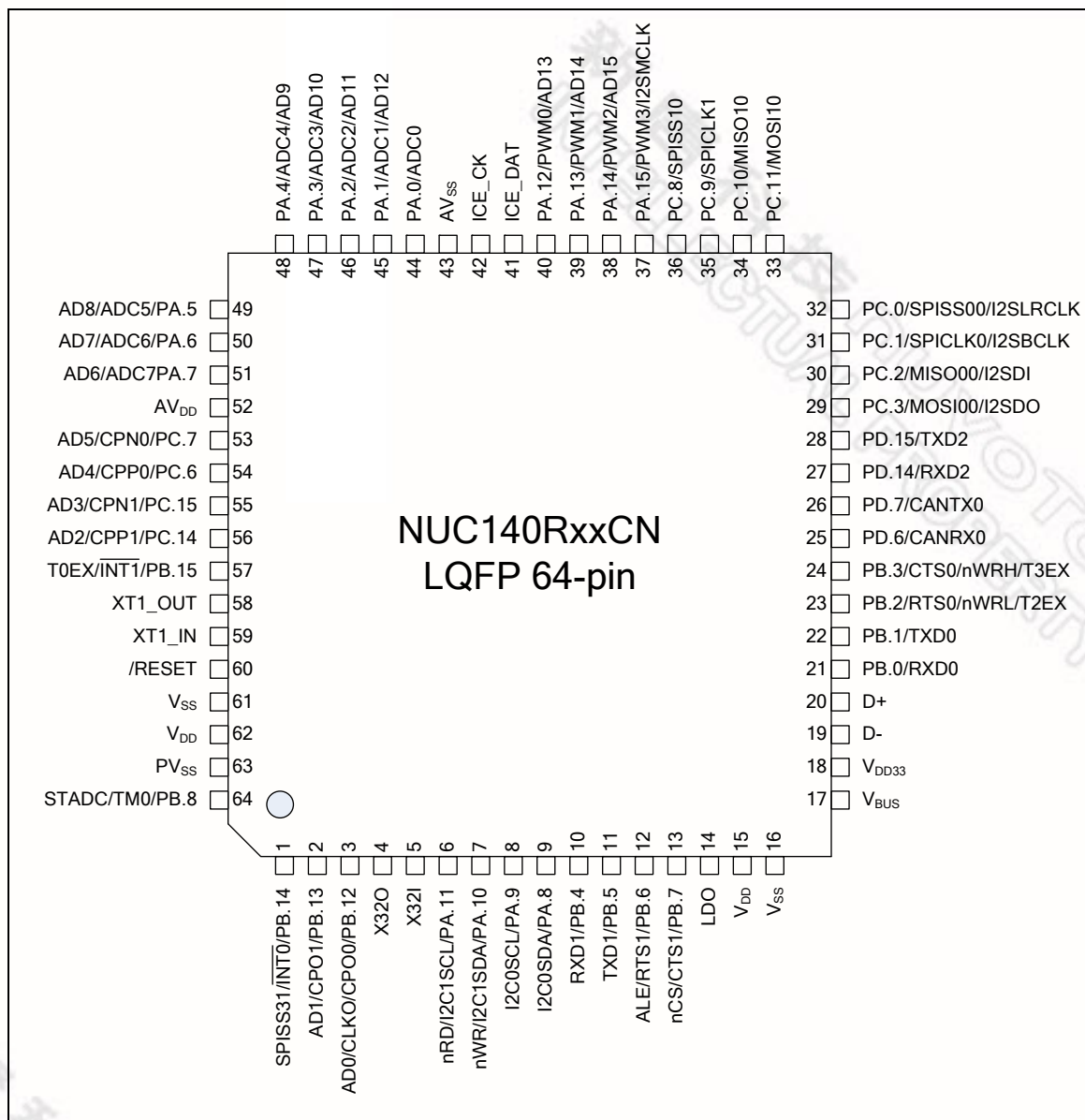


Figure 3-3 NuMicro™ NUC140 LQFP 64-pin Pin Diagram

3.2.1.3 NuMicro™ NUC140 LQFP 48 pin

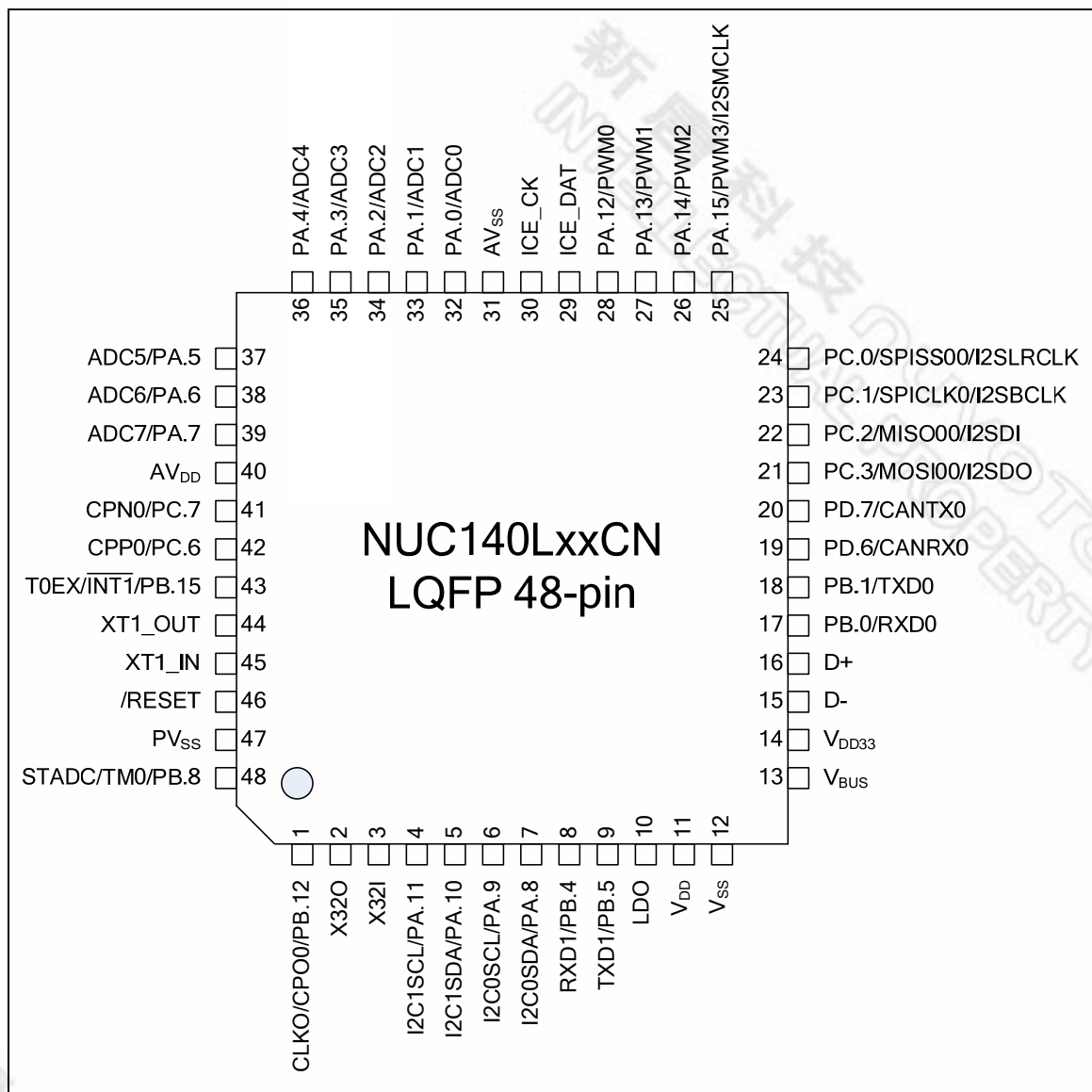


Figure 3-4 NuMicro™ NUC140 LQFP 48-pin Pin Diagram



4 BLOCK DIAGRAM

4.1 NuMicro™NUC140 Block Diagram

4.1.1 NuMicro™ NUC140 Block Diagram

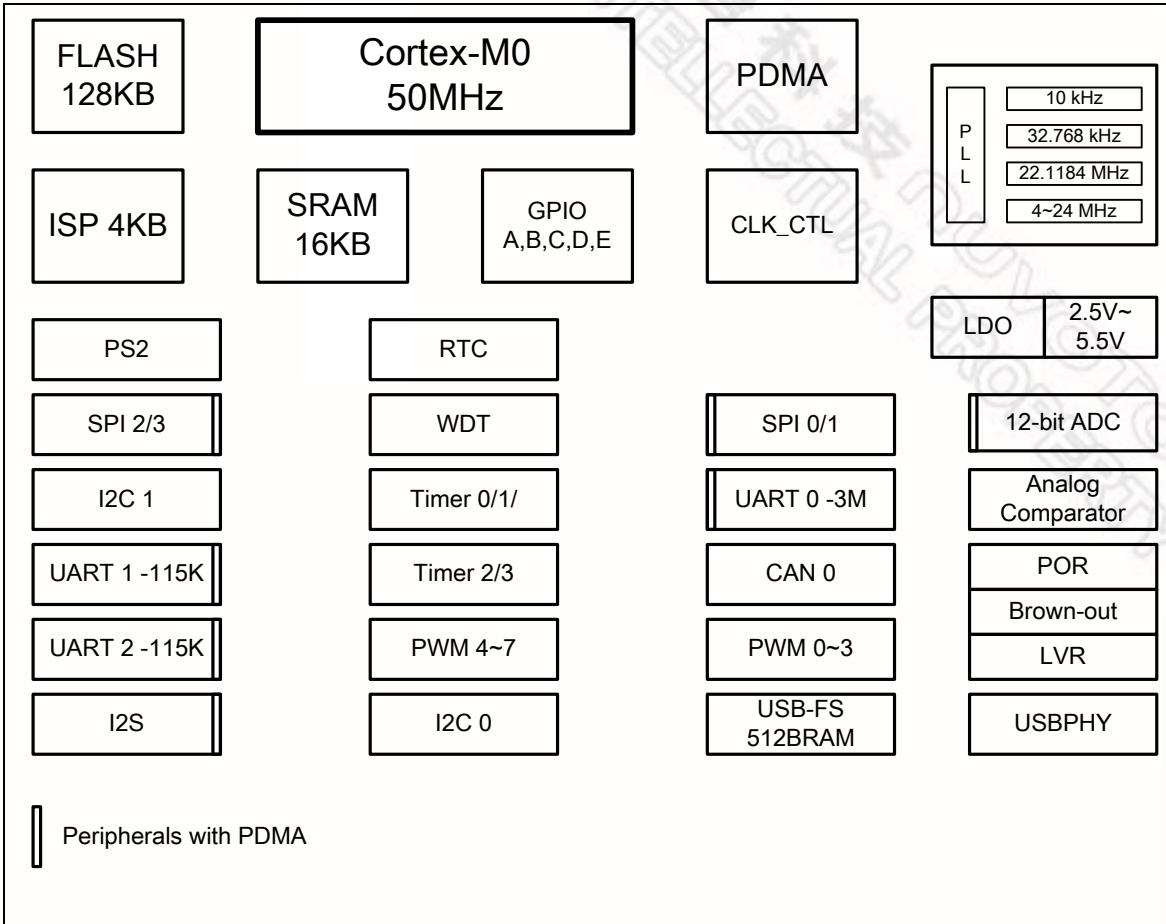


Figure 4-1 NuMicro™ NUC140 Block Diagram

5 ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN.	MAX	UNIT
DC Power Supply	$V_{DD}-V_{SS}$	-0.3	+7.0	V
Input Voltage	V_{IN}	$V_{SS}-0.3$	$V_{DD}+0.3$	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	TA	-40	+85	°C
Storage Temperature	TST	-55	+150	°C
Maximum Current into V_{DD}		-	120	mA
Maximum Current out of V_{SS}			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the life and reliability of the device.

5.2 DC Electrical Characteristics

5.2.1 NuMicro™ NUC130/NUC140 DC Electrical Characteristics

($V_{DD}-V_{SS}=3.3\text{ V}$, $T_A = 25^\circ\text{C}$, $F_{OSC} = 50\text{ MHz}$ unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation voltage	V_{DD}	2.5		5.5	V	$V_{DD} = 2.5\text{ V} \sim 5.5\text{ V}$ up to 50 MHz
Power Ground	V_{SS} AV_{SS}	-0.3			V	
LDO Output Voltage	V_{LDO}	-10%	2.5	+10%	V	$V_{DD} > 2.7\text{ V}$
Analog Operating Voltage	AV_{DD}	0		V_{DD}	V	
Analog Reference Voltage	V_{ref}	0		AV_{DD}	V	
Operating Current Normal Run Mode @ 50 MHz	I_{DD1}		51		mA	$V_{DD} = 5.5\text{ V}@50\text{ MHz}$, enable all IP and PLL, XTAL=12 MHz
	I_{DD2}		25		mA	$V_{DD} = 5.5\text{ V}@50\text{ MHz}$, disable all IP and enable PLL, XTAL=12 MHz
	I_{DD3}		48		mA	$V_{DD} = 3\text{ V}@50\text{ MHz}$, enable all IP and PLL, XTAL=12 MHz
	I_{DD4}		23		mA	$V_{DD} = 3\text{ V}@50\text{ MHz}$, disable all IP and enable PLL, XTAL=12 MHz
Operating Current Normal Run Mode @ 12 MHz	I_{DD5}		19		mA	$V_{DD} = 5.5\text{ V}@12\text{ MHz}$, enable all IP and disable PLL, XTAL=12 MHz
	I_{DD6}		7		mA	$V_{DD} = 5.5\text{ V}@12\text{ MHz}$, disable all IP and disable PLL, XTAL=12 MHz
	I_{DD7}		17		mA	$V_{DD} = 3\text{ V}@12\text{ MHz}$, enable all IP and disable PLL, XTAL=12 MHz

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
	I _{DD8}		6		mA	V _{DD} = 3 V@12 MHz, disable all IP and disable PLL, XTAL=12 MHz
Operating Current Normal Run Mode @ 4 MHz	I _{DD9}		11		mA	V _{DD} = 5 V@4 MHz, enable all IP and disable PLL, XTAL=4 MHz
	I _{DD10}		3		mA	V _{DD} = 5 V@4 MHz, disable all IP and disable PLL, XTAL=4 MHz
	I _{DD11}		10		mA	V _{DD} = 3 V@4 MHz, enable all IP and disable PLL, XTAL=4 MHz
	I _{DD12}		2.5		mA	V _{DD} = 3 V@4 MHz, disable all IP and disable PLL, XTAL=4 MHz
Operating Current Idle Mode @ 50 MHz	I _{IDLE1}		35		mA	V _{DD} = 5.5 V@50 MHz, enable all IP and PLL, XTAL=12 MHz
	I _{IDLE2}		15		mA	V _{DD} = 5.5 V@50 MHz, disable all IP and enable PLL, XTAL=12 MHz
	I _{IDLE3}		33		mA	V _{DD} = 3 V@50 MHz, enable all IP and PLL, XTAL=12 MHz
	I _{IDLE4}		13		mA	V _{DD} = 3 V@50 MHz, disable all IP and enable PLL, XTAL=12 MHz
Operating Current Idle Mode @ 12 MHz	I _{IDLE5}		10		mA	V _{DD} = 5.5 V@12 MHz, enable all IP and disable PLL, XTAL=12 MHz
	I _{IDLE6}		4.5		mA	V _{DD} = 5.5 V@12 MHz, disable all IP and disable PLL, XTAL=12 MHz
	I _{IDLE7}		9		mA	V _{DD} = 3 V@12 MHz, enable all IP and disable PLL, XTAL=12 MHz

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
	I _{IDLE8}		3.5		mA	V _{DD} = 3 V@12 MHz, disable all IP and disable PLL, XTAL=12 MHz
Operating Current Idle Mode @ 4 MHz	I _{IDLE9}		4		mA	V _{DD} = 5 V@4 MHz, enable all IP and disable PLL, XTAL=4 MHz
	I _{IDLE10}		2.5		mA	V _{DD} = 5 V@4 MHz, disable all IP and disable PLL, XTAL=4 MHz
	I _{IDLE11}		3.5		mA	V _{DD} = 3 V@4 MHz, enable all IP and disable PLL, XTAL=4 MHz
	I _{IDLE12}		1.5		mA	V _{DD} = 3 V@4 MHz, disable all IP and disable PLL, XTAL=4 MHz
Standby Current Power down Mode	I _{PWD1}		12		μA	V _{DD} = 5.5 V, RTC OFF, No load @ Disable BOV function
	I _{PWD2}		9		μA	V _{DD} = 3.3 V, RTC OFF, No load @ Disable BOV function
	I _{PWD3}				μA	V _{DD} = 5.5 V, RTC run, No load @ Disable BOV function
	I _{PWD4}				μA	V _{DD} = 3.3 V, RTC run, No load @ Disable BOV function
Input Current PA, PB, PC, PD, PE (Quasi-bidirectional mode)	I _{IN1}		-50	-60	μA	V _{DD} = 5.5 V, V _{IN} = 0 V or V _{IN} =V _{DD}
Input Current at /RESET ^[1]	I _{IN2}	-55	-45	-30	μA	V _{DD} = 3.3 V, V _{IN} = 0.45 V
Input Leakage Current PA, PB, PC, PD, PE	I _{LK}	-2	-	+2	μA	V _{DD} = 5.5 V, 0<V _{IN} <V _{DD}
Logic 1 to 0 Transition Current PA~PE (Quasi-bidirectional mode)	I _{TL} ^[3]	-650	-	-200	μA	V _{DD} = 5.5 V, V _{IN} <2.0 V
Input Low Voltage PA, PB, PC, PD, PE (TTL input)	V _{IL1}	-0.3	-	0.8	V	V _{DD} = 4.5 V
		-0.3	-	0.6		V _{DD} = 2.5 V
Input High Voltage PA, PB, PC, PD, PE (TTL input)	V _{IH1}	2.0	-	V _{DD} +0.2	V	V _{DD} = 5.5 V
		1.5	-	V _{DD} +0.2		V _{DD} = 3.0 V
Input Low Voltage PA, PB, PC, PD, PE (Schmitt input)	V _{IL2}	-0.5	-	0.3 V _{DD}	V	

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Input High Voltage PA, PB, PC, PD, PE (Schmitt input)	V _{IH2}	0.7 V _{DD}	-	V _{DD} +0.5	V	
Hysteresis voltage of PA~PE (Schmitt input)	V _{HY}		0.2 V _{DD}		V	
Input Low Voltage XT1 ^[*2]	V _{IL3}	0	-	0.8	V	V _{DD} = 4.5 V
		0	-	0.4		V _{DD} = 3.0 V
Input High Voltage XT1 ^[*2]	V _{IH3}	3.5	-	V _{DD} +0.2	V	V _{DD} = 5.5 V
		2.4	-	V _{DD} +0.2		V _{DD} = 3.0 V
Input Low Voltage X32I ^[*2]	V _{IL4}	0	-	0.4	v	
Input High Voltage X32I ^[*2]	V _{IH4}	1.7		2.5	V	
Negative going threshold (Schmitt input), /RESET	V _{ILS}	-0.5	-	0.3 V _{DD}	V	
Positive going threshold (Schmitt input), /RESET	V _{IHS}	0.7 V _{DD}	-	V _{DD} +0.5	V	
Source Current PA, PB, PC, PD, PE (Quasi-bidirectional Mode)	I _{SR11}	-300	-370	-450	μA	V _{DD} = 4.5 V, V _S = 2.4 V
	I _{SR12}	-50	-70	-90	μA	V _{DD} = 2.7 V, V _S = 2.2 V
	I _{SR13}	-40	-60	-80	μA	V _{DD} = 2.5 V, V _S = 2.0 V
Source Current PA, PB, PC, PD, PE (Push-pull Mode)	I _{SR21}	-20	-24	-28	mA	V _{DD} = 4.5 V, V _S = 2.4 V
	I _{SR22}	-4	-6	-8	mA	V _{DD} = 2.7 V, V _S = 2.2 V
	I _{SR23}	-3	-5	-7	mA	V _{DD} = 2.5 V, V _S = 2.0 V
Sink Current PA, PB, PC, PD, PE (Quasi-bidirectional and Push-pull Mode)	I _{SK11}	10	16	20	mA	V _{DD} = 4.5 V, V _S = 0.45 V
	I _{SK12}	7	10	13	mA	V _{DD} = 2.7 V, V _S = 0.45 V
	I _{SK13}	6	9	12	mA	V _{DD} = 2.5 V, V _S = 0.45 V
Brown-Out voltage with BOV_VL [1:0] = 00b	V _{BO2.2}	2.1	2.2	2.3	V	
Brown-Out voltage with BOV_VL [1:0] = 01b	V _{BO2.7}	2.6	2.7	2.8	V	
Brown-Out voltage with BOV_VL [1:0] = 10b	V _{BO3.8}	3.6	3.8	4.0	V	
Brown-Out voltage with BOV_VL [1:0] = 11b	V _{BO4.5}	4.3	4.5	4.7	V	
Hysteresis range of BOD voltage	V _{BH}	30	-	150	mV	V _{DD} = 2.5 V~5.5 V

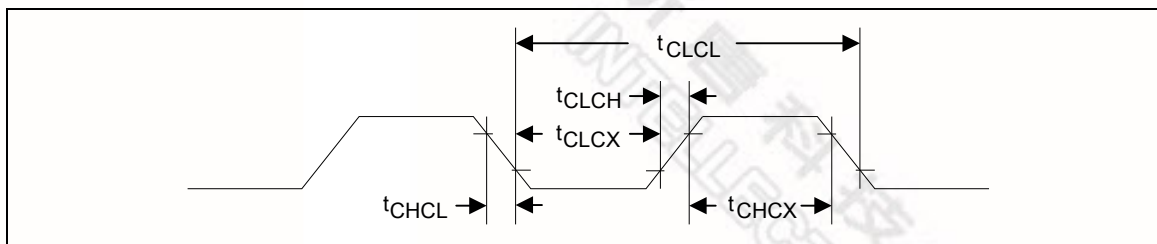
PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Bandgap voltage	V_{BG}	1.20	1.26	1.32	V	$V_{DD} = 2.5\text{ V} \sim 5.5\text{ V}$

Note:

1. /RESET pin is a Schmitt trigger input.
2. Crystal Input is a CMOS input.
3. Pins of PA, PB, PC, PD and PE can source a transition current when they are being externally driven from 1 to 0. In the condition of $V_{DD}=5.5\text{ V}$, the transition current reaches its maximum value when V_{IN} approximates to 2 V.

5.3 AC Electrical Characteristics

5.3.1 External 4~24 MHz High Speed Oscillator



Note: Duty cycle is 50%.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
t_{CHCX}	Clock High Time		20	-	-	nS
t_{CLCX}	Clock Low Time		20	-	-	nS
t_{CLCH}	Clock Rise Time		-	-	10	nS
t_{CHCL}	Clock Fall Time		-	-	10	nS

5.3.2 External 4~24 MHz High Speed Crystal

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	4	12	24	MHz
Temperature	-	-40	-	85	°C
V_{DD}	-	2.5	5	5.5	V
Operating current	12 MHz@ $V_{DD} = 5V$	-	1	-	mA

5.3.2.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R
4 MHz ~ 24 MHz	without	without	without

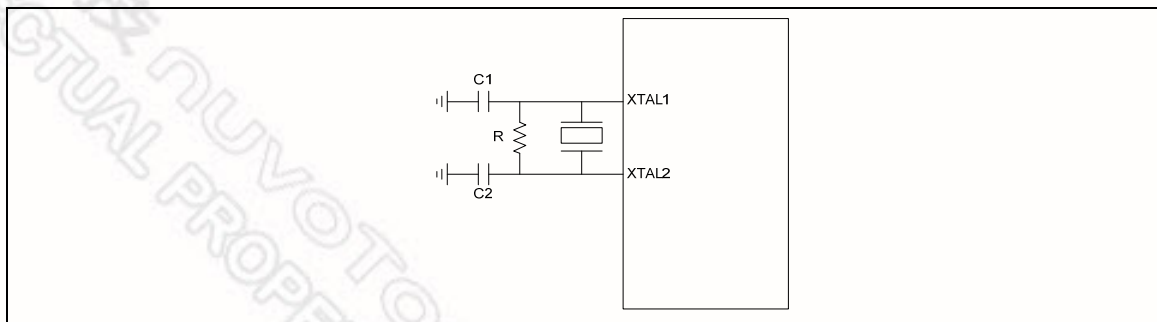


Figure 5-1 Typical Crystal Application Circuit

5.3.3 External 32.768 kHz Low Speed Crystal

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	-	32.768	-	kHz
Temperature	-	-40	-	85	°C
V _{DD}	-	2.5	-	5.5	V

5.3.4 Internal 22.1184 MHz High Speed Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage ^[1]	-	2.5	-	5.5	V
Center Frequency	-	-	22.1184	-	MHz
Calibrated Internal Oscillator Frequency	+25°C; V _{DD} =5 V	-1	-	+1	%
	-40°C ~+85°C; V _{DD} =2.5 V~5.5 V	-3	-	+3	%
Operation Current	V _{DD} =5 V	-	500	-	uA

5.3.5 Internal 10 kHz Low Speed Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage ^[1]	-	2.5	-	5.5	V
Center Frequency	-	-	10	-	kHz
Calibrated Internal Oscillator Frequency	+25°C; V _{DD} =5 V	-30	-	+30	%
	-40°C ~+85°C; V _{DD} =2.5 V~5.5 V	-50	-	+50	%

Note: Internal operation voltage comes from LDO.

5.4 Analog Characteristics

5.4.1 Specification of 12-bit SARADC

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
-	Resolution	-	-	12	Bit
DNL	Differential nonlinearity error	-	±3	-	LSB
INL	Integral nonlinearity error	-	±4	-	LSB
EO	Offset error	-	±1	10	LSB
EG	Gain error (Transfer gain)	-	1	1.005	-
-	Monotonic	Guaranteed			
FADC	ADC clock frequency ($AV_{DD}=5V/3V$)	-	-	16/8	MHz
FS	Sample rate	-	-	700	K SPS
V_{DDA}	Supply voltage	3	-	5.5	V
I_{DD}	Supply current (Avg.)	-	0.5	-	mA
I_{DDA}		-	1.5	-	mA
V_{REF}	Reference voltage	-	V_{DDA}	-	V
I_{REF}	Reference current (Avg.)	-	1	-	mA
V_{IN}	Input voltage	0	-	V_{REF}	V

5.4.2 Specification of LDO and Power management

PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
Input Voltage	2.7	5	5.5	V	V _{DD} input voltage
Output Voltage	-10%	2.5	+10%	V	V _{DD} > 2.7 V
Temperature	-40	25	85	°C	
Cbp	-	1	-	uF	Resr=1ohm

Note:

1. It is recommended that a 10uF or higher capacitor and a 100nF bypass capacitor are connected between V_{DD} and the closest V_{SS} pin of the device.
2. For ensuring power stability, a 1uF or higher capacitor must be connected between LDO pin and the closest V_{SS} pin of the device.

5.4.3 Specification of Low Voltage Reset

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation voltage	-	1.7	-	5.5	V
Quiescent current	V _{DD} =5.5 V	-	-	5	uA
Temperature	-	-40	25	85	°C
Threshold voltage	Temperature=25°C	1.7	2.0	2.3	V
	Temperature=-40°C	-	2.4	-	V
	Temperature=85°C	-	1.6	-	V
Hysteresis	-	0	0	0	V

5.4.4 Specification of Brown-Out Detector

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation voltage	-	2.5	-	5.5	V
Quiescent current	AV _{DD} =5.5 V	-	-	125	μA
Temperature	-	-40	25	85	°C
Brown-out voltage	BOV_VL[1:0]=11	4.3	4.5	4.7	V
	BOV_VL [1:0]=10	3.6	3.8	4.0	V
	BOV_VL [1:0]=01	2.6	2.7	2.8	V
	BOV_VL [1:0]=00	2.1	2.2	2.3	V
Hysteresis	-	30	-	150	mV

5.4.5 Specification of Power-On Reset (5 V)

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Temperature	-	-40	25	85	°C
Reset voltage	V+	-	2	-	V
Quiescent current	V _{in} >reset voltage	-	1	-	nA

5.4.6 Specification of Temperature Sensor

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply voltage ^[1]		2.5	-	5.5	V
Temperature		-40	-	125	°C
Current consumption		6.4	-	10.5	uA
Gain			-1.76		mV/°C
Offset	Temp=0 °C		720		mV

Note: Internal operation voltage comes from LDO.

5.4.7 Specification of Comparator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Temperature	-	-40	25	85	°C
V _{DD}	-	2.4	3	5.5	V
V _{DD} current	20 uA@V _{DD} =3 V	-	20	40	uA
Input offset voltage	-	-	5	15	mV
Output swing	-	0.1	-	V _{DD} -0.1	V
Input common mode range	-	0.1	-	V _{DD} -1.2	V
DC gain	-	-	70	-	dB
Propagation delay	@VCM=1.2 V and VDIFF=0.1 V	-	200	-	ns
Comparison voltage	20 mV@VCM=1 V 50 mV@VCM=0.1 V 50 mV@VCM=V _{DD} -1.2 @10 mV for non-hysteresis	10	20	-	mV
Hysteresis	One bit control W/O and W. hysteresis @VCM=0.4 V ~ V _{DD} -1.2 V	-	±10	-	mV
Wake-up time	@CINP=1.3 V CINN=1.2 V	-	-	2	us

5.4.8 Specification of USB PHY

5.4.8.1 USB DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{IH}	Input high (driven)		2.0			V
V _{IL}	Input low				0.8	V
V _{DI}	Differential input sensitivity	PADP-PADM	0.2			V
V _{CM}	Differential common-mode range	Includes V _{DI} range	0.8		2.5	V
V _{SE}	Single-ended receiver threshold		0.8		2.0	V
	Receiver hysteresis			200		mV
V _{OL}	Output low (driven)		0		0.3	V
V _{OH}	Output high (driven)		2.8		3.6	V
V _{CRS}	Output signal cross voltage		1.3		2.0	V
R _{PU}	Pull-up resistor		1.425		1.575	kΩ
V _{TRM}	Termination Voltage for upstream port pull up (RPU)		3.0		3.6	V
Z _{DRV}	Driver output resistance	Steady state drive*		10		Ω
C _{IN}	Transceiver capacitance	Pin to GND			20	pF

*Driver output resistance doesn't include series resistor resistance.

5.4.8.2 USB Full-Speed Driver Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T _{FR}	Rise Time	C _L =50p	4		20	ns
T _{FF}	Fall Time	C _L =50p	4		20	ns
T _{FRFF}	Rise and fall time matching	T _{FRFF} =T _{FR} /T _{FF}	90		111.11	%

5.4.8.3 USB Power Dissipation

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I _{VDDREG} (Full Speed)	V _{DDD} and V _{DDREG} Supply Current (Steady State)	Standby		50		uA
		Input mode				uA
		Output mode				uA

5.5 Flash DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
N _{endu}	Endurance		10000			cycles ^[1]
T _{ret}	Retention time	Temp=25 °C	100			year
T _{erase}	Page erase time		20		40	ms
T _{mass}	Mass erase time		40	50	60	ms
T _{prog}	Program time		35	40	55	us
V _{dd}	Supply voltage		2.25	2.5	2.75	V ^[2]
I _{dd1}	Read current				14	mA
I _{dd2}	Program/Erase current				7	mA
I _{pd}	Power down current				10	uA

1. Number of program/erase cycles.
2. V_{dd} is source from chip LDO output voltage.
3. This table is guaranteed by design, not test in production.

5.6 SPI Dynamic Characteristics

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
SPI master mode ($V_{DD} = 4.5V \sim 5.5V$, 30pF loading Capacitor)					
t_{DS}	Data setup time	4	2	-	ns
t_{DH}	Data hold time	0	-	-	ns
t_V	Data output valid time	-	7	11	ns
SPI master mode ($V_{DD} = 3.0V \sim 3.6V$, 30pF loading Capacitor)					
t_{DS}	Data setup time	5	3	-	ns
t_{DH}	Data hold time	0	-	-	ns
t_V	Data output valid time	-	13	18	ns
SPI slave mode ($V_{DD} = 4.5V \sim 5.5V$, 30pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	$2 \cdot PCLK + 4$	-	-	ns
t_V	Data output valid time	-	$2 \cdot PCLK + 11$	$2 \cdot PCLK + 19$	ns
SPI slave mode ($V_{DD} = 3.0V \sim 3.6V$, 30pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	$2 \cdot PCLK + 6$	-	-	ns
t_V	Data output valid time	-	$2 \cdot PCLK + 19$	$2 \cdot PCLK + 25$	ns

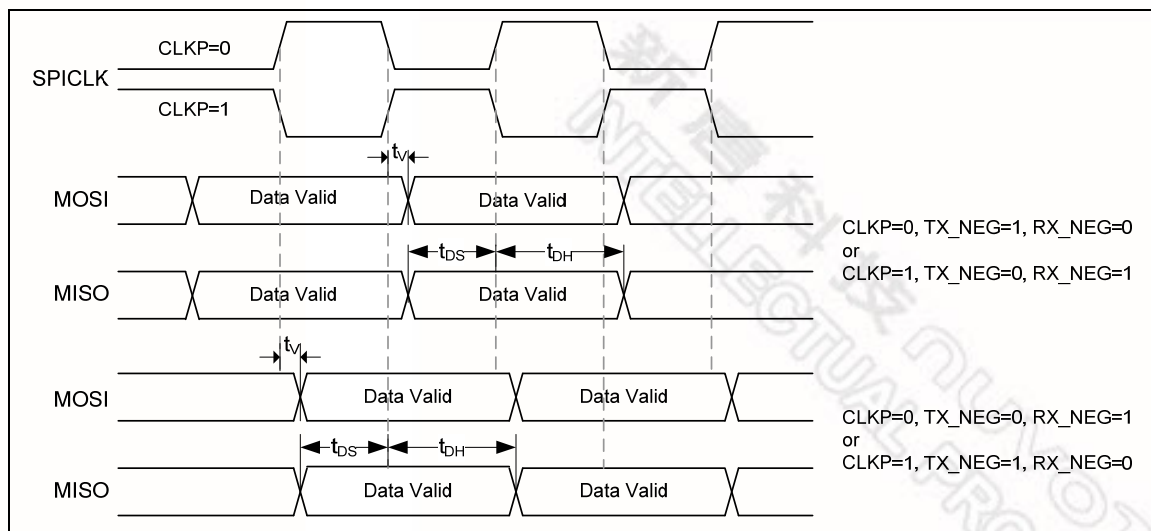


Figure 5-2 SPI Master dynamic characteristics timing

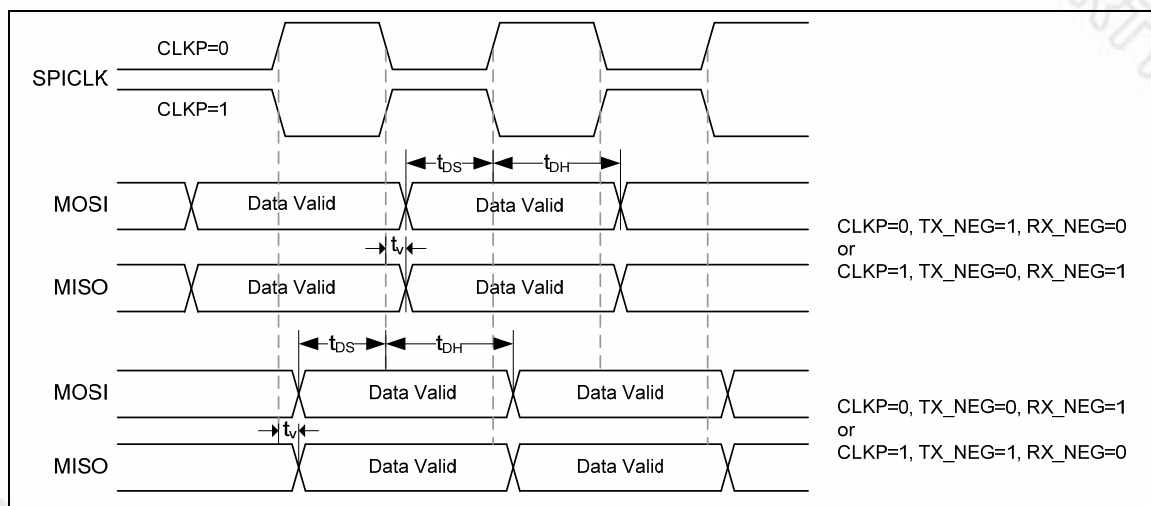
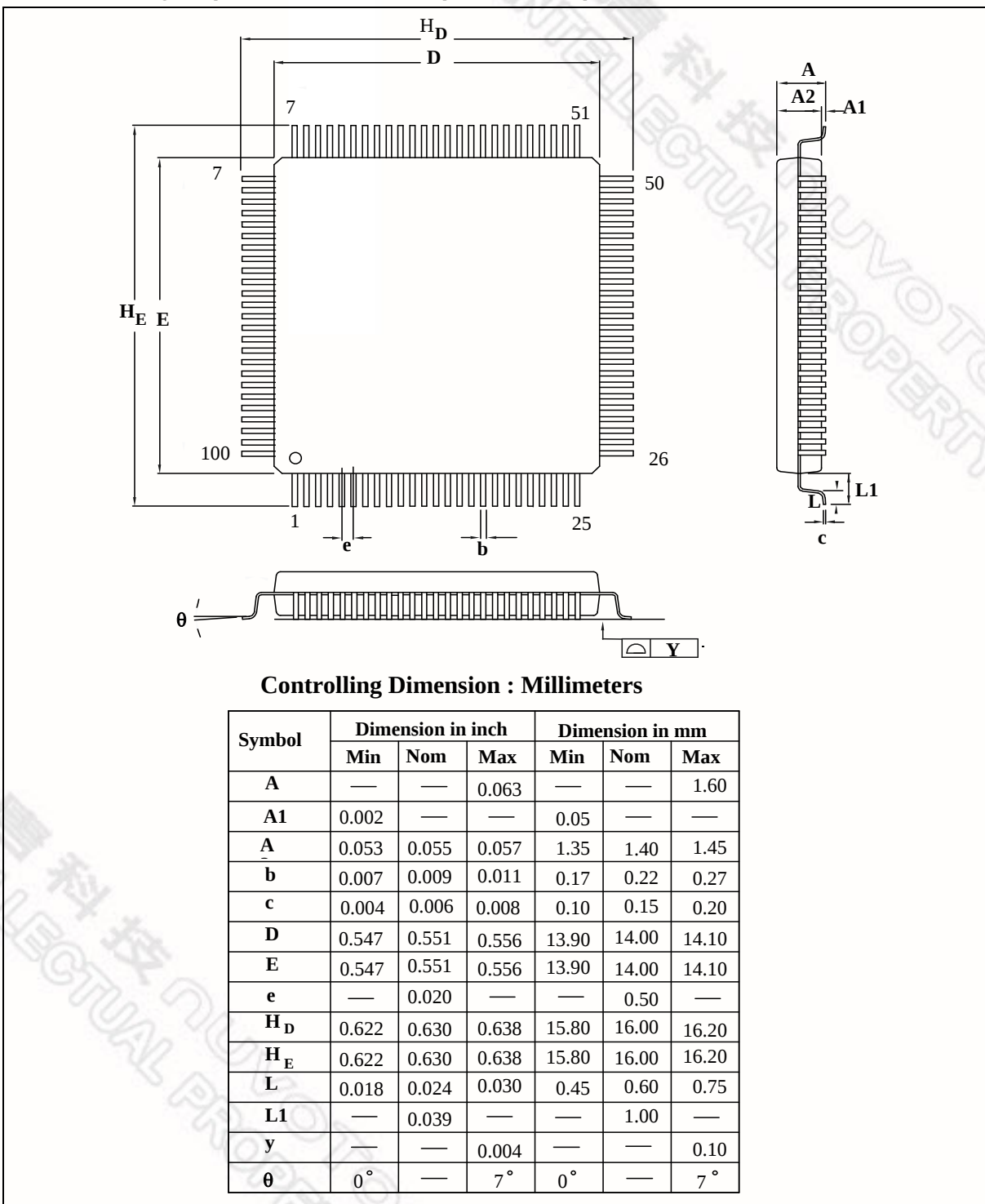


Figure 5-3 SPI Slave dynamic characteristics timing

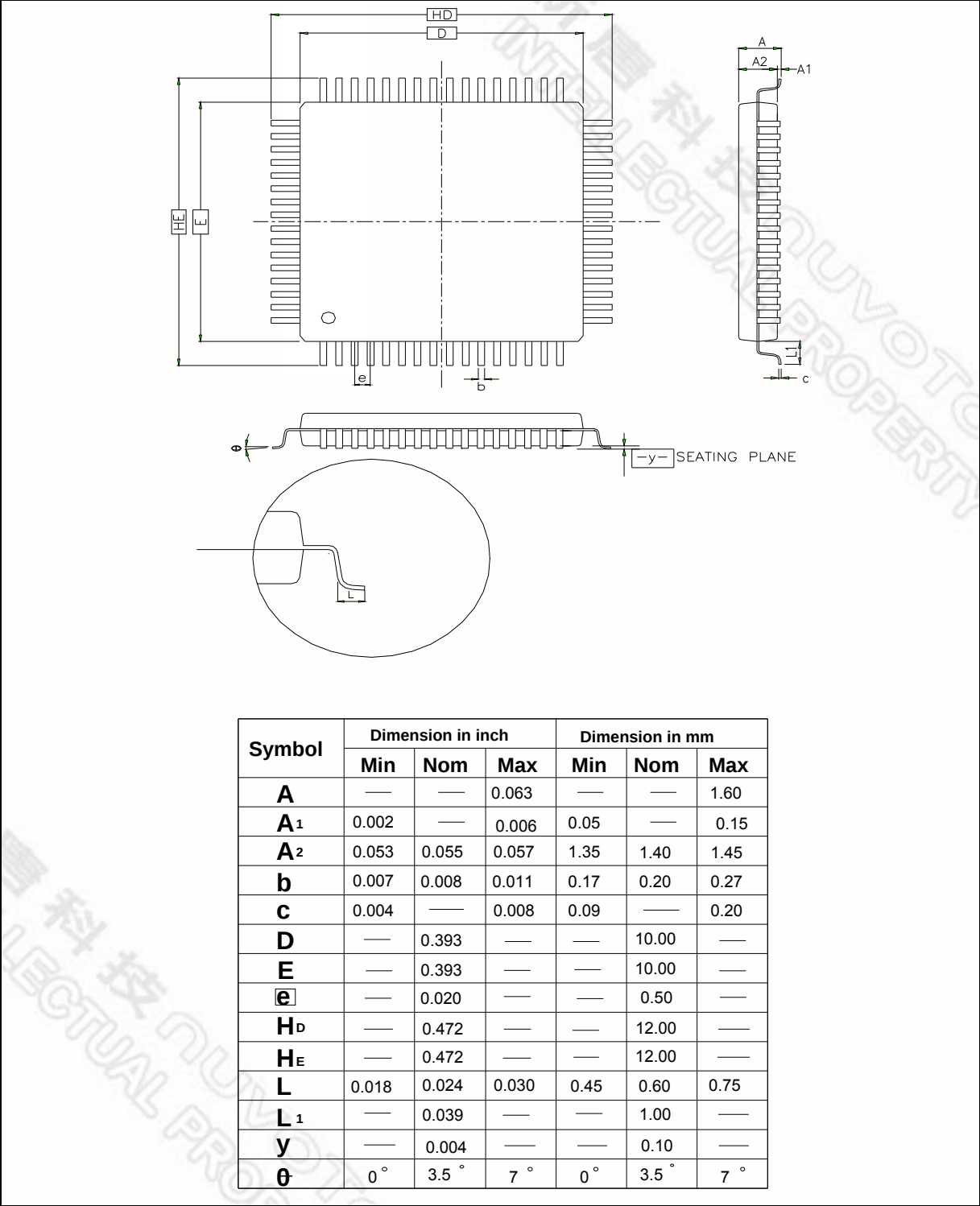
6 PACKAGE DIMENSIONS

6.1 100L LQFP (14x14x1.4 mm footprint 2.0mm)



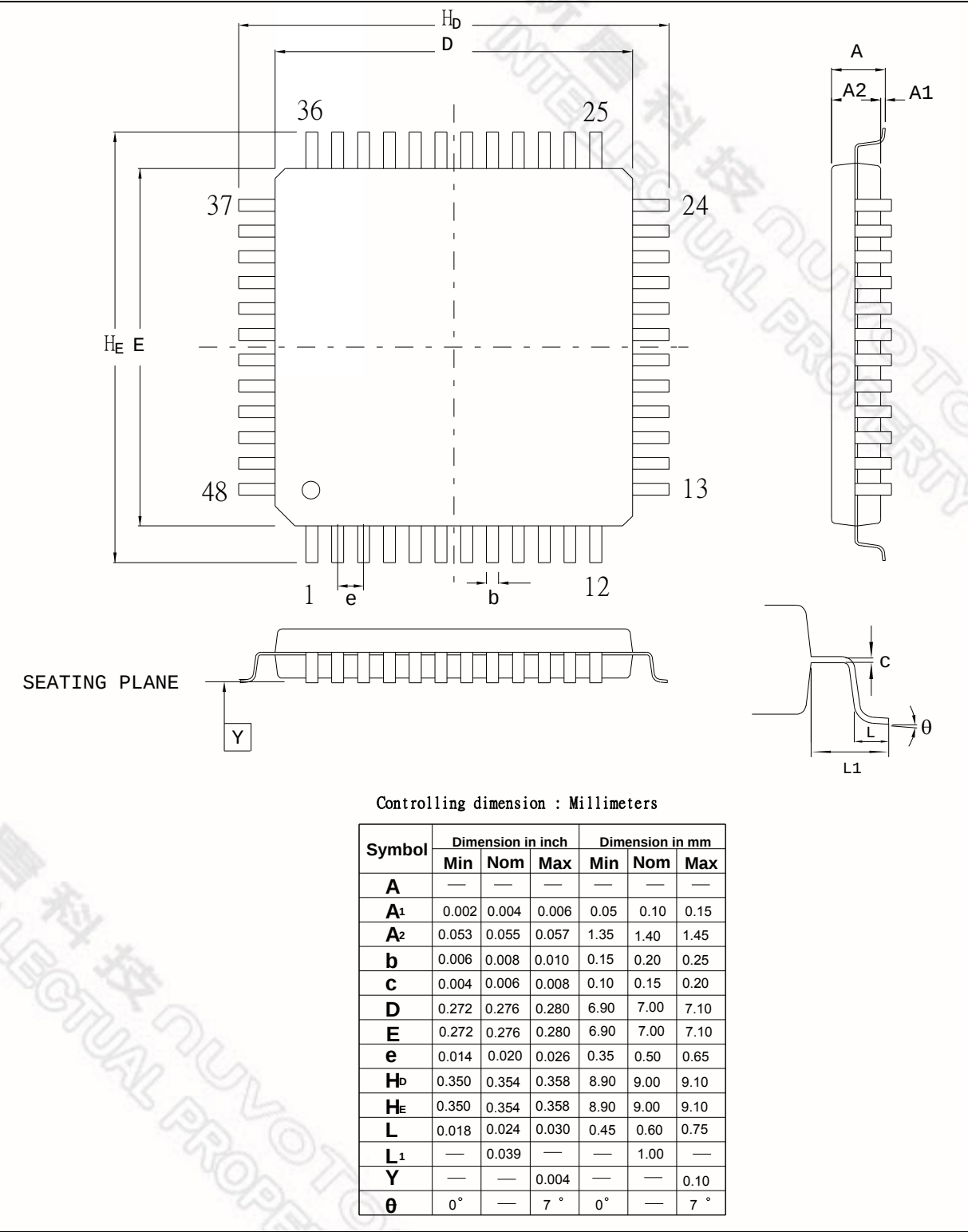


6.2 64L LQFP (10x10x1.4mm footprint 2.0 mm)





6.3 48L LQFP (7x7x1.4mm footprint 2.0mm)



7 REVISION HISTORY

VERSION	DATE	PAGE/ CHAP.	DESCRIPTION
V1.12	April 9, 2010	-	Initial issued
V1.13	May 31, 2010	4.2	Add operation current of DC characteristics
V1.14	Aug. 23, 2010	4.2	Modify operation current of DC characteristics
V2.00	Nov. 11, 2010	-	Update low density and selection table
V3.00	May 6, 2011	ALL	Revise from NUC140XXXAN or NUC140XXXBN to NUC140XXXCN Revise NUC140 selection guide Revise DC Electrical Characteristics
V3.01	June 22, 2011	-	modify temperature sensor spec Revise Pin description position for multi-function T2EX, T3EX, nRD, nWR update title of SPI Dynamic Characteristics update BOD spec
V3.02	Jan. 2, 2012	-	1. Modify ADC analog characteristic spec 2. Remove SPI FIFO mode



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