NTMFS4899NF

MOSFET – Power, Single, N-Channel, SO-8 FL
30 V, 75 A

Features
- Integrated Schottky Diode
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications
- CPU Power Delivery
- DC−DC Converters
- Low Side Switching

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

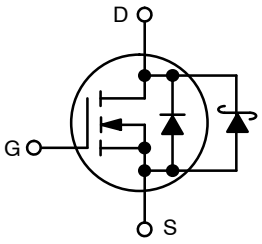
Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	30	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JA}$ (Note 1)	Steady State	T_A = 25°C	I_D	17.8	A
		T_A = 85°C		12.9	
Power Dissipation $R_{\theta JA}$ (Note 1)		T_A = 25°C	P_D	2.70	W
Continuous Drain Current $R_{\theta JA}$ ≤ 10 sec		T_A = 25°C	I_D	29.1	A
		T_A = 85°C		21	
Power Dissipation $R_{\theta JA}$, t ≤ 10 sec		T_A = 25°C	P_D	7.18	W
Continuous Drain Current $R_{\theta JA}$ (Note 2)		T_A = 25°C	I_D	10.4	A
		T_A = 85°C		7.5	
Power Dissipation $R_{\theta JA}$ (Note 2)		T_A = 25°C	P_D	0.92	W
Continuous Drain Current $R_{\theta JC}$ (Note 1)		T_C = 25°C	I_D	75	A
		T_C = 85°C		54	
Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25°C	P_D	48	W
Pulsed Drain Current	t_p=10μs	T_A = 25°C	I_{DM}	188	A
Current limited by package		T_A = 25°C	$I_{Dmaxpkg}$	90	A
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to +150	°C
Source Current (Body Diode)			I_S	46	A
Drain to Source dV/dt			dV/dt	6	V/ns

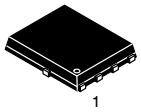
ON Semiconductor®

http://onsemi.com

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
30 V	5.0 mΩ @ 10 V	75 A
	7.5 mΩ @ 4.5 V	

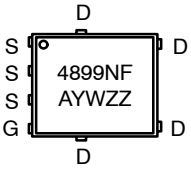
N−CHANNEL MOSFET





SO−8 FLAT LEAD CASE 488AA STYLE 1

MARKING DIAGRAM



A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping†
NTMFS4899NFT1G	SO−8FL (Pb−Free)	1500 / Tape & Reel
NTMFS4899NFT3G	SO−8FL (Pb−Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

© Semiconductor Components Industries, LLC, 2012

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter	Symbol	Value	Unit
Single Pulse Drain−to−Source Avalanche Energy (V_{DD} = 50 V, V_{GS} = 10 V, I_L = 41 A_{pk}, L = 0.1 mH, R_G = 25 Ω)	EAS	84	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case (Drain)	$R_{\theta JC}$	2.6	°C/W
Junction−to−Ambient − Steady State (Note 1)	$R_{\theta JA}$	46.3	
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	136.2	
Junction−to−Ambient − t ≤ 10 sec	$R_{\theta JA}$	17.4	

1. Surface−mounted on FR4 board using 1 sq−in pad, 1 oz Cu.
2. Surface−mounted on FR4 board using the minimum recommended pad size (50 mm^2, 1 oz Cu).

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1.0 mA		30			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				27		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 24 V	T_J = 25 °C			500	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 1.0 mA		1.5		2.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				10		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 30 A		3.9	5.0	mΩ
			I_D = 15 A		3.8		
		V_{GS} = 4.5 V	I_D = 30 A		6.0	7.5	
			I_D = 15 A		5.8		
Forward Transconductance	g_{FS}	V_{DS} = 1.5 V, I_D = 15 A			57		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 12 V			1600		pF
Output Capacitance	C_{OSS}				360		
Reverse Transfer Capacitance	C_{RSS}				165		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 15 V; I_D = 30 A			12.2		nC
Threshold Gate Charge	$Q_{G(TH)}$				1.6		
Gate−to−Source Charge	Q_{GS}				4.6		
Gate−to−Drain Charge	Q_{GD}				4.6		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 15 V, I_D = 30 A			25		nC
SWITCHING CHARACTERISTICS (Note 4)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DS} = 15 V, I_D = 15 A, R_G = 3.0 Ω			12.6		ns
Rise Time	t_r				20.3		
Turn−Off Delay Time	$t_{d(OFF)}$				20		
Fall Time	t_f				4.2		

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS (Note 4)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DS} = 15 V, I_D = 15 A, R_G = 3.0 Ω			8.8		ns
Rise Time	t_r				18.5		
Turn−Off Delay Time	$t_{d(OFF)}$				25.9		
Fall Time	t_f				2.5		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 2.0 A	T_J = 25°C		0.45	0.70	V
			T_J = 125°C		0.43		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 100 A/μs, I_S = 30 A			19		ns
Charge Time	t_a				9.2		
Discharge Time	t_b				9.8		
Reverse Recovery Charge	Q_{RR}				5.7		nC
PACKAGE PARASITIC VALUES							
Source Inductance	L_S	T_A = 25°C			0.38		nH
Drain Inductance	L_D				0.005		
Gate Inductance	L_G				1.84		
Gate Resistance	R_G				1.5	2.4	Ω

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

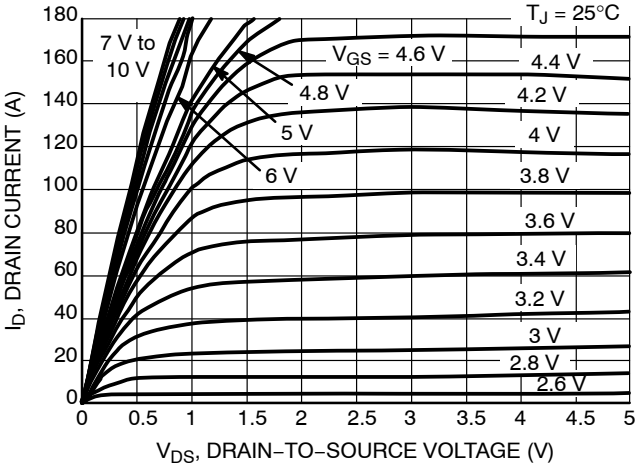


Figure 1. On−Region Characteristics

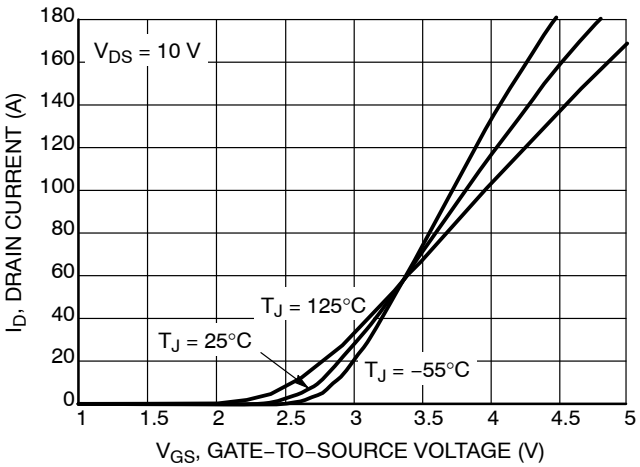


Figure 2. Transfer Characteristics

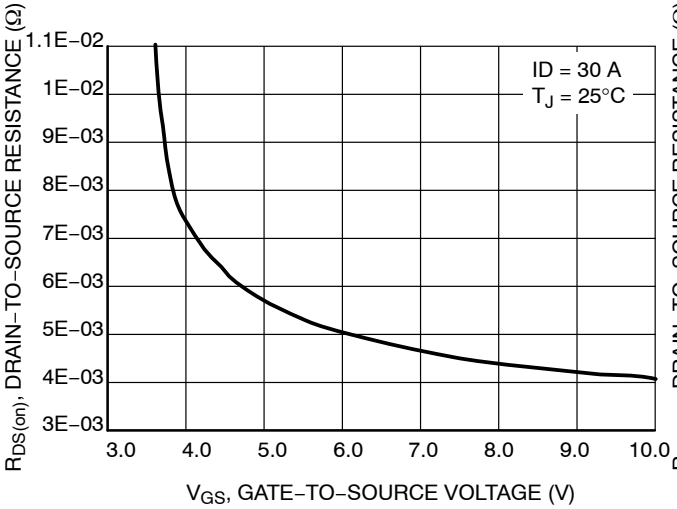


Figure 3. On−Region versus V_{GS}

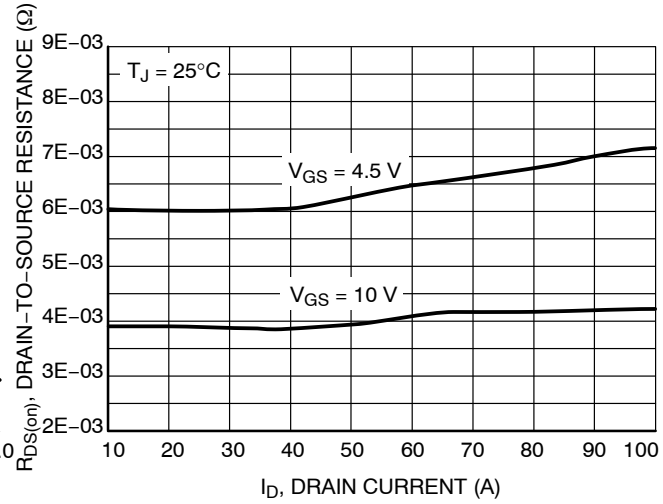


Figure 4. On−Resistance versus Drain Current and Gate Voltage

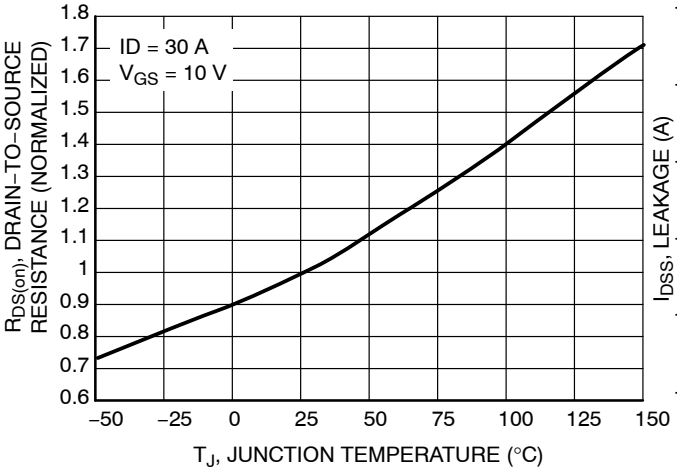


Figure 5. On−Resistance Variation with Temperature

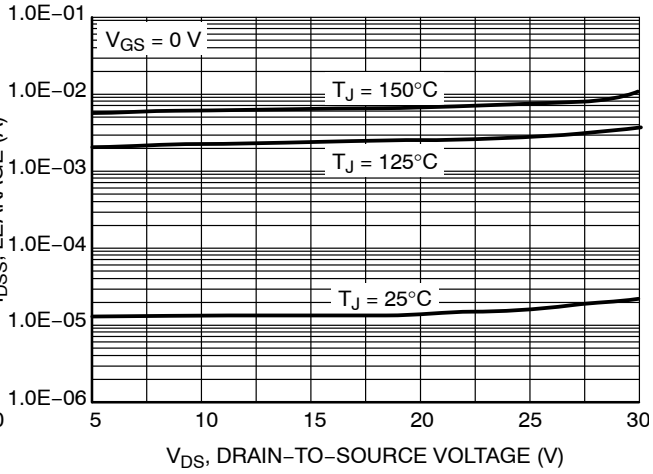


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

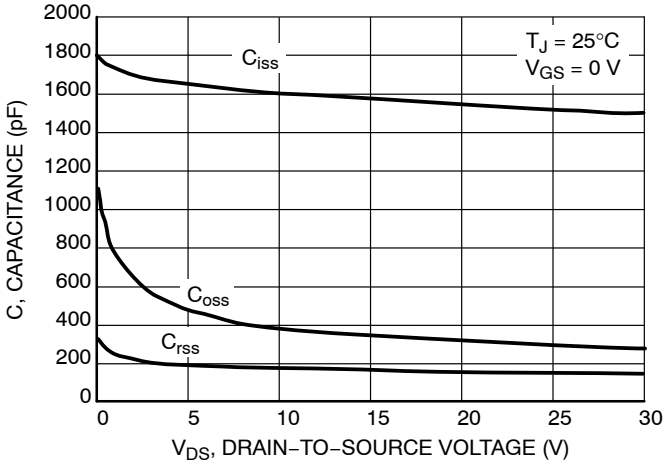


Figure 7. Capacitance Variation

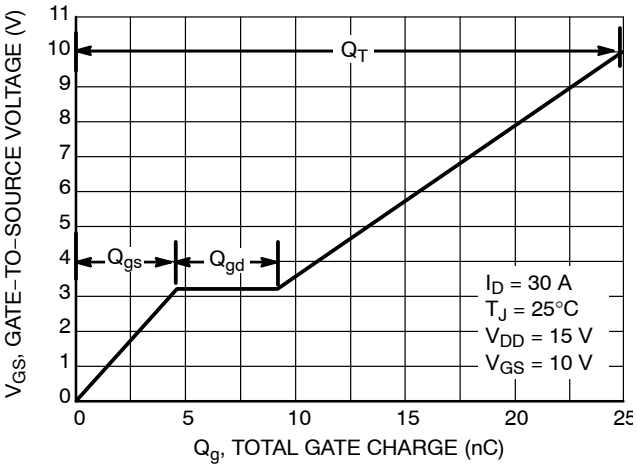


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

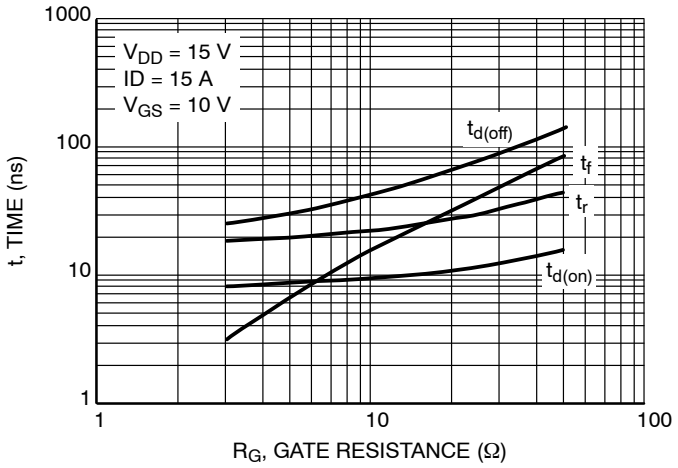


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

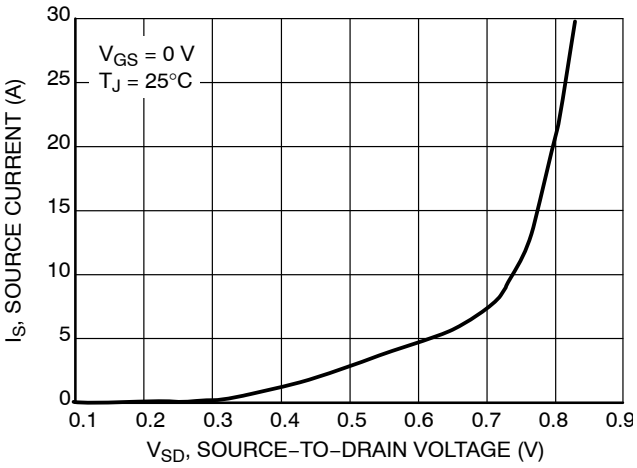


Figure 10. Diode Forward Voltage vs. Current

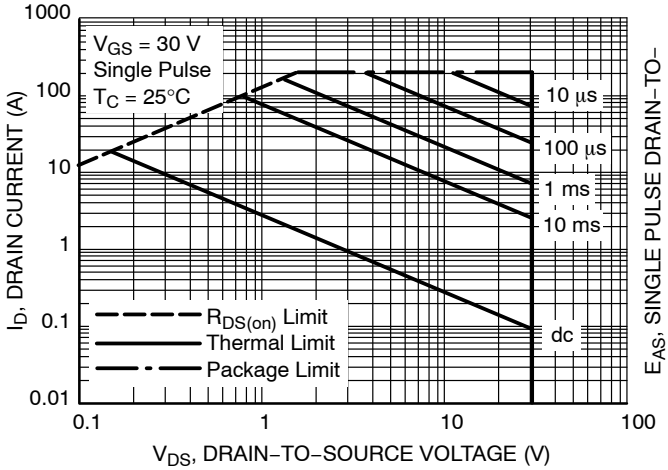


Figure 11. Maximum Rated Forward Biased Safe Operating Area

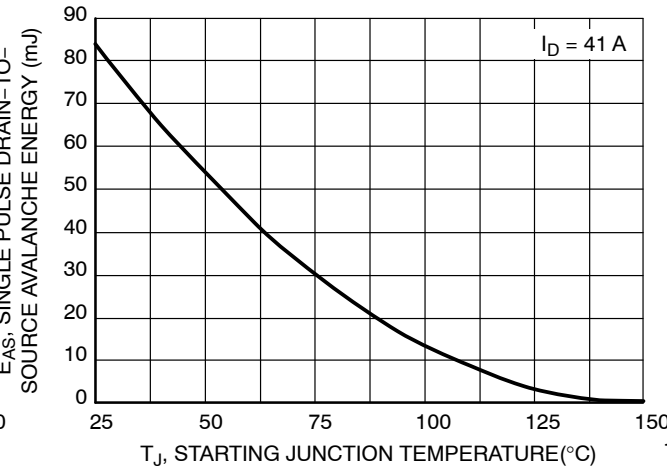


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

TYPICAL CHARACTERISTICS

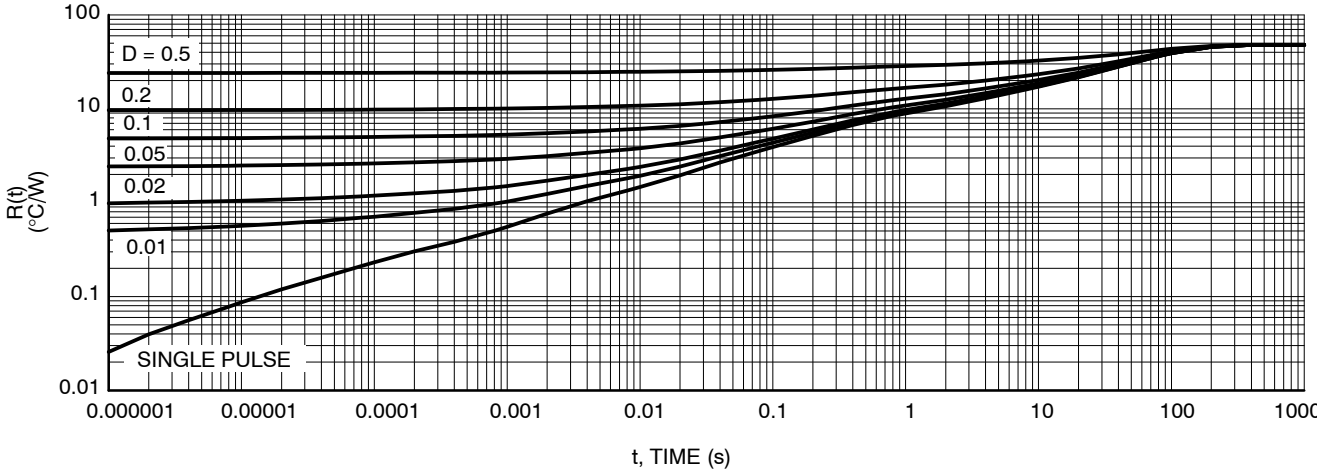
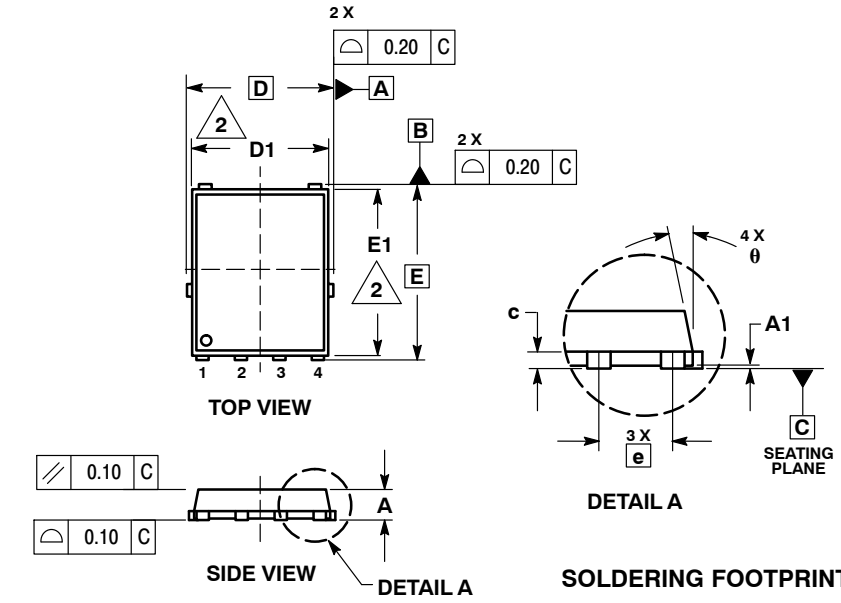


Figure 13. Thermal Response

PACKAGE DIMENSIONS

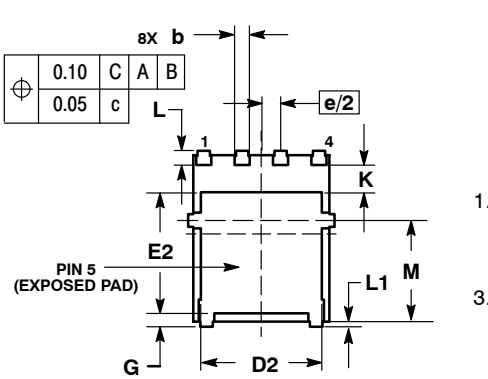
DFN5 5x6, 1.27P
(SO−8FL)
CASE 488AA
ISSUE G



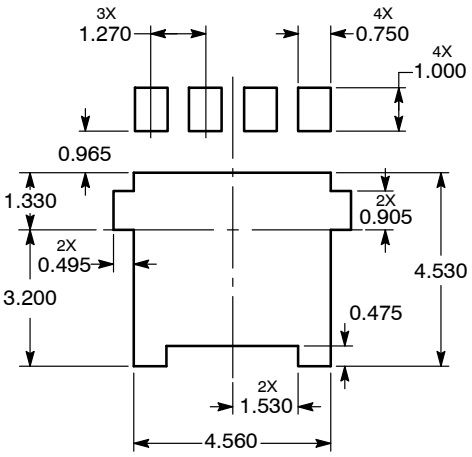
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	–––	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D		5.15 BSC	
D1	4.50	4.90	5.10
D2	3.50	–––	4.22
E		6.15 BSC	
E1	5.50	5.80	6.10
E2	3.45	–––	4.30
e		1.27 BSC	
G	0.51	0.61	0.71
K	1.20	1.35	1.50
L	0.51	0.61	0.71
L1	0.05	0.17	0.20
M	3.00	3.40	3.80
θ	0 °	–––	12 °

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN



SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and ON are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative