NMFAAAA

Product Preview

USB Clamps, RS232 and General Purpose Data Line Filters with ESD Protection; Optional Internal Switch

ON Semiconductor®

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USB line clamps (DOUT+, DOUT−) protect low operating voltage loads. Five additional low pass filters are built in to reject RF noise and EMI on RS232 and GP data lines. When the USB lines are used, a switch is utilized to open the RS232 lines in order to reduce the loading on the USB lines. There are two options available for this device. NMFAAAA−1 has the switch external, and NMFAAAA−2 integrates the switch on chip. Also, when the switch is integrated, the USB line resistors are integrated as well.

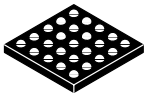
Features

- ESD Protection IEC 61000−4−2 Level 4 (Input Lines)
- ESD Protection IEC 61000−4−2 Level 1 (All I/O)
- RF Filtering (800 MHz–4.0 GHz): −30 dB Low Pass Filter (RS232 and General Purpose Data Lines)
- Input Voltage up to 5.25 V (USB Lines) and 6.0 V (RS232 and General Purpose Data Lines)
- Max Output Voltage: TBD by Customer (RS232 and GP Data Lines) and TBD by Customer (USB Lines)
- USB Minimum Input Signal Level: −1.0 V
- USB Line Capable of Withstanding Exposure to Burst (60 ns at 4.6 V)
- Optional Integrated Switch to Open the RS232 Lines (NMFAAAA−2)
- 25 Bump Flip−Chip Direct Chip Attach: 2.5 mm x 2.5 mm x 0.65 mm
- This is a Pb−Free Device

Typical Application

- Cellular Phones
- Portable Equipment

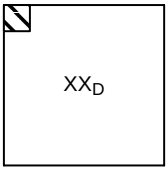
This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.



A1

FLIP−CHIP−25 CSP
CASE 499G

MARKING DIAGRAM



XX = Specific Device Code
D = Date Code

ORDERING INFORMATION

Device	Package	Shipping†
TBD	Flip−Chip	3000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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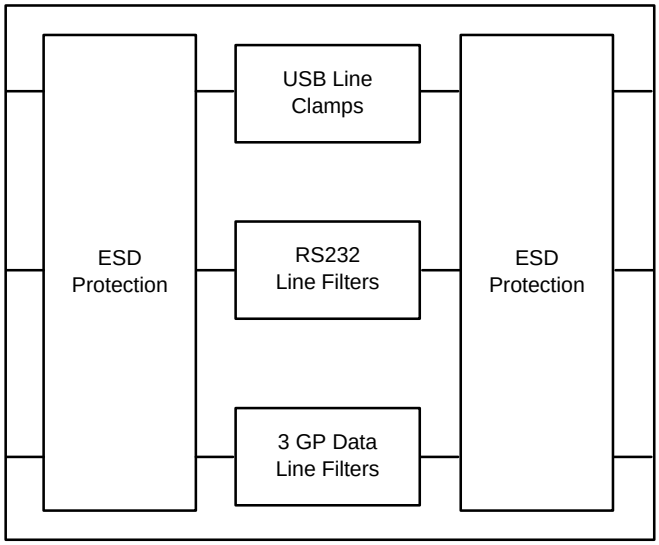


Figure 1. NMFAAAA−1: Without Integrated Switch

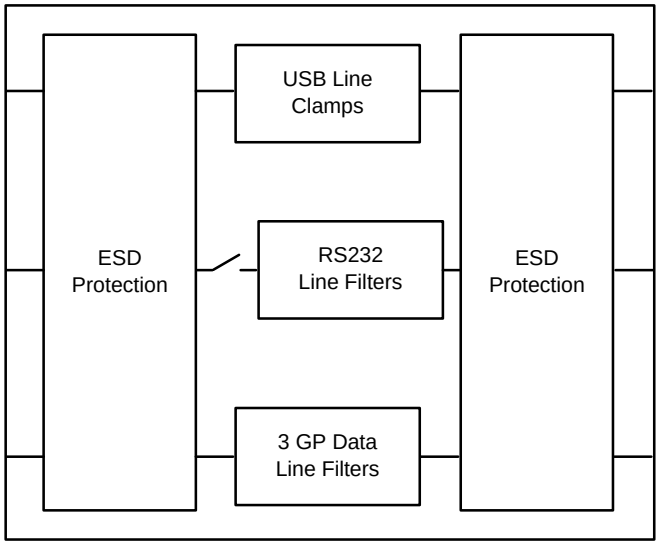


Figure 2. NMFAAAA−2: With Integrated Switch

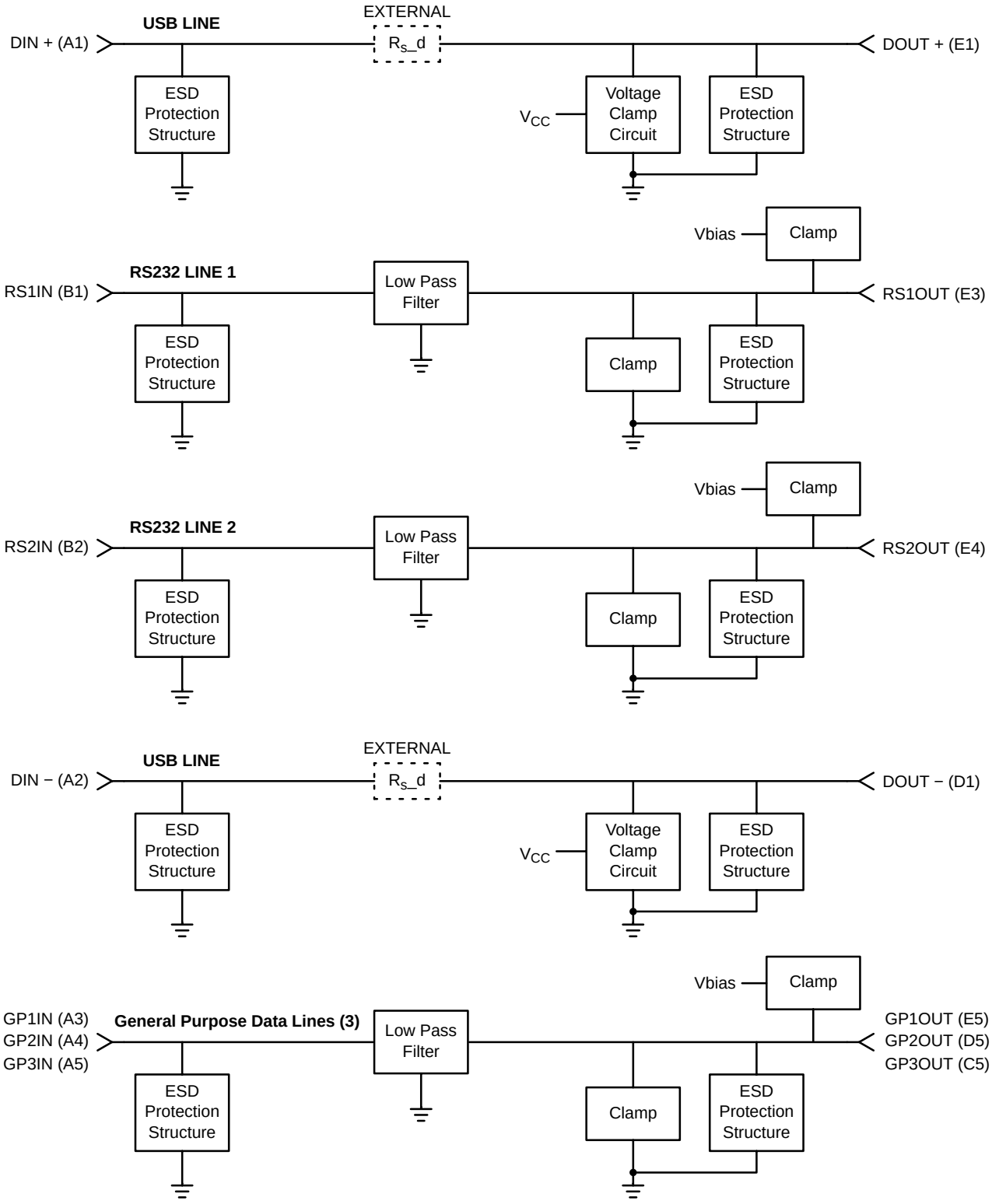


Figure 3. NMFAAAA−1: Without Integrated Switch

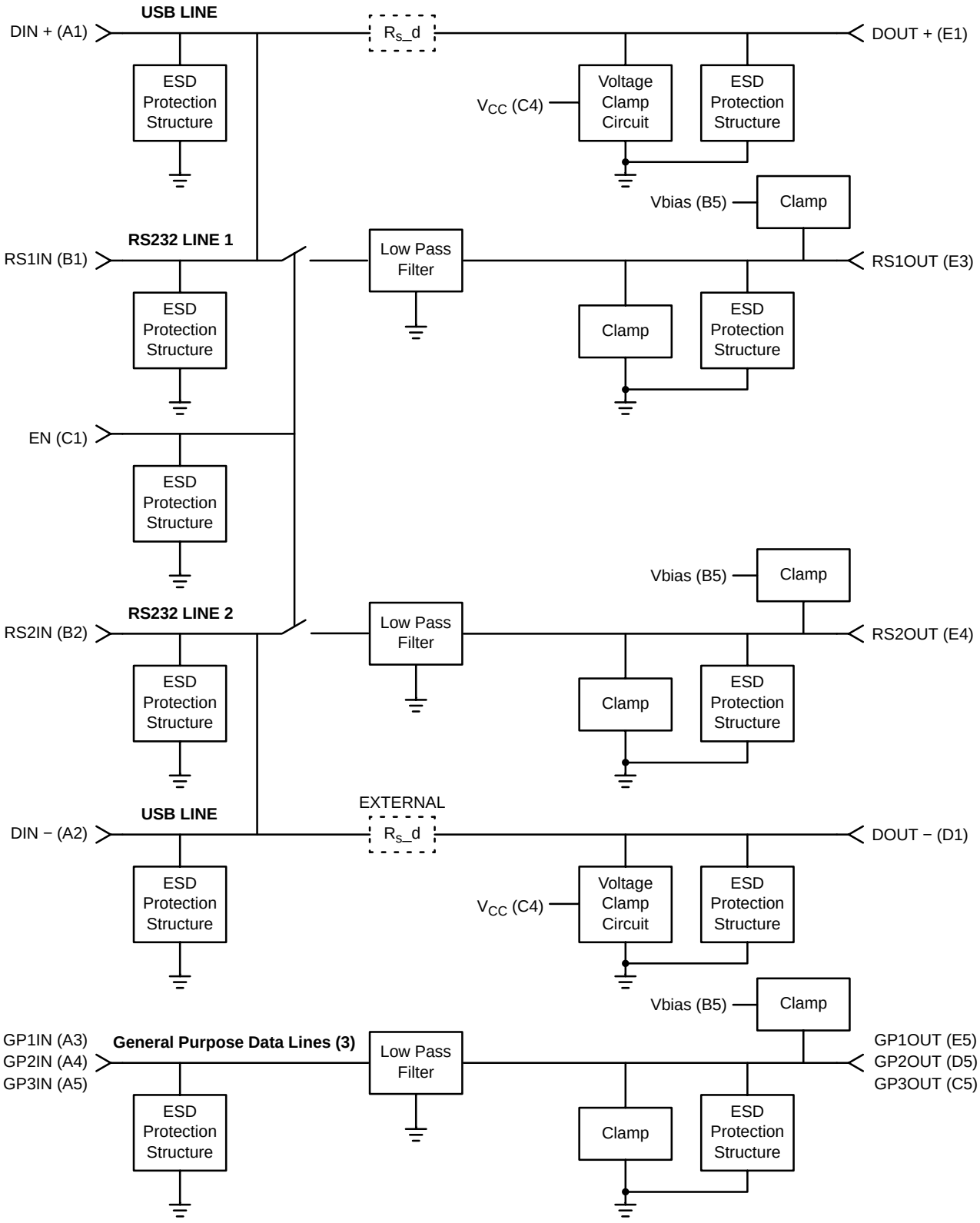


Figure 4. NMFAAAA−2: With Integrated Switch

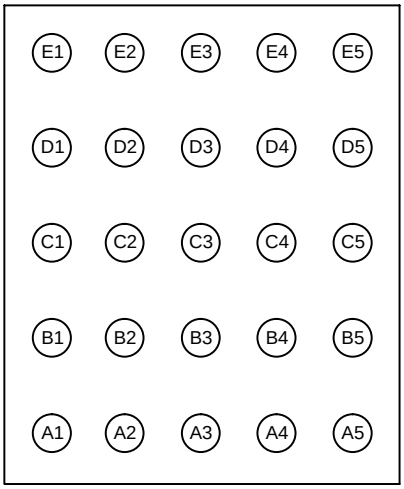
PIN FUNCTION DESCRIPTION

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
E1	Dout+	E2	GND	E3	RS1out	E4	RS2out	E5	GP1out
D1	Dout−	D2	GND	D3	GND	D4	GND	D5	GP2out
C1	NC/EN (Note 1)	C2	GND	C3	GND	C4	V_{CC}	C5	GP3out
B1	RS1in	B2	RS2in	B3	GND	B4	GND	B5	Vbias
A1	Din+	A2	Din−	A3	GP1in	A4	GP2in	A5	GP3in

1. For NMF3503−1, C1 is not connected, no ESD protection on this pin. For NMF3503−2, C1 is EN pin, ESD level 1 protection applies.

ESD Level 1

ESD Level 4



Bump Side Up

Figure 5. Pin Configuration

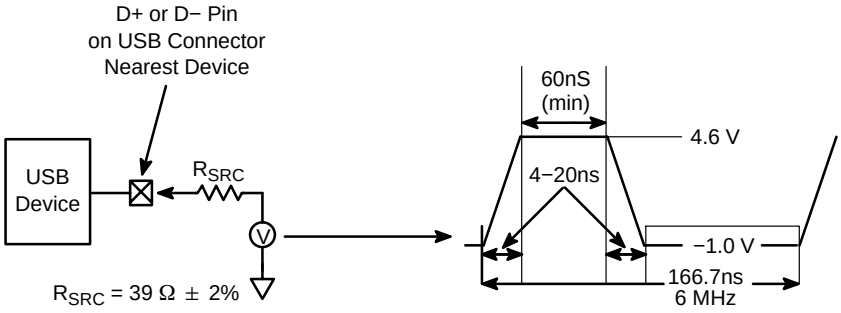
MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Max	Unit
ESD Discharge IEC61000−4−2 Air Discharge ESD Discharge IEC61000−4−2 Contact Discharge Machine Model	V_{PP}	15 15 0.2	kV
Junction Temperature	T_J	150	°C
Operating Temperature Range	T_{OP}	−40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
V_{CC}	V_{CC}					V
V_{bjas}	V_{bias}					V
ESD Structure Breakdown Voltage	V_{BRESD}					V
ESD Structure Leakage Current (Per Line)	I_R					μA
Line Capacitance for USB Line	C_{L+}, C_{L-}					pF
Passband Attenuation (RS232 and GP Data Lines)	PB_{att}					dB
Stopband Rejection (RS232 and GP Data Lines)	SB_{rej}					dB
Equivalent Load Resistance on Dout+, Dout−	R_{Leq}					KΩ
Clamp Voltage for Dout+, Dout−	$V_{CLAMPON}$	**TO BE DETERMINED BY CUSTOMER REQUIREMENTS**				V
Clamp Voltage for Dout+, Dout−	V_{CLAMP0}					V
Die Temperature During USB Short Test (Note 2)	T_{die}					°C
Maximum Input Signal on Din+ and Din− (Note 3)	Vin max					V
Rise Time for Dout+, Dout−	Tr					ns
Fall Time for Dout+, Dout−	Tf					ns
Differential Rise and Fall Time Matching for Dout+, Dout− (Note 4)	trfm					%
Crossover Voltage for Dout+, Dout− (Note 4)	V_{CRS}					V
Resistance of the Integrated Switch	R_{dson}					Ω

2. Test performed at T_A = 85°C during 24 hours.
3. Figure 3 depicts the waveform of the open circuit voltage of the source.
4. Excluding the first transition from idle state.



The signal produced by the voltage generator may be distorted when observed at the data pin due to input protection devices possibly incorporated in the USB device.

Figure 6. Maximum Input Waveform for USB Signaling

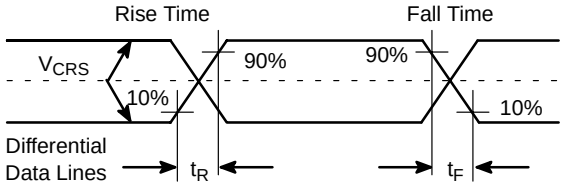


Figure 7. Data Signal Switching Parameters

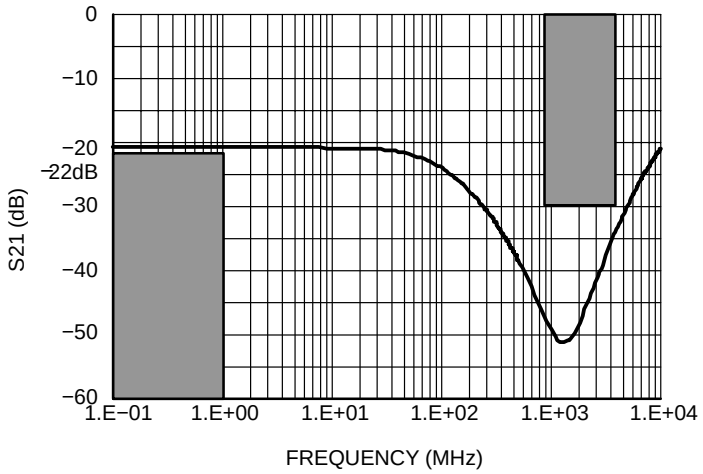


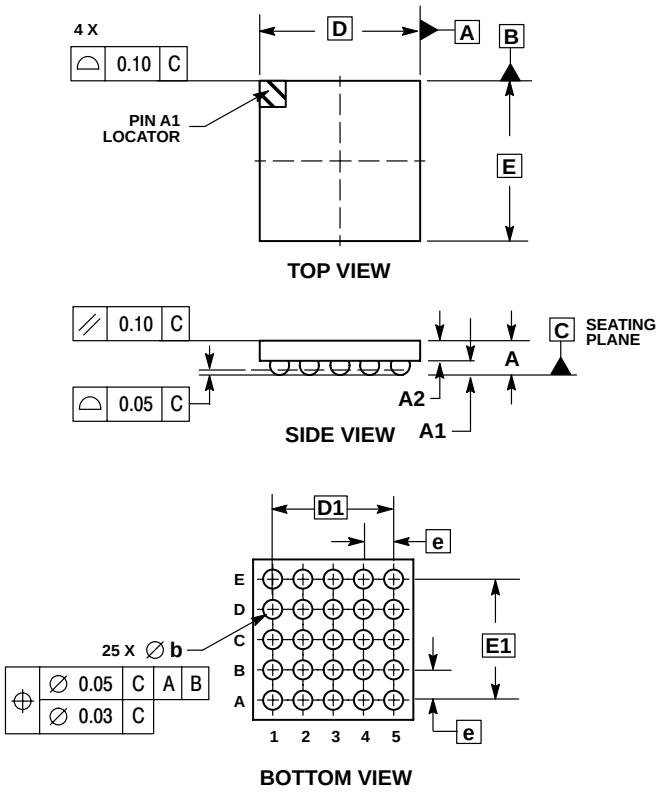
Figure 8. S21 Characteristics for RS232 and General Purpose Data Lines (50 Ω Load and Source)

PCB Layout Recommendations

Parameter	500 μm Pitch 300 μm Solder Ball
PCB Pad Size	250 μm (+25 / −0)
Pad Shape	Round
Pad Type	NSMD
Solder Mask Opening	350 μm ± 25
Solder Stencil Thickness	125 μm
Stencil Aperture	250 x 250 μm sq.
Solder Flux Ratio	50/50
Solder Paste Type	No Clean Type 3 or Finer
Trace Finish	OSP Cu
Trace Width	150 μm Max

PACKAGE DIMENSIONS

FLIP−CHIP−25 CSP
CASE 499G−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	−−−	0.650
A1	0.210	0.270
A2	0.280	0.380
D	2.650 BSC	
E	2.650 BSC	
b	0.290	0.340
e	0.500 BSC	
D1	2.000 BSC	
E1	2.000 BSC	

NMFAAAA

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